F71889

Super Hardware Monitor + LPC I/O

Release Date: April, 2010
Version: V0.28P

F71889 Datasheet Revision History

Version	Date	Page	Revision History
V0.10P	2007/11/23	-	Preliminary Version.
V0.11P	2008/1/16	-	Modify Pin25/26 description.
V0.12P	2008/1/29	-	Add function description and register description
V0.13P	2008/7/2	-	Add new functions by power on strapping
V0.14P	2008/8/15	-	Add application circuit and VID/GPIO new functions
V0.15P	2008/10/22	-	Modify typo.
V0.16P	2008/11/28	6,8	Modify the description of pin99, pin122
		118	Update application circuit page 1.
V0.17P	2008/12/3	38	Add VREF timing sequence sketch
		118	Update application circuit page 1.
V0.18P	2009/1/5	6	Rename pin99 AVCC to AVSB
		83	Modify the description of Index 27h bit2
		92	Remove Index F0h Clock Select Register
		118	Update application circuit page 1. (Rename pin99)
V0.19P	2009/1/6	-	Modify typo. (Blue Color) on page 8, 9, 10, 11, 12, 13, 14.
		79	Modify KBC device config. register table (Blue Color)
		83	Modify ROM address select register bit1-0 description.
		85	Modify Wakeup control register bit2-1 description.
		91	Modify default value of Index70/72 register.
		92	Add “Powered by VSB3V” description on all GPIO register.
V0.20P (Start from Version E)	2009/2/5	5	Revise pin configuration. The details can be referred in P.13
		13	Add IBX SCL/SDA pin description in pin 43, 44. Only description updated, no function change
		38, 76	Move the description of VREF to P.75 from P.37, and modify the contents
		47	CR01, bit 5,TSI_EN, cleared by LRESET#
		48	CR0A, bit 4,SST_EN, cleared by LRESET#
		74	Change SPI clock default to 16.7MHz
		81	Create a new bit “7” in Register 0x20 to choose the conversion rate of the temperature from the digital interface
		85	Create a new bit “7” in Register 0x2C to choose GPIO1x and GPIO2x clear condition

			Create a new bit ”5” in Register 0x2D to set VREF_VSYS and VREF_VTT status in the S3 state
V0.21P (Start from Version F)	2009/3/18	3	Rename: VREF_VTT to VREF3, VREF_VSYS to VREF2, VREF_VRAM to VREF1
		5	Revise Pin Configuration Pin 85: ~~VREF_VTT~~ → VREF3 Pin 86: ~~VREF_VSYS~~ → VREF2 Pin 87: ~~VREF_VDRAM~~ →VREF1
		14	Pin-out rename: Pin 85: ~~VREF_VTT~~ → VREF3 Pin 86: ~~VREF_VSYS~~ → VREF2 Pin 87: ~~VREF_VDRAM~~ →VREF1 Add dexcriptions for Pin84~87 Add pin 80 PWROK falling condition description Modify pin 81 RSMRST# falling condition to VSB3V under 2.95V
		16	Revise typo: ~~PWMDUTY~~ → FAN60_100
		40	Remove Fig. 7-5/7-6
		41	Remove Fig. 7-7/7-8 Revise Fig. 7-5, (original Fig. 7-10)
		42	Revise Fig. 7-6, (original Fig. 7-11)
		51	Rename V1~V6 to VIN1~VIN6 Revise CR20h, 27h, 28h to Reserved
		76	Typo revised and pin-out rename: The F71889 also supports ~~4~~ 3 output voltages for ~~VREF, VRAM, VSYS and VTT.~~VREF1~3. The output is generated Below is the timing sequence between ~~VFEF_VRAM/VREF_VSYS/VREF_VTT~~ VREF1~3pins: Revise VREF1~3 timing chart
		79	Revise Section 7.11 SST Fuction description
		83	Register 0xF0: Rename VREF_VTT to VREF3 Register 0xF1: Rename VREF_VSYS to VREF2 Register 0xF2: Rename VREF_VRAM to VREF1
		88	Swap CR0x2C bit 6 and 4 Create a new bit ”6” in Register 0x2D to set VREF1~3 are reset or not in the S3/S4/S5 state

			Revise Register0x2D bit5 description: revise the reference voltage output definition to VREF1~3
		115	Register 0xF0: Rename VREF_VTT to VREF3 in the relative description Register 0xF1: Rename VREF_VSYS to VREF2 in the relative description Register 0xF2: Rename VREF_VRAM to VREF1 in the relative description
		116	Revise Register 0xF3 bit2~0 description: revise the reference voltage output definition to VREF1~3 Revise Register 0xFF bit0 description: revise the reference voltage output definition to VREF1~3
		121	Revise Application circuit
0.22P	2009/05/04	16	Remove FDC, UART, Parallel port descriptions
		51	Revise CR20h, 27h, 28h typo
		55-57	Revise VREF timing chart
		73	Revise Typo: (8) CTRL + Alt + ~~user define key~~ Space
0.23P	2009/05/12	66	Revise CR2Dh bit 6 description
		93	Revise CRF6h bit 3 description
0.24P	2009/5/19	92	Revise CRF4h bit 5 description ~~1~~0: DUAL_GATE_N tri-state in S5 state. ~~0~~1: DUAL_GATE_N output low in S5 state.
0.25P	2009/8/3		Made Corrections & Clarification Update Power Type for Pin 72 Revise Application circuit (Sheet 1)
0.26P	2009/8/24		Made Corrections & Clarification Update Fan 1~3 Related Setting Index A6~A9, B6~B9, and C6~C9 BUSIN Register Index 04h GPIO0 and GPIO1 Pin Status Index F2h and E2h TSI and SMBus Related Register Index E0h~EDh Update Application Circuit (Add Intel IBX)
0.27P	2009		Made Corrections & Clarification Update Electrical Characteristics GPIO0 Drive Enable Register — Index F3h, bit 3
0.28P	2010/4/19		Made Corrections & Clarification

Please note that all data and specifications are subject to change without notice. All the trade marks of products and companies mentioned in this data sheet belong to their respective owners.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Fintek for any damages resulting from such improper use or sales.

Table of Content

1. General Description

The F71889 which is the featured IO chip for new generational PC system is equipped with one IEEE 1284 parallel port, two UART ports, KBC, Serial Peripheral Interface (SPI), 80-Port, SIR, VID controller and one FDC. The F71889 integrated with hardware monitor, 9 sets of voltage sensor, 3 sets of creative auto-controlling fans and 3 temperature sensor pins for the accurate dual current type temp. measurement for CPU thermal diode or external transistors 2N3906.

The F71889 provides flexible features for multi-directional application. For instance, supports Bus Interface pins, provides 59 GPIO pins (multi-pin), IRQ sharing function also designed in UART feature for particular usage and accurate current mode H/W monitor will be worth in measurement of temperature, provides 3 modes fan speed control mechanism included Manual Mode/Speed Mode/Temperature Mode for users' selection.

Additionally, integrated SPI interface, 80-Port, and 5VDUAL voltage switch switch and adjustable voltage reference outputs related functions. The SPI interface is for BIOS usage including bridge function (Supports up to 16M), and the 80-Port is for engineering and debuging usage. F71889 also provides 5V dual controller and some voltage reference outputs for system application. Others, the F71889 supports newest AMD new interface TSI and Intel PECI 1.1/SST interfaces for temperature reading. These features will help you more and improve product value. Finally, the F71889 is powered by 3.3V voltage, with the LPC interface in the package of 128-QFP green package.

2. Feature List

- **General Functions**
  - Comply with LPC Spec. 1.1
  - Support DPM (Device Power Management), ACPI
  - Bus Interface for CPU use
  - Provides one FDC, two UARTs, KBC and Parallel Port
  - 16 pins VID controller for VRM 11.x and OTF
  - Serial VID controller with CORE_TYPE input for AMD Processor
  - H/W monitor functions
  - Reference voltage outputs support
  - 5VDUAL voltage switch
  - SPI interface for BIOS Bridge
  - 80-Port interface from LPT or COM2
  - Support AMD TSI interface and Intel SST/PECI interface
  - PECI Spec.1.1 ready

- Support Ibex protocol SMBus interface
- 59 GPIO Pins for flexible application
- 24/48 MHz clock input
- Packaged in 128-PQFP green package and powered by 3.3VCC

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and under run conditions
- Built-in address mark detection circuit to simplify the read electronics
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate

UART

- Two high-speed 16C550 compatible UART with 16-byte FIFOs
- Fully programmable serial-interface characteristics
- Baud rate up to 115.2K
- Support IRQ sharing

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps

Parallel Port

- One PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Enhanced printer port back-drive current protection

Keyboard Controller

- Compatibility with the 8042
- Support PS/2 mouse
- Support both interrupt and polling modes
- Hardware Gate A20 and Hardware Keyboard Reset

- **Hardware Monitor Functions**
  - 3 dual current type (±3°C) thermal inputs for CPU thermal diode and 2N3906 transistors
  - Temperature range -40°C ~127°C
  - 9 sets voltage monitoring (6 external and 3 internal powers)
  - High limit signal (PME#) for Vcore level
  - 3 fan speed monitoring inputs
  - 3 fan speed PWM/DC control outputs(support 3 wire and 4 wire fans)
  - Issue PME# and OVT# hardware signals output
  - Case intrusion detection circuit
  - WATCHDOG# comparison of all monitored values

- **Serial Peripheral Interface Compatible**
  - Support SPI bridge function for BIOS use
  - Up to 16M bit Support

- **80-Port Interface**
  - Monitor 0x80 Port and output the value via signals defined for 7-segment display.
  - High nibble and low nibble are outputted interleaved at 1KHz frequency.
  - 80-Port output by LPT or COM2 interface.

- **8-IN and 8-OUT VID Controller for VRM11.x and OTF**
- **Serial VID Controller with CORE_TYPE Input for AMD CPU application**
- **Integrate AMD TSI interface**
- **Integrate Intel PECI 1.1 /SST interface**
- **Support Ibex Protocol SMBus interface**
- **Support FSB over clocking control bus**

- **5V Dual Voltage Switch**
  - Provide ACPI-compliant 5VDUAL voltage switch
  - 5VDUAL for USB/Keyboard/Mouse application

- **Adjustable Voltage Reference Outputs**
  - Enable pin for VREF2 and 3 Voltage Reference Output control
  - 0.9V default output on VREF1~3 pins
  - Adjustable voltage range from 0~2.295V

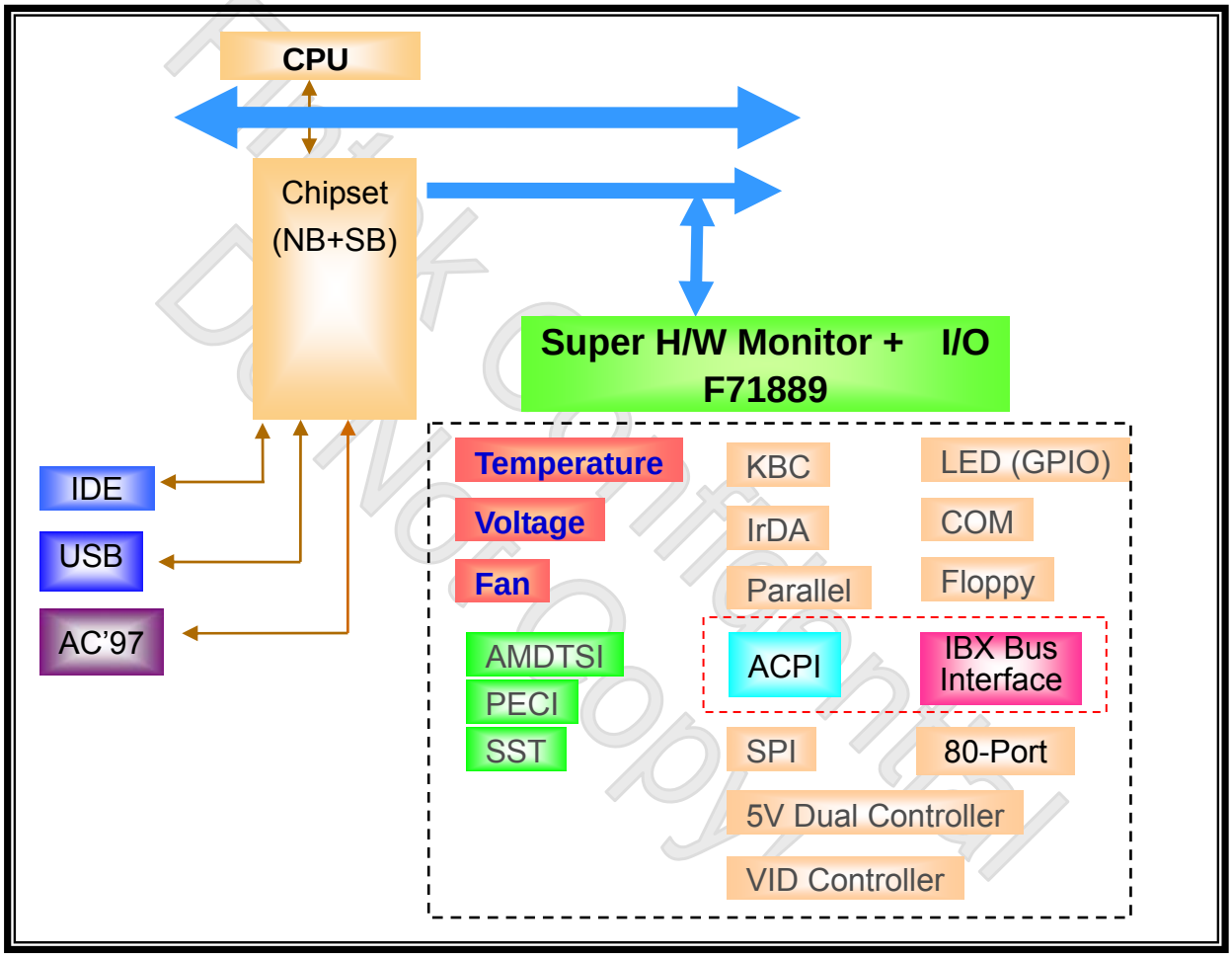
- **Package**
  - 128-pin PQFP green package

Noted: Patented TW207103 TW207104 TW220442 US6788131 B1 TWI235231 TW237183 TWI263778

3. Key Specification

- Supply Voltage 3.0V to 3.6V
- Operating Supply Current 10mA typ.

4. Block Diagram



5. Pin Configuration

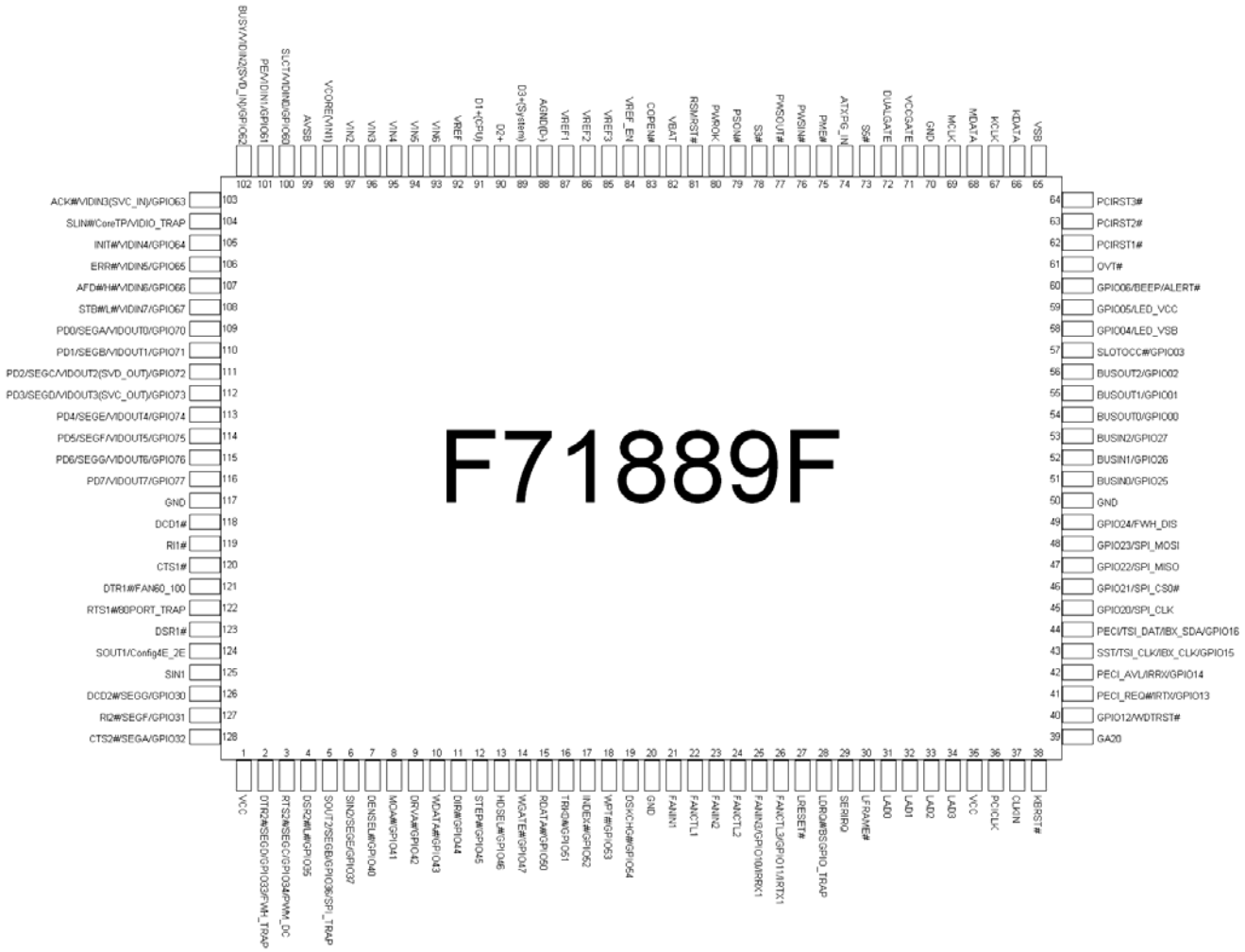


Figure1. F71889 pin configuration

6. Pin Description

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink cap ability.
I/OD_{12t} - TTL level bi-directional pin and schmitt trigger, Open-drain output with 12 mA sink
I/OOD_{12t} - TTL level bi-directional pin, can select to OD or OUT by register, with 12 mA source-sink capability.
$I/OOD_{12st,lv}$ - Low level bi-directional pin with schmitt trigger, can select to OD or OUT by register, with 12 mA source-sink capability.
$I/OD_{16st,5v}$ - TTL level bi-directional pin and schmitt trigger, Open-drain output with 16 mA sink capability, 5V tolerance.
$OD_{16,u10-5v}$ - Open-drain output pin with 16 mA sink capability, pull-up 10k ohms, 5V tolerance.
$I/OD_{12st,5v}$ - TTL level bi-directional pin and schmitt trigger, Open-drain output with 12 mA sink capability, 5V tolerance.
$I/O_{D8,st,lv}$ - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.) with schmitt trigger. Output with 8mA drive
$I/O_{s1,D8st,lv}$ - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.) with schmitt trigger. Output with 8mA drive and 1mA sink capability.
$I/OD_{12st,lv}$ - Low level bi-directional pin with schmitt trigger. Open-drain output with 12mA sink capability.
$O_{8,u47,5v}$ - Open-drain pin with 8 mA source-sink capability, pull-up 47k ohms, 5V tolerance.
O_{12} - Output pin with 12 mA source-sink capability.
O_{30} - Output pin with 30 mA source-sink capability.
AOUT - Output pin(Analog).
OD_{12} - Open-drain output pin with 12 mA sink capability.
$OD_{12,5v}$ - Open-drain output pin with 12 mA sink capability, 5V tolerance.
OD_{24} - Open-drain output pin with 24 mA sink capability.
OD_{14} - Open-drain output pin with 14 mA sink capability.
I/OD_{14t} - TTL level bi-directional pin, Open-drain output with 14 mA sink capability.
$IN_{t,5v}$ - TTL level input pin,5V tolerance.
IN_{st} - TTL level input pin and schmitt trigger.
$IN_{st,5v}$ - TTL level input pin and schmitt trigger, 5V tolerance.
$IN_{st,lv}$ - TTL low level input pin (VIH → 0.9V, VIL → 0.6V.)
AIN - Input pin(Analog).
P - Power.

6.1 Power Pin

Pin No.	Pin Name	Type	Description
1,35	VCC	P	Power supply voltage input with 3.3V
99	AVSB	P	Analog power supply voltage input with 3.3V stand-by power.
65	VSB	P	Stand-by power supply voltage input 3.3V
82	VBAT	P	Battery voltage input
88	AGND(D-)	P	Analog GND
20, 50, 70, 117	GND	P	Digital GND

6.2 LPC Interface

Pin No.	Pin Name	Type	PWR	Description
27	LRESET#	$IN_{st,5v}$	VCC	Reset signal. It can connect to PCIRST# signal on the host.
28	LDRQ#	O_{12}	VCC	Encoded DMA Request signal.
	BSGPIO_TRAP	$IN_{t,5v}$		Power on strapping : (Default internal pull high) 1(Default): Pin 51-56 are Bus Interface functions 0 : Pin 51-56 are GPIO pins
29	SERIRQ	I/O_{12t}	VCC	Serial IRQ input/Output.
30	LFRAME#	IN_{st}	VCC	Indicates start of a new cycle or termination of a broken cycle.
31-34	LAD[0:3]	I/O_{12t}	VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
36	PCICLK	IN_{st}	VCC	33MHz PCI clock input.
37	CLKIN	IN_{st}	VCC	System clock input. According to the input frequency 24/48MHz.

6.3 FDC

Pin No.	Pin Name	Type	PWR	Description
7	DENSEL#	OD_{14}	VCC	Drive Density Select. Set to 1 - High data rate.(500Kbps, 1Mbps) Set to 0 – Low data rate. (250Kbps, 300Kbps)
	GPIO40	I/OD_{14t}		General purpose IO. (Select by Register)
8	MOA#	OD_{14}	VCC	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
	GPIO41	I/OD_{14t}		General purpose IO. (Select by Register)
9	DRVA#	OD_{14}	VCC	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
	GPIO42	I/OD_{14t}		General purpose IO. (Select by Register)
10	WDATA#	OD_{14}	VCC	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
	GPIO43	I/OD_{14t}		General purpose IO. (Select by Register)
11	DIR#	OD_{14}	VCC	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
	GPIO44	I/OD_{14t}		General purpose IO. (Select by Register)
12	STEP#	OD_{14}	VCC	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
	GPIO45	I/OD_{14t}		General purpose IO. (Select by Register)
13	HDSEL#	OD_{14}	VCC	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
	GPIO46	I/OD_{14t}		General purpose IO. (Select by Register)
14	WGATE#	OD_{14}	VCC	Write enable. An open drain output.

	GPIO47	I/OD_{14t}		General purpose IO. (Select by Register)
15	RDATA#	$IN_{st,5v}$	VCC	The read data input signal from the FDD.
	GPIO50	I/OOD_{12t}		General purpose IO. (Select by Register)
16	TRK0#	$IN_{st,5v}$	VCC	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track.
	GPIO51	I/OOD_{12t}		General purpose IO. (Select by Register)
17	INDEX#	$IN_{st,5v}$	VCC	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole.
	GPIO52	I/OOD_{12t}		General purpose IO. (Select by Register)
18	WPT#	$IN_{st,5v}$	VCC	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected.
	GPIO53	I/OOD_{12t}		General purpose IO. (Select by Register)
19	DSKCHG#	$IN_{st,5v}$	VCC	Diskette change. This signal is active low at power on and whenever the diskette is removed.
	GPIO54	I/OOD_{12t}		General purpose IO. (Select by Register)

6.4 UART, SIR and 80-Port

Pin No.	Pin Name	Type	PWR	Description
118	DCD1#	$IN_{t,5v}$	VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
119	RI1#	$IN_{t,5v}$	VCC	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
120	CTS1#	$IN_{t,5v}$	VCC	Clear To Send is the modem control input.
121	DTR1#	$O_{8,u47,5v}$	VCC	UART 1 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. Internal 47k ohms pulled high and disable after power on strapping.
	FAN60_100	$IN_{t,5v}$		Power on strapping pin: 1(Default): (Internal pull high) Power on fan speed default duty is 60%.(PWM) 0: (External pull down) Power on fan speed default duty is 100%.(PWM)
122	RTS1#	$O_{8,u47,5v}$	VCC	UART 1 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. Internal 47k ohms pulled high and disable after power on strapping.
	80_TRAP	$IN_{t,5v}$		Power on strapping pin: 1(Default) : Default 80-port enable (Internal pull high) 80 port decode output from COM2 interface 0 : Disable 80-port function
123	DSR1#	$IN_{t,5v}$	VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
124	SOUT1	$O_{8,u47,5v}$	VCC	UART 1 Serial Output. Used to transmit serial data out to the communication link. Internal 47k ohms pulled high and disable after power on strapping.
	Config4E_2E	$IN_{t,5v}$		Power on strapping: (Internal pull high) 1(Default): Configuration register →4E 0 : Configuration register →2E

125	SIN1	$IN_{t,5v}$	VCC	Serial Input. Used to receive serial data through the communication link.
126	DCD2#	$IN_{t,5v}$	VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
	SEGG	O_{12}		SEGG for 7-segment display. (Select by pin 122 power on strapping)
	GPIO30	I/OOD_{12t}		General purpose IO. (Select by register)
127	RI2#	$IN_{t,5v}$	VCC	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
	SEGF	O_{12}		SEGF for 7-segment display. (Select by pin 122 power on strapping)
	GPIO31	I/OOD_{12t}		General purpose IO. (Select by register)
128	CTS2#	$IN_{t,5v}$	VCC	Clear To Send is the modem control input.
	SEGA	O_{12}		SEGA for 7-segment display. (Select by pin 122 power on strapping)
	GPIO32	I/OOD_{12t}		General purpose IO. (Select by register)
2	DTR2#	$O_{8,u47,5v}$	VCC	UART 2 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. Internal 47k ohms pulled high and disable after power on strapping.
	SEGD	O_{12}		SEGD for 7-segment display. (Select by pin 122 power on strapping)
	GPIO33	I/OOD_{12t}		General purpose IO. (Select by register)
	FWH_TRAP	$IN_{t,5v}$		Power on strapping : 1(Default): FWH as a primary BIOS 0 : SPI as a primary BIOS
3	RTS2#	$O_{8,u47,5v}$	VCC	UART 2 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. Internal 47k ohms pulled high and disable after power on strapping.
	SEGC	O_{12}		SEGC for 7-segment display. (Select by pin 122 power on strapping)
	GPIO34	I/OOD_{12t}		General purpose IO. (Select by register)
	PWM_DC	$IN_{t,5v}$		Power on strapping : 1 (Default): Fan control method will be PWM Mode 0 Drive :Fan control method will be Linear Mode
4	DSR2#	$IN_{t,5v}$	VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
	L#	O_{30}		L# for 7-segment display. (Select by pin 122 power on strapping)
	GPIO35	I/OOD_{12t}		General purpose IO. (Select by register)
5	SOUT2	$O_{8,u47,5v}$	VCC	UART 2 Serial Output. Used to transmit serial data out to the communication link. Internal 47k ohms pulled high and disable after power on strapping.
	SEGB	O_{12}		SEGB for 7-segment display. (Select by pin 122 power on strapping)
	GPIO36	I/OOD_{12t}		General purpose IO. (Select by register)
	SPI_TRAP	$IN_{t,5v}$		Power on strapping: (Internal pull high) 1(Default) : SPI function disable 0 : SPI function enable
6	SIN2	$IN_{t,5v}$	VCC	Serial Input. Used to receive serial data through the communication link.

	SEGE	O_{12}		SEGE for 7-segment display. (Select by pin 122 power on strapping)
	GPIO37	I/OOD_{12t}		General purpose IO. (Select by register)

6.5 Parallel Port

Pin No.	Pin Name	Type	PWR	Description
100	SLCT	$IN_{st,5v}$	VCC	An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
	VIDIN0	$IN_{st,lv}$		CPU VID input pin. (Select by pin 104 power on strapping) Special Level input VIH → 0.9V, VIL → 0.6V
	GPIO60	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)
101	PE	$IN_{st,5v}$	VCC	An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	VIDIN1	$IN_{st,lv}$		CPU VID input pin. (Select by pin 104 power on strapping) Special Level input VIH → 0.9V, VIL → 0.6V
	GPIO61	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)
102	BUSY	$IN_{st,5v}$	VCC	An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
	VIDIN2 (SVD_IN)	$IN_{st,lv}$		CPU VID input pin. (Select by pin 104 power on strapping) Special Level input VIH → 0.9V, VIL → 0.6V
	GPIO62	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)
103	ACK#	$IN_{st,5v}$	VCC	An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	VIDIN3 (SVC_IN)	$IN_{st,lv}$		CPU VID input pin. (Select by pin 104 power on strapping) Special Level input VIH → 0.9V, VIL → 0.6V
	GPIO63	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)
104	SLIN#	OD_{12-5v}	VCC	Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	CoreTP	$IN_{st,lv}$		Processor Core_Type pin for AMD CPU identification.
	VIDIO_TRAP	$IN_{t,5v}$		Power on strapping : Pull high 1K : Pin 100-116 as LPT interfaces Pull high 20K : Pin 100-116 as PVID Controller Pull down 1K: Pin 102/103/111/112 as SVID Controller Pull down 47K:Pin 100-103 and pin 105-116 as GPIO pins
105	INIT#	OD_{12-5v}	VCC	Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	VIDIN4	$IN_{st,lv}$		CPU VID input pin. (Select by pin 104 power on strapping) Special Level input VIH → 0.9V, VIL → 0.6V

	GPIO64	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)
106	ERR#	$IN_{st,5v}$	VCC	An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	VIDIN5	$IN_{st,lv}$		CPU VID input pin. (Select by pin 104 power on strapping) Special Level input VIH → 0.9V, VIL → 0.6V
	GPIO65	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)
107	AFD#	$OD_{12,5v}$	VCC	An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	H#	O_{30}		H# signal of 80-port for 7-segment display.
	VIDIN6	$IN_{st,lv}$		CPU VID input pin. (Select by pin 104 power on strapping) Special Level input VIH → 0.9V, VIL (0.6V
	GPIO66	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)
108	STB#	$OD_{12,5v}$	VCC	An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode
	L#	O_{30}		L# signal of 80-port for 7-segment display.
	VIDIN7	IN_{tslv}		CPU VID input pin. (Select by pin 104 power on strapping) Special Level input VIH (0.9V, VIL (0.6V
	GPIO67	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)
109	PD0	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	SEGA	O_{12}		SEGA signal of 80-port for 7-segment display.
	VIDOUT0	OD_{12}		CPU VID output pin. (Select by pin 104 power on strapping)
	GPIO70	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)
110	PD1	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 1.
	SEGB	O_{12}		SEGB signal of 80-port for 7-segment display.
	VIDOUT1	OD_{12}		CPU VID output pin. (Select by pin 104 power on strapping)
	GPIO71	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)
111	PD2	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 2.
	SEGC	O_{12}		SEGC signal of 80-port for 7-segment display.
	VIDOUT2 (SVD_OUT)	OD_{12}		CPU VID output pin. (Select by pin 104 power on strapping)
	GPIO72	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)
112	PD3	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 3.
	SEGD	O_{12}		SEGD signal of 80-port for 7-segment display.
	VIDOUT3 (SVC_OUT)	OD_{12}		CPU VID output pin. (Select by pin 104 power on strapping)
	GPIO73	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)

113	PD4	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 4.
	SEGE	O_{12}		SEGE signal of 80-port for 7-segment display.
	VIDOUT4	OD_{12}		CPU VID output pin. (Select by pin 104 power on strapping)
	GPIO74	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)
114	PD5	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 5.
	SEGF	O_{12}		SEGF signal of 80-port for 7-segment display.
	VIDOUT5	OD_{12}		CPU VID output pin. (Select by pin 104 power on strapping)
	GPIO75	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)
115	PD6	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 6.
	SEGG	O_{12}		SEGG signal of 80-port for 7-segment display.
	VIDOUT6	OD_{12}		CPU VID output pin. (Select by pin 104 power on strapping)
	GPIO76	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)
116	PD7	$I/O_{12st,5v}$	VCC	Parallel port data bus bit 7.
	VIDOUT7	OD_{12}		CPU VID output pin. (Select by pin 104 power on strapping)
	GPIO77	I/OOD_{12t}		General purpose IO. (Select by pin 104 power on strapping)

6.6 Hardware Monitor, SPI Interface

Pin No.	Pin Name	Type	PWR	Description
93-97	VIN6~VIN2	AIN	AVSB	Voltage Input 2 ~ 6.
98	Vcore(VIN1)	AIN	AVSB	Voltage Input for Vcore.
21	FANIN1	$IN_{st,5v}$	VCC	Fan 1 tachometer input.
22	FANCTL1	$OD_{12,5v}$ AOUT	VCC	Fan 1 control output. This pin provides PWM duty-cycle output or a voltage output.
23	FANIN2	$IN_{st,5,4v}$	VCC	Fan 2 tachometer input.
24	FANCTL2	$OD_{12,5v}$ AOUT	VCC	Fan 2 control output. This pin provides PWM duty-cycle output or a voltage output.
25	FANIN3	$IN_{st,5v}$	VCC	Fan 3 speed input.
	GPIO10	I/OOD_{12t}		General purpose IO. (Select by Register)
	IRRX1	IN_{st}		Infrared Receiver input. (Select by Register)
26	FANCTL3	$OD_{12,5v}$ AOUT	VCC	Fan 3 control output.
	GPIO11	I/OOD_{12t}		General purpose IO. (Select by Register)
	IRTX1	O_{12}		Infrared Transmitter Output. (Select by Register)
89	D3+(System)	AIN	AVSB	Thermal diode/transistor temperature sensor input for system use.
90	D2+	AIN	AVSB	Thermal diode/transistor temperature sensor input.
91	D1+(CPU)	AIN	AVSB	CPU thermal diode/transistor temperature sensor input. This pin is for CPU use.
92	VREF	AOUT	AVSB	Voltage sensor output.
75	PME#	$OD_{12,5v}$	VSB	Generated PME event. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the S3 state.
45	GPIO20	I/OOD_{12t}	VCC	General purpose IO.

	SPI_SLK	O_{12}		Serial clock output pin for SPI device. (Select by pin 2/5 power on strapping)
46	GPIO21	I/OOD_{12t}	VCC	General purpose IO.
	SPI_CS0#	O_{12}		Connect this pin to primary BIOS chip select pin. (Select by pin 2/5 power on strapping)
47	GPIO22	I/OOD_{12t}	VCC	General purpose IO.
	SPI_MISO	$IN_{t,5v}$		SPI master in/slave out pin. (Select by pin 2/5 power on strapping)
48	GPIO23	I/OOD_{12t}	VCC	General purpose IO.
	SPI_MOSI	O_{12}		SPI master out/slave in pin. (Select by pin 2/5 power on strapping)
49	GPIO24	I/OOD_{12t}	VCC	General purpose IO.
	FWH_DIS	O_{12}		Firmware hub disable (Select by pin 2/5 power on strapping)
61	OVT#	$OD_{12,5v}$	VSB3V	Over temperature signal output.
40	GPIO12	I/OOD_{12t}	VCC	General purpose IO.
	WDTRST#	$OD_{12,5v}$		Watch dog timer signal output. (Selecty by register)
41	PECI_REQ#	OD_{12}	VCC	PECI REQUEST signal (Default)
	IRTX	O_{12}		Infrared Transmitter Output. (Selecty by register)
	GPIO13	I/OOD_{12t}		General purpose IO. (Selecty by register)
42	PECI_AVL	$IN_{st,lv}$	VCC	PECI AVAILABLE signal (Default)
	IRRX	IN_{st}		Infrared Receiver input. (Selecty by register)
	GPIO14	I/OOD_{12t}		General purpose IO. (Selecty by register)
43	SST	$I/O_{D8,st,lv}$	VCC	Intel SST hardware monitor interface. (Default)
	TSI_CLK	$I/OD_{12st,lv}$		Clock output for AMD TSI interface. (Select by register)
	IBX_CLK	$I/OD_{12st,lv}$		Clock output for INTEL PCH (IBex Peak) interface. (Select by register)
	GPIO15	$I/OOD_{12st,lv}$		General purpose IO. (Selecty by register)
44	PECI	$I/O_{s1,D8st,lv}$	VCC	Intel PECI hardware monitor interface. (Default)
	TSI_DAT	$I/OD_{12st,lv}$		AMD TSI data interface. (Select by register)
	IBX_SDA	$I/OD_{12st,lv}$		INTEL PCH (IBex Peak) data interface pin. (Select by register)
	GPIO16	$I/OOD_{12st,lv}$		General purpose IO. (Selecty by register)

6.7 ACPI Function Pins

Pin No.	Pin Name	Type	PWR	Description
62	PCIRST1#	$OD_{12,5v}$	VSB3V	It is an output buffer of LRESET#.
63	PCIRST2#	O_{24}	VSB3V	It is an output buffer of LRESET#.
64	PCIRST3#	O_{24}	VSB3V	It is an output buffer of LRESET#.
71	VCCGATE	O_{12}	VSB3V	Driver output for 5VCC. Connect this pin to the gate of a suitable NMOS.
72	DUALGATE	OD_{12}	VSB3V	Driver output for 5VSB. Connect this pin to the gate of a suitable PMOS.
73	S5#	$IN_{st,5v}$	VSB3V	S3# input. This pin companies with S3# to indicate operating state from S0 to S3 and S4/S5 sleep states.
74	ATXPG_IN	$IN_{st,5v}$	VSB3V	ATX Power Good input.

76	PWSIN#	$IN_{st,5v}$	VSB3V	Main power switch button input.
77	PWSOUT#	$OD_{12,5v}$	VSB3V	Panel Switch Output. This pin is low active and pulse output. It is power on request output#.
78	S3#	$IN_{st,5v}$	VSB3V	S3# Input is Main power on-off switch input.
79	PSON#	$OD_{12,5v}$	VSB3V	Power supply on-off control output. Connect to ATX power supply PS_ON# signal.
80	PWROK	$OD_{12,5v}$	VBAT	PWROK function, It is power good signal of VCC, which is delayed 400ms (default) as VCC arrives at 2.8V. It falls when S3# gets low.
81	RSMRST#	$OD_{12,5v}$	VBAT	Resume Reset# function, It is power good signal of VSB, which is delayed 66ms as VSB arrives at 2.95V. There is an option to set RSMRST# falls wheb VSB drops to 2.3V.
83	COPEN#	$IN_{st,5v}$	VBAT	Case Open Detection #. This pin is connected to a specially designed low power CMOS flip-flop back by the battery for case open state preservation during power loss.
84	VREF_EN	$IN_{st,5v}$	AVSB	Reference Voltage DAC output enable pin. Input high to this pin to enable VREF2 and VREF3. On the contrary, VREF2 and VREF3 will be disabled when input low to this pin. The specific timing can be referred in Figure
85	VREF3	AOUT	AVSB	Deafault 0.9V reference voltage output. The on/off sequence of this pin can be controlled by S3#, S5#, and VREF_EN. The specific timing can be referred in Figure
86	VREF2	AOUT	AVSB	Deafault 0.9V reference voltage output. The on/off sequence of this pin can be controlled by S3#, S5#, and VREF_EN. The specific timing can be referred in Figure
87	VREF1	AOUT	AVSB	Deafault 0.9V reference voltage output. Deafault 0.9V reference voltage output. The on/off sequence of this pin can be controlled by S3# and S5#. The specific timing can be referred in Figure

6.8 Bus Interface

Pin No.	Pin Name	Type	PWR	Description
51-53	BUSIN[0:2]	$IN_{st,lv}$	VCC	BUSIN input pins. Special level input VIH→ 0.9, VIL → 0.6
	GPIO2[5:7]	$I/OOD_{12st,lv}$		General purpose pin. (Select by pin 28 power on strapping)
54-56	BUSOUT[0:2]	OD_{12}	VSB3V	BUS OUT output pins.
	GPIO0[0:2]	I/OOD_{12t}		General purpose pin. (Select by pin 28 power on strapping)
57	SLOTOCC#	$IN_{st,5v}$	VSB3V	CPU SLOTOCC# input.
	GPIO03	I/OD_{12t}		General purpose pin.
58	GPIO04	I/OOD_{12t}	VSB3V	General purpose pin.
	LED_VSB	OD_{12}		Power LED for VSB
59	GPIO05	I/OOD_{12t}	VSB3V	General purpose pin.
	LED_VCC	OD_{12}		Power LED for VCC
60	GPIO06	I/OOD_{12t}	VSB3V	General purpose pin.
	BEEP	OD_{12}		Beep pin.
	ALERT#	OD_{12}		Alert a signal when something issues

6.9 KBC Function

Pin No.	Pin Name	Type	PWR	Description
38	KBRST#	$OD_{16,u10,5v}$	VCC	Keyboard reset. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P20)
39	GA20	$OD_{16,u10,5v}$	VCC	Gate A20 output. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P21)
66	KDATA	$I/OD_{16st,5v}$	VSB3V	Keyboard Data.
67	KCLK	$I/OD_{16st,5v}$	VSB3V	Keyboard Clock.
68	MDAT	$I/OD_{16st,5v}$	VSB3V	PS2 Mouse Data.
69	MCLK	$I/OD_{16st,5v}$	VSB3V	PS2 Mouse Clock.

7. Function Description

7.1. Power on Strapping Option

The F71889 provides eight pins for power on hardware strapping to select functions. Power on strapping value follows TTL voltage level. Below table describes how to set the functions you want.

Table1. Power on trap configuration

Pin No.	Symbol	Value	Description
2	FWH_TRAP	1	FWH as a primary BIOS (Default)
		0	SPI as a primary BIOS
3	PWM_DC	1	Fan control mode: PWM mode. (Default)
		0	Fan control mode: DAC mode.
5	SPI_TRAP	1	SPI function disable(Default)
		0	SPI function enable
28	BSGPIO_TRAP	1	Pin 51-56 are Bus Interface functions (Default)
		0	Pin 51-56 are GPIO pins
104	VIDIO_TRAP	Pull high 1K	Pin 100-116 as LPT interfaces
		Pull high 20K	Pin 100-116 as PVID Controller
		Pull down 1K	Pin 102/103/111/112 as SVID Controller
		Pull down 47K	Pin 100-103 and pin 105-116 as GPIO pins
121	FAN60_100	1	Fan full duty is 60%.(Default)
		0	Fan full duty is 100%.
122	80PORT_TRAP	1	Enable the 80 port function. (Default)
		0	Disable the 80 port function.
124	Config4E_2E	1	Configuration Register I/O port is 4E/4F. (Default)
		0	Configuration Register I/O port is 2E/2F.

7.2. Hardware Monitor

For the 8-bit ADC has the 8mv LSB, the maximum input voltage of the analog pin is 2.04V. Therefore the voltage under 2.04V (ex:1.5V) can be directly connected to these analog inputs. The voltage higher than 2.04V should be reduced by a factor with external resistors so as to obtain the input range. Only 3Vcc is an exception for it is main power of the F71889. Therefore 3Vcc can directly connect to this chip's power pin and need no external resistors. There are two functions in this pin with 3.3V. The first function is to supply internal analog power of the F71889 and the second function is that voltage with 3.3V is connected to internal serial resistors to monitor the +3.3V voltage. The internal serial resistors are two 150K ohm, so that the internal reduced voltage is half of +3.3V.

There are four voltage inputs in the F71889 and the voltage divided formula is shown as follows:

$$VIN = V_{+12V} \times \frac{R_2}{R_1 + R_2}$$ where V_{+12V} is the analog input voltage, for example.

If we choose R1=27K, R2=5.1K, the exact input voltage for V+12v will be 1.907V, which is within the tolerance. As for application circuit, it can be refer to the figure shown as follows.

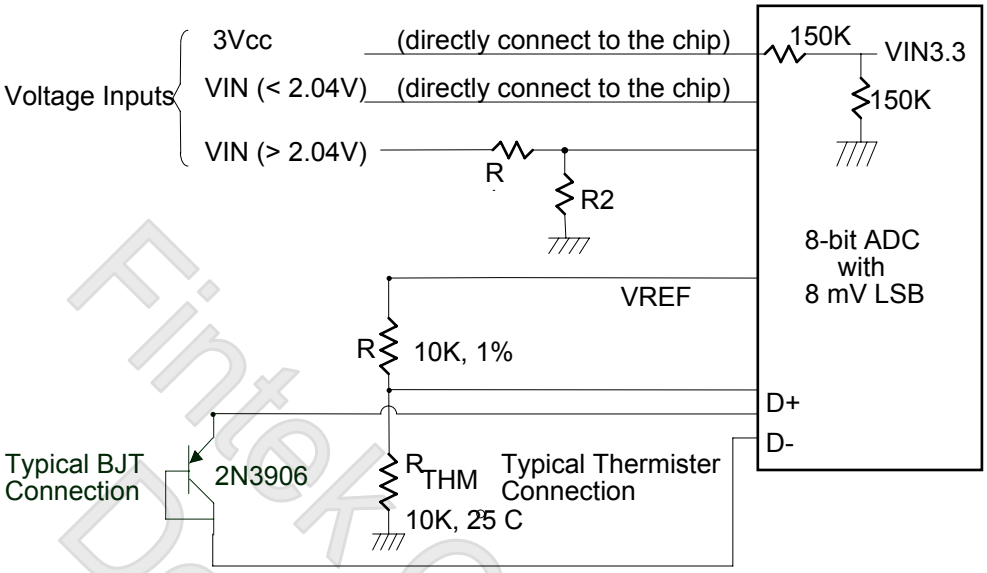
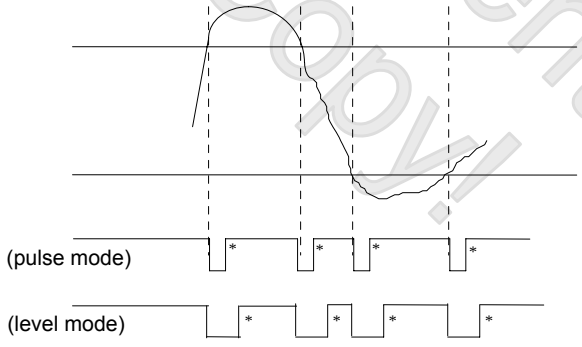


Figure 2. Hardware monitor configuration

SMI# interrupt for voltage is shown as figure. Voltage exceeding or going below high limit will cause an interrupt if the previous interrupt has been reset by writing "1" all the interrupt Status Register. Voltage exceeding or going below low limit will result the same condition as voltage exceeding or going below high limit.



*Interrupt Reset when Interrupt Status Registers are written 1

Voltage SMI# Mode

Figure 3

The F71889 monitors three remote temperature sensors. These sensors can be measured from -40°C to 127°C. More detail please refer to register description.

Table 2. Remote-sensor transistor manufacturers

Manufacturer	Model Number
Panasonic	2SB0709 2N3906
Philips	PMBT3906

Monitor Temperature from "thermistor"

The F71889 can connect three thermistors to measure environment temperature or remote temperature. The specification of thermistor should be considered to (1) value is 3435K (2) resistor value is 10K ohm at 25°C. In the Figure 7-1, the thermistor is connected by a serial resistor with 10K ohm, thenand then connected to VREF.

Monitor Temperature from "thermal diode"

Also, if the CPU, GPU or external circuits provide thermal diode for temperature measurement, the F71889 is capable to these situations. The build-in reference table is for PNP 2N3906 transistor, and each different kind of thermal diode should be matched with specific offset and BJT gain. In the Figure 7-1, the transistor is directly connected into temperature pins.

ADC Noise Filtering

The ADC is integrating type with inherently good noise rejection. Micro-power operation places constraints on high-frequency noise rejection; therefore, careful PCB board layout and suitable external filtering are required for high-accuracy remote measurement in electronically noisy environment. High frequency EMI is best filtered at D+ and D- with an external 2200pF or 3300pF capacitor. Too high capacitance may introduce errors due to the rise time of the switched current source. Nearly all noise sources tested cause the ADC measurement to be higher than the actual temperature, depending on the frequency and amplitude.

Over Temperature Signal (OVT#)

OVT# alert for temperature is shown as figure 7-4. When monitored temperature exceeds the over-temperature threshold value, OVT# will be asserted until the temperature goes below the hysteresis temperature.

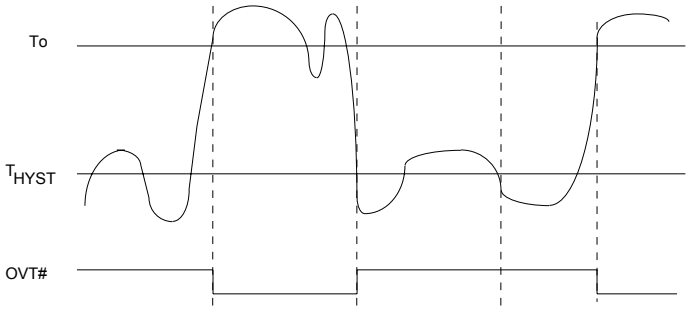
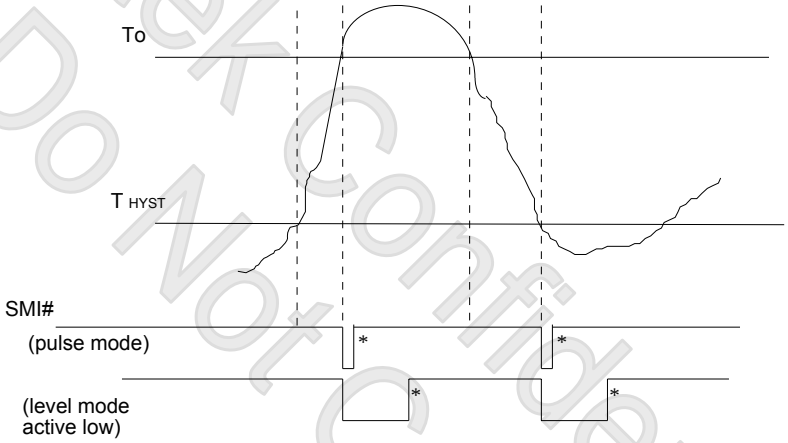


Figure 4

Temperature PME#

PME# interrupt for temperature is shown as figure 7-5. Temperature exceeding high limit or going below hysteresis will cause an interrupt if the previous interrupt has been reset by writing "1" all the interrupt Status Register.



*Interrupt Reset when Interrupt Status Registers are written 1

Figure 5

Fan speed count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over 5V. If the input signals from the tachometer outputs are over the 5V, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as follows:

Determine the fan counter according to:

$$\text{Count} = \frac{1.5 \times 10^6}{\text{RPM}}$$

In other words, the fan speed counter has been read from register, the fan speed can be evaluated by the following equation. As for fan, it would be best to use 2 pulses tachometer output per round.

$$\text{RPM} = \frac{1.5 \times 10^6}{\text{Count}}$$

Fan speed control

The F71889 provides 2 fan speed control methods:

1. DAC FAN CONTROL 2. PWM DUTY CYCLE

DAC Fan Control

The range of DC output is 0~VCC, controlled by 8-bit register. 1 LSB is about 0.013V (VCC=3.3V). The output DC voltage is amplified by external OP circuit, thus to reach maximum FAN OPERATION VOLTAGE, 12V. The output voltage will be given as followed:

$$\text{Output\_voltage (V)} = \text{Vcc} \times \frac{\text{Programmed 8bit Register Value}}{256}$$

And the suggested application circuit for linear fan control would be:

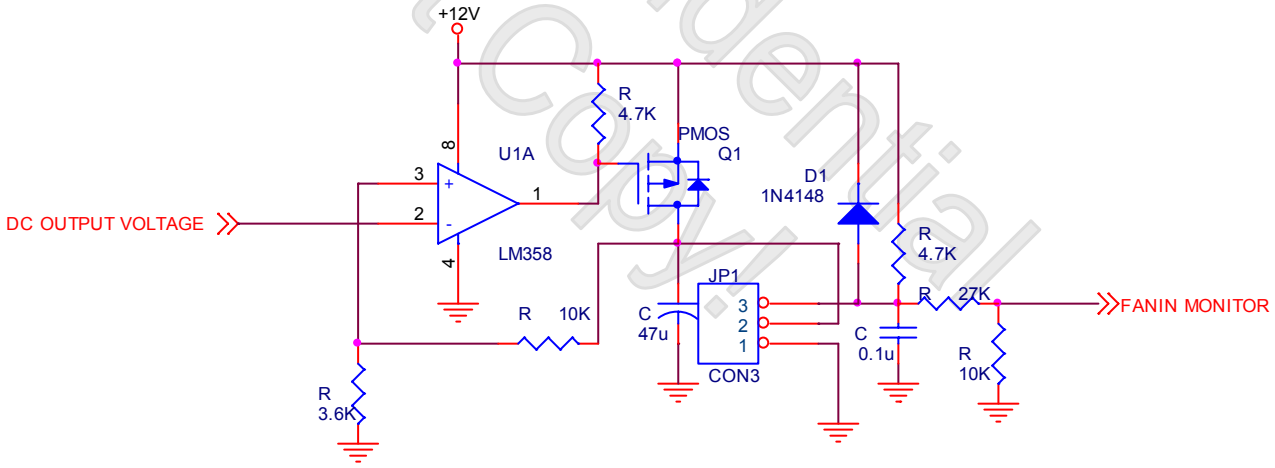


Figure 6 DAC fan control application circuit

PWM duty Fan Control

The duty cycle of PWM can be programmed by an 8-bit register. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty\_cycle}(\%) = \frac{\text{Programmed 8bit Register Value}}{255} \times 100\%$$

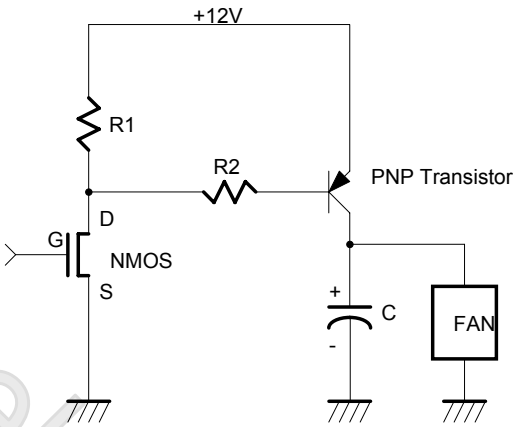


Figure 7 +12/5V PWM fan control application circuit

Fan speed control mechanism

There are some modes to control fan speed and they are 1.Manual mode, 2.Stage auto mode, 3. Linear auto mode. More detail, please refer to the description of registers.

Manual mode

For manual mode, it generally acts as software fan speed control.

Stage auto mode

At this mode, the F71889 provides automatic fan speed control related to temperature variation of CPU/GPU or the system. The F71889 can provide four temperature boundaries and five intervals, and each interval has its related fan speed count. All these values should be set by BIOS first.

There are some examples as below:

A. Stage auto mode (PWM Duty)

Set temperature as 60°C, 50°C, 40°C, 30°C and Duty as 100%, 90%, 80%, 70%, 60%

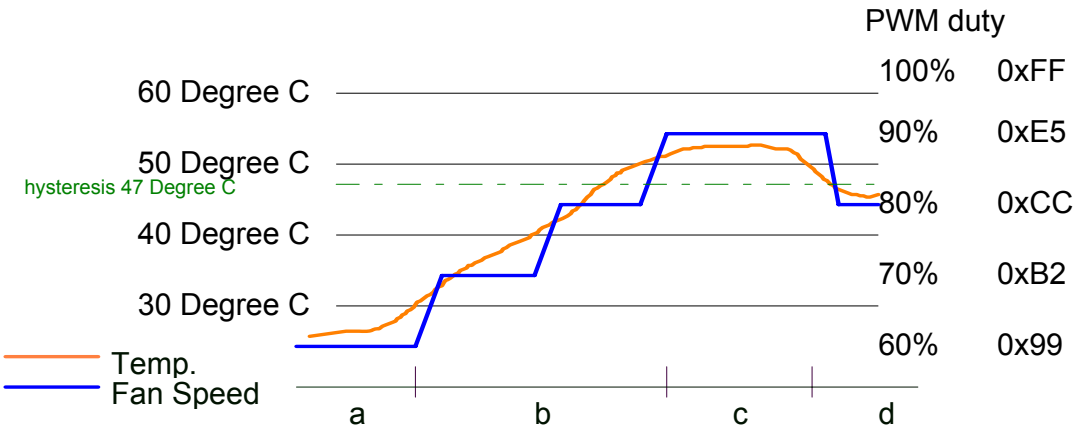


Figure 8 Stage mode fan control illustration-2

a. Once temp. is under 30°C, the lowest fan speed keeps 60% PWM duty
b. Once temp. is over 30°C,40°C,50°C, the fan speed will vary from 60% to 90% PWM duty and increase with temp. level.
c. Once temp. keeps in 55°C, fan speed keeps in 90% PWM duty
d. If set the hysteresis as 3°C (default 4°C), once temp reduces under 47°C, fan speed reduces to 80% PWM duty and stays there.

B. Stage auto mode (RPM%)

Set temperature as 60°C, 50°C, 40°C, 30°C and assume the Full Speed is 6000rpm, set 90% of full speed RPM(5400rpm), 80%(4800rpm), 70%(4200rpm), 60%(3600rpm) of full speed RPM

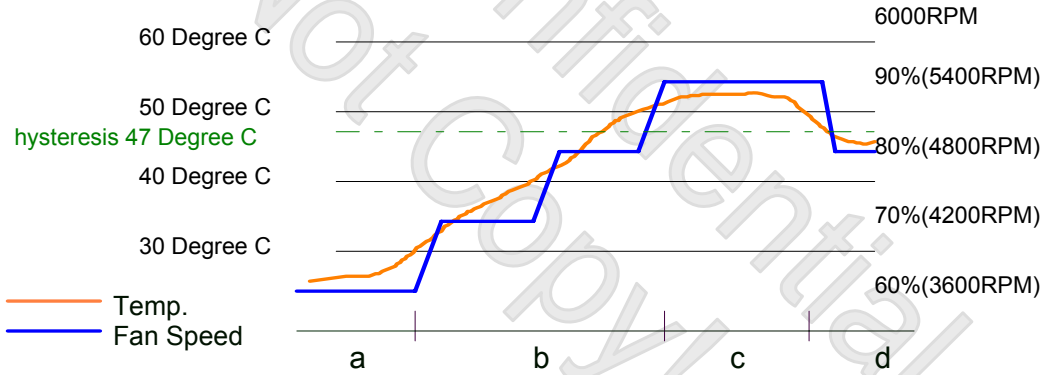


Figure 9 Stage mode fan control illustration-3

a. Once temp. is under 30°C, the lowest fan speed keeps 60% of full speed (3600RPM).
b. Once temp. is over 30°C,40°C,50°C, the fan speed will vary from 3600RPM to 5400RPM and increase with temp. level.
c. Once temp. keeps in 55°C, fan speed keeps in 90% of full speed (5400RPM)
d. If set the hysteresis as 3°C (default 4°C), once temp reduces under 47°C, fan speed reduces to 4800RPM and stays there.

Linear auto mode

Otherwise, F71889 supports linear auto mode. Below has two examples to describe this mode. More detail, please refer the register description.

A. Linear auto mode (PWM Duty I)

Set temperature as 70°C, 60°C, 50°C, 40°C and Duty as 100%, 70%, 60%, 50%, 40%

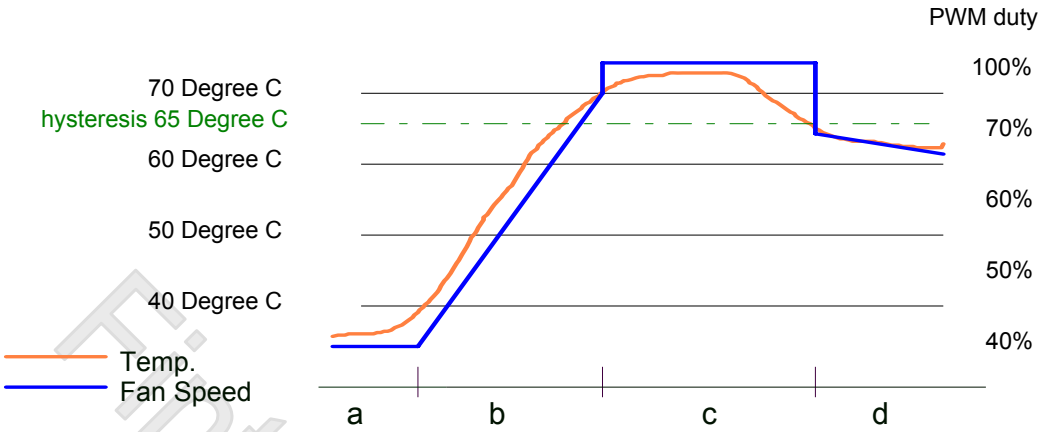


Figure 10 Linear mode fan control illustration-1

a. Once temp. is under 40°C, the lowest fan speed keeps 40% PWM duty
b. Once temp. is over 40°C,50°C,60°C, the fan speed will vary from 40% to 70% PWM duty and linearly increase with temp. variation. The temp.-fan speed monitoring and flash interval is 1sec.
c. Once temp. goes over 70°C, fan speed will directly increase to 100% PWM duty (full speed)
d. If set the hysteresis as 5°C (default is 4°C), once temp reduces under 65°C (not 70°C), fan speed reduces from 100% PWM duty and decrease linearly with temp..

B. Linear auto mode (RPM%)

Set temperature as 70°C, 60°C, 50°C, 40°C and if full speed is 6000RPM, setting 100%, 70%, 60%, 50%, 40% of full speed.

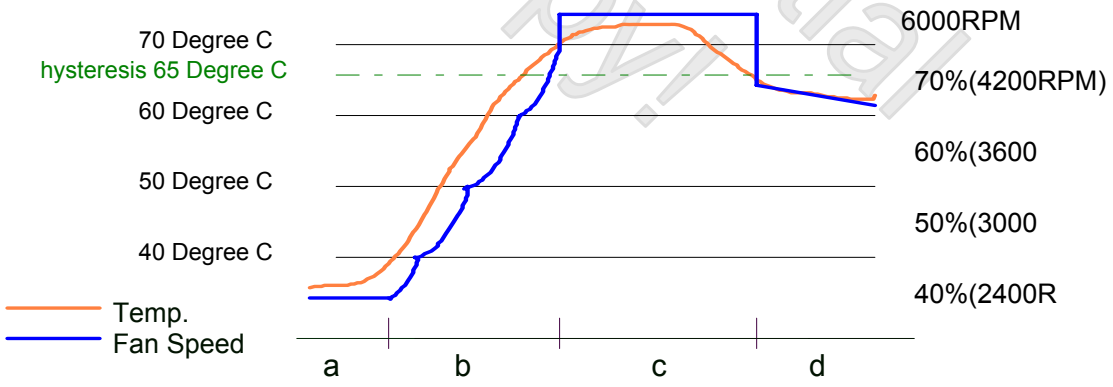


Figure 11 Linear mode fan control illustration-2

a. Once temp. is under 40°C, the lowest fan speed keeps 40% of full speed (2400RPM)
b. Once temp. is over 40°C,50°C,60°C, the fan speed will vary from 40% to 70% of full speed and almost linearly increase with temp. variation. The temp.-fan speed monitoring and flash interval is 1sec.
c. Once temp. goes over 70°C, fan speed will directly increase to full speed 6000RPM.
d. If set the hysteresis as 5°C, once temp reduces under 65°C (not 70°C), fan speed reduces from full speed and decrease linearly with temp..

PWMOUT Duty-cycle operating process

In both "Manual RPM" and "Temperature RPM" modes, the F71889 adjust PWMOUT duty-cycle according to current fan count and expected fan count. It will operate as follows:

(1). When expected count is 0xFFF, PWMOUT duty-cycle will be set to 0x00 to turn off fan.
(2). When expected count is 0x000, PWMOUT duty-cycle will be set to 0xFF to turn on fan with full speed.
(3). If both (1) and (2) are not true,
(4). When PWMOUT duty-cycle decrease to MIN_DUTY(≠ 00h), obviously the duty-cycle will decrease to 00h next, the F71889 will keep duty-cycle at 00h for 1.6 seconds. After that, the F71889 starts to compare current fan count and expected count in order to increase or decrease its duty-cycle. This ensures that if there is any glitch during the period, the F71889 will ignore it.

Figure 12

FAN_FAULT#

Fan_Fault# will be asserted when the fan speed doesn't meet the expected fan speed within a programmable period (default is 11 seconds) or when fan stops with respect to PWM duty-cycle which should be able to turn on the fan. There are two conditions may cause the FAN_FAULT# event.

(1). When PWM_Duty reaches 0xFF, the fan speed count can't reach the fan expected count in time. (Figure 7-13)

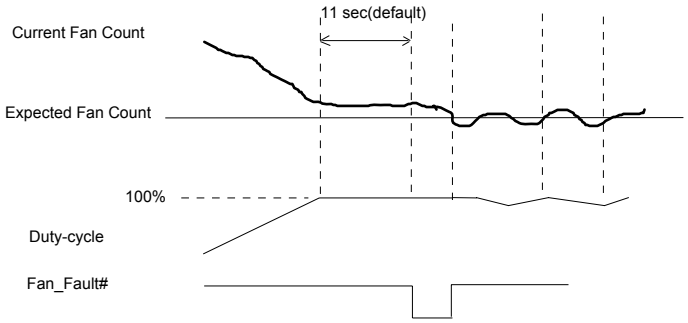


Figure 13 FAN_FAULT# event

(2). After the period of detecting fan full speed, when PWM_Duty > Min. Duty, and fan count still in 0xFFF.

T1 Architecture

The F71889 implement the Intel PECI/SST interface and AMD TSI interface to collect the CPU temperature for fan control. The CPU temperature source could be programmed to be from external diode, Intel PECI interface or AMD TSI interface.

Device registers, the following is a register map order which shows a summary of all registers. Please refer each one register if you want more detail information.

Register CR01 ~ CR03 → Configuration Registers

Register CR0A ~ CR0F → PECI/SST/TSI Control Register

Register CR10 ~ CR4F → Voltage Setting Register

Register CR60 ~ CR8E → Temperature Setting Register

Register CR90 ~ CRDF → Fan Control Setting Register

→Fan1 Detail Setting CRA0 ~ CRAF

→Fan2 Detail Setting CRB0 ~ CRBF

→Fan3 Detail Setting CRC0 ~ CRCF

Register CR5A ~ CR5D → HW Chip ID and Vender ID Register

7.5.1 Configuration Register — Index 01h

Bit	Name	R/W	Default	Description
7	BETA_EN	R/W	1	0: disable the T1 beta compensation. 1: enable the T1 beta compensation.
6	INTEL_MODEL	R/W	1	0: AMD model. 1: Intel model.

<table>
<tr><td>5</td><td>TSI_EN</td><td>R/W</td><td>0</td><td>0: Disable the TSI function via PECI/SST pins.
1: Enable the TSI function via PECI/SST pins.
This bit accompanying with INTEL_MODEL and SST_EN will determine the availability of AMD TSI, Intel PCH SMBus, PECI and SST.
<table>
<tr><th colspan="3">Setting</th><th colspan="4">Results</th></tr>
<tr><th>INTEL_ MODEL (CR01, bit6)</th><th>TSI_EN (CR01, bit5)</th><th>SST_EN (CR0A, bit4)</th><th>PECI</th><th>SST</th><th>AMD TSI</th><th>Intel PCH SMBus</th></tr>
<tr><td>0</td><td>0</td><td>X</td><td>N</td><td>N</td><td>N</td><td>N</td></tr>
<tr><td>0</td><td>1</td><td>X</td><td>N</td><td>N</td><td>Y</td><td>N</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Y</td><td>N</td><td>N</td><td>N</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Y</td><td>Y</td><td>N</td><td>N</td></tr>
<tr><td>1</td><td>1</td><td>X</td><td>N</td><td>N</td><td>N</td><td>Y</td></tr>
</table>
This bit is cleared by LRESET#.</td></tr>
<tr><td>4-3</td><td>Reserved</td><td>-</td><td>-</td><td>Reserved</td></tr>
<tr><td>2</td><td>POWER_DOWN</td><td>R/W</td><td>0</td><td>Hardware monitor function power down.</td></tr>
<tr><td>1</td><td>FAN_START</td><td>R/W</td><td>1</td><td>Set one to enable startup of fan monitoring operations; a zero puts the part in standby mode.</td></tr>
<tr><td>0</td><td>V_T_START</td><td>R/W</td><td>1</td><td>Set one to enable startup of temperature and voltage monitoring operations; a zero puts the part in standby mode.</td></tr>
</table>

7.5.2 Configuration Register — Index 02h

Bit	Name	R/W	Default	Description
7	Reserved	R/W	0	Dummy register.
6	CASE_BEEP_EN	R/W	0	0: Disable case open event output via BEEP. 1: Enable case open event output via BEEP.
5-4	OVT_MODE	R/W	0	00: The OVT# will be low active level mode. 01: The OVT# will be high active level mode. 10: The OVT# will indicate by 1Hz LED function. 11: The OVT# will indicate by (400/800HZ) BEEP output.
3	Reserved	R/W	0	Dummy register.
2	CASE_SMI_EN	R/W	0	0: Disable case open event output via PME. 1: Enable case open event output via PME.
1-0	ALERT_MODE	R/W	0	00: The ALERT# will be low active level mode. 01: The ALERT# will be high active level mode. 10: The ALERT# will indicate by 1Hz LED function. 11: The ALERT# will indicate by (400/800HZ) BEEP output.

7.5.3 Case Status Register — Index 03h

Bit	Name	R/W	Default	Description
7-1	Reserved	R/W	0	Return 0 when read.
0	CASE_STS	R/W	0	Case open event status, write 1 to clear if case open event cleared.

7.5.4 Debut Port Temp Register — Index 04h

Bit	Name	R/W	Default	Description
7-2	Reserved	R/W	0	Return 0 when read.

1-0	DPORT_TEMP_SEL	R/W	01	Debug port temperature source select: 00: 0xff. 01: T1 reading. 10: T2 reading. 11: T3 reading.

7.5.5 SST and VTT_SEL Register — Index 0Ah

Bit	Name	R/W	Default	Description
7-5	Reserved	-	0	Reserved.
4	SST_EN_REG	R/W	0	Set this bit "1" and select Intel model will enable SST interface. Otherwise will disable SST interface This bit is cleared by LRESET#.
3-2	VTT_SEL	R/W	0	PECI (Vtt) voltage select. 00: Vtt is 1.23V 01: Vtt is 1.13V 10: Vtt is 1.00V 11: Vtt is 1.00V
1	DIG_T1_EN	R/W	0	0: Disable the digital interface of T1 (PECI/TSI). 1: Enable the digital interface of T1.
0	DIODE_T1_EN	R/W	1	0: Disable the D1+ measurement. 1: Enable the D1+ measurement.

7.5.6 PECI Address Register — Index 0Bh

Bit	Name	R/W	Default	Description
7-4	CPU_SEL	R/W	0	Select the Intel CPU socket number. 0000: no CPU presented. PECI host will use Ping() command to find CPU address. 0001: CPU is in socket 0, i.e. PECI address is 0x30. 0010: CPU is in socket 0, i.e. PECI address is 0x31. 0100: CPU is in socket 0, i.e. PECI address is 0x32. 1000: CPU is in socket 0, i.e. PECI address is 0x33. Otherwise are reserved.
3-1	Reserved	-	0	Reserved.
0	DOMAIN1_EN	R/W	0	If the CPU selected is dual core. Set this register 1 to read the temperature of domain1.

7.5.7 TCC TEMP Register — Index 0Ch

Bit	Name	R/W	Default	Description
7-0	TCC_TEMP/TSI_OFFSET	R/W	8'h55	TCC Activation Temperature/TSI Offset. When PECI is enabled, the absolute value of CPU temperature is calculated by the equation: CPU_TEMP = TCC_TEMP + PECI Reading. The range of this register is -128 ~ 127. When AMD TSI or Intel PCH SMBus is enabled, this byte is used as the offset to be added to the reading.

7.5.8 SST ADDR Register — Index 0Dh

Bit	Name	R/W	Default	Description
7-0	SST_ADDR/ SMBUS_ADDR	R/W	8'h4C	When AMD TSI or Intel PCH SMBus is enabled, this byte is used as SMBUS_ADDR. SMBUS_ADDR[7:1] is the slave address sent by the embedded master to fetch the temperature. Otherwise, this byte is used as SST_ADDR if SST is enabled.

7.5.9 Voltage DIV Register — Index 0Eh

Bit	Name	R/W	Default	Description
7-6	VIN4_DIV	R/W	0	The value indicates the divisor of the voltage source. 00: voltage source is directly connected to VIN4. 01: voltage source is divided by 2 and connect to VIN4. 10: voltage source is divided by 4 and connect to VIN4. 11: voltage source is divided by 16 and connect to VIN4.
5-4	VIN3_DIV	R/W	0	The value indicates the divisor of the voltage source. 00: voltage source is directly connected to VIN3. 01: voltage source is divided by 2 and connect to VIN3. 10: voltage source is divided by 4 and connect to VIN3. 11: voltage source is divided by 16 and connect to VIN3.
3-2	VIN2_DIV	R/W	0	The value indicates the divisor of the voltage source. 00: voltage source is directly connected to VIN2. 01: voltage source is divided by 2 and connect to VIN2. 10: voltage source is divided by 4 and connect to VIN2. 11: voltage source is divided by 16 and connect to VIN2.
1-0	VIN1_DIV	R/W	0	The value indicates the divisor of the voltage source. 00: voltage source is directly connected to VIN1. 01: voltage source is divided by 2 and connect to VIN1. 10: voltage source is divided by 4 and connect to VIN1. 11: voltage source is divided by 16 and connect to VIN1. Above is available only if SST is enabled. Otherwise, bit 7-1 will be used as I2C_ADDR if Intel PCH SMBus is enabled.

7.5.10 PECI Config. and Voltage Register — Index 0Fh

Bit	Name	R/W	Default	Description
7	PECI_ERR	R	-	0: no PECI error occurred. 1: PECI error occurred.. The condition of PECI_ERR is the PECI return all 0's if PECI_AVL asserts at start of PECI message and during PECI message for continuous three times.
6	PECI_NOT_AVL	R	-	0: PECI is available. 1: PECI is not available. The condition of PECI_ERR is the PECI return all 0's if PECI_AVL asserts at start of PECI message and de-asserts during PECI message for continuous three times.
5	PECI_REQ_EN	R/W	1	0: disable the PECI_REQ# function. 1: Enable the PECI_REQ# function.
4	PECI_AVL_EN	R/W	1	0: disable the PECI_AVL function. 1: Enable the PECI_AVL function.
3-2	VIN6_DIV	R/W	0	The value indicates the divisor of the voltage source. 00: voltage source is directly connected to VIN6. 01: voltage source is divided by 2 and connect to VIN6. 10: voltage source is divided by 4 and connect to VIN6. 11: voltage source is divided by 16 and connect to VIN6.

1-0	VIN5_DIV	R/W	0	The value indicates the divisor of the voltage source. 00: voltage source is directly connected to VIN5. 01: voltage source is divided by 2 and connect to VIN5. 10: voltage source is divided by 4 and connect to VIN5. 11: voltage source is divided by 16 and connect to VIN5. VIN6_DIV[0] and VIN5_DIV are used as TSI_TEMP_SEL[2:0] if Intel PCH SMBus is enabled. TSI_TEMP_SEL is used to select the temperature source for fan control.

TSI_TEMP_SEL	Temperature Source
000	Maximum of MCH or CPU
001	PCH
010	CPU
011	MCH
100	DIMM0
101	DIMM1
110	DIMM2
111	DIMM3

Voltage Setting

7.5.11 Voltage1 PME# Enable Register — Index 10h

Bit	Name	R/W	Default	Description
7-2	Reserved	--	0	Reserved
1	EN_V1_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for VIN1.
0	Reserved	--	0	Reserved

7.5.12 Voltage1 Interrupt Status Register — Index 11h

Bit	Name	R/W	Default	Description
7-2	Reserved	--	0	Reserved
1	V1_ EXC _STS	R/W	0	This bit is set when the VIN1 is over the high limit. Write 1 to clear this bit, write 0 will be ignored.
0	Reserved	--	0	Reserved

7.5.13 Voltage1 Exceeds Real Time Status Register 1 — Index 12h

Bit	Name	R/W	Default	Description
7-2	Reserved	--	0	Reserved
1	V1_EXC	RO	0	A one indicates VIN1 exceeds the high or low limit. A zero indicates VIN1 is in the safe region.
0	Reserved	--	0	Reserved

7.5.14 Voltage1 BEEP Enable Register — Index 13h

Bit	Name	R/W	Default	Description
7-2	Reserved	--	0	Reserved
1	EN_V1_BEEP	R/W	0	A one enables the corresponding interrupt status bit for BEEP output of VIN1.
0	Reserved	--	0	Reserved

7.5.15 Voltage reading and limit— Index 20h- 4Fh

Address	Attribute	Default Value	Description
20h	RO	--	VCC3V reading. The unit of reading is 8mV.

21h	RO	--	VIN1 (Vcore) reading. The unit of reading is 8mV.
22h	RO	--	VIN2 reading. The unit of reading is 8mV.
23h	RO	--	VIN3 reading. The unit of reading is 8mV.
24h	RO	--	VIN4 reading. The unit of reading is 8mV.
25h	RO	--	VIN5 reading. The unit of reading is 8mV.
26h	RO	--	VIN6 reading. The unit of reading is 8mV.
27h	RO	--	VSB3V reading. The unit of reading is 8mV.
28h	RO	--	VBAT reading. The unit of reading is 8mV.
29~2Fh	RO	FF	Reserved
30~31h	RO	FF	Reserved
32h	R/W	FF	V1 High Limit setting register. The unit is 8mV.
33~4Fh	RO	FF	Reserved

Temperature Setting

7.5.16 Temperature PME# Enable Register — Index 60h

Bit	Name	R/W	Default	Description
7	EN_ T3_OVT_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP3 exceeds OVT limit setting.
6	EN_ T2_ OVT_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds OVT setting.
5	EN_ T1_ OVT_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds OVT setting.
4	Reserved	R/W	0	Reserved
3	EN_ T3_EXC_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP3 exceeds high limit setting.
2	EN_ T2_EXC_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds high limit setting.
0	Reserved	R/W	0	Reserved

7.5.17 Temperature Interrupt Status Register — Index 61h

Bit	Name	R/W	Default	Description
7	T3_OVT_STS	R/W	0	A one indicates TEMP3 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored.
6	T2_OVT _STS	R/W	0	A one indicates TEMP2 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored.
5	T1_OVT _STS	R/W	0	A one indicates TEMP1 temperature sensor has exceeded OVT limit or below the “OVT limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored.
4	Reserved	R/W	0	Reserved
3	T3_EXC _STS	R/W	0	A one indicates TEMP3 temperature sensor has exceeded high limit or below the “high limit –hysteresis”. Write 1 to clear this bit, write 0 will be ignored.
2	T2_EXC _STS	R/W	0	A one indicates TEMP2 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored.

1	T1_EXC _STS	R/W	0	A one indicates TEMP1 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored.
0	Reserved	R/W	0	Reserved

7.5.18 Temperature Real Time Status Register — Index 62h

Bit	Name	R/W	Default	Description
7	T3_OVT	R/W	0	Set when the TEMP3 exceeds the OVT limit. Clear when the TEMP3 is below the “OVT limit –hysteresis” temperature.
6	T2_OVT	R/W	0	Set when the TEMP2 exceeds the OVT limit. Clear when the TEMP2 is below the “OVT limit –hysteresis” temperature.
5	T1_OVT	R/W	0	Set when the TEMP1 exceeds the OVT limit. Clear when the TEMP1 is below the “OVT limit –hysteresis” temperature.
4	Reserved	R/W	0	Reserved
3	T3_EXC	R/W	0	Set when the TEMP3 exceeds the high limit. Clear when the TEMP3 is below the “high limit –hysteresis” temperature.
2	T2_EXC	R/W	0	Set when the TEMP2 exceeds the high limit. Clear when the TEMP2 is below the “high limit –hysteresis” temperature.
1	T1_EXC	R/W	0	Set when the TEMP1 exceeds the high limit. Clear when the TEMP1 is below the “high limit –hysteresis” temperature.
0	Reserved	R/W	0	Reserved

7.5.19 Temperature BEEP Enable Register — Index 63h

Bit	Name	R/W	Default	Description
7	EN_ T3_OVT_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP3 exceeds OVT limit setting.
6	EN_ T2_ OVT_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds OVT limit setting.
5	EN_ T1_ OVT_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds OVT limit setting.
4	Reserved	R/W	0	Reserved
3	EN_ T3_EXC_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP3 exceeds high limit setting.
2	EN_ T2_EXC_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds high limit setting.
0	Reserved	R/W	0	Reserved

7.5.20 OVT Output Enable Register 1 — Index 66h

Bit	Name	R/W	Default	Description
7	EN_T3_ALERT	R	0	Enable temperature 3 alert event (asserted when temperature over high limit)
6	EN_T2_ALERT	R	0	Enable temperature 2 alert event (asserted when temperature over high limit)
5	EN_T1_ALERT	R	0	Enable temperature 1 alert event (asserted when temperature over high limit)
4	Reserved	R	0	Reserved.
3	EN_T3_OVT	R/W	0	Enable over temperature (OVT) mechanism of temperature3.
2	EN_T2_OVT	R/W	0	Enable over temperature (OVT) mechanism of temperature2.
1	EN_T1_OVT	R/W	1	Enable over temperature (OVT) mechanism of temperature1.
0	Reserved	R	0h	Reserved.

7.5.21 Temperature Sensor Type Register — Index 6Bh

Bit	Name	R/W	Default	Description
7-4	Reserved	RO	0	--
3	T3_MODE	R/W	1	0: TEMP3 is connected to a thermistor 1: TEMP3 is connected to a BJT.(default)
2	T2_MODE	R/W	1	0: TEMP2 is connected to a thermistor. 1: TEMP2 is connected to a BJT. (default)
1	T1_MODE	R/W	1	0: TEMP1 is connected to a thermistor 1: TEMP1 is connected to a BJT.(default)
0	Reserved	R	0h	--

7.5.22 TEMP1 Limit Hystersis Select Register -- Index 6Ch

Bit	Name	R/W	Default	Description
7-4	TEMP1_HYS	R/W	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).
3-0	Reserved	R	0h	--

7.5.23 TEMP2 and TEMP3 Limit Hystersis Select Register -- Index 6Dh

Bit	Name	R/W	Default	Description
7-4	TEMP3_HYS	R/W	2h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).
3-0	TEMP2_HYS	R/W	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).

7.5.24 DIODE OPEN Status Register -- Index 6Fh

Bit	Name	R/W	Default	Description
7-4	Reserved	RO	0h	Reserved
3	T3_DIODE_OPEN	RO	0h	External diode 3 is open
2	T2_DIODE_OPEN	RO	0h	External diode 2 is open
1	T1_DIODE_OPEN	RO	0h	This register indicates the abnormality of temperature 1 measurement. When TSI interface is enabled, it indicates the error of not receiving NACK bit or a timeout occurred. When PECI interface is enabled, it indicates an error code (0x0080 or 0x0081) is received from PECI slave. When external diode is used, it indicates the BJT is open or short.
0	Reserved	R	0h	--

Temperature — Index 70h- 8Fh

Address	Attribute	Default Value	Description
70h	Reserved	FFh	Reserved
71h	Reserved	FFh	Reserved
72h	RO	--	Temperature 1 reading. The unit of reading is 1°C.At the moment of reading this register.
73h	RO	--	Reserved
74h	RO	--	Temperature 2 reading. The unit of reading is 1°C.At the moment of reading this register.
75h	RO	--	Reserved

76h	RO	--	Temperature 3 reading. The unit of reading is 1°C.At the moment of reading this register.
77-79h	RO	--	Reserved
7Ah	RO	--	The raw data of T3 read from digital interface. (Only available if Intel IBX interface is enabled)
7Bh	RO	--	The raw data of T2 read from digital interface. (Only available if Intel IBX interface is enabled)
7Ch	RO	--	The raw data of T1 read from digital interface.
7Dh	RO	--	The raw data of T1 read from D1+.
7Eh	R/W	00h-	T1 Slope Adjust.
7Fh	R/W	00h	T1 Source Select.
80h	Reserved	FFh	Reserved
81h	Reserved	FFh	Reserved
82h	R/W	64h	Temperature sensor 1 OVT limit. The unit is 1°C.
83h	R/W	55h	Temperature sensor 1 high limit. The unit is 1°C.
84h	R/W	64h	Temperature sensor 2 OVT limit. The unit is 1°C.
85h	R/W	55h	Temperature sensor 2 high limit. The unit is 1°C.
86h	R/W	55h	Temperature sensor 3 OVT limit. The unit is 1°C.
87h	R/W	46h	Temperature sensor 3 high limit. The unit is 1°C.
88-8Bh	RO	--	Reserved
8C~8Dh	RO	FFH	Reserved

7.5.25 T1 Slope Adjust Register -- Index 7Eh

Bit	Name	R/W	Default	Description
7	DIG_T1_ADD	R/W	0h	This bit is the sign bit for digital T1 reading slope adjustment. See DIG_T1_SCALE below for detail.

<table>
<tr><td>6-4</td><td>DIG_T1_SCALE</td><td>R/W</td><td>0h</td><td>Accompanying with DIG_T1_ADD, the slope adjustment of digital T1 is listed.
<table>
<tr><th>DIG_T1_ADD</th><th>DIG_T1_SCALE</th><th>Slope</th></tr>
<tr><td>0</td><td>000</td><td>No adjustment</td></tr>
<tr><td>0</td><td>001</td><td>1/2</td></tr>
<tr><td>0</td><td>010</td><td>3/4</td></tr>
<tr><td>0</td><td>011</td><td>7/8</td></tr>
<tr><td>0</td><td>100</td><td>15/16</td></tr>
<tr><td>0</td><td>101</td><td>31/32</td></tr>
<tr><td>0</td><td>110</td><td>63/64</td></tr>
<tr><td>0</td><td>111</td><td>127/128</td></tr>
<tr><td>1</td><td>000</td><td>No adjustment</td></tr>
<tr><td>1</td><td>001</td><td>3/2</td></tr>
<tr><td>1</td><td>010</td><td>5/4</td></tr>
<tr><td>1</td><td>011</td><td>9/8</td></tr>
<tr><td>1</td><td>100</td><td>17/16</td></tr>
<tr><td>1</td><td>101</td><td>33/32</td></tr>
<tr><td>1</td><td>110</td><td>65/64</td></tr>
<tr><td>1</td><td>111</td><td>129/128</td></tr>
</table></td></tr>
<tr><td>3</td><td>DIODE_T1_ADD</td><td>R/W</td><td>0h</td><td>The function of this bit is the same as DIG_T1_ADD expect that it is for D1+ reading.</td></tr>
<tr><td>2-0</td><td>DIODE_T1_SCALE</td><td>R/W</td><td>0h</td><td>The function of this bit is the same as DIG_T1_SCALE expect that it is for D1+ reading.</td></tr>
</table>

7.5.26 Temperature Filter Select Register -- Index 7Fh

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td>7-2</td><td>Reserved</td><td>-</td><td>-</td><td>Reserved.</td></tr>
<tr><td>1-0</td><td>T1_SRC_SEL_REG</td><td>R/W</td><td>00</td><td>The bits are used when DIODE_T1_EN and DIG_T1_EN are both enabled. The real select bits T1_SCR_SEL are fixed to 2’b01 if DIODE_T1_EN is “0” and 2’b00 if DIG_T1_EN is “0”. The T1 source is listed.
<table>
<tr><th>T1_SRC_SEL</th><th>T1 source</th></tr>
<tr><td>00</td><td>From D1+ only</td></tr>
<tr><td>01</td><td>From Digital reading (PECI/TSI)</td></tr>
<tr><td>10</td><td>Average</td></tr>
<tr><td>11</td><td>Maximum</td></tr>
</table></td></tr>
</table>

7.5.27 Temperature Filter Select Register -- Index 8Eh

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td>7-6</td><td>IIR-QUEUR3</td><td>R/W</td><td>0h</td><td>The queue time for second filter to quickly update values.
00: 8 times.
01: 12 times.
10: 16 times. (default)
11: 24 times.</td></tr>
<tr><td>5-4</td><td>IIR-QUEUR2</td><td>R/W</td><td>0h</td><td>The queue time for second filter to quickly update values.
00: 8 times.
01: 12 times.
10: 16 times. (default)
11: 24 times.</td></tr>
<tr><td>3-2</td><td>IIR-QUEUR1</td><td>R/W</td><td>0h</td><td>The queue time for second filter to quickly update values.
00: 8 timers.
01: 12 times.
10: 16 times. (default)
11: 24 times.</td></tr>
<tr><td>0</td><td>Reserved</td><td>R</td><td>0h</td><td>--</td></tr>
</table>

Fan Control Setting

7.5.28 FAN PME# Enable Register — Index 90h

Bit	Name	R/W	Default	Description
7-3	Reserved	RO	0h	Reserved
2	EN_FAN3_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan3.
1	EN_FAN2_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan2.
0	EN_FAN1_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan1.

7.5.29 FAN Interrupt Status Register — Index 91h

Bit	Name	R/W	Default	Description
7-3	Reserved	RO	0	Reserved
2	FAN3_STS	R/W	--	This bit is set when the fan3 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
1	FAN2_STS	R/W	--	This bit is set when the fan2 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
0	FAN1_STS	R/W	--	This bit is set when the fan1 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.

7.5.30 FAN Real Time Status Register — Index 92h

Bit	Name	R/W	Default	Description
7-3	Reserved	--	0	Reserved
2	FAN3_EXC	RO	--	This bit set to high mean that fan3 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.
1	FAN2_EXC	RO	--	This bit set to high mean that fan2 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.
0	FAN1_EXC	RO	--	This bit set to high mean that fan1 count can't meet expect count over than SMI time(CR9F) or when duty not zero but fan stop over then 3 sec.

7.5.31 FAN BEEP# Enable Register — Index 93h

Bit	Name	R/W	Default	Description
7	FULL_WITH_T3_EN	R/W	0	Set one will enable FAN to force full speed when T3 over high limit.
6	FULL_WITH_T2_EN	R/W	0	Set one will enable FAN to force full speed when T2 over high limit.
5	FULL_WITH_T1_EN	R/W	0	Set one will enable FAN to force full speed when T1 over high limit.
4	Reserved	R/W	0	Reserved for local temperature.
3	Reserved	-	-	Reserved.
2	EN_FAN3_ BEEP	R/W	0	A one enables the corresponding interrupt status bit for BEEP.
1	EN_FAN2_ BEEP	R/W	0	A one enables the corresponding interrupt status bit for BEEP.
0	EN_FAN1_ BEEP	R/W	0	A one enables the corresponding interrupt status bit for BEEP.

7.5.32 Fan Type Select Register -- Index 94h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.

5-4	FAN3_TYPE	R/W	2'b 0S	00: Output PWM mode (pushpull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by RTS2# 0: RTS2# is pull up by internal 47K resistor. 1: RTS2# is pull down by external resistor.
3-2	FAN2_TYPE	R/W	2'b 0S	00: Output PWM mode (pushpull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by RTS2# 0: RTS2# is pull up by internal 47K resistor. 1: RTS2# is pull down by external resistor.
1-0	FAN1_TYPE	R/W	2'b 0S	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by RTS2# 0: RTS2# is pull up by internal 47K resistor. 1: RTS2# is pull down by external resistor.

S: Register default values are decided by trapping.

7.5.33 Fan mode Select Register -- Index 96h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5-4	FAN3_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that defines in 0xC6-0xCE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** that defines in 0xC6-0xCE. 10: Manual mode fan control, user can write expect **RPM** count to 0xC2-0xC3, and F71889 will auto control duty cycle (PWM fan type) or voltage(linear fan type) to control fan speed. 11: Manual mode fan control, user can write expect **duty cycle** (PWM fan type) or voltage(linear fan type) to 0xC3, and F71889 will output this value duty or voltage to control fan speed.
3-2	FAN2_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that defines in 0xB6-0xBE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** (voltage) that defines in 0xB6-0xBE. 10: Manual mode fan control, user can write expect **RPM** count to 0xB2-0xB3, and F71889 will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed. 11: Manual mode fan control, user can write expect **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xB3, and F71889 will output this value duty or voltage to control fan speed.

1-0	FAN1_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that defines in 0xA6-0xAE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** that defines in 0xA6-0xAE. 10: Manual mode fan control, user can write expect **RPM** count to 0xA2-0xA3, and F71889 will auto control duty cycle (PWM fan type) or voltage(linear fan type) to control fan speed. 11: Manual mode fan control, user can write expect **duty cycle** (PWM fan type) or voltage(linear fan type) to 0xA3, and F71889 will output this value duty or voltage to control fan speed.

7.5.34 Auto Fan1 and Fan2 Boundary Hystersis Select Register -- Index 98h

Bit	Name	R/W	Default	Description
7-4	FAN2_HYS	R/W	4h	0000: Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).
3-0	FAN1_HYS	R/W	4h	0000: Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

7.5.35 Auto Fan3 Boundary Hystersis Select Register -- Index 99h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	FAN3_HYS	R/W	2h	0000: Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

7.5.36 Auto Fan Up Speed update Rate Select Register -- Index 9Bh (FAN_RATE_PROG_SEL = 0)

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5-4	FAN3_UP_RATE	R/W	1h	Fan3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
3-2	FAN2_UP_RATE	R/W	1h	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_UP_RATE	R/W	1h	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

7.5.37 Auto Fan Down Speed update Rate Select Register -- Index 9Bh (FAN_RATE_PROG_SEL = 1)

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5-4	FAN3_DOWN_RATE	R/W	1h	Fan3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

3-2	FAN2_DOWN_RATE	R/W	1h	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_DOWN_RATE	R/W	1h	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

7.5.38 FAN1 and FAN2 START UP DUTY-CYCLE/VOLTAGE — Index 9Ch

Bit	Name	R/W	Default	Description
7-4	FAN2_STOP_DUTY	R/W	5h	When fan start, the FAN_CTRL2 will increase duty-cycle from 0 to this (value x 8) directly. And if fan speed is down, the FAN_CTRL 2 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).
3-0	FAN1_STOP_DUTY	R/W	5h	When fan start, the FAN_CTRL 1 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 1 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

7.5.39 FAN3 START UP DUTY-CYCLE/VOLTAGE — Index 9Dh

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	FAN3_STOP_DUTY	R/W	5h	When fan start, the FAN_CTRL 3 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 3 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

7.5.40 Fan Fault Time Register -- Index 9Fh

Bit	Name	R/W	Default	Description
7	FAN_RATE_PROG_SEL	R/W	0	0: Index 9Bh is the fan up speed update rate select register. 1: Index 9Bh is the fan down speed update rate select register.
6-5	Reserved	--	--	Reservd
4	FULL_DUTY_SEL	R/W	--	0: the full duty is 100%. (pull down by external resistor) 1: the full duty is 60% (default, pull up by internal 47K resistor). This register is power on trap by DTR1#.
3-0	F_FAULT_TIME	R/W	Ah	This register determines the time of fan fault. The condition to cause fan fault event is: When PWM_Duty reaches FFh, if the fan speed count can't reach the fan expect count in time. The unit of this register is 1 second. The default value is 11 seconds. (Set to 0 , means 1 seconds. ; Set to 1, means 2 seconds. Set to 2, means 3 seconds. ….) Another condition to cause fan fault event is fan stop and the PWM duty is greater than the minimum duty programmed by the register index 9C-9Dh.

Fan1 Index A0h- AFh

Address	Attribute	Default Value	Description
A0h	RO	8'h0f	FAN1 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A1h	RO	8'hff	FAN1 count reading (LSB).
A2h	R/W	8'h00	**RPM mode(CR96 bit0=0):** FAN1 expect speed count value (MSB), in auto fan mode (CR96 bit1➔0) this register is auto updated by hardware. **Duty mode(CR96 bit0=1):** This byte is reserved byte.
A3h	R/W	8'h01	**RPM mode(CR96 bit0=0):** FAN1 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. **Duty mode(CR96 bit0=1):** The Value programming in this byte is duty value. In auto fan mode (CR96 bit1➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
A4h	R/W	8'h03	FAN1 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A5h	R/W	8'hff	FAN1 full speed count reading (LSB).

7.5.41 VT1 BOUNDARY 1 TEMPERATURE – Index A6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TMP1	R/W	3Ch (60°C)	The 1st BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expect value will load from segment 1 register (index AAh). When VT1 temperature is below this boundary – hysteresis, FAN1 expect value will load from segment 2 register (index ABh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

7.5.42 VT1 BOUNDARY 2 TEMPERATURE – Index A7

Bit	Name	R/W	Default	Description
7-0	BOUND2TMP1	R/W	32 (50°C)	The 2st BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expect value will load from segment 2 register (index ABh). When VT1 temperature is below this boundary – hysteresis, FAN1 expect value will load from segment 3 register (index ACh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

7.5.43 VT1 BOUNDARY 3 TEMPERATURE – Index A8h

Bit	Name	R/W	Default	Description
7-0	BOUND3TMP1	R/W	28h (40°C)	The 3st BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expect value will load from segment 3 register (index ACh). When VT1 temperature is below this boundary – hysteresis, FAN1 expect value will load from segment 4 register (index ADh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

7.5.44 VT1 BOUNDARY 4 TEMPERATURE – Index A9

Bit	Name	R/W	Default	Description
7-0	BOUND4TMP1	R/W	1Eh (30°C)	The 4st BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expect value will load from segment 4 register (index ADh). When VT1 temperature is below this boundary – hysteresis, FAN1 expect value will load from segment 5 register (index AEh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

7.5.45 FAN1 SEGMENT 1 SPEED COUNT – Index AAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED1	R/W	FFh (100%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%: full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.5.46 FAN1 SEGMENT 2 SPEED COUNT – Index ABh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED1	R/W	D9h (85%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.5.47 FAN1 SEGMENT 3 SPEED COUNT – Index ACh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED1	R/W	B2h (70%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.5.48 FAN1 SEGMENT 4 SPEED COUNT – Index ADh

Bit	Name	R/W	Default	Description
7-0	SEC4SPEED1	R/W	99h (60%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.5.49 FAN1 SEGMENT 5 SPEED COUNT – Index AEh

Bit	Name	R/W	Default	Description
7-0	SEC5SPEED1	R/W	80h (50%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.5.50 FAN1 Temperature Mapping Select – Index AFh

Bit	Name	R/W	Default	Description
7	FAN1_TEMP_SEL _DIG	R/W	0	This bit companying with FAN1_TEMP_SEL select the temperature source for controlling FAN1.
6	Reserved	--	0	Reserved
5	FAN1_UP_T_EN	R/W	0	Set 1 to force FAN1 to full speed if any temperature over its high limit.
4	FAN1_INTERPOLATION_ EN	R/W	0	Set 1 will enable the interpolation of the fan expect table.
3	FAN1_JUMP_HIGH_EN	R/W	0	This register controls the FAN1 duty movement when temperature over highest boundary. 0: The FAN1 duty will increases with the slope selected by FAN1_RATE_SEL register. 1: The FAN1 duty will directly jumps to the value of SEC1SPEED1 register. This bit only activates in duty mode.
2	FAN1_JUMP_LOW_EN	R/W	0	This register controls the FAN1 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN1 duty will decreases with the slope selected by FAN1_RATE_SEL register. 1: The FAN1 duty will directly jumps to the value of SEC2SPEED1 register. This bit only activates in duty mode.
1-0	FAN1_TEMP_SEL	R/W	1	This registers companying with FAN1_TEMP_SEL_DIG select the temperature source for controlling FAN1. The following value is comprised by {FAN1_TEMP_SEL_DIG, FAN1_TEMP_SEL} 001: fan1 follows temperature 1 (CR72h). 010: fan1 follows temperature 2 (CR74h). 011: fan1 follows temperature 3 (CR76h). 101: fan1 follows digital temperature 1 (CR7Ch). 110: fan1 follows digital temperature 2 (CR7Bh). 111: fan1 follows digital temperature 3 (CR7Ah). Otherwise: reserved.

Fan2 Index B0h- BFh

Address	Attribute	Default Value	Description
B0h	RO	8'h0f	FAN2 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B1h	RO	8'hff	FAN2 count reading (LSB).
B2h	R/W	8'h00	**RPM mode(CR96 bit2=0):** FAN2 expect speed count value (MSB), in auto fan mode (CR96 bit3➔0) this register is auto updated by hardware. **Duty mode(CR96 bit2=1):** This byte is reserved byte.
B3h	R/W	8'h01	**RPM mode(CR96 bit2=0):** FAN2 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. **Duty mode(CR96 bit2=1):** The Value programming in this byte is duty value. In auto fan mode (CR96 bit3➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255➔ 100%
B4h	R/W	8'h03	FAN2 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read

			the fan count correctly, read MSB first and followed read the LSB.
B5h	R/W	8'hff	FAN2 full speed count reading (LSB).

7.5.51 VT2 BOUNDARY 1 TEMPERATURE – Index B6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TMP2	R/W	3Ch (60°C)	The 1st BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expect value will load from segment 1 register (index BAh). When VT2 temperature is below this boundary – hysteresis, FAN2 expect value will load from segment 2 register (index BBh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

7.5.52 VT2 BOUNDARY 2 TEMPERATURE – Index B7

Bit	Name	R/W	Default	Description
7-0	BOUND2TMP2	R/W	32 (50°C)	The 2st BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expect value will load from segment 2 register (index BBh). When VT2 temperature is below this boundary – hysteresis, FAN2 expect value will load from segment 3 register (index BCh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

7.5.53 VT2 BOUNDARY 3 TEMPERATURE – Index B8h

Bit	Name	R/W	Default	Description
7-0	BOUND3TMP2	R/W	28h (40°C)	The 3st BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expect value will load from segment 3 register (index BCh). When VT2 temperature is below this boundary – hysteresis, FAN2 expect value will load from segment 4 register (index BDh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

7.5.54 VT2 BOUNDARY 4 TEMPERATURE – Index B9

Bit	Name	R/W	Default	Description
7-0	BOUND4TMP2	R/W	1Eh (30°C)	The 4st BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expect value will load from segment 4 register (index BDh). When VT2 temperature is below this boundary – hysteresis, FAN2 expect value will load from segment 5 register (index BEh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

7.5.55 FAN2 SEGMENT 1 SPEED COUNT – Index BAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED2	R/W	FFh (100%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%: full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.5.56 FAN2 SEGMENT 2 SPEED COUNT – Index BBh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED2	R/W	D9h (85%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.5.57 FAN2 SEGMENT 3 SPEED COUNT – Index BCh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED2	R/W	B2h (70%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.5.58 FAN2 SEGMENT 4 SPEED COUNT – Index BDh

Bit	Name	R/W	Default	Description
7-0	SEC4SPEED2	R/W	99h (60%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.5.59 FAN2 SEGMENT 5 SPEED COUNT – Index BEh

Bit	Name	R/W	Default	Description
7-0	SEC5SPEED2	R/W	80h (50%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.5.60 FAN2 Temperature Mapping Select – Index BFh

Bit	Name	R/W	Default	Description
7	FAN2_TEMP_SEL_DIG	R/W	0	This bit companying with FAN2_TEMP_SEL select the temperature source for controlling FAN2.
6	Reserved	–	0	Reserved
5	FAN2_UP_T_EN	R/W	0	Set 1 to force FAN2 to full speed if any temperature over its high limit.
4	FAN2_INTERPOLATION_EN	R/W	0	Set 1 will enable the interpolation of the fan expect table.
3	FAN2_JUMP_HIGH_EN	R/W	0	This register controls the FAN2 duty movement when temperature over highest boundary. 0: The FAN2 duty will increases with the slope selected by FAN2_RATE_SEL register. 1: The FAN2 duty will directly jumps to the value of SEC1SPEED2 register. This bit only activates in duty mode.
2	FAN2_JUMP_LOW_EN	R/W	0	This register controls the FAN2 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN2 duty will decreases with the slope selected by FAN2_RATE_SEL register. 1: The FAN2 duty will directly jumps to the value of SEC2SPEED2 register. This bit only activates in duty mode.

1-0	FAN2_TEMP_SEL	R/W	1	This registers companying with FAN2_TEMP_SEL_DIG select the temperature source for controlling FAN2. The following value is comprised by {FAN2_TEMP_SEL_DIG, FAN2_TEMP_SEL} 001: fan1 follows temperature 1 (CR72h). 010: fan1 follows temperature 2 (CR74h). 011: fan1 follows temperature 3 (CR76h). 101: fan1 follows digital temperature 1 (CR7Ch). 110: fan1 follows digital temperature 2 (CR7Bh). 111: fan1 follows digital temperature 3 (CR7Ah). Otherwise: reserved.

Fan3 Index C0h- CFh

Address	Attribute	Default Value	Description
C0h	RO	8'h0F	FAN3 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C1h	RO	8'hff	FAN3 count reading (LSB).
C2h	R/W	8'h00	**RPM mode(CR96 bit4=0):** FAN3 expect speed count value (MSB), in auto fan mode (CR96 bit5➔0) this register is auto updated by hardware. **Duty mode(CR96 bit4=1):** This byte is reserved byte.
C3h	R/W	8'h01	**RPM mode(CR96 bit4=0):** FAN3 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. **Duty mode(CR96 bit4=1):** The Value programming in this byte is duty value. In auto fan mode (CR96 bit5➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
C4h	R/W	8'h03	FAN3 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C5h	R/W	8'hff	FAN3 full speed count reading (LSB).

7.5.61 VT3 BOUNDARY 1 TEMPERATURE – Index C6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TMP3	R/W	3Ch ($60^{o}C$)	The 1st BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expect value will load from segment 1 register (index CAh). When VT3 temperature is below this boundary – hysteresis, FAN3 expect value will load from segment 2 register (index CBh). This byte is a 2's complement value ranging from -128 ^{o}C ~ 127 ^{o}C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

7.5.62 VT3 BOUNDARY 2 TEMPERATURE – Index C7

Bit	Name	R/W	Default	Description
7-0	BOUND2TMP3	R/W	32 (50°C)	The 2st BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expect value will load from segment 2 register (index CBh). When VT3 temperature is below this boundary – hysteresis, FAN3 expect value will load from segment 3 register (index CCh). This byte is a 2's complement value ranging from -128 °C ~ 127 °C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

7.5.63 VT3 BOUNDARY 3 TEMPERATURE – Index C8h

Bit	Name	R/W	Default	Description
7-0	BOUND3TMP3	R/W	28h (40°C)	The 3st BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expect value will load from segment 3 register (index CCh). When VT3 temperature is below this boundary – hysteresis, FAN3 expect value will load from segment 4 register (index CDh). This byte is a 2's complement value ranging from -128 °C ~ 127 °C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

7.5.64 VT3 BOUNDARY 4 TEMPERATURE – Index C9

Bit	Name	R/W	Default	Description
7-0	BOUND4TMP3	R/W	1Eh (30°C)	The 4st BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expect value will load from segment 4 register (index CDh). When VT3 temperature is below this boundary – hysteresis, FAN3 expect value will load from segment 5 register (index CEh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

7.5.65 FAN3 SEGMENT 1 SPEED COUNT – Index CAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED3	R/W	FFh (100%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%: full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ((100-X)*32/X 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.5.66 FAN3 SEGMENT 2 SPEED COUNT – Index CBh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED3	R/W	D9h (85%)	The meaning of this register is depending on the FAN3_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.5.67 FAN3 SEGMENT 3 SPEED COUNT – Index CCh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED3	R/W	B2h (70%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.5.68 FAN3 SEGMENT 4 SPEED COUNT – Index CDh

Bit	Name	R/W	Default	Description
7-0	SEC4SPEED3	R/W	99h (60%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.5.69 FAN3 SEGMENT 5 SPEED COUNT – Index CEh

Bit	Name	R/W	Default	Description
7-0	SEC5SPEED3	R/W	80h (50%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

7.5.70 FAN3 Temperature Mapping Select – Index CFh

Bit	Name	R/W	Default	Description
7	FAN3_TEMP_SEL_DIG	R/W	0	This bit companying with FAN3_TEMP_SEL select the temperature source for controlling FAN3.
6	Reserved	--	0	Reserved
5	FAN3_UP_T_EN	R/W	0	Set 1 to force FAN3 to full speed if any temperature over its high limit.
4	FAN3_INTERPOLATION_EN	R/W	0	Set 1 will enable the interpolation of the fan expect table.
3	FAN3_JUMP_HIGH_EN	R/W	0	This register controls the FAN3 duty movement when temperature over highest boundary. 0: The FAN3 duty will increases with the slope selected by FAN3_RATE_SEL register. 1: The FAN3 duty will directly jumps to the value of SEC1SPEED3 register. This bit only activates in duty mode.
2	FAN3_JUMP_LOW_EN	R/W	0	This register controls the FAN3 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN3 duty will decreases with the slope selected by FAN3_RATE_SEL register. 1: The FAN3 duty will directly jumps to the value of SEC2SPEED3 register. This bit only activates in duty mode.
1-0	FAN3_TEMP_SEL	R/W	1	This registers companying with FAN3_TEMP_SEL_DIG select the temperature source for controlling FAN3. The following value is comprised by {FAN3_TEMP_SEL_DIG, FAN3_TEMP_SEL} 001: fan1 follows temperature 1 (CR72h). 010: fan1 follows temperature 2 (CR74h). 011: fan1 follows temperature 3 (CR76h). 101: fan1 follows digital temperature 1 (CR7Ch). 110: fan1 follows digital temperature 2 (CR7Bh). 111: fan1 follows digital temperature 3 (CR7Ah). Otherwise: reserved.

7.5.71 TSI Temperature 0 – Index E0h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP0	R/W	8'h00	This byte is used as multi-purpose as follows: 1. AMD TSI reading if AMD TSI enable (0~255 ^{o} C). 2. Highest temperature among CPU, MCH and PCH if Intel IBex enable (0~255 ^{o} C). 3. The 1st byte of read block protocol. To access this byte, MCH_BANK_SEL must set to "0".
	SMB_DATA0	R/W	8'h00	This byte is used as multi-purpose: 1. The received data of receive protocol. 2. The first received byte of read word protocol. 3. The 10th received byte of read block protocol. 4. The sent data for send byte protocol and write byte protocol. 5. The first send byte for write word protocol. 6. The first send byte for write block protocol. To access this byte, MCH_BANK_SEL should be set to "1".

7.5.72 TSI Temperature 1 – Index E1h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP1	R	8'h00	This byte is used as multi-purpose as follows: 1. The PCH temperature reading (0~255 ^{o} C). This byte is only valid if Intel IBex is enabled. 2. The 2nd byte of read block protocol. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA1	R/W	8'h00	This byte is used as multi-purpose: 1. The second received byte of read word protocol. 2. The 11th received byte of read block protocol. 3. The second send byte for write word protocol. 4. The second send byte for write block protocol. To access this byte, MCH_BANK_SEL should be set to "1".

7.5.73 TSI Temperature 2 Low Byte – Index E2h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP2_LO	R	8'h00	This byte is used as multi-purpose as follows: 1. The low byte of Intel temperature interface CPU reading. The reading is the fraction part of CPU temperature. Bit 0 indicates the error status. Logic "1" indicates an error code. This byte is only valid if Intel Ibex is enabled. 2. The 3rd byte of the block read protocol. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA2	R/W	8'h00	This is the 12th byte of the block read protocol. This byte is also used as the 3rd byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

7.5.74 TSI Temperature 2 High Byte – Index E3h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP2_HI	R	8'h00	This byte is used as multi-purpose as follows: 1. The high byte of Intel temperature interface CPU reading. The reading is the decimal part of CPU temperature. This byte is only valid if Intel Ibex is enabled. 2. The 4th byte of the block read protocol. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA3	R/W	8'h00	This is the 13th byte of the block read protocol. This byte is also used as the 4th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

7.5.75 TSI Temperature 3 – Index E4h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP3	R	8'h00	This byte is used as multi-purpose as follows: 1. The MCH temperature reading (0~255 °C). This byte is only valid if Intel Ibex is enabled. 2. The 5th byte of the block read protocol. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA4	R/W	8'h00	This is the 14th byte of the block read protocol. This byte is also used as the 5th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

7.5.76 TSI Temperature 4 – Index E5h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP4	R	8'h00	This byte is used as multi-purpose as follows: 1. The DIMM0 temperature reading (0~255 °C). This byte is only valid if Intel Ibex is enabled. 2. The 6th byte of the block read protocol. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA5	R/W	8'h00	This is the 15th byte of the block read protocol. This byte is also used as the 6th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

7.5.77 TSI Temperature 5 – Index E6h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP5	R	8'h00	This byte is used as multi-purpose: 1. The DIMM1 temperature reading (0~255 °C). This byte is only valid if Intel Ibex is enabled. 2. The 7th byte of the block read protocol. To access this byte, MCH_BANK_SEL should be set to "0".

	SMB_DATA6	R/W	8'h00	This is the 16th byte of the block read protocol. This byte is also used as the 7th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

7.5.78 TSI Temperature 6 – Index E7h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP6	R	8'h00	This byte is used as multi-purpose as follows: 1. The DIMM2 temperature reading (0~255 ^{o} C). This byte is only valid if Intel Ibex is enabled. 2. The 8th byte of the block read protocol. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA7	R/W	8'h00	This is the 17th byte of the block read protocol. This byte is also used as the 8th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

7.5.79 TSI Temperature 7 – Index E8h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP7	R	8'h00	This byte is used as multi-purpose: 1. The DIMM3 temperature reading (0~255 ^{o} C). The byte is only valid if Intel Ibex is enabled. 2. The 9th byte of block read protocol. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA8	R/W	8'h00	This is the 18th byte of the block read protocol. This byte is also used as the 9th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

7.5.80 SMB Data Buffer 9 – Index E9h (MCH_BANK_SEL = 1)

Bit	Name	R/W	Default	Description
7-0	SMB_DATA9	R/W	0	This is the 19th byte of the block read protocol. This byte is also used as the 10th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

7.5.81 SMB Data Buffer 10 – Index EAh (MCH_BANK_SEL = 1)

Bit	Name	R/W	Default	Description
7-0	SMB_DATA10	R/W	0	This is the 20th byte of the block read protocol. This byte is also used as the 11th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

7.5.82 Block Write Count Register – Index ECh

Bit	Name	R/W	Default	Description
7	MCH_BANK_SEL	R/W	0	This bit is used to select the register in index E0h to E9h. Set "0" to read the temperature bank and "1" to access the data bank.
6	Reserved	-	0	Reserved
5-0	BLOCK_WR_CNT	R/W	0	Use the register to specify the byte count of block write protocol. Support up to 10 bytes.

7.5.83 SMB Command Byte/TSI Comamdn Byte – Index EDh (TSI_CMD_PROG = 0)

Bit	Name	R/W	Default	Description
7-0	SMB_CMD	R/W	8'h0	Command code for write byte/word, read byte/word, block write/read and process call protocol.

7.5.84 SMB Command Byte/TSI Comamdn Byte – Index EDh (TSI_CMD_PROG = 1)

Bit	Name	R/W	Default	Description
7-0	TSI_CMD	R/W	8'h1	The command code for Intel temperature interface block read protocol and the data byte for AMD TSI send byte protocol.

7.5.85 SMB Status – Index EEh

Bit	Name	R/W	Default	Description
7	TSI_PENDING	R/W	0	Set 1 to pending auto TSI accessing. (In AMD model, auto accessing will issue a send-byte followed a receive-byte; In Intel model, auto accessing will issue a block read). To use the TSI_SCL/TSI_SDA as a SMBus master, set this bit to "1" first.
6	TSI_CMD_PROG	R/W	0	Set 1 to program TSI_CMD.
5	PROC_KILL	R/W	0	Kill the current SMBus transfer and return the state machine to idle. It will set an fail status if the current transfer is not completed.
4	FAIL_STS	R	0	This is set when PROC_KI LL kill an un-completed transfer. It will be auto cleared by next SMBus transfer.
3	SMB_ABT_ERR	R	0	This is the arbitration lost status if a SMBus command is issued. Auto cleared by next SMBus command.
2	SMB_TO_ERR	R	0	This is the timeout status if a SMBus command is issued. Auto cleared by next SMBus command.
1	SMB_NAC_ERR	R	0	This is the NACK error status if a SMBus command is issued. Auto cleared by next SMBus command.
0	SMB_READY	R	1	0: a SMBus transfer is in process. 1: Ready for next SMBus command.

7.5.86 SMB Protocol Select – Index EFh

Bit	Name	R/W	Default	Description
7	SMB_START	W	0	Write "1" to trigger a SMBus transfer with the protocol specified by SMB_PROTOCOL.
6-4	Reserved	-	-	Reserved.

3-0	SMB_PROTOCOL	R/W	0	Select what protocol if SMBus transfer is triggered. 0001b: send byte. 0010b: write byte. 0011b: write word. 0100b: process call. 0101b: block write. 0111b: quick command (write). 1001b: receive byte. 1010b: read byte. 1011b: read word. 1101b: block read. 1111b: quick command (read). Otherwise: reserved.

HW Chip ID and Vender ID Information

7.5.87 HM Chip ID 1 Register — Index 5Ah

Bit	Name	R/W	Default	Description
7-0	HM_CHIP_ID1	R	03h	Chip ID 1 of HM Device.

7.5.88 HM Chip ID 2 Register — Index 5Bh

Bit	Name	R/W	Default	Description
7-0	HM_CHIP_ID2	R	04h	Chip ID 2 of HM Device.

7.5.89 HM Vendor ID 1 Register — Index 5Dh

Bit	Name	R/W	Default	Description
7-0	HM_VENDOR_ID1	R	19h	Chip ID 1 of HM Device.

7.5.90 HM Vendor ID 2 Register — Index 5Eh

Bit	Name	R/W	Default	Description
7-0	HM_VENDOR_ID2	R	34h	Chip ID 2 of HM Device.

7.3. Keyboard Controller

The KBC provides the functions included a keyboard and a PS/2 mouse, and can be used with IBM-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. The controller will assert an interrupt to the system when data are placed in its output buffer.

The below content is about the KBC device register descriptions. All the registers are for software porting reference.

Status Register

The status register is an 8 bits register at I/O address 64h that provides information about the status of the KBC

Bit	Name	R/W	Default	Description
7	Parity error	R	0	0:odd parity 1:even parity
6	Time out	R	0	0:no time out error 1:time out error
5	Auxiliary device OBF	R	0	0: Auxiliary output buffer empty 1: Auxiliary output buffer full
4	Inhinit	R	0	0:keyboard is inhibited 1: keyboard is not inhibited
3	Command/data	R	0	0:data byte 1:command byte
2	SYSTEM_FLAG	R	0	This bit is set or clear by command byte of KBC
1	IBF	R	0	0:input buffer empty 1: input buffer full
0	OBF	R	0	0:output buffer empty 1: output buffer full

Command register

The internal KBC operation is controlled by the KBC command byte (KCCB). The KCCB resides in I/O address 64h that is read with a 20h command and written with a 60h command data.

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	Translate code	R/W	1	0: Pass un-translated scan code. 1: Translate scan code to IBM PC standard.
5	Disable Auxiliary Device	R/W	0	1: Disable Auxiliary inhibit function.
4	Disable Keyboard	R/W	0	1: Disable keyboard inhibit function.
3	Reserved	-	-	Reserved
2	System flag	R/W	1	0: The system is executing POST as a result of a cold boot. 1: The system is executing POST as a result of a shutdown or warm boot.
1	Enable Auxiliary Interrupt	R/W	1	0: Ao interrupt 1: A system interrupt is generated when a byte is placed in output buffer (IRQ12).
0	Enable keyboard Interrupt	R/W	1	0:No interrupt 1: A system interrupt is generated when a byte is placed in output buffer (IRQ1).

DATA register

The DATA register is an 8 bits register at I/O address 60h. the KBC used the output buffer to send the scan code received from keyboard and data byte replay by command to the system.
Power on default <7:0> = 00000000 binary

Commands

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte</td></tr>
<tr><td>60h</td><td>Write Command Byte
<table>
<tr><th>BIT</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
<tr><td>1</td><td>Enable Mouse Interrupt</td></tr>
<tr><td>2</td><td>System flag</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>4</td><td>Disable Keyboard Interface</td></tr>
<tr><td>5</td><td>Disable Mouse interface</td></tr>
<tr><td>6</td><td>IBM keyboard Translate Mode</td></tr>
<tr><td>7</td><td>Reserve</td></tr>
</table></td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Auxiliary Interface Test
8’h00: indicate Auxiliary interface is ok.
8’h01: indicate Auxiliary clock is low.
8’h02: indicate Auxiliary clock is high
8’h03: indicate Auxiliary data is low
8’h04: indicate Auxiliary data is high</td></tr>
<tr><td>AAh</td><td>Self-test
Returns 055h if self test succeeds</td></tr>
<tr><td>ABh</td><td>keyboard Interface Test
8’h00: indicate keyboard interface is ok.
8’h01: indicate keyboard clock is low.
8’h02: indicate keyboard clock is high
8’h03: indicate keyboard data is low
8’h04: indicate keyboard data is high</td></tr>
<tr><td>ADh</td><td>Disable Keyboard Interface</td></tr>
<tr><td>AEh</td><td>Enable Keyboard Interface</td></tr>
<tr><td>C0h</td><td>Read Input Port(P1) and send data to the system</td></tr>
<tr><td>C1h</td><td>Continuously puts the lower four bits of Port1 into STATUS register</td></tr>
<tr><td>C2h</td><td>Continuously puts the upper four bits of Port1 into STATUS register</td></tr>
<tr><td>CAh</td><td>Read the data written by CBh command.</td></tr>
<tr><td>CBh</td><td>Written a scratch data. This byte could be read by CAh command.</td></tr>
<tr><td>D0h</td><td>Send Port2 value to the system</td></tr>
<tr><td>D1h</td><td>Only set/reset GateA20 line based on the system data bit 1</td></tr>
<tr><td>D2h</td><td>Send data back to the system as if it came from Keyboard</td></tr>
</table>

D3h	Send data back to the system as if it came from Muse
D4h	Output next received byte of data from system to Mouse
FEh	Pulse only RC(the reset line) low for 6μS if Command byte is even

KBC Command Description

PS2 wakeup function

The KBC supports keyboard and mouse wakeup function, keyboard wakeup function has 4 kinds of conditions, when key is pressed combinational key (1) CTRL +ESC (2) CTRL+F1 (3) CTRL+SPACE (4) ANY KEY (5) windows 98 wakeup up key (6) windows 98 Power key (7) CTRL + ALT + Backspace (8) CTRL + Alt + Space, KBC will assert PME signal. Mouse wakeup function has 2 kinds of conditions, when mouse (1) BUTTON CLICK or (2) BUTTON CLICK AND MOVEMENT, KBC will assert PME signal. Those wakeup conditions are controlled by configuration register.

7.4. SPI Interface

Communication between the two devices is handling the serial peripheral interface (SPI). Every SPI system consist of one master and one or more slaves, where a master provides the SPI clock and slave receives clock from the master.

This design is only master function, for basic signal, master-out/slave-in (MOSI), master-in/slave-out (MISO), serial clock (SCK), and 4 slaves select (CS#), are needed for SPI interface. Each of slave select supports from 1Mbits to 16Mbits flash is decided by configuration register. Serial clock (SCK) signal is optional 16.7 or 33MHz, and the default is 16.7MHz. The serial data (MOSI) for SPI interface translates to depend on SCK rising edge or falling edge is decided by configuration register.

7.5. 80 Port

Monitor the value of 0x80 port and output the value via the signals defined for 7-segment display. High nibble and low nibble are outputted interleaved at 1KHz frequency. The 80 Port could also be output to LPT pins if all the input pins of LPT is “0” during power on.

7.6. ACPI Function

The Advanced Configuration and Power Interface (ACPI) is a system for controlling the use of power in a computer. It lets computer manufacturer and user to determine the computer’s power usage

dynamically.

There are three ACPI states that are of primary concern to the system designer and they are designated S0, S3 and S5. S0 is a full-power state; the computer is being actively used in this state. The other two are called sleep states and reflect different power consumption when power-down. S3 is a state that the processor is powered down but the last procedural state is being stored in memory which is still active. S5 is a state that memory is off and the last procedural state of the processor has been stored to the hard disk. Take S3 and S5 as comparison, since memory is fast, the computer can quickly come back to full-power state, the disk is slower than the memory and the computer takes longer time to come back to full-power state. However, since the memory is off, S5 draws the minimal power comparing to S0 and S3.

It is anticipated that only the following state transitions may happen:

S0→S3, S0→S5, S5→S0, S3→S0 and S3→S5.

Among them, S3→S5 is illegal transition and won't be allowed by state machine. It is necessary to enter S0 first in order to get to S5 from S3. As for transition S5→S3 will occur only as an immediate state during state transition from S5→S0. It isn't allowed in the normal state transition.

The below diagram described the timing, the always on and always off, keep last state could be set in control register. In keep last state mode, one register will keep the status of before power loss. If it is power on before power loss, it will remain power on when power is resumed, otherwise, if it is power off before power loss, it will remain power off when power is resumed.

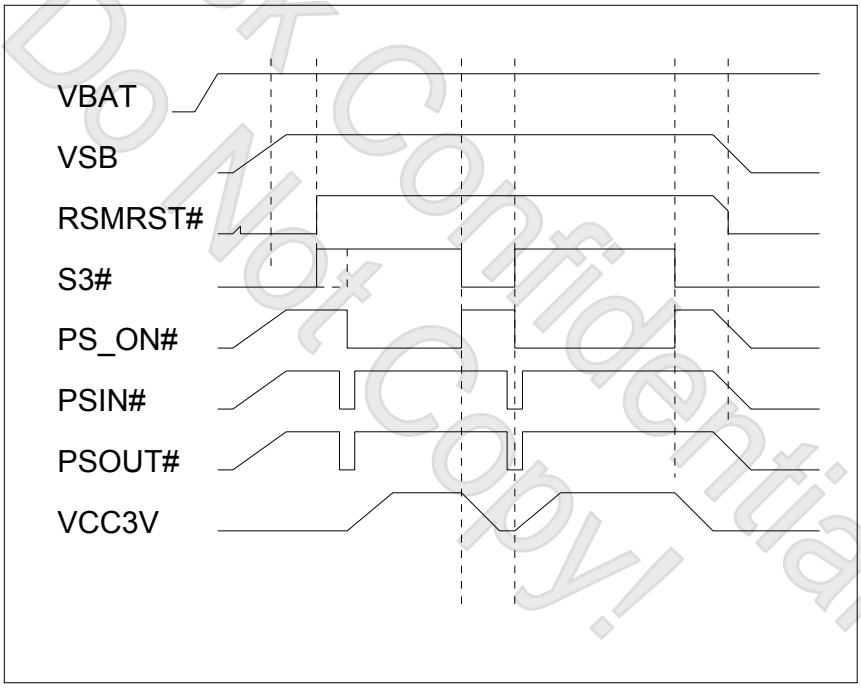


Figure 14 Default timing: Always off

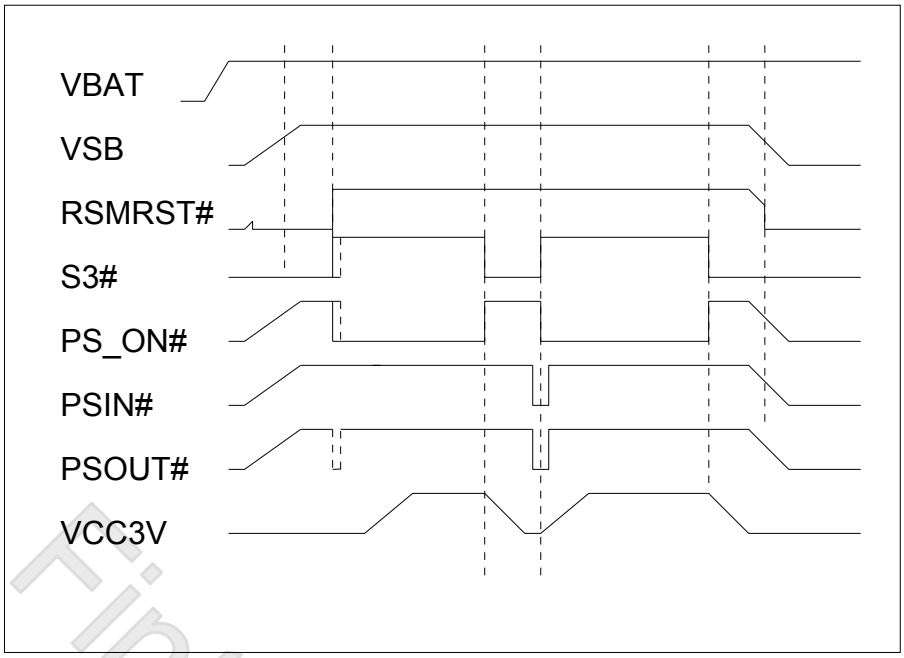
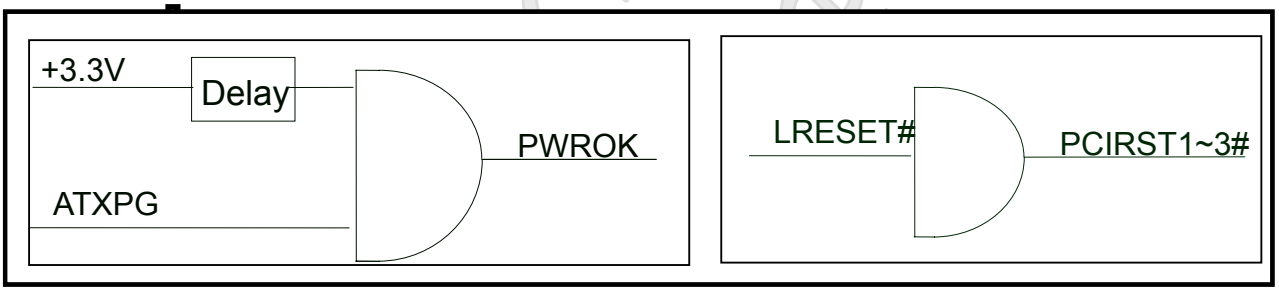


Figure 15 Optional timing: Always on

PCI Reset and PWROK Signals

The F71889 supports 3 output buffers for 3 reset signals. The result of PCIRST# outcome will be affected by conditions as below:

PCIRST1# → Output buffer of LRESET#.
PCIRST2# → Output buffer of LRESET#.
PCIRST3# → Output buffer of LRESET#.



So far as the PWROK issue is as the figure above. PWROK is delayed 400ms (default) as VCC arrives 2.8V, and the delay timing can be programmed by register. (100ms ~ 400ms)

The F71889 also supports 3 output voltages for VREF1~3. The output is generated from DACs which is powered by trimmed 2.304V reference voltage. One LSB is 2.304V/512.

Below is the timing sequence between VREF1~3 pins:

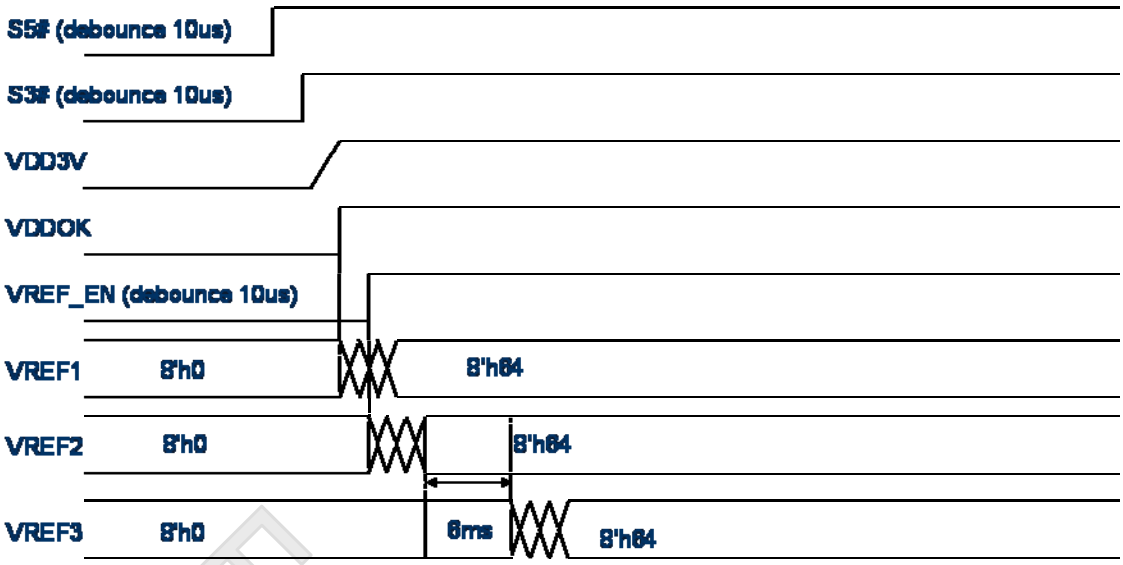


Figure 16 VREF timing: S5→S0

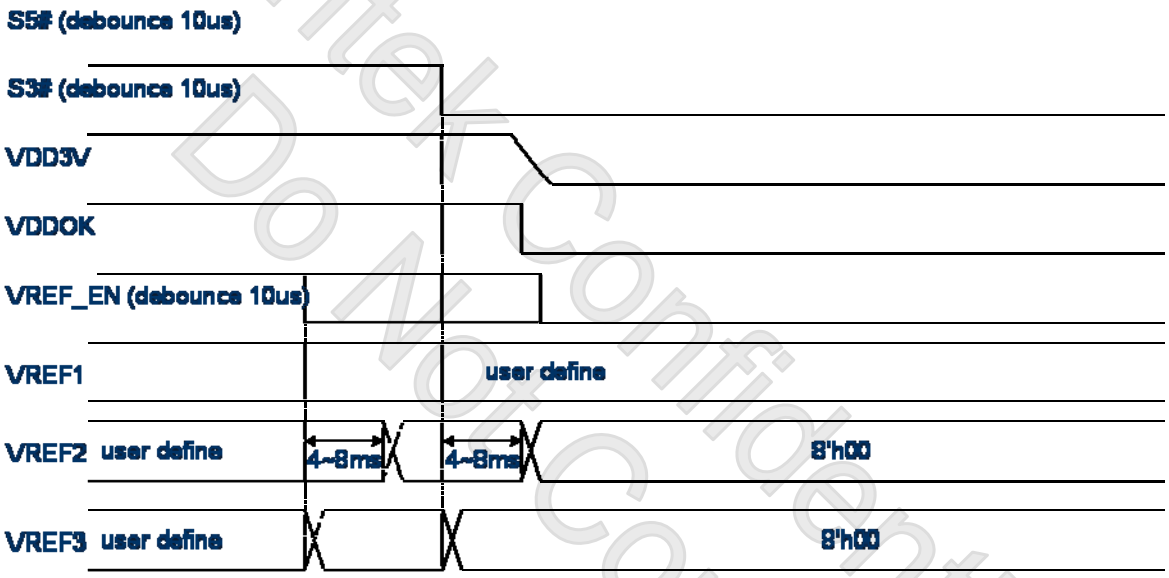


Figure 17 VREF timing: S0→S3

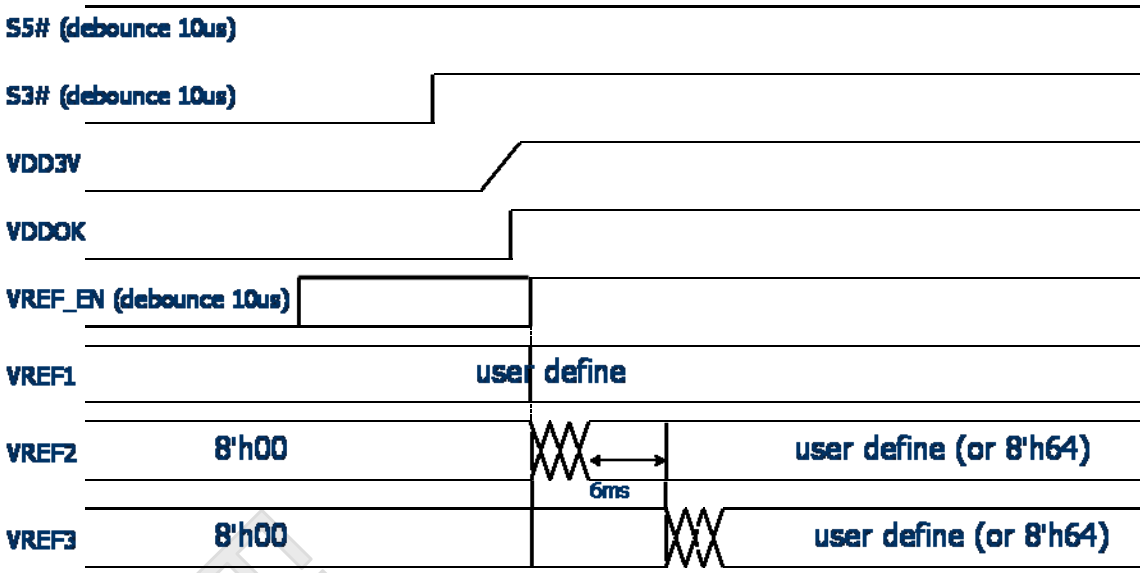
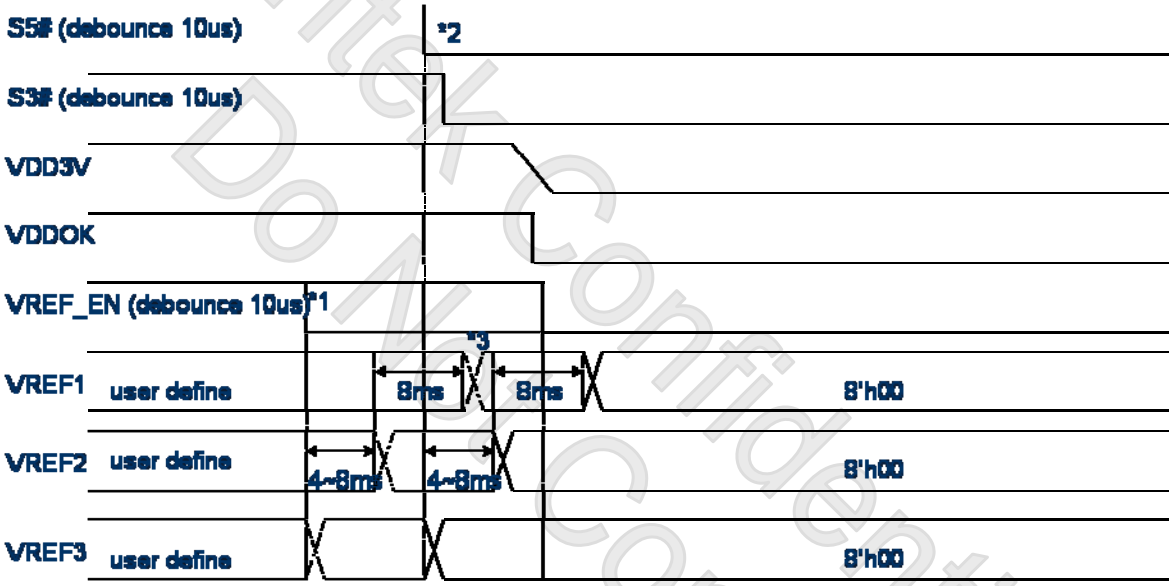


Figure 18 VREF timing: S3→S0



*1: VREF_EN de-active before S5# active.
*2: S5# active before VREF_EN de-active.
*3: VRAM power down after 8ms of VSYS power down and S5# active.

Figure 19 VREF timing: S0→S5

7.7. PECI Function

The Platform Environment Control Interface (PECI) uses a single wire for self-clocking and data transfer. The bus requires no additional control lines. The physical layer is a self-clocked on-wire bus that begins each bit with a driven, rising edge from an idle level near zero volts. The duration of the signal driven high depends on whether the bit value is a logic ‘0’ or login ‘1’. PECI also includes variable data transfer rate established with every message. In this way, it is highly

flexible even though underlying logic is simple.

The interface design was optimized for interfacing to Intel processor and chipset components in both single processor and multiple processor environments. The single wire interface provides low board routing overhead for the multiple load connections in the congested routing area near the processor and chipset components. Bus speed, error checking, and low protocol overhead provides adequate link bandwidth and reliability to transfer critical device operating conditions and configuration information.

7.8. SST Function

The Simple Serial Transfer (SST) temperature sensor provides a means to digitize an analog signal and send that information over a digital bus enabling remote temperature sensing in areas previously not monitored in the PC. The temperature sensor supports an internal and external thermal diode.

The Simple Serial Transfer (SST) interface provides sensed temperatures and voltages. The sensed temperatures are T1, T2, and T3 whose reading values stored in CR72h, CR74h, and CR76h. The sensed voltages are V1~V6 whose reading values stored in CR21h~26h.

7.9. TSI Function

The Temperature Sensor Interface (TSI) was a simple SMBUS master to communicate with AMD CPU or Intel CPU to getting the temperature of CPU. It supports byte sending, byte reveiving, read/write byte, read/write block and quick command of SMBus protocol. When power on the hardware automatically fetch the temperature use the protocol per the specification of AMD/Intel. User can use the provided registers to control the SCL/SDA as a SMBus master. For Intel platform, the SMBUS supports next generational IBX protocol for temperature reading.

7.10. FSB Bus Interface

The Bus interface is simply GPIs and GPIOs. There are two modes supported: bypass mode and manual mode. Default is the bypass mode, BUSIN will bypass to BUSOUT. In manual mode, BUSOUT is controlled by registers. Nomally this function is for FSB over/under colcking application.

7.11. VID Controller

VID Controller provides two types of interface parallel to parallel and serial to serial (AMD only). There are three modes for each type: bypass, manual and on the fly. It's used to over-voltage

control. In bypass mode, the hardware monitors the input and bypass to the output. In manual mode, the input is monitored but the output is controlled by registers. In on-the-fly mode, user programs the offset, the hardware monitors the input, adds the offset and then pass to the output.

8. Register Description

The configuration register is used to control the behavior of the corresponding devices. To configure the register, using the index port to select the index and then writing data port to alter the parameters. The default index port and data port are 0x4E and 0x4F respectively. Pull down the SOUT1 pin to change the default value to 0x2E/0x2F. To enable configuration, the entry key 0x87 must be written to the index port. To disable configuration, write exit key 0xAA to the index port. Following is a example to enable configuration and disable configuration by using debug.

-o 4e 87
-o 4e 87 (enable configuration)
-o 4e aa (disable configuration)

The Following is a register map (total devices) grouped in hexadecimal address order, which shows a summary of all registers and their default value. Please refer each device chapter if you want more detail information.

"-" Reserved or Tri-State

Global Control Registers									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
02	Software Reset Register	-	-	-	-	-	-	-	0
07	Logic Device Number Register (LDN)	0	0	0	0	0	0	0	0
20	Chip ID Register	0	0	0	0	0	1	1	1
21	Chip ID Register	0	0	1	0	0	0	1	1
23	Vender ID Register	0	0	0	1	1	0	0	1
24	Vender ID Register	0	0	1	1	0	1	0	0
25	Software Power Down Register	-	-	0	0	0	0	0	0
26	UART IRQ Sharing Register	0	-	0	0	-	-	0	0
27	ROM Address Select Register	0	0/1	1/0	1/0	-	1/0	1/0	1/0
28	80 Port Enable Register	0/1	-	0/1	0	-	-	-	-
2A	Multi Function Select 1 Register	1	1	1	1	0	0	0	0
2B	Multi Function Select 2 Register	0	0	1	1	0	0	0	0
2C	Multi Function Select 3 Register	-	0	0	0	0	0	0	0
2D	Wakeup Control Register	0	-	-	0	0	0	0	0

"-" Reserved or Tri-State

FDC Device Configuration Registers (LDN CR00)									
Register 0x[HEX]	**Register Name**	**Default Value**							
		MSB							**LSB**
30	FDC Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	1	1	1	1	0	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	1	0
74	DMA Channel Select Register	-	-	-	-	-	0	1	0

F0	FDD Mode Register	-	-	-	0	1	1	1	0
F2	FDD Drive Type Register	-	-	-	-	-	-	1	1
F4	FDD Selection Register	-	-	-	0	0	-	0	0

UART1 Device Configuration Registers (LDN CR01)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	UART1 Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	1	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	0	0
F0	RS485 Enable Register	-	-	-	0	-	-	-	-

UART2 Device Configuration Registers (LDN CR02)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	UART2 Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	0	1	1
F0	RS485 Enable Register	-	-	-	0	0	0	-	-
F1	SIR Mode Control Register	-	-	-	0	0	1	0	0

Parallel Port Device Configuration Registers (LDN CR03)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Parallel Port Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	0	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	1	1
74	DMA Channel Select Register	-	-	-	0	-	0	1	1
F0	PRT Mode Select Register	0	1	0	0	0	0	1	0

Hardware Monitor Device Configuration Registers (LDN CR04)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	H/W Monitor Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	0	0	1	0	1	0	1
70	IRQ Channel Select Register	-	-	-	-	0	0	0	0

KBC Device Configuration Registers (LDN CR05)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	KBC Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	1	1	0	0	0	0	0
70	KB IRQ Channel Select Register	-	-	-	-	0	0	0	1
72	Mouse IRQ Channel Select Register	-	-	-	-	1	1	0	0
F0	Clock Select Register	1	0	-	-	-	-	1	1
FE	Swap Register	1	-	-	0	0	0	0	1

GPIO Device Configuration Registers (LDN CR06)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
F0	GPIO Output Enable Register	-	0	0	0	0	0	0	0
F1	GPIO Output Data Register	-	1	1	1	1	1	1	1
F2	GPIO Pin Status Register	-	-	-	-	-	-	-	-
F3	GPIO Drive Enable Register	-	0	0	0	0	0	0	0

FE	LED_VSB Control Register	-	-	0	0	0	0	0	0
FF	LED_VCC Control Register	-	-	0	0	0	0	0	0
E0	GPIO1 Output Enable Register	-	0	0	0	0	0	0	0
E1	GPIO1 Output Data Register	-	1	1	1	1	1	1	1
E2	GPIO1 Pin Status Register	-	-	-	-	-	-	-	-
E3	GPIO1 Drive Enable Register	-	0	0	0	0	0	0	0
D0	GPIO2 Output Enable Register	0	0	0	0	0	0	0	0
D1	GPIO2 Output Data Register	1	1	1	1	1	1	1	1
D2	GPIO2 Pin Status Register	-	-	-	-	-	-	-	-
D3	GPIO2 Drive Enable Register	0	0	0	0	0	0	0	0
C0	GPIO3 Output Enable Register	0	0	0	0	0	0	0	0
C1	GPIO3 Output Data Register	1	1	1	1	1	1	1	1
C2	GPIO3 Pin Status Register	-	-	-	-	-	-	-	-
C3	GPIO3 Drive Enable Register	0	0	0	0	0	0	0	0
B0	GPIO4 Output Enable Register	0	0	0	0	0	0	0	0
B1	GPIO4 Output Data Register	1	1	1	1	1	1	1	1
B2	GPIO4 Pin Status Register	-	-	-	-	-	-	-	-
A0	GPIO5 Output Enable Register	-	-	-	0	0	0	0	0
A1	GPIO5 Output Data Register	-	-	-	1	1	1	1	1
A2	GPIO5 Pin Status Register	-	-	-	-	-	-	-	-
A3	GPIO5 Drive Enable Register	-	-	-	0	0	0	0	0
90	GPIO6 Output Enable Register	0	0	0	0	0	0	0	0
91	GPIO6 Output Data Register	1	1	1	1	1	1	1	1
92	GPIO6 Pin Status Register	-	-	-	-	-	-	-	-
93	GPIO6 Drive Enable Register	0	0	0	0	0	0	0	0
80	GPIO7 Output Enable Register	0	0	0	0	0	0	0	0
81	GPIO7 Output Data Register	1	1	1	1	1	1	1	1
82	GPIO7 Pin Status Register	-	-	-	-	-	-	-	-
83	GPIO7 Drive Enable Register	0	0	0	0	0	0	0	0

VID Device Configuration Registers (LDN CR07)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	VID Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
F0	Watchdog Timer Enable Register	0	-	-	-	-	-	-	0
F2	BUS Manual Register	0	0	0	0	0	0	0	0
F3	Key Data Register	0	0	0	0	0	0	0	0
F4	BUSIN Status Register	-	-	-	-	-	-	-	-
F5	WDT Unit Select Register	-	0	0	0	0	0	0	0
F6	WDT Count Register	0	0	0	0	0	0	0	0
F7	NB Offset Register	0	0	0	0	0	0	0	0
F8	VDD0 Offset Register	0	0	0	0	0	0	0	0
F9	VDD1 Offset Register	0	0	0	0	0	0	0	0
FA	Watchdog Timer PME Register	0	0	0	0	0	0	0	0
FB	NB Manaul Register	0	0	0	0	0	0	0	0
FC	VDD0 Manaul Register	0	0	0	0	0	0	0	0
FD	VDD1 Manaul Register	0	0	0	0	0	0	0	0
FE	PSI Control Register	0	0	0	0	1	1	1	0

SPI Device Configuration Registers (LDN CR08)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
F0	SPI Control Register	-	-	0	-	0	0	-	0
F1	SPI Timeout Value Register	0	0	0	0	0	1	0	0

F2	SPI Baud Rate Divisor Register	-	-	-	-	-	0	0	0
F3	SPI Status Register	0	-	-	-	0	-	-	-
F4	SPI High Byte Data Register	0	0	0	0	0	0	0	0
F5	SPI Command Data Register	0	0	0	0	0	0	0	0
F6	SPI Chip Select Register	-	-	-	-	0	0	0	0
F7	SPI Memory Mapping Register	-	-	-	1	0	0	0	0
F8	SPI Operate Register	0	0	0	0	0	0	0	0
FA	SPI Low Byte Data Register	0	0	0	0	0	0	0	0
FB	SPI Address High Byte Register	0	0	0	0	0	0	0	0
FC	SPI Address Medium Byte Register	0	0	0	0	0	0	0	0
FD	SPI Address Low Byte Register	0	0	0	0	0	0	0	0
FE	SPI Program Byte Register	0	0	0	0	0	0	0	0
FF	SPI Write Data Register	0	0	0	0	0	0	0	0

PME and ACPI Device Configuration Registers (LDN CR0A)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	PME Device Enable Register	-	-	-	-	-	-	-	0
F0	PME Event Enable Register	-	0	0	0	0	0	0	0
F1	PME Event Status Register	-	-	-	-	-	-	-	-
F4	ACPI Control Register1	0	0	1	0	0	1	1	0
F5	ACPI Control Register2	0	0	0	1	1	1	0	0
F6	ACPI Control Register3	0	0	0	0	0	1	1	1

Vref Control Device Configuration Registers (LDN CR0B)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
F0	VREF3 output value	0	1	1	0	0	1	0	0
F1	VREF2output value	0	1	1	0	0	1	0	0
F2	VREF1 output value	0	1	1	0	0	1	0	0
F3	Voltage LSB	-	-	-	-	-	0	0	0
FF	WDT Reset Enable	-	-	-	-	-	-	-	0

8.1 Global Control Registers

8.1.1 Software Reset Register — Index 02h

Bit	Name	R/W	Default	Description
7	Temp_Update_Rate	R/W	0	0: Digital interface (PECI/TSI/IBX) transmits when every temperature updates 1: Digital interface (PECI/TSI/IBX) transmits when every four times temperature updates
6-1	Reserved	-	-	Reserved
0	SOFT_RST	R/W	0	Write 1 to reset the register and device powered by VDD (VCC).

8.1.2 Logic Device Number Register (LDN) — Index 07h

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Select FDC device configuration registers. 01h: Select UART 1 device configuration registers. 02h: Select UART 2 device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select VID device configuration registers. 08h: Select SPI device configuration registers. 0ah: Select PME & ACPI device configuration registers. 0bh: Select VREF Control device configuration registers.

8.1.3 Chip ID Register — Index 20h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID1	R	07h	Chip ID 1.

8.1.4 Chip ID Register — Index 21h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID2	R	23h	Chip ID2.

8.1.5 Vendor ID Register — Index 23h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID1	R	19h	Vendor ID 1 of Fintek devices.

8.1.6 Vendor ID Register — Index 24h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID2	R	34h	Vendor ID 2 of Fintek devices.

8.1.7 Software Power Down Register — Index 25h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved
5	SOFTPD_KBC	R/W	0	Power down the KBC device. This will stop the KBC clock. (Reserved for future use)
4	SOFTPD_HM	R/W	0	Power down the Hardware Monitor device. This will stop the Hardware Monitor clock.
3	SOFTPD_PRT	R/W	0	Power down the Parallel Port device. This will stop the Parallel Port clock.
2	SOFTPD_UR2	R/W	0	Power down the UART 2 device. This will stop the UART 2 clock.
1	SOFTPD_UR1	R/W	0	Power down the UART 1 device. This will stop the UART 1 clock.
0	SOFTPD_FDC	R/W	0	Power down the FDC device. This will stop the FDC clock.

8.1.8 UART IRQ Sharing Register — Index 26h

Bit	Name	R/W	Default	Description
7	CLK24M_SEL	R/W	0	0: CLKIN is 48MHz 1: CLKIN is 24MHz
6	Reserved	-	-	Reserved.
5	DPORT_DEC_SEL	R/W	0	0: The 80 Port address is decoded as 0x0080. 1: The 80 port address is decoded as the SCR of UART2. This bit is powered by VBAT.
4	SPI_TM_RST_SEL	R/W	0	0: The SPI timeout status is reset by internal VDD3VOK. 1: The SPI timeout status is reset by internal VSB3VOK. This bit is powered by VBAT.
3-2	Reserved	-	-	Reserved.
1	IRQ_MODE	R/W	0	0: PCI IRQ sharing mode (low level). 1: ISA IRQ sharing mode (low pulse).
0	IRQ_SHAR	R/W	0	0: disable IRQ sharing of two UART devices. 1: enable IRQ sharing of two UART devices.

8.1.9 ROM Address Select Register — Index 27h

Bit	Name	R/W	Default	Description
7	ROM_WR_EN	R/W	0	0: disable ROM writing 1: enable ROM writing
6	SPI_EN	R/W	-	0: SPI disable 1: SPI enable This register is power on trapped by SOUT2/SPI_TRAP. Pull down to enable SPI.
5	SPI_BIOS_EN	R/W	-	0: use SPI bridge for BIOS 1: Reserved This register is power on trapped by DTR2#/FWH_TRAP. Pull down to enable SPI bridge for BIOS.
4	PORT_4E_EN	R/W	-	0: The configuration register port is 2E/2F. 1: The configuration register port is 4E/4F. This register is power on trapped by SOUT1/ Config4E_2E. Pull down to select port 2E/2F.
3	Reserved	-	-	Reserved.
2	BSEL_EN	R/W	-	0: The BUSIN/BUSOUT functions as GPIOs. 1: The BUSIN/BUSOUT functions as BUS interface. This register is power on trapped by BSGPIO_TRP. Pull down to select GPIO function.
1-0	LPT_FUNC_SEL	R/W	-	00: The parallel port pins function as LPT. x1: The parallel port pins function as VID control. 10: The parallel port pins function as GPIOs. This register is power on trapped by VIDIO_TRAP. Different resistor will determine these three functions.

8.1.10 80 Port Enable Register — Index 28h

Bit	Name	R/W	Default	Description
7	LPT_DPORT_EN	R/W	-	0: The 80 port data could not be output to LPT pins. 1: The 80 port data could be output to LPT pins in DPORT_EN is set to "1".
6	Reserved	-	-	Reserved.
5	DPORT_EN	R/W	-	0: The 80 port function is disabled. 1: The 80 port function is enabled.
4	TEMP_OUT_EN	R/W	0	Set this bit to "1" will output the CPU temperature to the 7-segment LED.
3-0	Reserved	-	-	Reserved.

8.1.11 Multi Function Select 1 Register — Index 2Ah (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7-6	GPIO06_SEL	R/W	2'b11	GPIO06/BEEP/ALERT# function select. 00: The pin function is ALERT#. 01: The pin function is BEEP. 10: Reserved. 11: The pin function is GPIO06.
5	GPIO05_SEL	R/W	1	GPIO05/LED_VCC function select. 0: The pin function is LED_VCC. 1: The pin function is GPIO05.
4	GPIO04_SEL	R/W	1	GPIO04/LED_VSB function select. 0: The pin function is LED_VSB. 1: The pin function is GPIO04.
3	GPIO03_SEL	R/W	0	SLOTOCC#/GPIO03 function select. 0: The pin function is SLOTOCC#. 1: The pin function is GPIO03.
2	Reserved	R/W	0	Reserved
1	Reserved	R/W	0	Reserved
0	Reserved	R/W	0	Reserved

8.1.12 Multi Function Select 2 Register — Index 2Bh (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7-6	GPIO13_SEL	R/W	00b	PECI_REQ#/IRTX/GPIO13 function select. 00: The pin function is PECI_REQ# 01: The pin function is IRTX. 10: Reserved. 11: The pin function is GPIO13
5-4	GPIO12_SEL	R/W	11b	GPIO12/WDTRST# function select. 00: The pin function is WDTRST#. 01: reserved. 10: reserved. 11: The pin function is GPIO12.

3-2	GPIO11_SEL	R/W	00b	FANCTRL3/GPIO11/IRTX1 function select. 00: The pin function is FANCTRL3. 01: The pin function is IRTX1. 10: Reserved. 11: The pin function is GPIO11.
1-0	GPIO10_SEL	R/W	00b	FANIN3/GPIO10/IRRX1 function select. 00: The pin function is FANIN3. 01: The pin function is IRRX1. 10: Reserved. 11: The pin function is GPIO10.

8.1.13 Multi Function Select 3 Register — Index 2Ch (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	GPIO1/2_Clear	R/W	0	0: Cleared by 3VSB 1: Cleared by LRESET#
6	UR2_GP_EN2	R/W	0	0: Pin2~4 and pin126~128 function as UART2 modem control. 1: Pin2~4 and pin126~128 function as GPIO3x.
5	UR2_GP_EN1	R/W	0	0: Pin5, 6 function as UART2 SOUT2/SIN2. 1: Pin5, 6 function as GPIO3x.
4	FDC_GP_EN	R/W	0	0: Pin 7 ~ 19 function as FDC. 1: Pin 7 ~19 function as GPIOs.
3	GPIO16_SEL	R/W	0	PECI/TSI_DAT/IBX_SDA/GPIO16 function select. 0: The pin function is PECI/TSI_DAT/IBX_SDA decided by INTEL_MODEL register. 1: The pin function is GPIO16.
2	GPIO15_SEL	R/W	0	SST/TSI_CLK/IBX_CLK/GPIO15 function select. 0: The pin function is SST/TSI_CLK/IBX_CLK decided by INTEL_MODEL register. 1: The pin function is GPIO15.
1-0	GPIO14_SEL	R/W	00b	PECI_AVL/IRRX/GPIO14 function select. 00: The pin function is PECI_AVL. 01: The pin function is IRRX. 10: Reserved. 11: The pin function is GPIO14.

8.1.14 Wakeup Control Register — Index 2Dh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	SLOT_PWR_SEL	R/W	0	0: SLOTOCC# is pull-up to VSB3V. 1: SLOTOCC# is pull-up to VBAT.
6	VSBOK_HYS_DIS	R/W	0	0: RSMRST# will sink low when VSB3V is below 2.6V. 1: RSMRST# will sink low when VSB3V is below 2.95V. VSB3V power good level is 2.95V.

6	S3_Reset	R/W	0	0: VREF1~3 settings are kept when S3# becomes low 1: VREF1~3 will be reset to default when S3# becomes low
5	VREF_S3	R/W	0	1: VREF2 and 3 keep power on In the S3 state 0: VREF2 and 3 are power down In the S3 state
4	KEY_SEL_ADD	R/W	0	This bit is added to add more wakeup key function.
3	WAKEUP_EN	R/W	1	0: disable keyboard/mouse wake up. 1: enable keyboard/mouse wake up.
2-1	KEY_SEL	R/W	00	This registers select the keyboard wake up key. Accompanying with KEY_SEL_ADD, there are eight wakeup keys:
0	MO_SEL	R/W	0	This register selects the mouse wake up key. 0: Wake up by click. 1: Wake up by click and movement.

KEY_SEL_ADD	KEY_SEL	Wakeup Key
0	00	Ctrl + Esc
0	01	Ctrl + F1
0	10	Ctrl + Space
0	11	Any Key
1	00	Windows Wakeup
1	01	Windows Power
1	10	Ctrl + Alt + Space
1	11	Space

8.2 FDC Registers (CR00)

FDC Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	FDC_EN	R/W	1	0: disable FDC. 1: enable FDC.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of FDC base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	F0h	The LSB of FDC base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELFDCIRQ	R/W	06h	Select the IRQ channel for FDC.

DMA Channel Select Register — Index 74h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	-	Reserved.
2-0	SELFDCDMA	R/W	010	Select the DMA channel for FDC.

FDD Mode Register — Index F0h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	FDC_SW_WP	R/W	0	Write “1” to this bit will force FDC to write protect. Otherwise, write protect is controlled by hardware pin WP#.
3-2	IF_MODE	R/W	11	00: Model 30 mode. 01: PS/2 mode. 10: Reserved. 11: AT mode (default).
1	FDMAMODE	R/W	1	0: enable burst mode. 1: non-busrt mode (default).
0	Reserved	R/W	0	Reserved

FDD Drive Type Register — Index F2h

Bit	Name	R/W	Default	Description
7-2	Reserved	-	-	Reserved.
1-0	FDD_TYPE	R/W	11	FDD drive type.

FDD Selection Register — Index F4h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4-3	FDD_DRT	R/W	00	Data rate table select, refer to table A. 00: select regular drives and 2.88 format. 01: Reserved. 10: 2 mega tape. 11: reserved.
2	Reserved	-	-	Reserved.
1-0	FDD_DT	R/W	00	Drive type select, refer to table B.

TABLE A

Data Rate Table Select		Data Rate		Selected Data Rate		DENSEL
FDD_DRT[1]	FDD_DRT[0]	DATARATE1	DATARATE0	MFM	FM	
0	0	0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
		1	1	1Meg	---	1
0	1	0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
		1	1	1Meg	---	1
1	0	0	0	500K	250K	1

		0	1	2Meg	---	0
		1	0	250K	125K	0
		1	1	1Meg	---	1

TABLE B

Drive Type		DRVDEN0	Remark
FDD_DT1	FDD_DT0		
0	0	DENSEL	4/2/1 MB 3.5” 2/1 MB 5.25”
0	1	DATARATE1	
1	0	DENSEL#	
1	1	DATARATE0	

8.3 UART1 Registers (CR01)

UART 1 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR1_EN	R/W	1	0: disable UART 1. 1: enable UART 1.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of UART 1 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	F8h	The LSB of UART 1 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELUR1IRQ	R/W	4h	Select the IRQ channel for UART 1.

RS485 Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	RS485_EN	R/W	0	0: RS232 driver. 1: RS485 driver. Auto drive RTS# low when transmitting data.
3-0	Reserved	-	-	Reserved.

8.4 UART 2 Registers (CR02)

UART 2 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR2_EN	R/W	1	0: disable UART 2. 1: enable UART 2.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	02h	The MSB of UART 2 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	F8h	The LSB of UART 2 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELUR2IRQ	R/W	3h	Select the IRQ channel for UART 2.

RS485 Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	RS485_EN	R/W	0	0: RS232 driver. 1: RS485 driver. Auto drive RTS# low when transmitting data.
3	RXW4C_IR	R/W	0	0: No reception delay when SIR is changed form TX to RX. 1: Reception delays 4 characters time when SIR is changed form TX to RX.
2	TXW4C_IR	R/W	0	0: No transmission delay when SIR is changed form RX to TX. 1: Transmission delays 4 characters time when SIR is changed form RX to TX.
1-0	Reserved	-	-	Reserved.

SIR Mode Control Register — Index F1h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	Reserved	-	-	Reserved.
5	Reserved	-	-	Reserved.
4-3	IRMODE	R/W	00	00: disable IR function. 01: disable IR function. 10: IrDA function, active pulse is 1.6uS. 11: IrDA function, active pulse is 3/16 bit time.
2	HDUPLX	R/W	1	0: SIR is in full duplex mode for loopbak test. TXW4C_IR and RXW4C_IR are of no use. 1: SIR is in half duplex mode.
1	TXINV_IR	R/W	0	0: IRTX1 is in normal condition. 1: inverse the IRTX1.
0	RXINV_IR	R/W	0	0: IRRX1is in normal condition. 1: inverse the IRRX1.

8.5 Parallel Port Registers (CR03)

Parallel Port Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	PRT_EN	R/W	1	0: disable Parallel Port. 1: enable Parallel Port.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of Parallel Port base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	78h	The LSB of Parallel Port base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
3-0	SELPRTIRQ	R/W	7h	Select the IRQ channel for Parallel Port.

DMA Channel Select Register — Index 74h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	ECP_DMA_MODE	R/W	0	0: non-burst mode DMA. 1: enable burst mode DMA.
3	Reserved	-	-	Reserved.
2-0	SELPRTDMA	R/W	011	Select the DMA channel for Parallel Port.

PRT Mode Select Register — Index F0h

Bit	Name	R/W	Default	Description
7	SPP_IRQ_MODE	R/W	0	Interrupt mode in non-ECP mode. 0: Level mode. 1: Pulse mode.
6-3	ECP_FIFO_THR	R/W	1000	ECP FIFO threshold.
2-0	PRT_MODE	R/W	010	000: Standard and Bi-direction (SPP) mode. 001: EPP 1.9 and SPP mode. 010: ECP mode (default). 011: ECP and EPP 1.9 mode. 100: Printer mode. 101: EPP 1.7 and SPP mode. 110: Reserved. 111: ECP and EPP1.7 mode.

8.6 Hardware Monitor Registers (CR04)

8.6.1 Hardware Monitor Configuration Registers

Hardware Monitor Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved

0	HM_EN	R/W	1	0: disable Hardware Monitor. 1: enable Hardware Monitor.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	02h	The MSB of Hardware Monitor base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	95h	The LSB of Hardware Monitor base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELHMIRQ	R/W	0000	Select the IRQ channel for Hardware Monitor.

8.7 KBC Registers (CR05)

KBC Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	KBC_EN	R/W	1	0: disable KBC. 1: enable KBC.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of KBC command port address. The address of data port is command port address + 4;

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	60h	The LSB of KBC command port address. The address of data port is command port address + 4.

KB IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELKIRQ	R/W	1h	Select the IRQ channel for keyboard interrupt.

Mouse IRQ Channel Select Register — Index 72h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELMIRQ	R/W	Ch	Select the IRQ channel for PS/2 mouse interrupt.

Auto Swap Register — Index FEh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	AUTO_DET_EN	R/W	1b	0: disable auto detect keyboard/mouse swap. 1: enable auto detect keyboard/mouse swap.
6-5	Reserved	-	-	Reserved.

4	KB_MO_SWAP	R/W	0b	0: Keyboard/mouse not swap. 1: Keyboard/mouse swap. This bit is set/clear by hardware if AUTO_DET_EN is set to "1". Users could also program this bit manually.
3-0	Reserved	R/W	1h	Reserved

8.8 GPIO Registers (CR06) (All registers of GPIO are powered by VSB3V)

GPIO0 Output Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO06_OE	R/W	0	0: GPIO06 is in input mode. 1: GPIO06 is in output mode.
5	GPIO05_OE	R/W	0	0: GPIO05 is in input mode. 1: GPIO05 is in output mode.
4	GPIO04_OE	R/W	0	0: GPIO04 is in input mode. 1: GPIO04 is in output mode.
3	GPIO03_OE	R/W	0	0: GPIO03 is in input mode. 1: GPIO03 is in output mode.
2	GPIO02_OE	R/W	0	0: GPIO02 is in input mode. 1: GPIO02 is in output mode.
1	GPIO01_OE	R/W	0	0: GPIO01 is in input mode. 1: GPIO01 is in output mode.
0	GPIO00_OE	R/W	0	0: GPIO00 is in input mode. 1: GPIO00 is in output mode.

GPIO0 Output Data Register — Index F1h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO06_VAL	R/W	1	0: GPIO06 outputs 0 when in output mode. 1: GPIO06 outputs1 when in output mode.
5	GPIO05_VAL	R/W	1	0: GPIO05 outputs 0 when in output mode. 1: GPIO05 outputs 1 when in output mode.
4	GPIO04_VAL	R/W	1	0: GPIO04 outputs 0 when in output mode. 1: GPIO04 outputs 1 when in output mode.
3	GPIO03_VAL	R/W	1	0: GPIO03 outputs 0 when in output mode. 1: GPIO03 outputs 1 when in output mode.
2	GPIO02_VAL	R/W	1	0: GPIO02 outputs 0 when in output mode. 1: GPIO02 outputs 1 when in output mode.
1	GPIO01_VAL	R/W	1	0: GPIO01 outputs 0 when in output mode. 1: GPIO01 outputs 1 when in output mode.
0	GPIO00_VAL	R/W	1	0: GPIO00 outputs 0 when in output mode. 1: GPIO00 outputs 1 when in output mode.

GPIO0 Pin Status Register — Index F2h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO06_IN	R	-	The pin status of GPIO06/Beep/Alert#.
5	GPIO05_IN	R	-	The pin status of GPIO05/LED_VCC.
4	GPIO04_IN	R	-	The pin status of GPIO04/LED_VSB.
3	GPIO03_IN	R	-	The pin status of SLOTCC#/GPIO03.
2	GPIO02_IN	R	-	The pin status of BUSOUT2/GPIO02.
1	GPIO01_IN	R	-	The pin status of BUSOUT1/GPIO01.
0	GPIO00_IN	R	-	The pin status of BUSOUT0/GPIO00.

GPIO0 Drive Enable Register — Index F3h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO06_DRV_EN	R/W	0	0: GPIO06 is open drain in output mode. 1: GPIO06 is push pull in output mode.
5	GPIO05_DRV_EN	R/W	0	0: GPIO05 is open drain in output mode. 1: GPIO05 is push pull in output mode.
4	GPIO04_DRV_EN	R/W	0	0: GPIO04 is open drain in output mode. 1: GPIO04 is push pull in output mode.
3	GPIO03_DRV_EN	R/W	0	0: GPIO03 is open drain in output mode. 1: Reserved.
2	GPIO02_DRV_EN	R/W	0	0: GPIO02 is open drain in output mode. 1: GPIO02 is push pull in output mode.
1	GPIO01_DRV_EN	R/W	0	0: GPIO01 is open drain in output mode. 1: GPIO01 is push pull in output mode.
0	GPIO00_DRV_EN	R/W	0	0: GPIO00 is open drain in output mode. 1: GPIO00 is push pull in output mode.

LED_VSB Control Register — Index FEh

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5-4	LED_VSB_S5_MODE	R/W	0	These bits control the LED_VSB output mode in S5 state. 00: Sink 0 01: Tri-state. 10: 0.5Hz clock 11: 1Hz clock.
3-2	LED_VSB_S3_MODE	R/W	0	These bits control the LED_VSB output mode in S3 state. 00: Sink 0 01: Tri-state. 10: 0.5Hz clock 11: 1Hz clock.

1-0	LED_VSB_S0_MODE	R/W	0	These bits control the LED_VSB output mode in S0 state. 00: Sink 0 01: Tri-state. 10: 0.5Hz clock 11: 1Hz clock.

LED_VCC Control Register — Index FFh

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5-4	LED_VCC_S5_MODE	R/W	0	These bits control the LED_VCC output mode in S5 state. 00: Sink 0 01: Tri-state. 10: 0.5Hz clock 11: 1Hz clock.
3-2	LED_VCC_S3_MODE	R/W	0	These bits control the LED_VCC output mode in S3 state. 00: Sink 0 01: Tri-state. 10: 0.5Hz clock 11: 1Hz clock.
1-0	LED_VCC_S0_MODE	R/W	0	These bits control the LED_VCC output mode in S0 state. 00: Sink 0 01: Tri-state. 10: 0.5Hz clock 11: 1Hz clock.

GPIO1 Output Enable Register — Index E0h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO16_OE	R/W	0	0: GPIO16 is in input mode. 1: GPIO16 is in output mode.
5	GPIO15_OE	R/W	0	0: GPIO15 is in input mode. 1: GPIO15 is in output mode.
4	GPIO14_OE	R/W	0	0: GPIO14 is in input mode. 1: GPIO14 is in output mode.
3	GPIO13_OE	R/W	0	0: GPIO13 is in input mode. 1: GPIO13 is in output mode.
2	GPIO12_OE	R/W	0	0: GPIO12 is in input mode. 1: GPIO12 is in output mode.
1	GPIO11_OE	R/W	0	0: GPIO11 is in input mode. 1: GPIO11 is in output mode.
0	GPIO10_OE	R/W	0	0: GPIO10 is in input mode. 1: GPIO10 is in output mode.

GPIO1 Output Data Register — Index E1h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.

6	GPIO16_VAL	R/W	1	0: GPIO16 outputs 0 when in output mode. 1: GPIO16 outputs1 when in output mode.
5	GPIO15_VAL	R/W	1	0: GPIO15 outputs 0 when in output mode. 1: GPIO15 outputs 1 when in output mode.
4	GPIO14_VAL	R/W	1	0: GPIO14 outputs 0 when in output mode. 1: GPIO14 outputs 1 when in output mode.
3	GPIO13_VAL	R/W	1	0: GPIO13 outputs 0 when in output mode. 1: GPIO13 outputs 1 when in output mode.
2	GPIO12_VAL	R/W	1	0: GPIO12 outputs 0 when in output mode. 1: GPIO12 outputs 1 when in output mode.
1	GPIO11_VAL	R/W	1	0: GPIO11 outputs 0 when in output mode. 1: GPIO11 outputs 1 when in output mode.
0	GPIO10_VAL	R/W	1	0: GPIO10 outputs 0 when in output mode. 1: GPIO10 outputs 1 when in output mode.

GPIO1 Pin Status Register — Index E2h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO16_IN	R	-	The pin status of PECI/TSI_DAT/IBX_SDA/GPIO16
5	GPIO15_IN	R	-	The pin status of SST/TSI_CLK/IBX_CLK/GPIO15.
4	GPIO14_IN	R	-	The pin status of PECI_AVL/IRRX/GPIO14.
3	GPIO13_IN	R	-	The pin status of PECI_REQ#/IRTX/GPIO13.
2	GPIO12_IN	R	-	The pin status of GPIO12/WDTRST#
1	GPIO11_IN	R	-	The pin status of FANCTL3/GPIO11/IRTX1.
0	GPIO10_IN	R	-	The pin status of FANIN3/GPIO10/IRRX1.

GPIO1 Drive Enable Register — Index E3h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO16_DRV_EN	R/W	0	0: GPIO16 is open drain in output mode. 1: GPIO16 is push pull in output mode.
5	GPIO15_DRV_EN	R/W	0	0: GPIO15 is open drain in output mode. 1: GPIO15 is push pull in output mode.
4	GPIO14_DRV_EN	R/W	0	0: GPIO14 is open drain in output mode. 1: GPIO14 is push pull in output mode.
3	GPIO13_DRV_EN	R/W	0	0: GPIO13 is open drain in output mode. 1: GPIO13 is push pull in output mode.
2	GPIO12_DRV_EN	R/W	0	0: GPIO12 is open drain in output mode. 1: GPIO12 is push pull in output mode.
1	GPIO11_DRV_EN	R/W	0	0: GPIO11 is open drain in output mode. 1: GPIO11 is push pull in output mode.
0	GPIO10_DRV_EN	R/W	0	0: GPIO10 is open drain in output mode. 1: GPIO10 is push pull in output mode.

GPIO2 Output Enable Register — Index D0h

Bit	Name	R/W	Default	Description
7	GPIO27_OE	R/W	0	0: GPIO27 is in input mode. 1: GPIO27 is in output mode.
6	GPIO26_OE	R/W	0	0: GPIO26 is in input mode. 1: GPIO25 is in output mode.
5	GPIO25_OE	R/W	0	0: GPIO25 is in input mode. 1: GPIO25 is in output mode.
4	GPIO24_OE	R/W	0	0: GPIO24 is in input mode. 1: GPIO24 is in output mode.
3	GPIO23_OE	R/W	0	0: GPIO23 is in input mode. 1: GPIO23 is in output mode.
2	GPIO22_OE	R/W	0	0: GPIO22 is in input mode. 1: GPIO22 is in output mode.
1	GPIO21_OE	R/W	0	0: GPIO21 is in input mode. 1: GPIO21 is in output mode.
0	GPIO20_OE	R/W	0	0: GPIO20 is in input mode. 1: GPIO20 is in output mode.

GPIO2 Output Data Register — Index D1h

Bit	Name	R/W	Default	Description
7	GPIO27_VAL	R/W	1	0: GPIO27 outputs 0 when in output mode. 1: GPIO27 outputs 1 when in output mode.
6	GPIO26_VAL	R/W	1	0: GPIO26 outputs 0 when in output mode. 1: GPIO26 outputs 1 when in output mode.
5	GPIO25_VAL	R/W	1	0: GPIO25 outputs 0 when in output mode. 1: GPIO25 outputs 1 when in output mode.
4	GPIO24_VAL	R/W	1	0: GPIO24 outputs 0 when in output mode. 1: GPIO24 outputs 1 when in output mode.
3	GPIO23_VAL	R/W	1	0: GPIO23 outputs 0 when in output mode. 1: GPIO23 outputs 1 when in output mode.
2	GPIO22_VAL	R/W	1	0: GPIO22 outputs 0 when in output mode. 1: GPIO22 outputs 1 when in output mode.
1	GPIO21_VAL	R/W	1	0: GPIO21 outputs 0 when in output mode. 1: GPIO21 outputs 1 when in output mode.
0	GPIO20_VAL	R/W	1	0: GPIO20 outputs 0 when in output mode. 1: GPIO20 outputs 1 when in output mode.

GPIO2 Pin Status Register — Index D2h

Bit	Name	R/W	Default	Description
7	GPIO27_IN	R	-	The pin status of BSUIN2/GPIO27.
6	GPIO26_IN	R	-	The pin status of BUSIN1/GPIO26.
5	GPIO25_IN	R	-	The pin status of BUSIN0/GPIO25.
4	GPIO24_IN	R	-	The pin status of GPIO24/FWH_DIS.
3	GPIO23_IN	R	-	The pin status of GPIO23/SPI_MOSI.

2	GPIO22_IN	R	-	The pin status of GPIO22/SPI_MISO.
1	GPIO21_IN	R	-	The pin status of GPIO21/SPI_CS0#.
0	GPIO20_IN	R	-	The pin status of GPIO20/SPI_SLK#.

GPIO2 Drive Enable Register — Index D3h

Bit	Name	R/W	Default	Description
7	GPIO27_DRV_EN	R/W	0	0: GPIO27 is open drain in output mode. 1: GPIO27 is push pull in output mode.
6	GPIO26_DRV_EN	R/W	0	0: GPIO26 is open drain in output mode. 1: GPIO26 is push pull in output mode.
5	GPIO25_DRV_EN	R/W	0	0: GPIO25 is open drain in output mode. 1: GPIO25 is push pull in output mode.
4	GPIO24_DRV_EN	R/W	0	0: GPIO24 is open drain in output mode. 1: GPIO24 is push pull in output mode.
3	GPIO23_DRV_EN	R/W	0	0: GPIO23 is open drain in output mode. 1: GPIO23 is push pull in output mode.
2	GPIO22_DRV_EN	R/W	0	0: GPIO22 is open drain in output mode. 1: GPIO22 is push pull in output mode.
1	GPIO21_DRV_EN	R/W	0	0: GPIO21 is open drain in output mode. 1: GPIO21 is push pull in output mode.
0	GPIO20_DRV_EN	R/W	0	0: GPIO20 is open drain in output mode. 1: GPIO20 is push pull in output mode.

GPIO3 Output Enable Register — Index C0h

Bit	Name	R/W	Default	Description
7	GPIO37_OE	R/W	0	0: GPIO37 is in input mode. 1: GPIO37 is in output mode.
6	GPIO36_OE	R/W	0	0: GPIO36 is in input mode. 1: GPIO35 is in output mode.
5	GPIO35_OE	R/W	0	0: GPIO35 is in input mode. 1: GPIO35 is in output mode.
4	GPIO34_OE	R/W	0	0: GPIO34 is in input mode. 1: GPIO34 is in output mode.
3	GPIO33_OE	R/W	0	0: GPIO33 is in input mode. 1: GPIO33 is in output mode.
2	GPIO32_OE	R/W	0	0: GPIO32 is in input mode. 1: GPIO32 is in output mode.
1	GPIO31_OE	R/W	0	0: GPIO31 is in input mode. 1: GPIO31 is in output mode.
0	GPIO30_OE	R/W	0	0: GPIO30 is in input mode. 1: GPIO30 is in output mode.

GPIO3 Output Data Register — Index C1h

Bit	Name	R/W	Default	Description
7	GPIO37_VAL	R/W	1	0: GPIO37 outputs 0 when in output mode. 1: GPIO37 outputs 1 when in output mode.

6	GPIO36_VAL	R/W	1	0: GPIO36 outputs 0 when in output mode. 1: GPIO36 outputs 1 when in output mode.
5	GPIO35_VAL	R/W	1	0: GPIO35 outputs 0 when in output mode. 1: GPIO35 outputs 1 when in output mode.
4	GPIO34_VAL	R/W	1	0: GPIO34 outputs 0 when in output mode. 1: GPIO34 outputs 1 when in output mode.
3	GPIO33_VAL	R/W	1	0: GPIO33 outputs 0 when in output mode. 1: GPIO33 outputs 1 when in output mode.
2	GPIO32_VAL	R/W	1	0: GPIO32 outputs 0 when in output mode. 1: GPIO32 outputs 1 when in output mode.
1	GPIO31_VAL	R/W	1	0: GPIO31 outputs 0 when in output mode. 1: GPIO31 outputs 1 when in output mode.
0	GPIO30_VAL	R/W	1	0: GPIO30 outputs 0 when in output mode. 1: GPIO30 outputs 1 when in output mode.

GPIO3 Pin Status Register — Index C2h

Bit	Name	R/W	Default	Description
7	GPIO37_IN	R	-	The pin status of SIN2/SEGE/GPIO37.
6	GPIO36_IN	R	-	The pin status of SOUT2/SEGB/GPIO36/SPI_TRAP.
5	GPIO35_IN	R	-	The pin status of DSR2#/L#/GPIO35.
4	GPIO34_IN	R	-	The pin status of RTS2#/SEGC/GPIO34/PWM_DC.
3	GPIO33_IN	R	-	The pin status of DTR2#/SEGD/GPIO33/FWH_TRAP.
2	GPIO32_IN	R	-	The pin status of CTS2#/SEGA/GPIO32.
1	GPIO31_IN	R	-	The pin status of RI2#/GPIO31.
0	GPIO30_IN	R	-	The pin status of DCD2#/GPIO30.

GPIO3 Drive Enable Register — Index C3h

Bit	Name	R/W	Default	Description
7	GPIO37_DRV_EN	R/W	0	0: GPIO37 is open drain in output mode. 1: GPIO37 is push pull in output mode.
6	GPIO36_DRV_EN	R/W	0	0: GPIO36 is open drain in output mode. 1: GPIO36 is push pull in output mode.
5	GPIO35_DRV_EN	R/W	0	0: GPIO35 is open drain in output mode. 1: GPIO35 is push pull in output mode.
4	GPIO34_DRV_EN	R/W	0	0: GPIO34 is open drain in output mode. 1: GPIO34 is push pull in output mode.
3	GPIO33_DRV_EN	R/W	0	0: GPIO33 is open drain in output mode. 1: GPIO33 is push pull in output mode.
2	GPIO32_DRV_EN	R/W	0	0: GPIO32 is open drain in output mode. 1: GPIO32 is push pull in output mode.
1	GPIO31_DRV_EN	R/W	0	0: GPIO31 is open drain in output mode. 1: GPIO31 is push pull in output mode.
0	GPIO30_DRV_EN	R/W	0	0: GPIO30 is open drain in output mode. 1: GPIO30 is push pull in output mode.

GPIO4 Output Enable Register — Index B0h

Bit	Name	R/W	Default	Description
7	GPIO47_OE	R/W	0	0: GPIO47 is in input mode. 1: GPIO47 is in output mode.
6	GPIO46_OE	R/W	0	0: GPIO46 is in input mode. 1: GPIO45 is in output mode.
5	GPIO45_OE	R/W	0	0: GPIO45 is in input mode. 1: GPIO45 is in output mode.
4	GPIO44_OE	R/W	0	0: GPIO44 is in input mode. 1: GPIO44 is in output mode.
3	GPIO43_OE	R/W	0	0: GPIO43 is in input mode. 1: GPIO43 is in output mode.
2	GPIO42_OE	R/W	0	0: GPIO42 is in input mode. 1: GPIO42 is in output mode.
1	GPIO41_OE	R/W	0	0: GPIO41 is in input mode. 1: GPIO41 is in output mode.
0	GPIO40_OE	R/W	0	0: GPIO40 is in input mode. 1: GPIO40 is in output mode.

GPIO4 Output Data Register — Index B1h

Bit	Name	R/W	Default	Description
7	GPIO47_VAL	R/W	1	0: GPIO47 outputs 0 when in output mode. 1: GPIO47 outputs 1 when in output mode.
6	GPIO46_VAL	R/W	1	0: GPIO46 outputs 0 when in output mode. 1: GPIO46 outputs 1 when in output mode.
5	GPIO45_VAL	R/W	1	0: GPIO45 outputs 0 when in output mode. 1: GPIO45 outputs 1 when in output mode.
4	GPIO44_VAL	R/W	1	0: GPIO44 outputs 0 when in output mode. 1: GPIO44 outputs 1 when in output mode.
3	GPIO43_VAL	R/W	1	0: GPIO43 outputs 0 when in output mode. 1: GPIO43 outputs 1 when in output mode.
2	GPIO42_VAL	R/W	1	0: GPIO42 outputs 0 when in output mode. 1: GPIO42 outputs 1 when in output mode.
1	GPIO41_VAL	R/W	1	0: GPIO41 outputs 0 when in output mode. 1: GPIO41 outputs 1 when in output mode.
0	GPIO40_VAL	R/W	1	0: GPIO40 outputs 0 when in output mode. 1: GPIO40 outputs 1 when in output mode.

GPIO4 Pin Status Register — Index B2h

Bit	Name	R/W	Default	Description
7	GPIO47_IN	R	-	The pin status of WGATE#/GPIO47.
6	GPIO46_IN	R	-	The pin status of HDSEL#/GPIO46.
5	GPIO45_IN	R	-	The pin status of STEP#/GPIO45.
4	GPIO44_IN	R	-	The pin status of DIR#/GPIO44.
3	GPIO43_IN	R	-	The pin status of WDATA#/GPIO43.

2	GPIO42_IN	R	-	The pin status of DRVA#/GPIO42.
1	GPIO41_IN	R	-	The pin status of MOA#/GPIO41.
0	GPIO40_IN	R	-	The pin status of DENSEL#/GPIO40.

GPIO5 Output Enable Register — Index A0h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO54_OE	R/W	0	0: GPIO54 is in input mode. 1: GPIO54 is in output mode.
3	GPIO53_OE	R/W	0	0: GPIO53 is in input mode. 1: GPIO53 is in output mode.
2	GPIO52_OE	R/W	0	0: GPIO52 is in input mode. 1: GPIO52 is in output mode.
1	GPIO51_OE	R/W	0	0: GPIO51 is in input mode. 1: GPIO51 is in output mode.
0	GPIO50_OE	R/W	0	0: GPIO50 is in input mode. 1: GPIO50 is in output mode.

GPIO5 Output Data Register — Index A1h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO54_VAL	R/W	1	0: GPIO54 outputs 0 when in output mode. 1: GPIO54 outputs 1 when in output mode.
3	GPIO53_VAL	R/W	1	0: GPIO53 outputs 0 when in output mode. 1: GPIO53 outputs 1 when in output mode.
2	GPIO52_VAL	R/W	1	0: GPIO52 outputs 0 when in output mode. 1: GPIO52 outputs 1 when in output mode.
1	GPIO51_VAL	R/W	1	0: GPIO51 outputs 0 when in output mode. 1: GPIO51 outputs 1 when in output mode.
0	GPIO50_VAL	R/W	1	0: GPIO50 outputs 0 when in output mode. 1: GPIO50 outputs 1 when in output mode.

GPIO5 Pin Status Register — Index A2h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO54_IN	R	-	The pin status of DSKCHG#/GPIO54.
3	GPIO53_IN	R	-	The pin status of WPT#/GPIO53.
2	GPIO52_IN	R	-	The pin status of INDEX#/GPIO52.
1	GPIO51_IN	R	-	The pin status of TRK0#/GPIO51.
0	GPIO50_IN	R	-	The pin status of RDDATA#/GPIO50.

GPIO5 Drive Enable Register — Index A3h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.

4	GPIO54_DRV_EN	R/W	0	0: GPIO54 is open drain in output mode. 1: GPIO54 is push pull in output mode.
3	GPIO53_DRV_EN	R/W	0	0: GPIO53 is open drain in output mode. 1: GPIO53 is push pull in output mode.
2	GPIO52_DRV_EN	R/W	0	0: GPIO52 is open drain in output mode. 1: GPIO52 is push pull in output mode.
1	GPIO51_DRV_EN	R/W	0	0: GPIO51 is open drain in output mode. 1: GPIO51 is push pull in output mode.
0	GPIO50_DRV_EN	R/W	0	0: GPIO50 is open drain in output mode. 1: GPIO50 is push pull in output mode.

GPIO6 Output Enable Register — Index 90h

Bit	Name	R/W	Default	Description
7	GPIO67_OE	R/W	0	0: GPIO67 is in input mode. 1: GPIO67 is in output mode.
6	GPIO66_OE	R/W	0	0: GPIO66 is in input mode. 1: GPIO65 is in output mode.
5	GPIO65_OE	R/W	0	0: GPIO65 is in input mode. 1: GPIO65 is in output mode.
4	GPIO64_OE	R/W	0	0: GPIO64 is in input mode. 1: GPIO64 is in output mode.
3	GPIO63_OE	R/W	0	0: GPIO63 is in input mode. 1: GPIO63 is in output mode.
2	GPIO62_OE	R/W	0	0: GPIO62 is in input mode. 1: GPIO62 is in output mode.
1	GPIO61_OE	R/W	0	0: GPIO61 is in input mode. 1: GPIO61 is in output mode.
0	GPIO60_OE	R/W	0	0: GPIO60 is in input mode. 1: GPIO60 is in output mode.

GPIO6 Output Data Register — Index 91h

Bit	Name	R/W	Default	Description
7	GPIO67_VAL	R/W	1	0: GPIO67 outputs 0 when in output mode. 1: GPIO67 outputs 1 when in output mode.
6	GPIO66_VAL	R/W	1	0: GPIO66 outputs 0 when in output mode. 1: GPIO66 outputs 1 when in output mode.
5	GPIO65_VAL	R/W	1	0: GPIO65 outputs 0 when in output mode. 1: GPIO65 outputs 1 when in output mode.
4	GPIO64_VAL	R/W	1	0: GPIO64 outputs 0 when in output mode. 1: GPIO64 outputs 1 when in output mode.
3	GPIO63_VAL	R/W	1	0: GPIO63 outputs 0 when in output mode. 1: GPIO63 outputs 1 when in output mode.
2	GPIO62_VAL	R/W	1	0: GPIO62 outputs 0 when in output mode. 1: GPIO62 outputs 1 when in output mode.

1	GPIO61_VAL	R/W	1	0: GPIO61 outputs 0 when in output mode. 1: GPIO61 outputs 1 when in output mode.
0	GPIO60_VAL	R/W	1	0: GPIO60 outputs 0 when in output mode. 1: GPIO60 outputs 1 when in output mode.

GPIO6 Pin Status Register — Index 92h

Bit	Name	R/W	Default	Description
7	GPIO67_IN	R	-	The pin status of STB#/L#/VIDIN7/GPIO67.
6	GPIO66_IN	R	-	The pin status of AFD#/H#/VIDIN6/GPIO66.
5	GPIO65_IN	R	-	The pin status of ERR#/VIDIN5/GPIO65.
4	GPIO64_IN	R	-	The pin status of INIT#/VIDIN4/GPIO64.
3	GPIO63_IN	R	-	The pin status of ACK#/VIDIN3 (SVC_IN)/GPIO63.
2	GPIO62_IN	R	-	The pin status of BUSY/VIDIN2 (SVD_IN)/GPIO62.
1	GPIO61_IN	R	-	The pin status of PE/VIDIN1/GPIO61.
0	GPIO60_IN	R	-	The pin status of SLCT/VIDIN0/GPIO60.

GPIO6 Drive Enable Register — Index 93h

Bit	Name	R/W	Default	Description
7	GPIO67_DRV_EN	R/W	0	0: GPIO67 is open drain in output mode. 1: GPIO67 is push pull in output mode.
6	GPIO66_DRV_EN	R/W	0	0: GPIO66 is open drain in output mode. 1: GPIO66 is push pull in output mode.
5	GPIO65_DRV_EN	R/W	0	0: GPIO65 is open drain in output mode. 1: GPIO65 is push pull in output mode.
4	GPIO64_DRV_EN	R/W	0	0: GPIO64 is open drain in output mode. 1: GPIO64 is push pull in output mode.
3	GPIO63_DRV_EN	R/W	0	0: GPIO63 is open drain in output mode. 1: GPIO63 is push pull in output mode.
2	GPIO62_DRV_EN	R/W	0	0: GPIO62 is open drain in output mode. 1: GPIO62 is push pull in output mode.
1	GPIO61_DRV_EN	R/W	0	0: GPIO61 is open drain in output mode. 1: GPIO61 is push pull in output mode.
0	GPIO60_DRV_EN	R/W	0	0: GPIO60 is open drain in output mode. 1: GPIO60 is push pull in output mode.

GPIO7 Output Enable Register — Index 80h

Bit	Name	R/W	Default	Description
7	GPIO77_OE	R/W	0	0: GPIO77 is in input mode. 1: GPIO77 is in output mode.
6	GPIO76_OE	R/W	0	0: GPIO76 is in input mode. 1: GPIO75 is in output mode.
5	GPIO75_OE	R/W	0	0: GPIO75 is in input mode. 1: GPIO75 is in output mode.

4	GPIO74_OE	R/W	0	0: GPIO74 is in input mode. 1: GPIO74 is in output mode.
3	GPIO73_OE	R/W	0	0: GPIO73 is in input mode. 1: GPIO73 is in output mode.
2	GPIO72_OE	R/W	0	0: GPIO72 is in input mode. 1: GPIO72 is in output mode.
1	GPIO71_OE	R/W	0	0: GPIO71 is in input mode. 1: GPIO71 is in output mode.
0	GPIO70_OE	R/W	0	0: GPIO70 is in input mode. 1: GPIO70 is in output mode.

GPIO7 Output Data Register — Index 81h

Bit	Name	R/W	Default	Description
7	GPIO77_VAL	R/W	1	0: GPIO77 outputs 0 when in output mode. 1: GPIO77 outputs 1 when in output mode.
6	GPIO76_VAL	R/W	1	0: GPIO76 outputs 0 when in output mode. 1: GPIO76 outputs 1 when in output mode.
5	GPIO75_VAL	R/W	1	0: GPIO75 outputs 0 when in output mode. 1: GPIO75 outputs 1 when in output mode.
4	GPIO74_VAL	R/W	1	0: GPIO74 outputs 0 when in output mode. 1: GPIO74 outputs 1 when in output mode.
3	GPIO73_VAL	R/W	1	0: GPIO73 outputs 0 when in output mode. 1: GPIO73 outputs 1 when in output mode.
2	GPIO72_VAL	R/W	1	0: GPIO72 outputs 0 when in output mode. 1: GPIO72 outputs 1 when in output mode.
1	GPIO71_VAL	R/W	1	0: GPIO71 outputs 0 when in output mode. 1: GPIO71 outputs 1 when in output mode.
0	GPIO70_VAL	R/W	1	0: GPIO70 outputs 0 when in output mode. 1: GPIO70 outputs 1 when in output mode.

GPIO7 Pin Status Register — Index 82h

Bit	Name	R/W	Default	Description
7	GPIO77_IN	R	-	The pin status of PD7/VIDOUT7/GPIO77.
6	GPIO76_IN	R	-	The pin status of PD6/SEGG/VIDOUT6/GPIO76.
5	GPIO75_IN	R	-	The pin status of PD5/SEGF/VIDOUT5/GPIO75.
4	GPIO74_IN	R	-	The pin status of PD4/SEGE/VIDOUT4/GPIO74.
3	GPIO73_IN	R	-	The pin status of PD3/SEGD/VIDOUT3 (SVC_OUT)/GPIO73.
2	GPIO72_IN	R	-	The pin status of PD2/SEGC/VIDOUT2 (SVD_OUT)/GPIO72.
1	GPIO71_IN	R	-	The pin status of PD1/SEGB/VIDOUT1/GPIO71.
0	GPIO70_IN	R	-	The pin status of PD0/SEGA/VIDOUT0/GPIO70.

GPIO7 Drive Enable Register — Index 83h

Bit	Name	R/W	Default	Description
7	GPIO77_DRV_EN	R/W	0	0: GPIO77 is open drain in output mode. 1: GPIO77 is push pull in output mode.

6	GPIO76_DRV_EN	R/W	0	0: GPIO76 is open drain in output mode. 1: GPIO76 is push pull in output mode.
5	GPIO75_DRV_EN	R/W	0	0: GPIO75 is open drain in output mode. 1: GPIO75 is push pull in output mode.
4	GPIO74_DRV_EN	R/W	0	0: GPIO74 is open drain in output mode. 1: GPIO74 is push pull in output mode.
3	GPIO73_DRV_EN	R/W	0	0: GPIO73 is open drain in output mode. 1: GPIO73 is push pull in output mode.
2	GPIO72_DRV_EN	R/W	0	0: GPIO72 is open drain in output mode. 1: GPIO72 is push pull in output mode.
1	GPIO71_DRV_EN	R/W	0	0: GPIO71 is open drain in output mode. 1: GPIO71 is push pull in output mode.
0	GPIO70_DRV_EN	R/W	0	0: GPIO70 is open drain in output mode. 1: GPIO70 is push pull in output mode.

8.9 VID Registers (CR07)

8.9.1 VID Configuration Registers

VID Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	0	Reserved
0	VID_EN	R/W	0	0: disable VID. 1: enable VID.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of VID base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	00h	The LSB of VID base address.

8.9.2 Device Registers

Configuration Register — Index 00h (* cleared by slotocc_n and watch dog timeout)

Bit	Name	R/W	Default	Description
7	WDOUT_EN	R/W	0	If this bit is set to 1 and watchdog timeout event occurs, WDTRST# output is enabled.
6-1	Reserved	-	0	Reserved
0	WD_RST_EN	R/W	0	0: Disable WDT to reset the VID register marked with *. 1: Enable WDT to reset the VID register marked with *.

BUSOUT Manual Register — Index 02h

Bit	Name	R/W	Default	Description
7*	MANUAL_MODE	R/W	0	0: BUSIN2-0 is bypassed to BUSOUT2-0. 1: BUSOUT2-0 is controlled by BUSOUT_MANUAL. This bit is reset by SLOTOCC# falling edge or WDT (with WD_RT_EN set).
6	KEY_OK	R	-	This bit is 1 represents that the serial key is entered correctly.
5-3	Reserved	R/W	0	Dummy register for future use.
2-0	BUSOUT_MANUAL	R/W	0	The output value for BUSOUT2-0 if MANUAL_MODE is set.

Serial Key Data Register — Index 03h

Bit	Name	R/W	Default	Description
7-0	KEY_DATA	R/W	0	Write serial data to this register correctly, the KEY_OK bit will be set to 1. Hence, users are able to write key protected registers. The sequence to enable KEY_OK is 0x32, 0x5D, 0x42, 0xAC. When KEY_OK is set, write this register 0x35 will clear KEY_OK.

BUSIN Register — Index 04h

Bit	Name	R/W	Default	Description
7-3	Reserved	R	0	Reserved
2:0	BUSIN	R	-	The value of this register depends on the BUSIN_MODE register: BUSIN_MODE is 1: the register indicates the BUS reading from CPU (the pin status of BUS_IN [2:0]). BUSIN_MODE is 0: the register latches the value of BUS_IN [2:0] when BUSIN_MODE changed from 1 to 0.

Watchdog Timer Configuration Register 1— Index 05h

Bit	Name	R/W	Default	Description
7	Reserved	R	0	Reserved
6	WDTMOUT_STS	R/W	0	If watchdog timeout event occurs, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	R/W	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	0	Select output mode (0: level, 1: pulse) of RSTOUT# by setting this bit.
3	WD_UNIT	R/W	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	0	Select output polarity of RSTOUT# (1: high active, 0: low active) by setting this bit.
1:0	WD_PSWIDTH	R/W	0	Select output pulse width of RSTOUT# 0: 1 ms 1: 25 ms 2: 125 ms 3: 5 sec

Watchdog Timer Configuration Register 2 — Index 06h

Bit	Name	R/W	Default	Description
7:0	WD_TIME	R/W	0	Time of watchdog timer

NB Offset Register — Index 07h

Bit	Name	R/W	Default	Description
7:0	*NB_OFFSET	R/W	0	Program this byte to add offset to VDDNB in AMD SVID interface. The value will be “0” before PWROK.

VDD0 Offset Register — Index 08h

Bit	Name	R/W	Default	Description
7:0	*VDD0_OFFSET	R/W	0	Program this byte to add offset to 1. VDD0 in AMD SVID interface. 2. VININ in AMD PVID interface (LSB is not used, VDD0_OFFSET[1] is the smallest step). 3. VIDIN in Intel VRM11. The value will be “0” before PWROK.

VDD1 Offset Register — Index 09h

Bit	Name	R/W	Default	Description
7:0	*VDD1_OFFSET	R/W	0	Program this byte to add offset to VDD1 in AMD SVID interface. The value will be “0” before PWROK.

WDT PME Register — Index 0Ah

Bit	Name	R/W	Default	Description
7	WDT_PME	R	0	0: No WDT PME occurred. 1: WDT PME occurred. The WDT PME is occurred one unit before WDT timeout.
6	WDT_PME_EN	R/W	0	0: Disable WDT PME. 1: Enable WDT PME.
5-1	Reserved	R	0	Reserved
0	CPU_CHANGE	R/W	0	This bit will be set at SLOTOCC# rise edge. Internal 1us de-bounce circuit is implemented. Write “1” to this bit will clear the status.

VDDNB Manual Register — Index 0Bh

Bit	Name	R/W	Default	Description
7:0	VDDNB_MANUAL	R/W	0	This byte is used to program the manual value for VDDNB of AMD SVID interface in manual mode. Set VID_BANK_SEL “1” to access this byte.
	VDDNB_IN	R	-	The value of VDDNB from CPU (AMD SVID interface only). Set VID_BANK_SEL “0” to read this byte.

VDD0 Manual Register — Index 0Ch

Bit	Name	R/W	Default	Description
7:0	VDD0_MANUAL	R/W	0	This byte is used to program the manual value for 1. VDD0 of AMD SVID interface in manual mode. 2. VIDOUT of AMD PVID interface in manual mode (The output is controlled by VDD0_MANUAL [6:1] since AMD PVID only has 6 pins). 3. VIDOUT of Intel VRM11 in manual mode. Set VID_BANK_SEL “1” to access this byte.
	VDD0_IN	R	-	This byte has three functions: 1. VDD0 read from CPU in AMD SVID interface. 2. {1’b0, VIDIN [5:0], 1’b0} in AMD PVID interface. 3. VIDIN in Intel VRM11. Set VID_BANK_SEL “0” to read this byte.

VDD1 Manual Register — Index 0Dh

Bit	Name	R/W	Default	Description
7:0	VDD1_MANUAL	R/W	0	This byte is used to program the manual value for VDD1 of AMD SVID interface in manual mode. Set VID_BANK_SEL "1" to access this byte.
	VDD1_IN	R	-	The value of VDD1 from CPU (AMD SVID interface only). Set VID_BANK_SEL "0" to read this byte.

PSI Control Register — Index 0Eh

Bit	Name	R/W	Default	Description
7	VID_BANK_SEL	R/W	0	Select the different bank to access other register at the same index.
6-5	Reserved	-	0	Reserved
4	VRM_SEL	R/W	0	If parallel VID interface is detected. Program this bit to determine AMD/Intel model. 0: Intel VRM11 1: AMD PVID
3	PSI_VDD1	R/W	1	This bit is used for AMD SVID only. 0: force PSI of VDD1 "0". 1: PSI of VDD1 is determined by the reading from CPU.
2	PSI_VDD0	R/W	1	This bit is used for AMD SVID only. 0: force PSI of VDD0 "0". 1: PSI of VDD0 is determined by the reading from CPU.
1	PSI_NB	R/W	1	This bit is used for AMD SVID only. 0: force PSI of VDDNB "0". 1: PSI of VDDNB is determined by the reading from CPU.
0	*VID_MANUAL_MODE	R/W	0	0: VID is in bypass mode or on-the-fly mode determined by the offset value. 1: VID is in manual mode. This bit will be "0" before PWROK.

*Those register is reset by SLOTOCC# falling edge (CPU change) or Watchdog timer timeout (if enabled).

8.10 SPI Registers (CR08)

SPI Control Register — Index F0h (powered by VAT)

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	SPTIE	R/W	0	SPI interrupt enable. Set to 1, SPIE interrupt enabled, set to 0 spie interrupt disabled.
4	Reserved	-	-	Reserved.
3	CPOL	R/W	0	Clock polarity this bit selects inverted or non-inverted SPI clock. Set to 1, active low clock selected; SCK idles high. Set to 0, active high clock selected; SCK idles low.
2	CPHA	R/W	0	Clock phase. This bit is used to shift the SCK serial clock. Set to 1, the first SCK edge is issued at the beginning of the transfer operation. Set to 0, the first SCK edge is issued one-half cycle into the transfer operation.
1	Reserved	-	0	Reserved
0	LSBFE	R/W	0	This bit control data shift from lsb or msb. Set to 1, data is transferred from lsb to msb. Set to 0, data is transferred from msb to lsb.

Reserved — Index F1h

Bit	Name	R/W	Default	Description
7-0	Reserved	-	-	Reserved

SPI Baud Rate Divisor Register — Index F2h

Bit	Name	R/W	Default	Description
7-3	Reserved	-	0	Reserved
2-0	BAUD_VAL	R/W	1	This register decides to SCK frequency. Baud rate divisor equation is 33MHz/2*(BAUD_VAL). 00: 33MHz. 01: 16.7MHz.

SPI Status Register — Index F3h

Bit	Name	R/W	Default	Description
7	SPIE	R/W	0	SPI interrupt status. When SPI is transferred or received data from device finish, this bit will be set. Write 1 to clear this bit.
6	Reserved	-	-	Reserved
5	SPE	R	-	This bit reflects the SPI_EN register (which will be 1 when SPI is enabled.)
4	Reserved	-	-	Reserved
3	SPTEF	R	0	SPI operation status. When SPI is transferred or received data from device, this bit will be set 1, Clear by SPI operation finish.
2-0	Reserved	-	-	Reserved

SPI High Byte Data Register — Index F4h

Bit	Name	R/W	Default	Description
7-0	H_DATA	R	0	When SPI is received 16 bits data from device. This register saves high byte data.

SPI command data Register — Index F5h

Bit	Name	R/W	Default	Description
7-0	CMD_DATA	R/W	0	This register provides command value for flash command.

SPI chip select Register — Index F6h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved
3	CS3	R/W	0	Chip select 3. To select device 3
2	CS2	R/W	0	Chip select 2. To select device 2
1	CS1	R/W	0	Chip select 1. To select device 1
0	CS0	R/W	0	Chip select 0. To select device 0

SPI memory mapping Register — Index F7h (powered by VBAT)

Bit	Name	R/W	Default	Description
7-5	Reserved	-	0	Reserved
4-0	Reserved	-	-	Reserved

SPI operate Register — Index F8h

Bit	Name	R/W	Default	Description
7	TYPE	R/W	0	This bit decide flash continuous programming mode. Set to 1, if programming continuous mode is same as the SST flash. Set to 0 if programming continuous mode is same as the ATMEL flash
6	IO_SPI	R/W	0	This bit control SPI function transfer 8 bit command to device. Clear 0 by operation finish.
5	RDSR	R/W	0	This bit control SPI function read status from to device. Clear 0 by operation finish.
4	WRSR	R/W	0	This bit control SPI function write status to device. Clear 0 by operation finish.
3	SECTOR_ERASE	R/W	0	This bit control SPI function sector erase device. Clear 0 by operation finish.
2	READ_ID	R/W	0	This bit control SPI function read id from device. Clear 0 by operation finish.
1	PROG	R/W	0	This bit control SPI function program data to device or set to 1 when memory cycle for LPC interface program flash. Clear 0 by operation finish.
0	READ	R/W	0	This bit control SPI function read data from device or set to 1 when memory cycle for LPC interface read flash. Clear 0 by operation finish.

SPI Low Byte Data Register — Index FAh

Bit	Name	R/W	Default	Description
7-0	L_DATA	R	0	When SPI is received 16 bits or 8 bits data from device. This register saves low byte data.

SPI address high byte Register — Index FBh

Bit	Name	R/W	Default	Description
7-0	Addr_H_byte	R/W	0	This register provides high byte address for sector erase, program, read operation.

SPI address medium byte Register — Index FCh

Bit	Name	R/W	Default	Description
7-0	Addr_M_byte	R/W	0	This register provides medium byte address for sector erase, program, read operation.

SPI address low byte Register — Index FDh

Bit	Name	R/W	Default	Description
7-0	Addr_L_byte	R/W	0	This register provides low byte address for sector erase, program, read operation.

SPI program byte Register — Index FEh

Bit	Name	R/W	Default	Description
7-0	PORG_BYTE	R/W	0	This register provides number to program flash for continuous mode.

SPI write data Register — Index FFh

Bit	Name	R/W	Default	Description
7-0	WR_dat	R/W	0	This register provides data to write flash for program, write status function.

8.11 PME and ACPI Registers (CR0A)

Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	PME_EN	R/W	0	0: disable PME. 1: enable PME.

PME Event Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	MO_PME_EN	R/W	0	Mouse PME event enable. 0: disable mouse PME event. 1: enable mouse PME event.
5	KB_PME_EN	R/W	0	Keyboard PME event enable. 0: disable keyboard PME event. 1: enable keyboard PME event.
4	HM_PME_EN	R/W	0	Hardware monitor PME event enable. 0: disable hardware monitor PME event. 1: enable hardware monitor PME event.
3	PRT_PME_EN	R/W	0	Parallel port PME event enable. 0: disable parallel port PME event. 1: enable parallel port PME event.
2	UR2_PME_EN	R/W	0	UART 2 PME event enable. 0: disable UART 2 PME event. 1: enable UART 2 PME event.
1	UR1_PME_EN	R/W	0	UART 1 PME event enable. 0: disable UART 1 PME event. 1: enable UART 1 PME event.
0	FDC_PME_EN	R/W	0	FDC PME event enable. 0: disable FDC PME event. 1: enable FDC PME event.

PME Event Status Register — Index F1h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	MO_PME_ST	R/W	-	Mouse PME event status. 0: Mouse has no PME event. 1: Mouse has a PME event to assert. Write 1 to clear to be ready for next PME event.
5	KB_PME_ST	R/W	-	Keyboard PME event status. 0: Keyboard has no PME event. 1: Keyboard has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	HM_PME_ST	R/W	-	Hardware monitor PME event status. 0: Hardware monitor has no PME event. 1: Hardware monitor has a PME event to assert. Write 1 to clear to be ready for next PME event.

3	PRT_PME_ST	R/W	-	Parallel port PME event status. 0: Parallel port has no PME event. 1: Parallel port has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	UR2_PME_ST	R/W	-	UART 2 PME event status. 0: UART 2 has no PME event. 1: UART 2 has a PME event to assert. Write 1 to clear to be ready for next PME event.
1	UR1_PME_ST	R/W	-	UART 1 PME event status. 0: UART 1 has no PME event. 1: UART 1 has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	FDC_PME_ST	R/W	-	FDC PME event status. 0: FDC has no PME event. 1: FDC has a PME event to assert. Write 1 to clear to be ready for next PME event.

ACPI Control Register 1 — Index F4h

Bit	Name	R/W	Default	Description
7	Reserved	R/W	0	Reserved
6	Reserved	R/W	0	Dummy for future use.
5	DUAL_GATE_S5_ON	R/W	1	0: DUAL_GATE_N tri-state in S5 state. 1: DUAL_GATE_N output low in S5 state.
4	EN_KBWAKEUP	R/W	0	Set one to enable keyboard wakeup event asserted via PWSOUT#.
3	EN_MOWAKEUP	R/W	0	Set one to enable mouse wakeup event asserted via PWSOUT#.
2-1	PWRCTRL	R/W	11	The ACPI Control the PSON_N to always on or always off or keep last state 00 : keep last state 10 : Always on 01 : Always on without PSOUT# 11: Always off
0	VSB_PWR_LOSS	R/W	0	When VSB 3V comes, it will set to 1, and write 1 to clear it

ACPI Control Register 2 — Index F5h

Bit	Name	R/W	Default	Description
7	Reserved	R/W	0	Dummy for future use.
6-5	PWROK_DELAY	R/W	0	The additional PWROK delay. 00: no delay 01: 100ms. 10: 200ms 11: 400ms.
4-3	VDD_DELAY	R/W	11	The PWROK delay timing from VDD3VOK by followed setting 00 : 100ms 01 : 200ms 10 : 300ms 11 : 400ms
2	VINDB_EN	R/W	1	Enable the PCIRSTIN_N and ATXPWGD de-bounce.
1	PCIRST_DB_EN	R/W	0	Enable the LRESET_N de-bounce.
0	Reserved	R/W	0	Dummy register.

ACPI Control Register — Index F6h

Bit	Name	R/W	Default	Description
7	S3_SEL	R/W	0	Select the KBC S3 state. 0: Enter S3 state when internal VDD3VOK signal de-asserted. 1: Enter S3 state when S3# is low or the TS3 register is set to 1.
6	SPI_RST_EN	R/W	0	0: Disable SPI time out reset signal 1: Enable SPI time out reset signal output form PWROK and PCIRST#.
5	WDT_RST_EN	R/W	0	0: Disable WDT time out reset signal 1: Enable WDT time out reset signal output form PWROK.
4	PSON_DEL_EN	R/W	0	0: PSON# is the inverted of S3# signal. 1: PSON# will sink low only if the time after the last turn-off elapse at least 4 seconds.
3	VREF_S3_RST_EN	R/W	0	0: The VREF output value programmed by user will keep in S3/S5 state. 1: The VREF output value will be reset to default (64h) when enter S3/S5 state.
2	PCIRST3_GATE	R/W	1	Write “0” to this bit will force PCIRST3# to sink low.
1	PCIRST2_GATE	R/W	1	Write “0” to this bit will force PCIRST2# to sink low.
0	PCIRST1_GATE	R/W	1	Write “0” to this bit will force PCIRST1# to sink low.

8.12 VREF Control Registers (CR0B)

VREF3 Output Value — Index F0h

Bit	Name	R/W	Default	Description
7-0	VREF3_H	R/W	8’h64	The bit8-1 of VREF3 output value.

VREF2 Output Value — Index F1h

Bit	Name	R/W	Default	Description
7-0	VREF2_H	R/W	8’h64	The bit8-1 of VREF2 output value.

VREF1 Output Value — Index F2h

Bit	Name	R/W	Default	Description
7-0	VREF1_H	R/W	8’h64	The bit8-1 of VREF1 output value.

Voltage LSB — Index F3h

Bit	Name	R/W	Default	Description
7-3	Reserved	R/W	-	Reserved.
2	VREF1_L	R/W	0	The bit0 of VREF1 output value.
1	VREF2_L	R/W	0	The bit0 of VREF2 output value.
0	VREF3_L	R/W	0	The bit0 of VREF3 output value.

WDT Reset Enable — Index FFh

Bit	Name	R/W	Default	Description
7-1	Reserved.	-	-	Reserved.
0	WD_RST_EN	R/W	0	0: disable the WDT reset function. 1: VREF1~3 will be reset to default if WDT timeout occurs.

9. Electrical Characteristics

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.5	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	0 to 70	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

DC Characteristics

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V) (Note)

Parameter	Conditions	MIN	TYP	MAX	Unit
Temperature Error, Remote Diode	60 °C < T_D < 100 °C, VCC = 3.0V to 3.6V -40 °C <T_D < 60°C 100 °C <T_D < 127°C		± 1 ± 1	± 3 ± 3	°C
Supply Voltage range		3.0	3.3	3.6	V
Average operating supply current			10		mA
Standby supply current			5		uA
VBAT Current			1		uA
Resolution			1		°C
Power on reset threshold			2.2	2.4	V
Diode source current	High Level		95		uA
	Low Level		10		uA

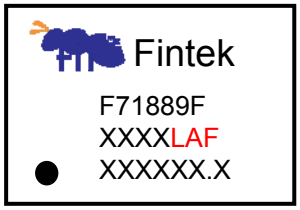
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/$OD_{12st,5v}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with12 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OD_{12t}-TTL level bi-directional pin, Open-drain output with12 mA sink capability.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		-12		mA	VOL = 0.4 V
I/OOD_{12t}-TTL level bi-directional pin, Output pin with 12mA source-sink capability, and can programming to open-drain function.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/O_{12t}- TTL level bi-directional pin, Output pin with 12mA source-sink capability.						
Input Low Threshold Voltage	Vt-			0.6	V	VDD = 3.3 V

Input High Threshold Voltage	Vt+	0.9			V	VDD = 3.3 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = 1.2V
Input Low Leakage	ILIL	-1			μA	VIN = 0V
IN_{st} - TTL level input pin with schmitt trigger						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{t,5v}$ - TTL level input pin with 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{st,5v}$ - TTL level input pin with schmitt trigger, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
OD_{12}-Open-drain output with12 mA sink capability.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
$OD_{12,5v}$-Open-drain output with12 mA sink capability, 5V tolerance.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
OD_{24}-Open-drain output with 24 mA sink capability.						
Output Low Current	IOL		-24		mA	VOL = 0.4V
$OD_{16,u10,5v}$-Open-drain output with 16 mA sink capability, pull-up 10k ohms, 5V tolerance.						
Output Low Current	IOL		-16		mA	VOL = 0.4V
$O_{8,u47,5v}$- Output pin with 8 mA source-sink capability, pull-up 47k ohms, 5V tolerance.						
Output High Current	IOH	+6	+8		mA	VOH = 2.4V
O_{12}- Output pin with 12 mA source-sink capability.						
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
O_{30}- Output pin with 30 mA source-sink capability.						
Output High Current	IOH	+26	+30		mA	VOH = 2.4V
I/OD_{14t}-TTL level bi-directional pin, Open-drain output with14 mA sink capability.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		-14		mA	VOL = 0.4 V
$I/O_{s1, D8,st, lv}$ - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.) with schmitt trigger. Output with 8mA drive and 1mA sink capability.						
Input Low Voltage	VIL			0.6	V	
Input High Voltage	VIH	0.9			V	
Output High Current	IOH		+8		mA	VOH = 1.0V
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$I/O_{D8,st, lv}$ - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.) with schmitt trigger. Output with 8mA drive						
Input Low Voltage	VIL			0.6	V	
Input High Voltage	VIH	0.9			V	
Output High Current	IOH		+8		mA	VOH = 1.0V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$I/OD_{12,st,lv}$ - Low level bi-directional pin with schmitt trigger. Open-drain output with 12mA sink capability.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	

Output Low Current	IOL		-12		mA	VOH = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$I/OOD_{12,st,lv}$ - Low level bi-directional pin with schmitt trigger, can select to OD or OUT by register, with 12 mA source-sink capability.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		-12		mA	VOH = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$I/OD_{12st,lv}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with12 mA sink capability, low voltage.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V

10.Ordering Information

Part Number	Package Type	Production Flow
F71889F	128-PQFP Green Package	Commercial, 0°C to +70°C



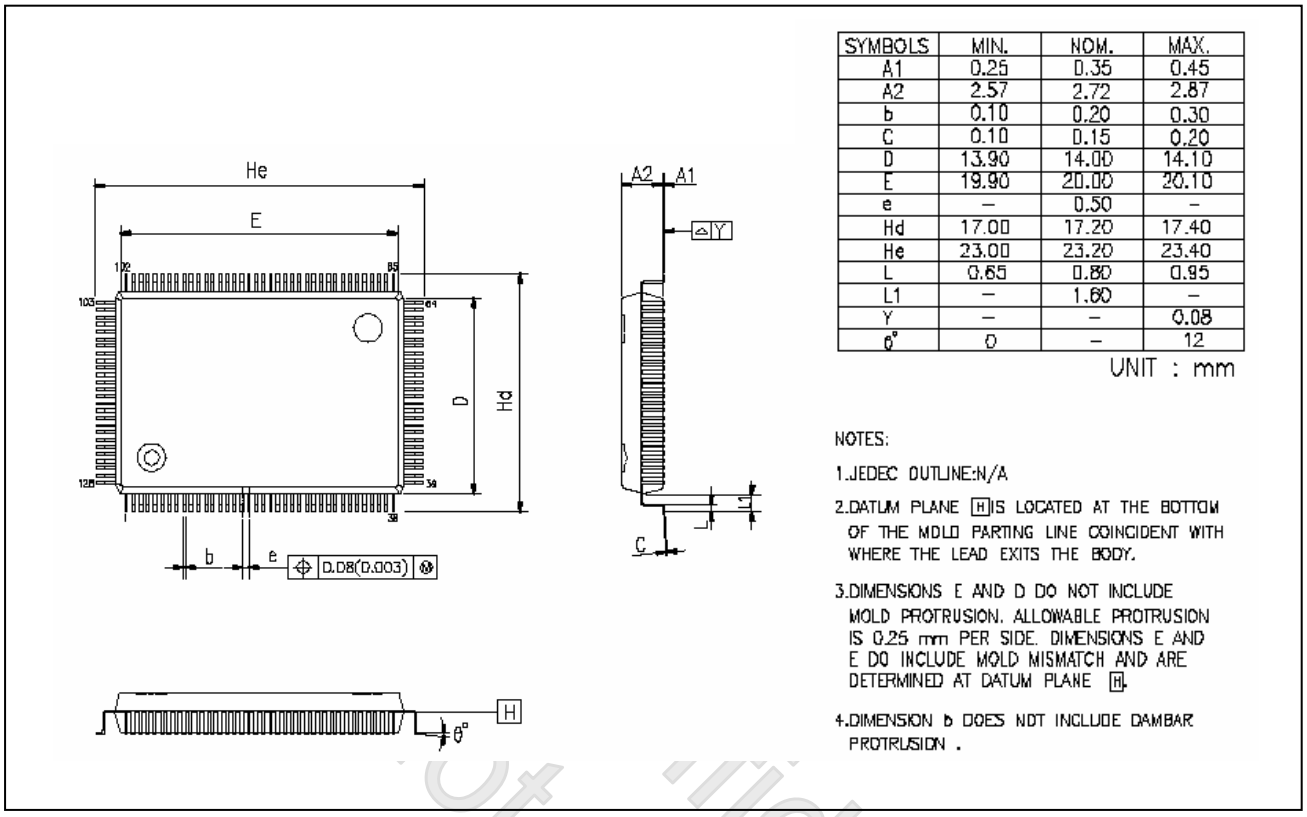
Version Identification:

An example for LAF version:

The version shows on RED area. Ex: LAF

11.Package Dimensions

128 PQFP (14*20)



SYMBOLS	MIN.	NOM.	MAX.
A1	0.25	0.35	0.45
A2	2.57	2.72	2.87
b	0.10	0.20	0.30
C	0.10	0.15	0.20
D	13.90	14.00	14.10
E	19.90	20.00	20.10
e	–	0.50	–
Hd	17.00	17.20	17.40
He	23.00	23.20	23.40
L	0.65	0.80	0.95
L1	–	1.60	–
Y	–	–	0.08
θ°	0	–	12

UNIT : mm

NOTES:

1.JEDEC OUTLINE:N/A

2.DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3.DIMENSIONS E AND D DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS E AND E DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].

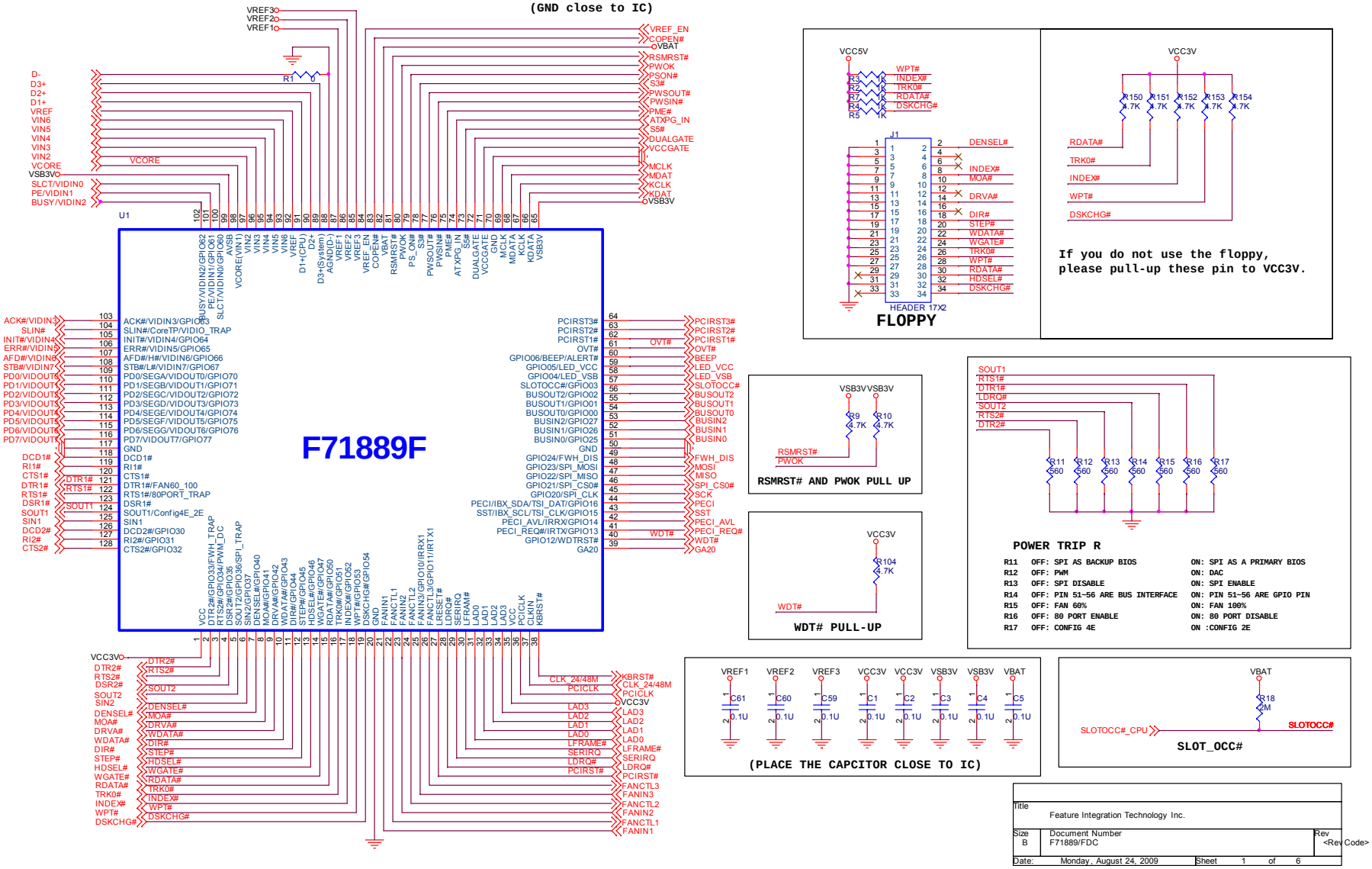
4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .

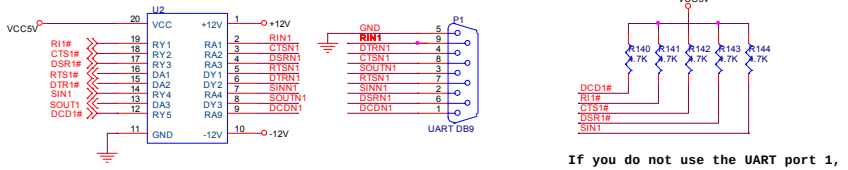
Feature Integration Technology Inc.

Headquarters
3F-7, No 36, Tai Yuan St.,
Chupei City, Hsinchu, Taiwan 302, R.O.C.
TEL : 886-3-5600168
FAX : 886-3-5600166
www: http://www.fintek.com.tw

Taipei Office
Bldg. K4, 7F, No.700, Chung Cheng Rd.,
Chungho City, Taipei, Taiwan 235, R.O.C.
TEL : 866-2-8227-8027
FAX : 866-2-8227-8037

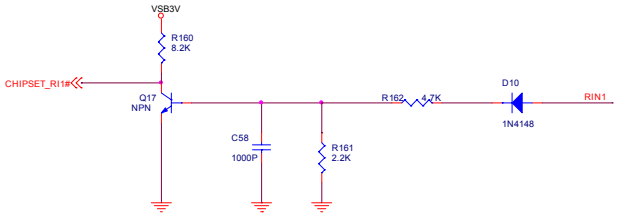
12.Application Circuit



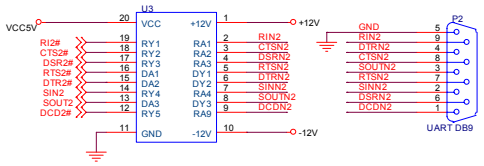


UART 1 PORT INTERFACE

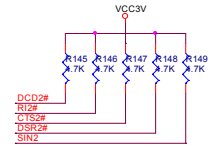
If you do not use the UART port 1, please pull-up these pin to VCC3V.



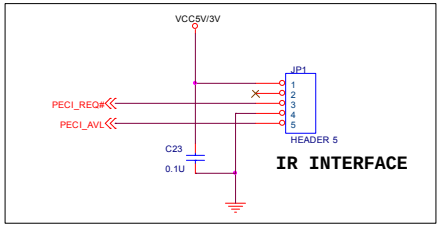
Wake up on ring for serial port circuit.



UART 2 PORT INTERFACE

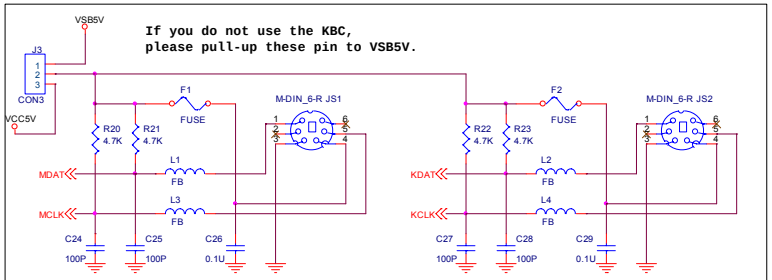


If you do not use the UART port 2, please pull-up these pin to VCC3V.



IR INTERFACE

If you do not use the KBC, please pull-up these pin to VSB5V.

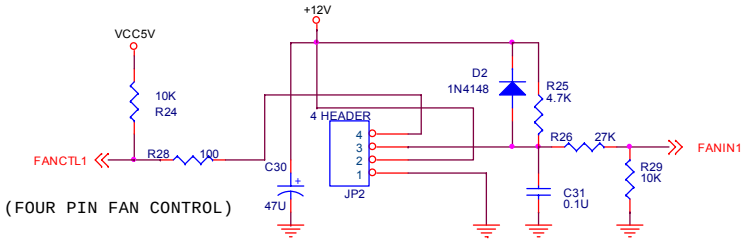


PS2 MOUSE INTERFACE

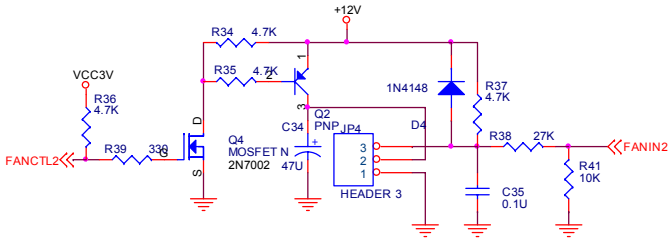
PS2 KEYBOARD INTERFACE

Title	Feature Intergration Technology Inc	
Size: Custom	Document Number: UART_PS2_IR	Rev: 0.1
Date: Wednesday, August 13, 2008	Sheet 2 of 6	

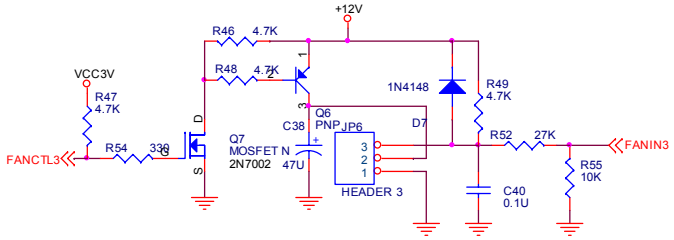
F71889



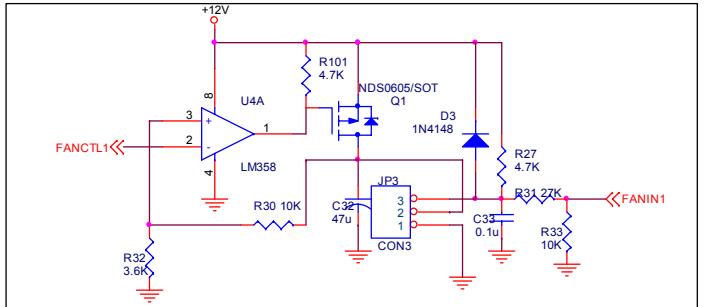
PWM FAN1 SPEED CONTROL



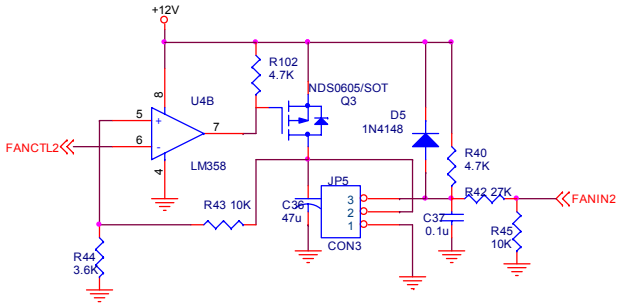
PWM FAN2 SPEED CONTROL



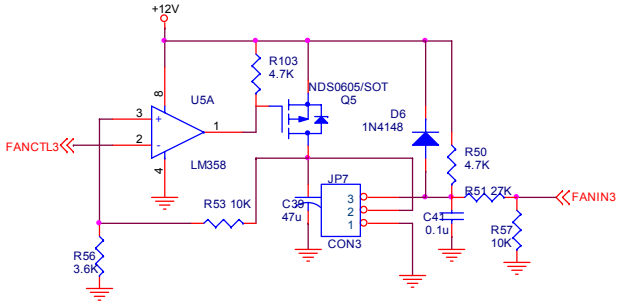
PWM FAN3 SPEED CONTROL



DC FAN CONTROL WITH OP 1



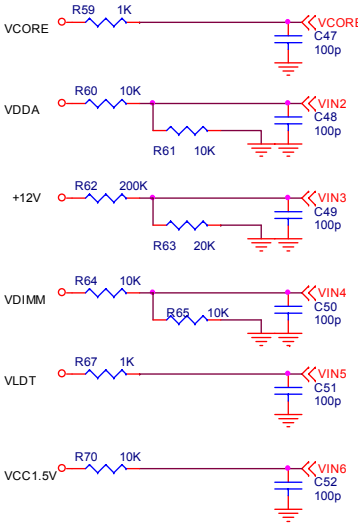
DC FAN CONTROL WITH OP 2



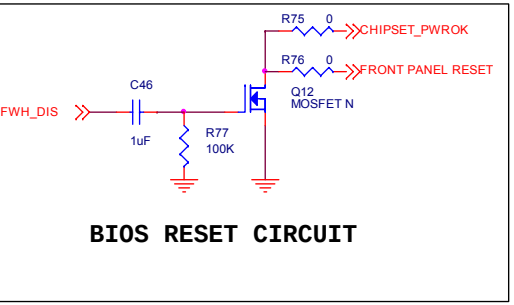
DC FAN CONTROL WITH OP 3

FAN CONTROL FOR PWM OR DC

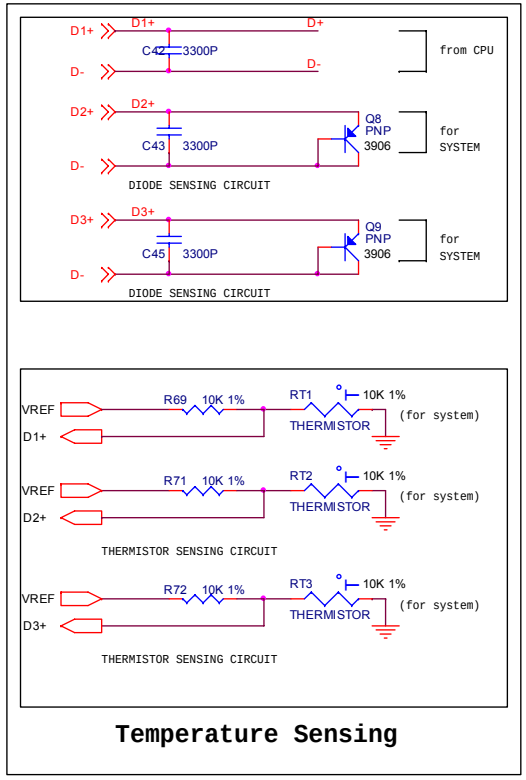
Title: Feature Integration Technology Inc.			
Size: B	Document Number: FAN Control		Rev: 0.1
Date: Wednesday, August 13, 2008	Sheet 3 of 6		



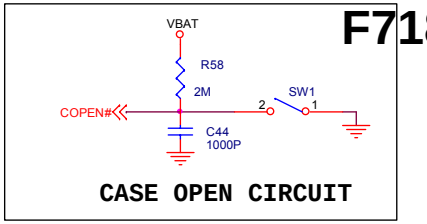
VOLTAGE SENSING.
The best voltage input level is about 1V.



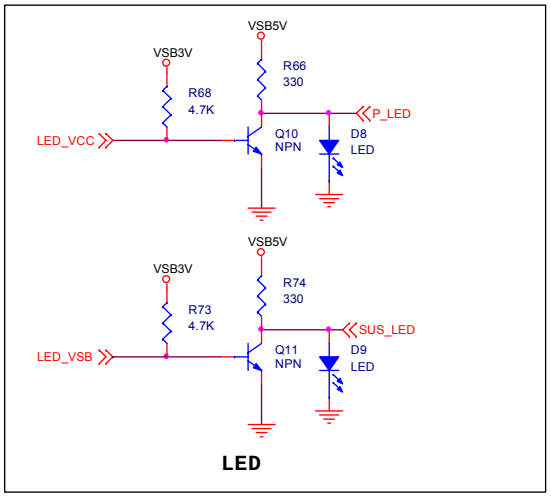
BIOS RESET CIRCUIT



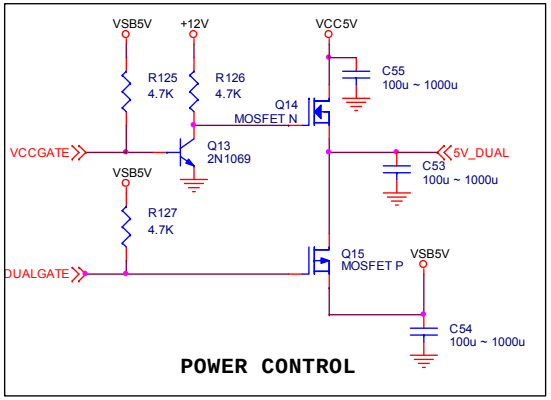
Temperature Sensing



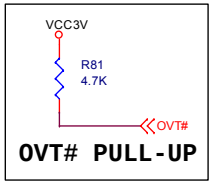
CASE OPEN CIRCUIT



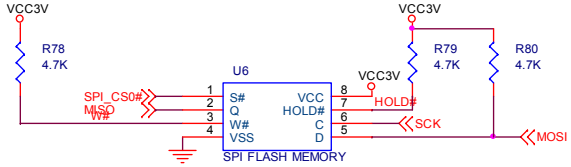
LED



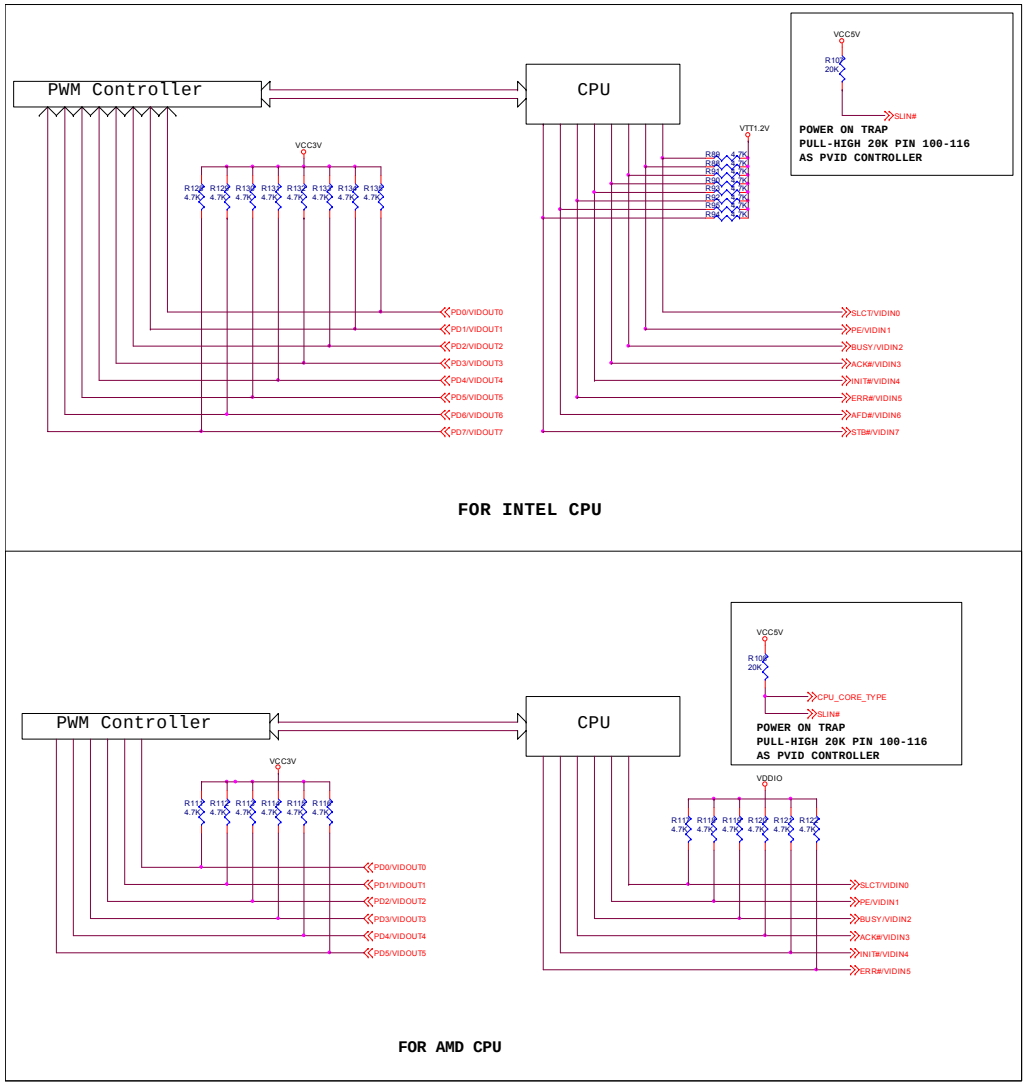
POWER CONTROL

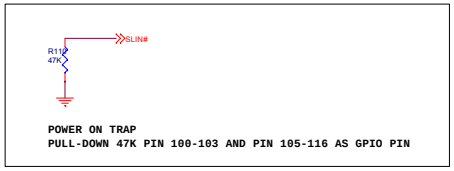


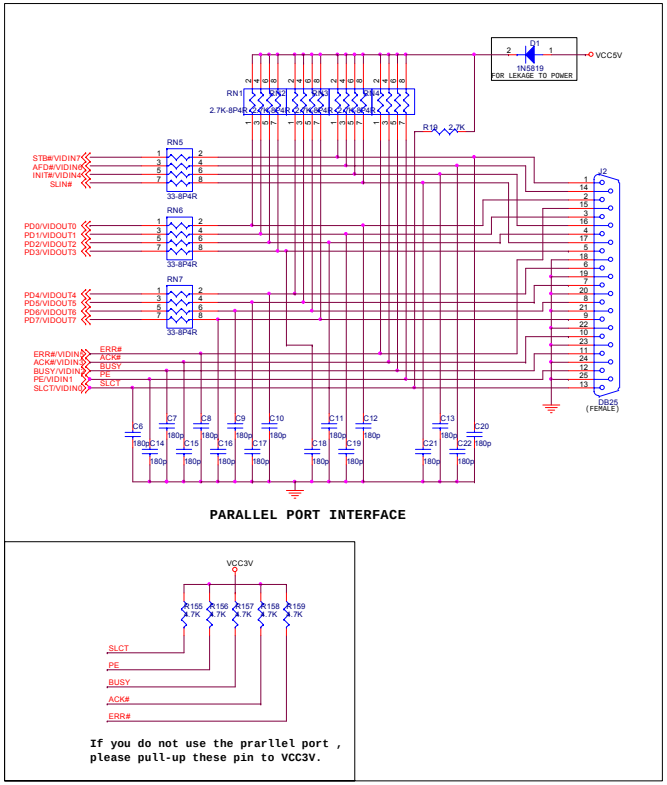
OVT# PULL-UP



Title	Feature Integration Technology Inc.	
Size B	Document Number Hardware Monitor	Rev <Rev Code>
Date: Wednesday, August 05, 2009	Sheet 4 of 6	

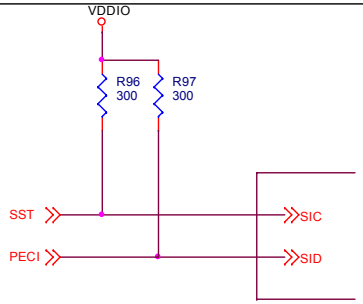




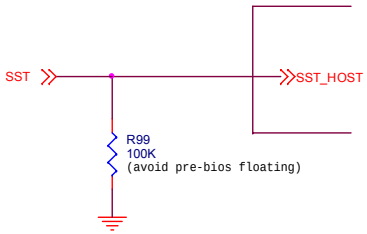


Title	Feature Integration Technology Inc.		
Size C	Document Number VID/PRINTER PORT		Rev <Rev Code>
Date: Wednesday, August 13, 2008	Sheet 5 of 6		

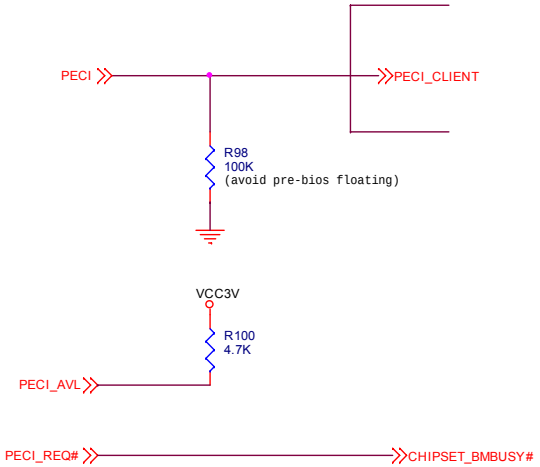
F71889



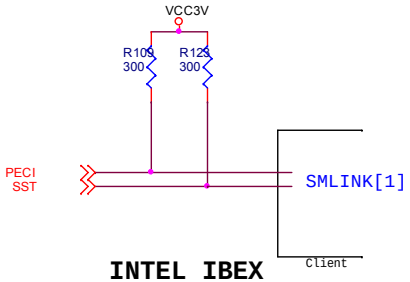
AMDSI



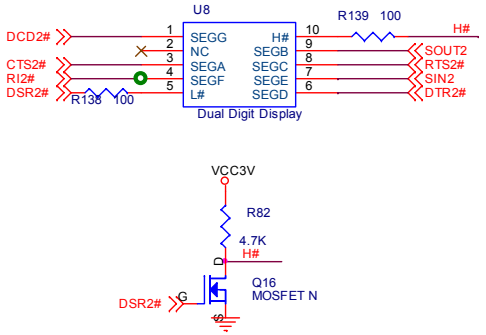
SST



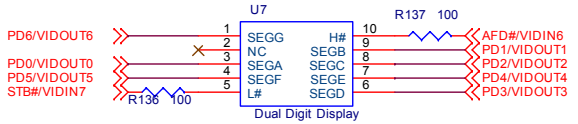
PECI



INTEL IBEX

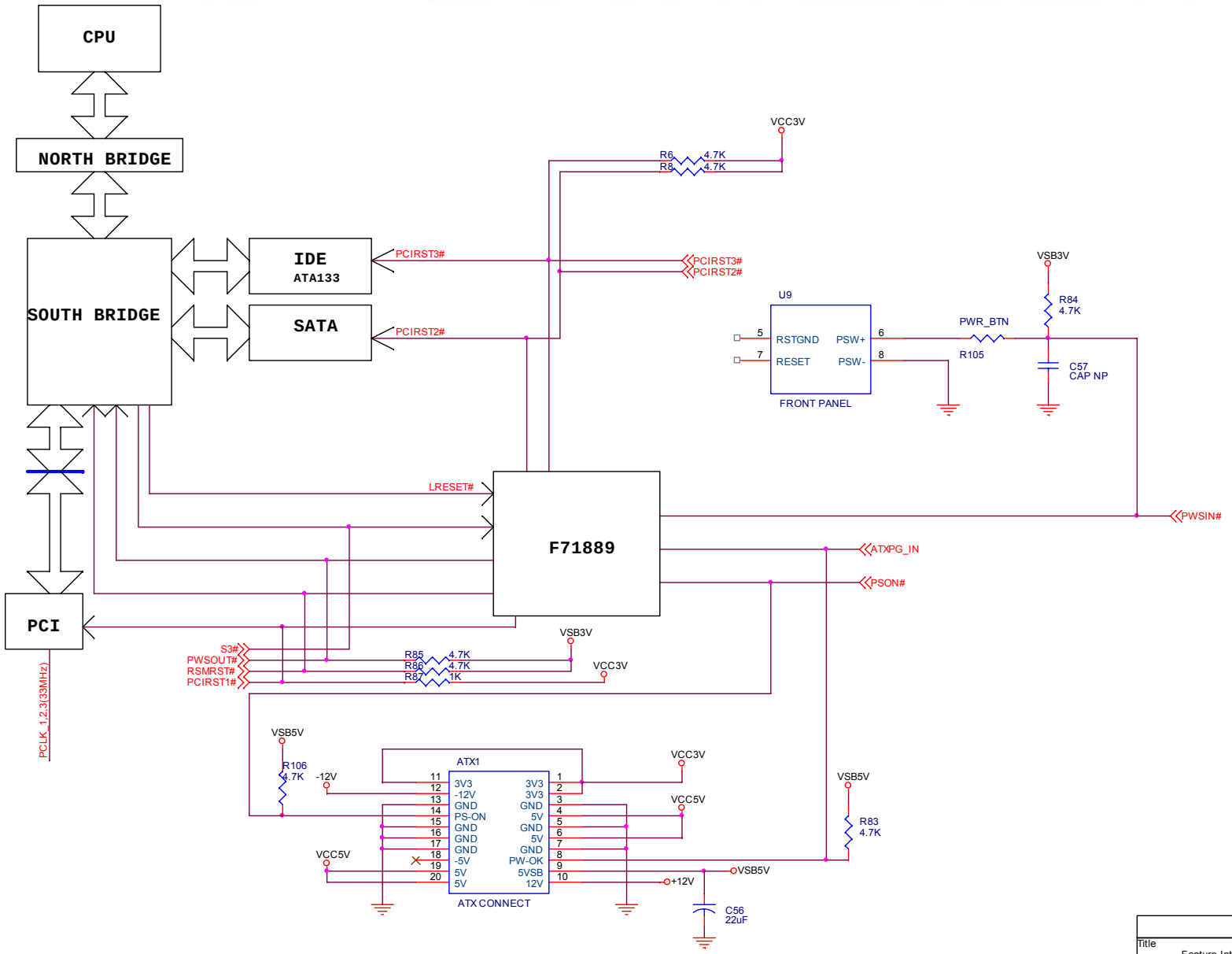


80 PORT 1 (output by COM2 interface)



80 PORT 2 (output by parallel port interface)

Title: Feature Integration Technology Inc.		
Size: B	Document Number: AMDSI/SST/PECI/80PORT	Rev: <Rev Code>
Date: Monday, August 24, 2009	Sheet 6 of 6	



Title	Feature Integration Technology Inc.	
Size B	Document Number ACPI SAMPLE	Rev <Rev Code>
Date: Wednesday, August 13, 2008	Sheet 1 of 7	