TDA18211HD

DVB-T Silicon Tuner IC

Rev. 05 — 2 June 2009 Product data sheet

1. General description

The TDA18211HD is a Silicon Tuner IC designed for digital terrestrial (DVB-T) TV reception. The TDA18211HD integrates the overall tuning function, including selectivity, and provides a low-IF output signal.

The TDA18211HD uses integrated IF filters to support 6/7/8 MHz channel bandwidths. The TDA18211HD requires only one single 16 MHz crystal for clock generation. A clock signal is available on crystal oscillator output pins (XTOUTP/XTOUTN) to synchronize the channel decoder and slave front end in case of DVR configuration.

This specification is based on software version 3.4

2. Features

- Fully integrated RF tracking filters for unwanted signal suppression
- Fully integrated IF selectivity (no need for external SAW filters)
- Fully integrated oscillators with no external components
- Integrated wideband gain control
- Alignment free
- RF loop-through for easy implementation in the STB
- Input power level indicator
- Integrated die thermal sensor
- Single 3.3 V power supply
- Low power consumption (780 mW)
- Crystal oscillator output buffer (16 MHz) to allow single crystal applications
- I^2C-bus interface compatible with 3.3 V and 5 V microcontrollers
- Three Standby modes
- RoHS packaging

3. Applications

3.1 Target applications

- DVB-T Set-Top-Box (STB) and TV receiver
- Application optimization is described in the application notes

3.2 Key benefits

- The TDA18211HD is a low cost Silicon Tuner targeting digital terrestrial applications. The TDA18211HD matches the performance of the conventional can tuners while reducing the size of the tuner function drastically. Additionally, the following benefits can be stated:
  - Allows easy on-board integration
  - Allows easy dual-tuner configuration
  - Drastically reducing the size of the tuner function and power consumption

4. Quick reference data

Table 1. Quick reference data

T_{amb} = 25 °C; V_{CC} = 3.3 V; IF output level option = 2 V (p-p); IF output load = 1 kΩ on each terminal.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{RF}	RF frequency	center of channel		174	-	864	MHz
NF_{tun}	tuner noise figure	maximum gain		-	5.5	6	dB
φ_n	phase noise			-	–89	-	dBc/Hz
P	power dissipation			-	780	-	mW
$V_{i(max)}$	maximum input voltage	1 dB gain compression, one analog TV signal at RF input (–5 dBm)		-	103	-	dBμV
α_{image}	image rejection			53	65	-	dB
S_{dig}	digital sensitivity	DVB-T (64 QAM 2/3); BER = 2.10^{-4}	[1]	-	–82	-	dBm

[1] Measured with TDA10048HN channel decoder.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA18211HD/C2	HLQFN64R	plastic thermal enhanced low profile quad flat package; no leads; 64 terminals; resin based; body 9 × 9 × 1.6 mm	SOT903-1

6. Block diagram

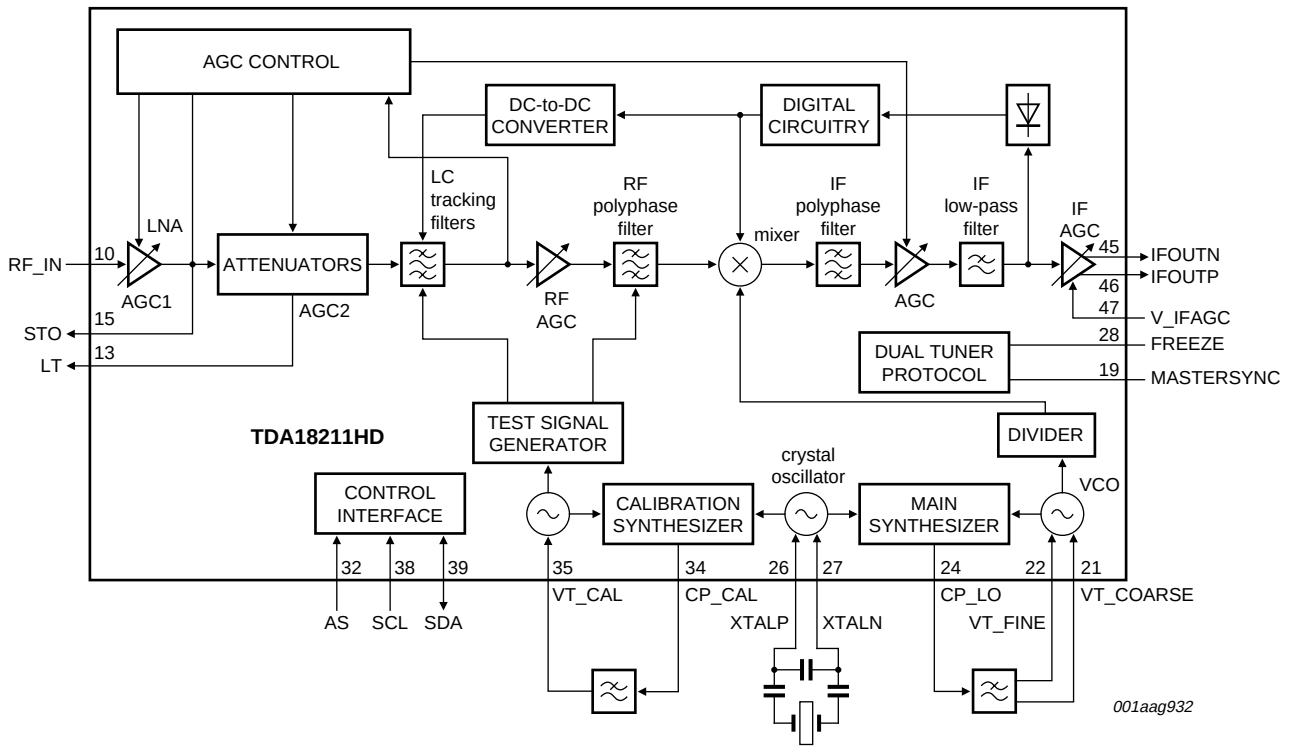


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

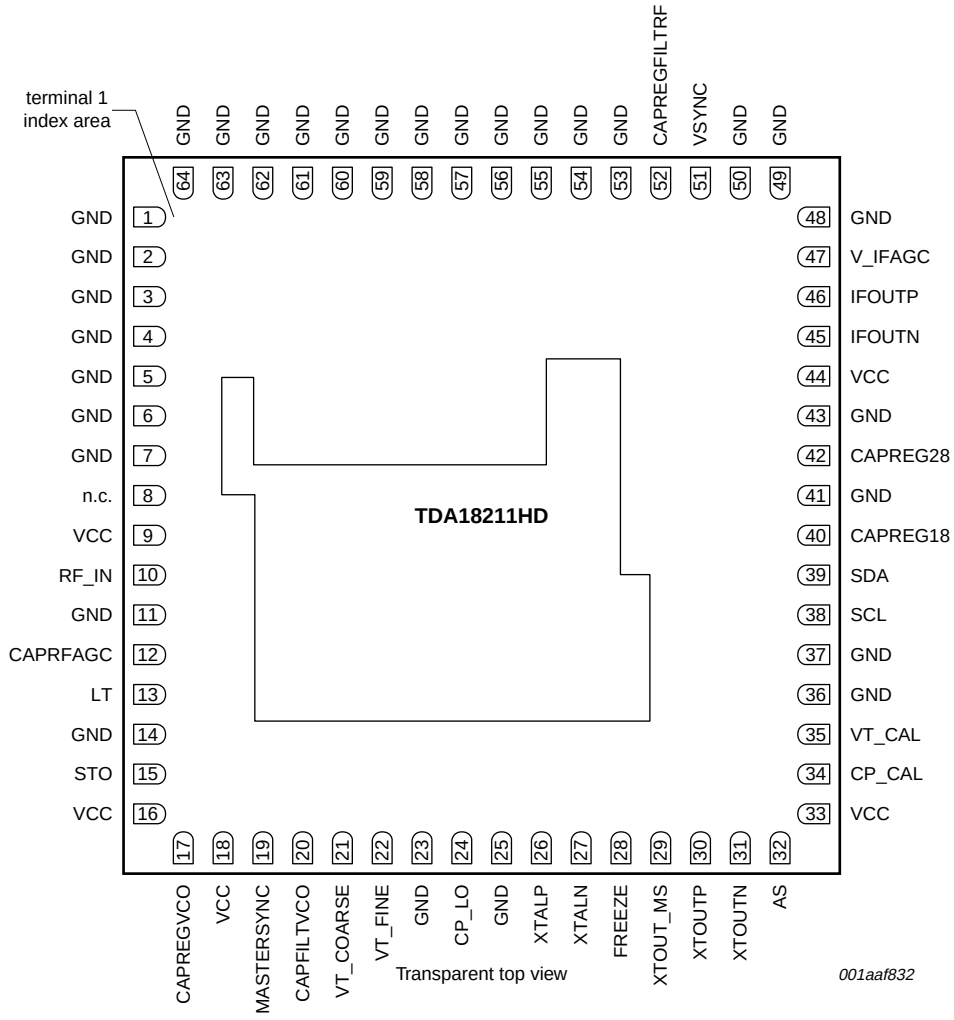


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GND	1 to 7	ground
n.c.	8	not connected
VCC	9	3.3 V supply voltage
RF_IN	10	unbalanced RF (TV) input
GND	11	ground
CAPRFAGC	12	RF AGC filtering
LT	13	loop-through output

Table 3. Pin description *…continued*

Symbol	Pin	Description
GND	14	ground
STO	15	slave tuner output
VCC	16	3.3 V supply voltage
CAPREGVCO	17	VCO supply decoupling
VCC	18	3.3 V supply voltage
MASTERSYNC	19	synchronization signal for dual-tuner applications; leave open for single-tuner applications
CAPFILTVCO	20	VCO reference decoupling
VT_COARSE	21	LO oscillator tuning voltage input
VT_FINE	22	LO oscillator tuning voltage input
GND	23	ground
CP_LO	24	charge pump of the local synthesizer
GND	25	ground
XTALP	26	crystal oscillator input
XTALN	27	crystal oscillator input
FREEZE	28	synchronization signal for multi-tuner applications; leave open for single-tuner applications
XTOUT_MS	29	XTOUT mode and master/slave selection input
XTOUTP	30	crystal oscillator output buffer
XTOUTN	31	crystal oscillator output buffer
AS	32	I^2C-bus address selection input
VCC	33	3.3 V supply voltage
CP_CAL	34	charge pump of the calibration synthesizer
VT_CAL	35	tuning voltage of the calibration synthesizer
GND	36, 37	ground
SCL	38	I^2C-bus clock input
SDA	39	I^2C-bus data input/output
CAPREG18	40	internal regulator decoupling
GND	41	ground
CAPREG28	42	internal regulator decoupling
GND	43	ground
VCC	44	3.3 V supply voltage
IFOUTN	45	IF output
IFOUTP	46	IF output
V_IFAGC	47	IF gain control input
GND	48 to 50	ground
VSYNC	51	vertical synchronization input for analog applications; connect to ground for digital applications
CAPREGFILTRF	52	internal regulator decoupling
GND	53 to 64	ground
-	exposed die	ground

8. Functional description

The RF input signal is driven to a low-noise amplifier. It is then band-pass filtered, amplified and fed to the image rejection mixer. The mixer downconverts the RF signal to a low IF, which depends on channel bandwidth (standard IF filters are implemented for 6/7/8 MHz channel bandwidths; see Table 41).

The gain between the antenna pin (pin RF_IN) and the loop-through pin (pin LT) is 0 dB.

The TDA18211HD requires a single 16 MHz crystal for clock generation.

When bit XTOUT_ON = 1, a differential sine wave clock reference is available on pins XTOUTP and XTOUTN to drive a channel decoder.

8.1 Master and slave operation

The TDA18211HD allows easy dual-tuner configuration.

Each individual tuner has to be set either in Master mode or Slave mode by applying a DC voltage on the XTOUT_MS pin; see Table 4. This will decide whether the crystal oscillator part is used as negative impedance connected to the crystal part or as a current buffer.

Table 4. Master and slave selection

Voltage on pin XTOUT_MS	Tuner type	Crystal oscillator
0 V to $0.1V_{CC}$	master	negative impedance presented to the crystal
$0.4V_{CC}$ to $0.6V_{CC}$	slave	current input buffer

In dual-tuner application:

- The first tuner is set in Master mode
- The second tuner has to be set in Slave mode

In single-tuner application:

- The tuner must be set in Master mode.

8.2 Tuner outputs

The tuner provides a slave tuner output (pin STO) and a loop-through output (pin LT). Those outputs are used to transmit the antenna signal to other tuners. Each output has its own characteristics (see Table 56 and Table 57)

8.2.1 Loop-through output

The gain between the antenna connector and the loop-through pin (pin LT) equals 0 dB. This pin can be connected to any consumer electronic equipment.

8.2.2 Slave tuner output

The slave tuner output (pin STO) must be connected to the RF input of the slave tuner TDA18211HD in case of dual-tuner applications.

The gain between the antenna connector and the slave tuner output can change according to the input level. The slave tuner will automatically compensate the gain change, using the MASTERSYNC and FREEZE signals.

8.3 Crystal input mode

The TDA18211HD requires a 16 MHz crystal reference. The chosen crystal must withstand at least 100 µW drive level. An additional shunt capacitor as shown in Figure 1 is also needed. Its typical value is 5.6 pF. The quartz references for which performance is guaranteed are:

- NDK NX5032
- Siward SX-5032
- TXC 9C series
- Chungho Elcom HC49/S profile

Clock reference:

- In Master mode, the clock reference must be provided by a 16 MHz crystal connected between pins XTALP and XTALN of the master tuner
- In Slave mode, the clock reference must be provided by pins XTOUTP and XTOUTN of the tuner in Master mode to pins XTALP and XTALN of the tuner in Slave mode

8.4 Crystal output mode

Pins XTOUTP and XTOUTN deliver a symmetrical sine waveform to drive the channel decoder and/or IF demodulator. The load on both outputs should be made similar to ensure optimum performances. Hence, if only one crystal output is used, the unused output should be loaded by an equivalent capacitance.

9. Control interface

9.1 I^2C-bus format, write/read mode

Remark: In I^2C-bus read mode, the TDA18211HD must read the entire I^2C map with the required subaddress 00h. The number of bytes to be read is 16, or 39 in extended register mode; see Table 7. Reading write-only bits can return values that are different from the programmed values.

Table 5. I²C-bus format

Name	Byte name	Sub address	Bit							
			7	6	5	4	3	2	1	0
Address byte 1	-	-	1	1	0	0	0	MA[1]	MA[0]	R/W
Address byte 2	-	-	0	0	AD[5:0]					
ID byte	ID	00h	1	ID[6:0]						
Thermo byte	TM	01h	POR	LOCK	TM_RANGE	TM_ON	TM_D[3:0]			
Power level byte	PL	02h	POWER_LEVEL[7:0]							
Easy Prog byte 1	EP1	03h	POWER_LEVEL[8]	DIS_POWER_LEVEL	0	RF_CAL_OK	IR_CAL_OK	BP_FILTER[2:0]		
Easy Prog byte 2	EP2	04h	RF_BAND[2:0]			GAIN_TAPER[4:0]				
Easy Prog byte 3	EP3	05h	SM	SM_LT	SM_XT	STD[4:0]				
Easy Prog byte 4	EP4	06h	FM_RFN	XTOUT_ON	1	IF_LEVEL[2:0]			CAL_MODE[1:0]	
Easy Prog byte 5	EP5	07h	EXTENDED_REG	IR_GSTEP[2:0]			0	IR_MEAS[2:0]		
Cal Post-Divider byte	CPD	08h	CAL_POST_DIV[7:0]							
Cal Divider byte 1	CD1	09h	0	CAL_DIV[22:16]						
Cal Divider byte 2	CD2	0Ah	CAL_DIV[15:8]							
Cal Divider byte 3	CD3	0Bh	CAL_DIV[7:0]							
Main Post-Divider byte	MPD	0Ch	IF_NOTCH	MAIN_POST_DIV[6:0]						
Main Divider byte 1	MD1	0Dh	0	MAIN_DIV[22:16]						
Main Divider byte 2	MD2	0Eh	MAIN_DIV[15:8]							
Main Divider byte 3	MD3	0Fh	MAIN_DIV[7:0]							
Extended byte 1	EB1	10h	EB1[7:3]					CALVCO_FORLON	AGC1_ALWAYS_MASTERN	AGC1_FIRSTN
Extended byte 2	EB2	11h	EB2[7:0]							
Extended byte 3	EB3	12h	EB3[7:0]							
Extended byte 4	EB4	13h	EB4[7:6]		LO_FORCESRCE	EB4[4:0]				
Extended byte 5	EB5	14h	EB5[7:0]							
Extended byte 6	EB6	15h	EB6[7:0]							

Table 5. I²C-bus format *…continued*

Name	Byte name	Sub address	Bit							
			7	6	5	4	3	2	1	0
Extended byte 7	EB7	16h	EB7[7:6]		CAL_ FORCE_ SRCE	EB7[4:0]				
Extended byte 8	EB8	17h	CID_ALARM	EB8[6:4]			EB8[3]	EB8[2:0]		
Extended byte 9	EB9	18h	EB9[7:0]							
Extended byte 10	EB10	19h	EB10[7:6]		CID_GAIN[5:0]					
Extended byte 11	EB11	1Ah	EB11[7:0]							
Extended byte 12	EB12	1Bh	EB12[7:6]		PD_AGC1_ DET	PD_AGC2_ DET	EB12[3:0]			
Extended byte 13	EB13	1Ch	EB13[7]	RFC_K[2:0]			RFC_M[1:0]		EB13[1:0]	
Extended byte 14	EB14	1Dh	RFC_CPROG[7:0]							
Extended byte 15	EB15	1Eh	EB15[7:4]				EB15[3:0]			
Extended byte 16	EB16	1Fh	EB16[7:0]							
Extended byte 17	EB17	20h	EB17[7:0]							
Extended byte 18	EB18	21h	AGC1_ LOOP_OFF	EB18[6:2]					AGC1_GAIN[1:0]	
Extended byte 19	EB19	22h	EB19[7:0]							
Extended byte 20	EB20	23h	EB20[7:6]		FORCE_ LOCK	EB20[4:0]				
Extended byte 21	EB21	24h	AGC2_ LOOP_OFF	EB21[6:2]					AGC2_GAIN[1:0]	
Extended byte 22	EB22	25h	EB22[7]	RF_TOP[2:0]			IF_TOP[3:0]			
Extended byte 23	EB23	26h	EB23[7:3]					FORCELP_ FC2_EN	LP_FC[2]	EB23[0]

9.2 I²C-bus at power-on reset

Table 6. I²C-bus at power-on reset[1]

Name	Byte	Subaddress	Bit							
			7	6	5	4	3	2	1	0
Address byte 1	-	-	1	1	0	0	0	MA[1]	MA[0]	X
Address byte 2	-	-	X	X	AD[5]	AD[4]	AD[3]	AD[2]	AD[1]	AD[0]
ID byte	ID	00h	1	0	0	0	0	1	0	0
Thermo byte	TM	01h	1	0	0	0	X	X	X	X
Power Level byte	PL	02h	X	X	X	X	X	X	X	X
Easy Prog byte 1	EP1	03h	X	1	0	0	0	1	1	0
Easy Prog byte 2	EP2	04h	1	1	0	1	1	1	1	1
Easy Prog byte 3	EP3	05h	1	0	0	1	0	0	1	0
Easy Prog byte 4	EP4	06h	0	1	1	0	0	0	0	0
Easy Prog byte 5	EP5	07h	0	0	1	1	0	0	0	0
Cal Post-Divider byte	CPD	08h	0	0	0	0	0	0	0	0
Cal Divider byte 1	CD1	09h	0	0	0	0	0	0	0	0
Cal Divider byte 2	CD2	0Ah	0	0	0	0	0	0	0	0
Cal Divider byte 3	CD3	0Bh	0	0	0	0	0	0	0	0
Main Post-Divider byte	MPD	0Ch	0	0	0	0	0	0	0	0
Main Divider byte 1	MD1	0Dh	0	0	0	0	0	0	0	0
Main Divider byte 2	MD2	0Eh	0	0	0	0	0	0	0	0
Main Divider byte 3	MD3	0Fh	0	0	0	0	0	0	0	0
Extended byte 1	EB1	10h	1	1	1	1	1	1	1	1
Extended byte 2	EB2	11h	0	0	0	0	0	0	0	1
Extended byte 3	EB3	12h	1	0	0	0	0	1	0	0
Extended byte 4	EB4	13h	0	1	0	0	0	0	0	1
Extended byte 5	EB5	14h	0	0	0	0	0	0	0	1
Extended byte 6	EB6	15h	1	0	0	0	0	1	0	0
Extended byte 7	EB7	16h	0	1	0	0	1	0	0	0
Extended byte 8	EB8	17h	0	1	1	1	X	1	0	1
Extended byte 9	EB9	18h	0	0	0	0	0	0	0	0
Extended byte 10	EB10	19h	X	X	X	X	X	X	X	X
Extended byte 11	EB11	1Ah	1	0	0	0	0	1	1	0
Extended byte 12	EB12	1Bh	0	0	0	0	0	1	1	1
Extended byte 13	EB13	1Ch	1	1	0	0	0	0	1	0
Extended byte 14	EB14	1Dh	0	0	0	0	0	0	0	0
Extended byte 15	EB15	1Eh	1	0	0	0	X	X	X	X
Extended byte 16	EB16	1Fh	0	0	0	X	X	X	0	0
Extended byte 17	EB17	20h	0	0	0	X	X	X	X	X
Extended byte 18	EB18	21h	0	0	0	0	0	0	0	0
Extended byte 19	EB19	22h	0	0	0	X	X	X	0	0
Extended byte 20	EB20	23h	1	0	0	X	X	X	X	X

Table 6. I²C-bus at power-on reset[1] …continued

Name	Byte	Subaddress	Bit							
			7	6	5	4	3	2	1	0
Extended byte 21	EB21	24h	0	0	1	1	0	0	1	1
Extended byte 22	EB22	25h	0	1	0	0	1	0	0	0
Extended byte 23	EB23	26h	1	0	1	1	0	0	0	0

[1] X indicates a bit not changed on reset.

9.3 Description of symbols used in I²C-bus format table

Table 7. I²C-bus registers bits explanation

Address	Byte	Symbol	Description	Reference
		MA[1:0]	programmable address bits	Table 8
		AD[5:0]	programmable address bits of the first byte of the programming	Table 9
Data bytes				
00h	ID	ID[6:0]	chip identification number	Table 10
01h	TM	POR	Power-on reset bit	Table 11
		LOCK	indicates that the main synthesizer is locked to the programmed frequency	
		TM_RANGE	range selection bit for the internal die sensor	
		TM_ON	enables die temperature measurement	
		TM_D[3:0]	data from die temperature measurement (read only)	
02h	PL	POWER_LEVEL[7:0]	Power level indicator value (read only)	Table 12
03h	EP1	POWER_LEVEL[8]	Power level indicator value (read only	Table 12
		DIS_POWER_LEVEL	disables the power-on level function	Table 13
		RF_CAL_OK	indicates that the RF tracking filter calibration procedure has been successful	
		IR_CAL_OK	indicates that the complete image rejection calibration procedure has been successful	
		BP_FILTER[2:0]	RF band-pass filter selection	
04h	EP2	RF_BAND[2:0]	RF tracking filter band selection	Table 14
		GAIN_TAPER[4:0]	gain taper value	
05h	EP3	SM	Sleep mode, Standby modes	Table 15
		SM_LT		
		SM_XT		
		STD[4:0]	define the standard	
06h	EP4	FM_RFN	selection which input is fed to RF filter	Table 17
		XTOUT_ON	provides the 16 MHz on the XTOUTP and XTOUTN pins	
		IF_LEVEL[2:0]	IF output level selection	
		CAL_MODE[1:0]	calibration mode selection	
07h	EP5	EXTENDED_REG	enables the extended register addressing	Table 18
		IR_GSTEP[2:0]	gain step for image rejection calibration	
		IR_MEAS[2:0]	image rejection measurement frequency range	
08h	CPD	CAL_POST_DIV[7:0]	calibration synthesizer post-divider	Table 19

Table 7. I²C-bus registers bits explanation *…continued*

Address	Byte	Symbol	Description	Reference
09h	CD1	CAL_DIV[22:16]	calibration synthesizer main divider bits	Table 20
0Ah	CD2	CAL_DIV[15:8]	calibration synthesizer main divider bits	Table 20
0Bh	CD3	CAL_DIV[7:0]	calibration synthesizer main divider bits	Table 20
0Ch	MPD	IF_NOTCH	adds a DC notch in IF for a better adjacent channels rejection; depends on standards	Table 21
		MAIN_POST_DIV[6:0]	LO synthesizer post-divider bits	
0Dh	MD1	MAIN_DIV[22:16]	LO synthesizer main divider bits	Table 22
0Eh	MD2	MAIN_DIV[15:8]	LO synthesizer main divider bits	Table 22
0Fh	MD3	MAIN_DIV[7:0]	LO synthesizer main divider bits	Table 22
Extended bytes				
10h	EB1	CALVCO_FORLON	determines which VCO is used during Normal mode operations	Table 23
		AGC1_ALWAYS_MASTERN	enables AGC1 normal operation whatever the tuner type (master or slave)	
		AGC1_FIRSTN	determines which AGC (1 or 2) will be detected when detectors 1 and 2 are up	
13h	EB4	LO_FORCESRCE	forces the main PLL charge pump to source current to the main PLL loop filter	Table 23
15h	EB6	CAL_FORCESRCE	forces the calibration PLL charge pump to source current to the calibration PLL loop filter	Table 23
17h	EB8	CID_ALARM	indicates that signal sensed by the power detector used during calibrations is out of range	Table 23
19h	EB10	CID_GAIN[5:0]	calibration power detector output	Table 23
1Bh	EB12	PD_AGC1_DET	power-down of AGC1 detector	Table 23
		PD_AGC2_DET	power-down of AGC2 detector	
1Ch	EB13	RFC_K[2:0]	parameter used during the RF tracking filters calibration	Table 23
		RFC_M[1:0]	parameter used during the RF tracking filters calibration	
1Dh	EB14	RFC_CPROG[7:0]	tuning word of the RF tracking filters	Table 23
21h	EB18	AGC1_LOOP_OFF	turns off the AGC1 loop	Table 23
		AGC1_GAIN[1:0]	AGC1 gain	
23h	EB20	FORCE_LOCK	forces the internal lock indicator to logic 1	Table 23
24h	EB21	AGC2_LOOP_OFF	turns off the AGC2 loop	Table 23
		AGC2_GAIN[1:0]	AGC2 gain	
25h	EB22	RF_TOP[2:0]	Take Over Point (TOP) of the RF AGC, detection in RF	Table 23
		IF_TOP[3:0]	TOP of the RF AGC, detection in IF	
26h	EB23	FORCELP_FC2_EN	1.5 MHz bandwidth filter selection	Table 23
		LP_FC[2]		

9.3.1 I²C-bus address selection

The module address contains programmable address bits (MA[1:0]), which offer the possibility to have several synthesizers (up to 4) in one system by applying a specific voltage on the AS input (V_{AS}).

Table 8. Address byte 1 bit description

*Legend: * power-on reset value*

Bit	Symbol	Access	Value	Description
7 to 3	-	R/W	1 1000*	must be set to 1 1000
2 to 1	MA[1:0]	R/W		programmable address bits
			00	V_{AS} = 0 V to 0.1 × V_{CC}
			01	V_{AS} = 0.2 × V_{CC} to 0.3 × V_{CC}
			10	V_{AS} = 0.4 × V_{CC} to 0.6 × V_{CC}
			11	V_{AS} = 0.9 × V_{CC} to V_{CC}
0	R/W	R/W	0	write mode
			1	read mode

Table 9. Address byte 2 bit description

*Legend: * power-on reset value*

Bit	Symbol	Access	Value	Description
7 to 6	-	R/W	00	must be set to 00
5 to 0	AD[5:0]	R/W	-	programmable address bits of the first byte of the programming

9.3.2 Description of chip ID byte

Table 10. ID - Identification byte (subaddress 00h) bit description

*Legend: * power-on reset value*

Bit	Symbol	Access	Value	Description
7	-	R	1*	must be logic 1
6 to 0	ID[6:0]	R	000 0100*	TDA18211HD/C2 identification number

9.3.3 Description of temperature sensor byte

The temperature sensor is not available in Device-off mode as it requires a 16 MHz clock to operate.

Table 11. TM - Thermo byte (subaddress 01h) bit description

*Legend: * power-on reset value*

Bit	Symbol	Access	Value	Description
7	POR	R	1*	power supply falls below the power-on reset level and is reset after a read operation ending with a stop condition
			0	power supply is above the power-on reset level
6	LOCK	R	1	main synthesizer is locked to the programmed frequency
			0*	main synthesizer is not locked to the programmed frequency

Table 11. TM - Thermo byte (subaddress 01h) bit description *…continued*

*Legend: * power-on reset value*

Bit	Symbol	Access	Value	Description
5	TM_RANGE	R/W		temperature range selection for the internal die sensor (see Table 50)
			1	92 °C to 122 °C
			0*	60 °C to 90 °C
4	TM_ON	R/W	1	enables die temperature measurement (see Table 50)
			0*	disables die temperature measurement (see Table 50)
3 to 0	TM_D[3:0]	R	XXXX	data from die temperature measurement (see Table 50)

9.3.4 Description of power level byte (read mode)

There are 9 power level bits, dispatched in byte 2 and 3. They indicate the composite voltage gain of the LNA, the loaded attenuator voltage gain, and the level at the input of the RF AGC.

Table 12. PL - Power level (address 02h and 03h) bit description

*Legend: * power-on reset value*

Address	Register	Bit	Symbol	Access	Value	Description
03h	EP1	7	POWER_LEVEL[8]	R		AGC2 gain, attenuator voltage gain included load, the attenuator load is 50 Ω (explaining the maximum gain of −6 dB)
02h	PL	7	POWER_LEVEL[7]	R		
					00	−15 dB
					01	−12 dB
					10	−9 dB
					11	−6 dB
		6 to 5	POWER_LEVEL[6:5]	R		AGC1 gain, LNA voltage gain, the LNA voltage gain assumes a 75 Ω source impedance and a low output impedance
					00	6 dB
					01	9 dB
					10	12 dB
					11	15 dB
		4 to 0	POWER_LEVEL[4:0]	R		sensed level at the input of the RF AGC, detector slope is −1 dB/step
					0 0000	103 dBµV (RMS value)
					0 0001	102 dBµV (RMS value)
					...	...
					1 1110	73 dBµV (RMS value)
					1 1111	72 dBµV (RMS value)

9.3.5 Description of Easy Prog byte 1

Table 13. EP1 - Easy Prog byte 1 (subaddress 03h) bit description

*Legend: * power-on reset value*

Bit	Symbol	Access	Value	Description
7	POWER_LEVEL[8]	R		see Table 12
6	DIS_POWER_LEVEL	R/W	1*	power level disabled
			0	power level enabled
5	-	R/W	0*	must be set to logic 0
4	RF_CAL_OK	R/W		RF tracking filter calibration procedure (see Section 9.4.9); updated each time the procedure is started
			1	successful
			0*	not successful
3	IR_CAL_OK	R/W		complete image rejection calibration procedure (see Section 9.4.4); can only be reset with POR
			1	successful
			0*	not successful
2 to 0	BP_FILTER[2:0]	R/W	110*	RF band-pass filter selection (see Table 42)

9.3.6 Description of Easy Prog byte 2

Table 14. EP2 - Easy Prog byte 2 (subaddress 04h) bit description

*Legend: * power-on reset value*

Bit	Symbol	Access	Value	Description
7 to 5	RF_BAND[2:0]	R/W	110*	RF tracking filter band selection (see Table 43)
4 to 0	GAIN_TAPER[4:0]	R/W		gain taper value (see Table 47)
			1 1111*	minimum attenuation
			0 0000	maximum attenuation

9.3.7 Description of Easy Prog byte 3

The TDA18211HD has three different Standby modes. Two Standby modes are dedicated to special application demands; the real Standby mode is called ‘device-off’. It represents the smallest achievable power consumption.

Table 15. EP3 - Easy Prog byte 3 (subaddress 05h) bit description

*Legend: * power-on reset value*

Bit	Symbol	Access	Value	Description
7	SM	R/W	1*	Sleep mode (see Table 16)
			0	Normal mode (see Table 16)
6	SM_LT	R/W	0*	see Table 16
5	SM_XT	R/W	0*	see Table 16
4 to 0	STD[4:0]	R/W	1 0010*	description of standards (see Table 41)

Table 16. Standby modes[1]

Bit			Circuit			Mode
SM	SM_LT	SM_XT	Loop-through	Slave-tuner output	Crystal oscillator	
0	0	0	on	on	on	Normal mode
1	0	0	on	on	on	Standby mode with crystal oscillator, slave-tuner output and loop-through output on
1	1	0	off	off	on	Standby mode with only crystal oscillator and its output buffer on
1	1	1	off	off	off	Device-off mode

[1] In all modes, the I^2C-bus interface remains active. All other codes are not valid.

9.3.8 Description of Easy Prog byte 4

Table 17. EP4 - Easy Prog byte 4 (subaddress 06h) bit description

*Legend: * power-on reset value*

Bit	Symbol	Access	Value	Description
7	FM_RFN	R/W		selection which input is fed to RF filter
			1	FM input (RF LNA on; FM LNA on)
			0*	RF input (RF LNA on; FM LNA off)
6	XTOUT_ON	R/W	1*	16 MHz on pins XTOUTP and XTOUTN
			0	not 16 MHz on pins XTOUTP and XTOUTN
3	-	R/W	1*	must be set to logic 1
4 to 2	IF_LEVEL[2:0]	R/W		IF output level selection and attenuation with regard to 2 V (p-p)
			000*	2 V (p-p); 0 dB
			001	1.25 V (p-p); 4 dB
			010	1 V (p-p); 6 dB
			011	0.8 V (p-p); 8 dB
			100	not used
			101	not used
			110	not used
			111	0.5 V (p-p); 12 dB
1 to 0	CAL_MODE[1:0]	R/W		calibration mode selection
			00*	no calibration (Normal mode)
			01	Power detection mode
			10	image rejection calibration (IRCAL) mode
			11	RF tracking filters calibration (RFCAL) mode

It is recommended to follow the flowcharts described in Section 9.4 in order to perform any calibration, as they require a precise set of sequential operations. The further comments can only give an overview of what is typically done during the flowchart.

The TDA18211HD has two calibration modes: one for the image rejection calibration, and one for the RF tracking filters calibration.

The image rejection calibration consists in optimizing some tunable parameters inside the mixer throughout a set of internal measurements, leading to ensure a 65 dB typical value of image rejection. The internal signal used during this phase is generated by the PLL calibration (CAL PLL).

The RF tracking filters central frequency can be adjusted with the tuning word RFC_CPROG. The RF tracking filters calibration (RFCAL) consists of an internal tone at the input of the tracking filters (with the CAL PLL), and finding the RFC_CPROG corresponding to the maximum transmitted power. The RFCAL is just a little part of a more complex algorithm fully described in the flowcharts in Section 9.4.

The Power detection mode is a Normal mode where the detector used for the calibrations is switched ON. This special mode enables to sense the power at the input of the TDA18211HD and makes the power scan algorithm possible (see Section 9.4.8 "Flowchart TDA18211PowerScan").

9.3.9 Description of Easy Prog byte 5

Table 18. EP5 - Easy Prog byte 5 (subaddress 07h) bit description

*Legend: * power-on reset value*

Bit	Symbol	Access	Value	Description
7	EXTENDED_REG	R/W		enables the extended register addressing
			1	extended register (00h to 26h)
			0*	limited register (00h to 0Fh); only 1 byte can be programmed after address 0Fh within 1 transmission
6 to 4	IR_GSTEP[2:0]	R/W	011*	gain step for image rejection calibration
3	-	R/W	0*	must be set to logic 0
2 to 0	IR_MEAS[2:0]	R/W	000*	image rejection measurement frequency range (see Table 51)

9.3.10 Description of Cal Post-Divider byte

Table 19. CPD - Cal Post-Divider byte (subaddress 08h) bit description

*Legend: * power-on reset value*

Bit	Symbol	Access	Value	Description
7 to 0	CAL_POST_DIV[7:0]	R/W	00h*	calibration synthesizer post-divider (see Table 46)

9.3.11 Description of Cal divider bytes 1, 2 and 3

Table 20. CD1, CD2 and CD3 - Cal divider bytes 1, 2 and 3 (address 09h, 0Ah and 0Bh) bit description

*Legend: * power-on reset value*

Address	Register	Bit	Symbol	Access	Value	Description
09h	CD1	7	-	R/W	0*	must be set to logic 0
		6 to 0	CAL_DIV[22:16]	R/W	00h*	calibration synthesizer main divider bits
0Ah	CD2	7 to 0	CAL_DIV[15:8]	R/W	00h*	
0Bh	CD3	7 to 0	CAL_DIV[7:0]	R/W	00h*	

9.3.12 Description of Main Post-Divider byte

Table 21. MPD - Main Post-Divider byte (subaddress 0Ch) bit description

*Legend: * power-on reset value*

Bit	Symbol	Access	Value	Description
7	IF_NOTCH	R/W	0*	adds a DC notch in IF for a better adjacent channels rejection; depends on standards; see Table 41
6 to 4	MAIN_POST_DIV[6:4]	R/W	000*	LO synthesizer post-divider (see Table 45)
3	DCDC_CKSW	R/W		allows switching between 16 MHz and sub-harmonic LO for DC-to-DC converter locking
			1	16 MHz
			0*	sub-harmonic LO
2 to 0	MAIN_POST_DIV[2:0]	R/W	000*	LO synthesizer post-divider (see Table 45)

9.3.13 Description of Main divider bytes 1, 2 and 3

Table 22. MD1, MD2 and MD3 - Main divider bytes 1, 2 and 3 (address 0Dh, 0Eh and 0Fh) bit description

*Legend: * power-on reset value*

Address	Register	Bit	Symbol	Access	Value	Description
0Dh	MD1	7	-	R/W	0*	must be set to logic 0
		6 to 0	MAIN_DIV[22:16]	R/W	00h*	LO synthesizer main divider bits
0Eh	MD2	7 to 0	MAIN_DIV[15:8]	R/W	00h*	
0Fh	MD3	7 to 0	MAIN_DIV[7:0]	R/W	00h*	

9.3.14 Description of Extended bytes 1 to 23

Table 23. EB1 to EB23 - Extended bytes 1 to 23 (address 10h to 26h) bit description

*Legend: * power-on reset value*

Address	Register	Bit	Symbol	Access	Value	Description
10h	EB1	7 to 3	EB1[7:3]	R	1 1111*	extended byte 1
		2	CALVCO_FORLON	R		determines VCO used during Normal mode operations
					1*	LO VCO is used
					0	CAL VCO is used
		1	AGC1_ALWAYS_MASTERN	R		enables AGC1 normal operation whatever the tuner type, master or slave.
					1*	normal operation for the master; 6 dB fixed for the slave
					0	normal operation for both the master and the slave
		0	AGC1_FIRSTN	R		determines which AGC will be updated when detectors 1 and 2 are up
					1*	AGC1 and AGC2 both updated
					0	AGC1 has priority on AGC2
11h	EB2	7 to 0	EB2[7:0]	R/W	0000 0001*	extended byte 2
12h	EB3	7 to 0	EB3[7:0]	R/W	1000 0100*	extended byte 3
13h	EB4	7 to 6	EB4[7:6]	R/W	01*	extended byte 4
		5	LO_FORCESRCE	R/W	1	forces the main PLL charge pump to source current to the main PLL loop filter
					0*	no force
		4 to 0	EB4[4:0]	R/W	0 0001*	extended byte 4
14h	EB5	7 and 6	EB5[7:0]	R/W	0000 0001*	extended byte 5
15h	EB6	7 to 0	EB6[7:0]	R/W	1000 0100*	extended byte 6
16h	EB7	7 and 6	EB7[7:6]	R/W	01*	extended byte 7
		5	CAL_FORCESRCE	R/W	1	forces the main PLL charge pump to source current to the main PLL loop filter
					0*	no force
		4 to 0	EB7[4:0]	R/W	0 1000*	extended byte 7
17h	EB8	7	CID_ALARM	R		signal sensed by the power detector used during calibrations
					1	out of range
					0*	in range
		6 to 4	EB8[6:4]	R/W	111*	extended byte 8
		3	EB8[3]	R	0*	
		2 to 0	EB8[2:0]	R/W	101*	
18h	EB9	7 to 0	EB9[7:0]	W	0000 0000*	extended byte 9
19h	EB10	7 and 6	EB10[7:6]	R	XX	extended byte 10
		5 to 0	CID_GAIN[5:0]	R	XX XXXX	calibration power detector output

Table 23. EB1 to EB23 - Extended bytes 1 to 23 (address 10h to 26h) bit description *…continued*

*Legend: * power-on reset value*

Address	Register	Bit	Symbol	Access	Value	Description
1Ah	EB11	7 to 0	EB11[7:0]	R/W	1000 0110*	extended byte 11
1Bh	EB12	7 and 6	EB12[7:6]	R	00*	extended byte 12
		5	PD_AGC1_DET	R/W		AGC1 detector
					1	power-down
					0*	no power-down
		4	PD_AGC2_DET	R/W		AGC2 detector
					1	power-down
					0*	no power-down
		3 to 0	EB12[3:0]	R/W	0111*	extended byte 12
1Ch	EB13	7	EB13[7]	R/W	1*	extended byte 13
		6 to 4	RFC_K[2:0]	R/W	100*	parameters used during the RF tracking filters calibration (see Table 44)
		3 and 2	RFC_M[1:0]	R/W	00*	
		1 to 0	EB13[1:0]	R/W	10*	extended byte 13
1Dh	EB14	7 to 0	RFC_CPROG[7:0]	R/W	0000 0000*	tuning word of the RF tracking filters
1Eh	EB15	7 to 4	EB15[7:4]	R/W	1000*	extended byte 15
		3 to 0	EB15[3:0]	R	XXXX*	
1Fh	EB16	7 to 0	EB16[7:0]	W	000X XX00*	extended byte 16
20h	EB17	7 to 0	EB17[7:0]	W	000X XXXX*	extended byte 17
21h	EB18	7	AGC1_LOOP_OFF	R/W		turns the AGC1 loop
					1	off
					0*	on
		6 to 2	EB18[6:2]	R/W	000 00*	extended byte 18
		1 and 0	AGC1_GAIN[1:0]	R/W		AGC1 gain
					00*	6 dB
					01	9 dB
					10	12 dB
					11	15 dB
22h	EB19	7 to 0	EB19[7:0]	W	000X XX00*	extended byte 19
23h	EB20	7 and 6	EB20[7:6]	W	10*	extended byte 20
		5	FORCE_LOCK	W		forces the internal lock indicator
					1	forced to logic 1
					0*	not forced
		4 to 0	EB20[4:0]	W	X XXXX*	extended byte 20

Table 23. EB1 to EB23 - Extended bytes 1 to 23 (address 10h to 26h) bit description *…continued*

*Legend: * power-on reset value*

Address	Register	Bit	Symbol	Access	Value	Description
24h	EB21	7	AGC2_LOOP_OFF	R/W		turns the AGC2 loop
					1	off
					0*	on
		6 to 2	EB21[6:2]	R/W	0 1100*	extended byte 21
		1 and 0	AGC2_GAIN[1:0]	R/W		AGC2 gain
					00	−15 dB
					01	−12 dB
					10	−9 dB
					11*	−6 dB
25h	EB22	7	EB22[7]	R	0*	extended byte 22
		6 to 4	RFAGC_TOP[2:0]	R/W	100*	take over point of the RF AGC, detection in RF
		3 to 0	IFAGC_TOP[3:0]	R/W	1000*	take over point of the RF AGC, detection in IF
26h	EB23	7 to 3	EB23[7:3]	R/W	1 0110*	extended byte 23
		2	FORCELP_FC2_EN	R/W	0*	1.5 MHz bandwidth filter selection; see Table 24
		1	LP_FC[2]	R/W	0*	
		0	EB23[0]	R/W	0*	extended byte 23

Table 24. Low pass cut-off frequency

FORCELP_FC2_EN	LP_FC[2]	STD[1:0]	Cut-off frequency (MHz)
0	X	00	6
0	X	01	7
0	X	10	8
0	X	11	9

9.4 I²C-bus programming flowcharts

The following flowcharts describe how to:

- Initialize the TDA18211HD
- Launch the calibrations
- Go to Normal mode

The image rejection calibration as well as RF tracking filters calibration must be launched the way explicitly described in the flowchart. If not done this way, it may result in bad calibration or even blocking the TDA18211HD, which makes it impossible to communicate via the I²C-bus.

For proper internal initialization, switching to Normal mode also requires a single I²C-bus sequence from subaddresses 03h to 0Fh.

9.4.1 Flowchart explanation

This section provides instructions for reading the flowcharts.

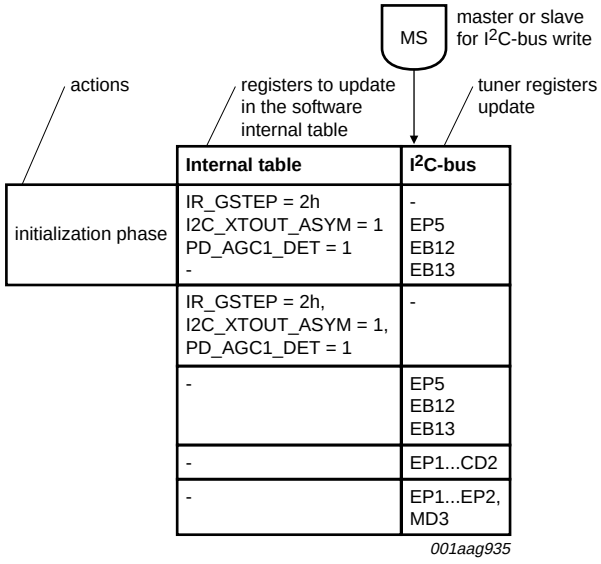


Fig 3. Programming sequence

1. I²C-bus write:
   - IR_GSTEP is updated, no immediate I²C-bus write
   - I2C_XTOUT_ASYM is updated followed by an I²C-bus write of EP5
   - PD_AGC1_DET is updated followed by an I²C-bus write of EB12
   - I²C-bus write of EB13 with current value of the software internal table of EB13

   I²C-bus read:
   - Sub-addressing is not supported in read mode
   - The only recommended I²C-bus read access procedures of the TDA18211HD are described in Section 9.4.16 “Flowchart TDA18211Read” and Section 9.4.17 “Flowchart TDA18211ReadExtended”

2. Update at the same moment is indicated by separation with commas:

   IR_GSTEP, I2C_XTOUT_ASYM and PD_AGC1_DET are updated, no I²C-bus registers update

3. I²C-bus registers update of the bytes EP5, EB12 and EB13
4. Bytes EP1 to CD2 are written in a single I²C-bus sequence

   Example:

   Start C0 03 EP1 EP2 EP3 EP4 EP5 CPD CD1 CD2 Stop

5. Bytes EP1, EP2 and MD3 are written in as many I²C-bus sequences as needed

   Example:

   Start C0 03 EP1 EP2 Stop

   Start C0 0F MD3 Stop

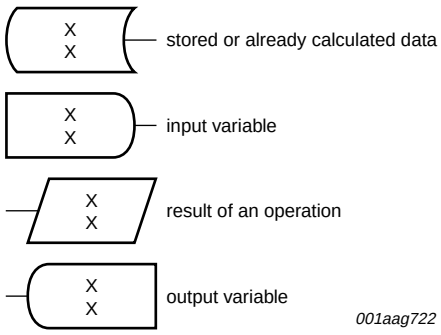
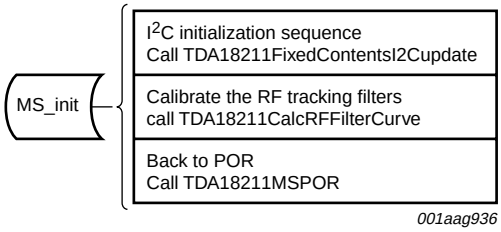
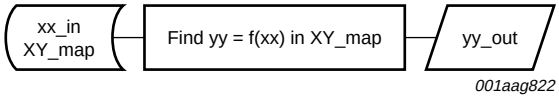


Fig 4. Blocks used in the flowcharts



Master/slave variable MS_init is input for each of the three procedures.

Fig 5. Variable used in multiple procedures

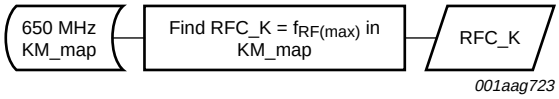


xx is a list of values stored in the first column of the map XY_map.

yy is a list of values stored in column in XY_map.

yy_out is the particular value of yy to find row n. $xx(n-1) < xx\_in \leq xx(n)$.

a. General description to find a value in a table



Finding the row of RFC_K: 350000 < 650000 ≤ 720000. Result n = 1. The value of RFC_K is then 3 (see Table 44).

b. Example to find the value RFC_K corresponding to f_{RF} = 650 MHz in the KM_map.

Fig 6. Finding a value in a table

Units

- In the flowcharts, hexadecimal values end with “h”, decimal values with “d”
- Frequency variables used in computations are expressed in kHz, for example 1 GHz is written as 1000000.

9.4.2 Flowchart TDA18211SetRf_dual

Table 25. TDA18211SetRf_dual

Function	Description	Reference
Description	protocol top view for a dual-tuner application	
Input	RF_freq, Standard (from microcontroller), MS (from microcontroller)	
Table	-	
Output	-	

The initialization phase has to be launched before any SetRf.

MS = 1: master is selected for the channel configuration.

MS = 0: slave is selected for the channel configuration.

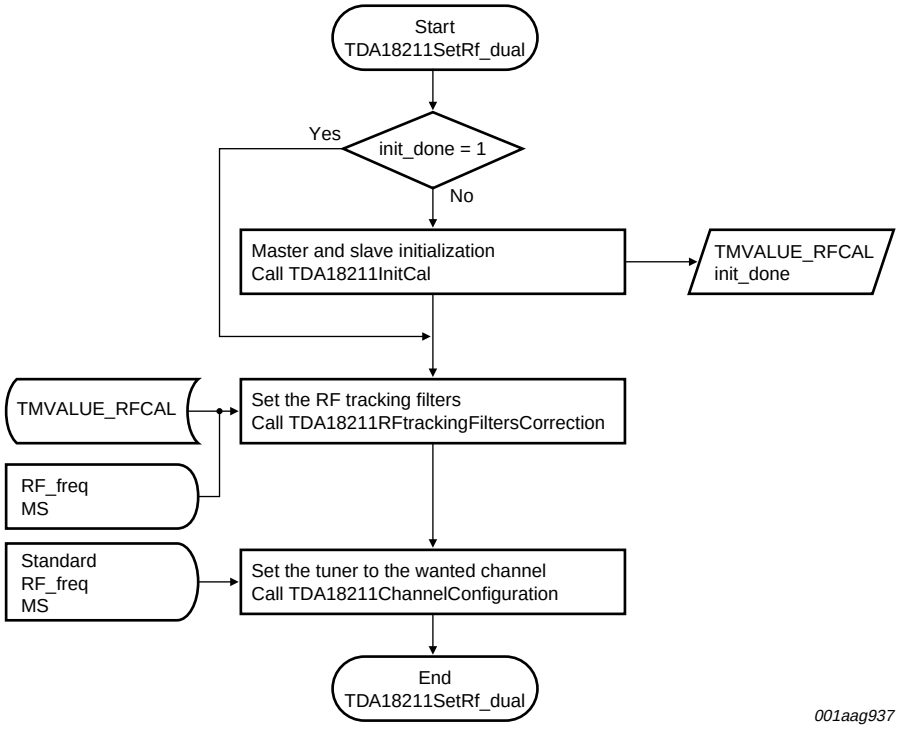


Fig 7. Flowchart TDA18211SetRf_dual

9.4.3 Flowchart TDA18211InitCal

Table 26. TDA18211InitCal

Function	Description	Reference
Description	systematic initialization for master and slave tuners	
Input	MS_init	
Table	-	
Output	TMVALUE_RFCAL, init_done	

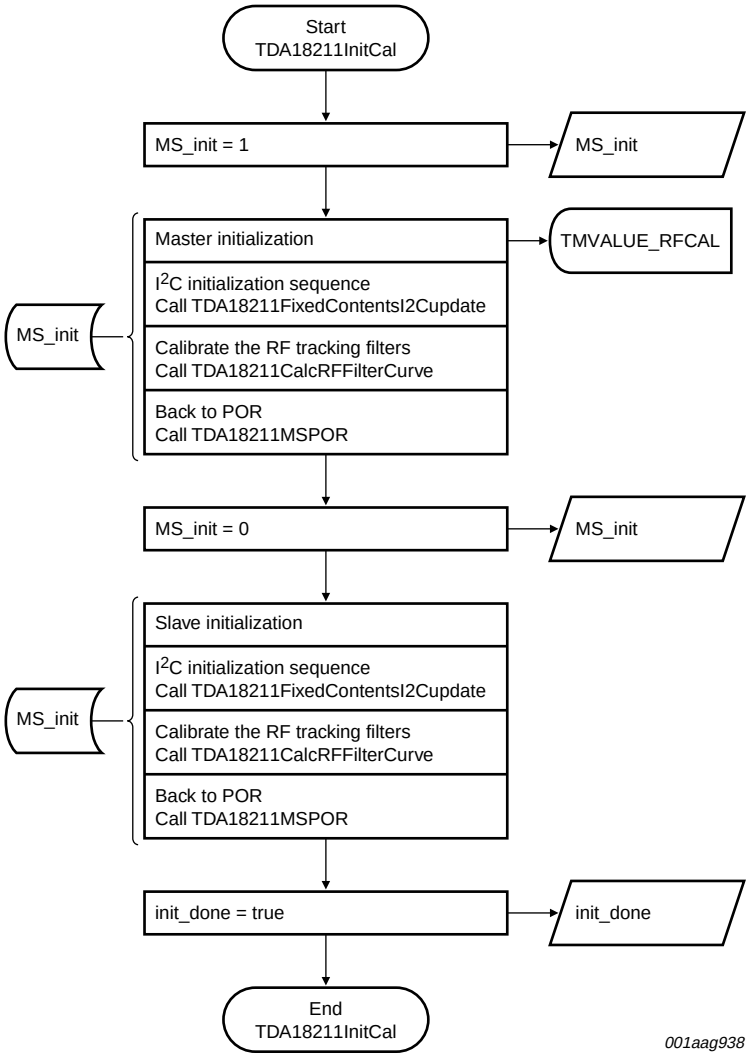


Fig 8. Flowchart TDA18211InitCal

9.4.4 Flowchart TDA18211FixedContentsI2Cupdate

Table 27. TDA18211FixedContentsI2Cupdate

Function	Description	Reference
Description	update and write the TDA18211HD registers, sequential update of AGC1 and AGC2, image calibration algorithm	
Input	MS	
Table	-	
Output	-	

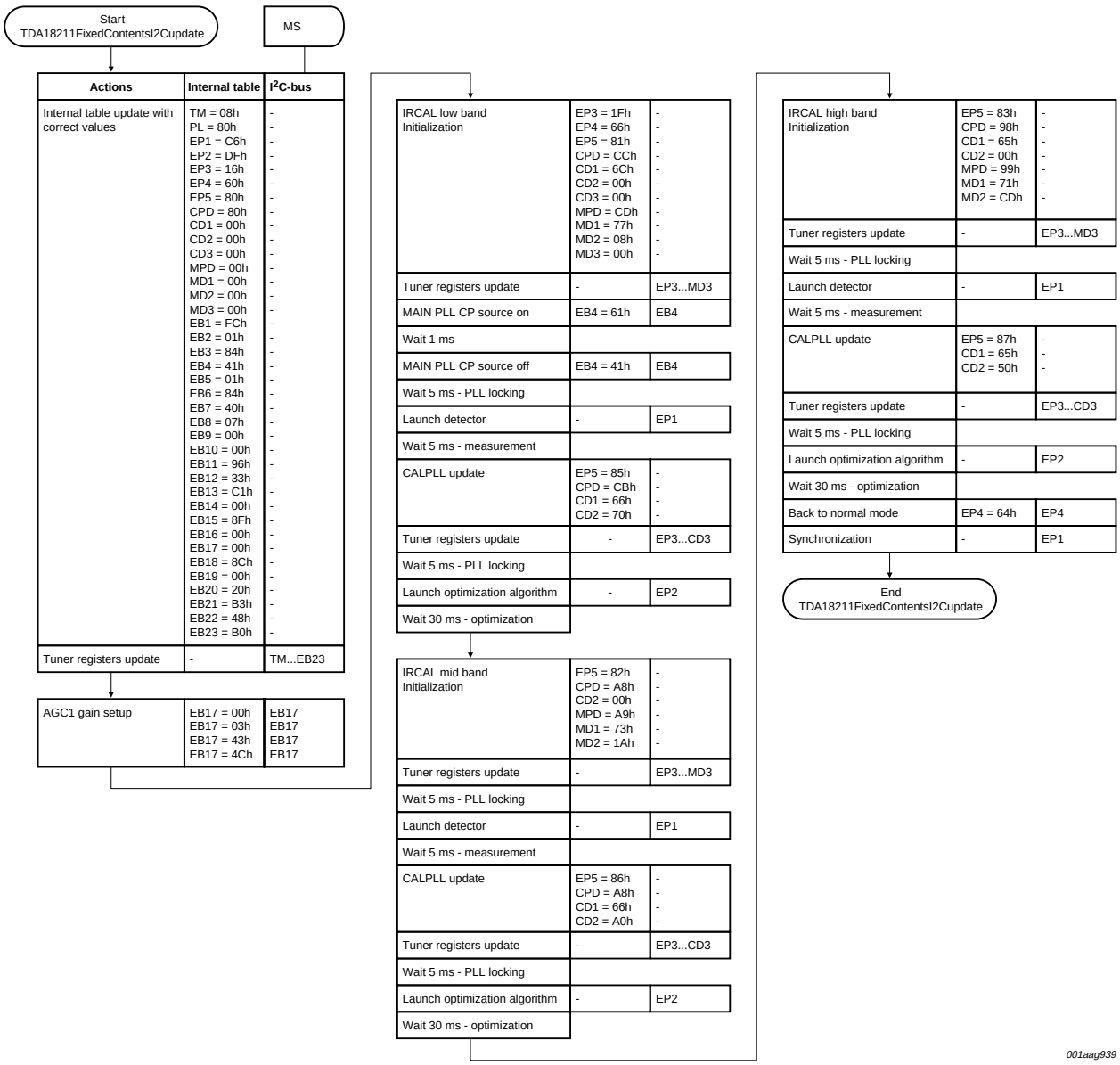


Fig 9. Flowchart TDA18211FixedContentsI2Cupdate

9.4.5 Flowchart TDA18211CalcRFFilterCurve

Table 28. TDA18211CalcRFFilterCurve

Function	Description	Reference
Description	calculate the RF filter curves coefficients	
Input	RF1_default, RF2_default, RF3_default, MS	
Table	RF_BAND_map	Table 43 “RF_BAND_map”
Output	TMVALUE_RFCAL	

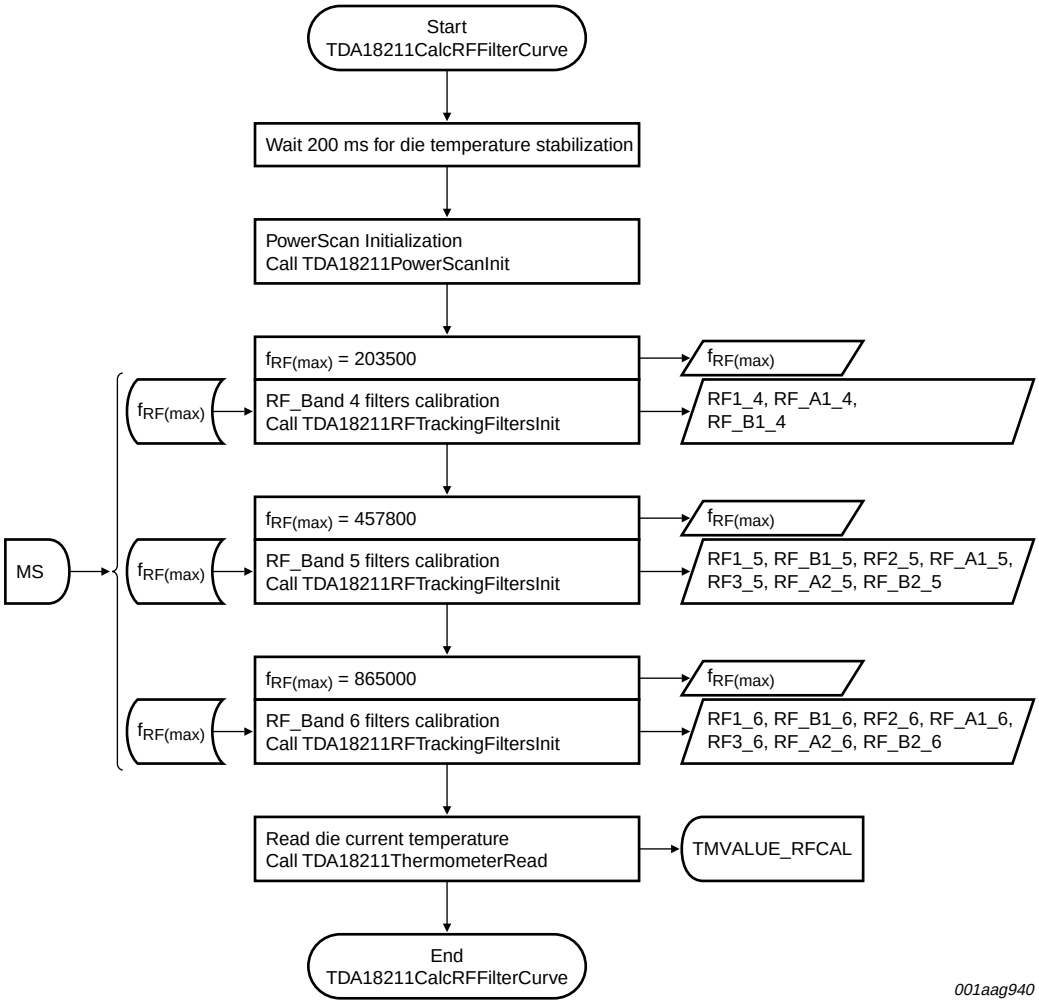


Fig 10. Flowchart TDA18211CalcRFFilterCurve

9.4.6 Flowchart TDA18211RFTrackingFiltersInit

Table 29. TDA18211RFTrackingFiltersInit

Function	Description	Reference
Description	calculate the RF filter curve coefficients used for their approximation	
Input	$f_{RF(max)}$, MS	
Table	RF_CAL_map (Cprog_table = f(frequency))	Table 49 “RF_CAL_map”
Output	RF1, RF2, RF3, RF_A1, RF_B1, RF_B2	

bcal is a boolean output from TDA18211PowerScan:

bcal = 1 (true): enables the calibration of the RF tracking filters

bcal = 0 (false): no calibration is performed, default values for RFC_CPROG are used

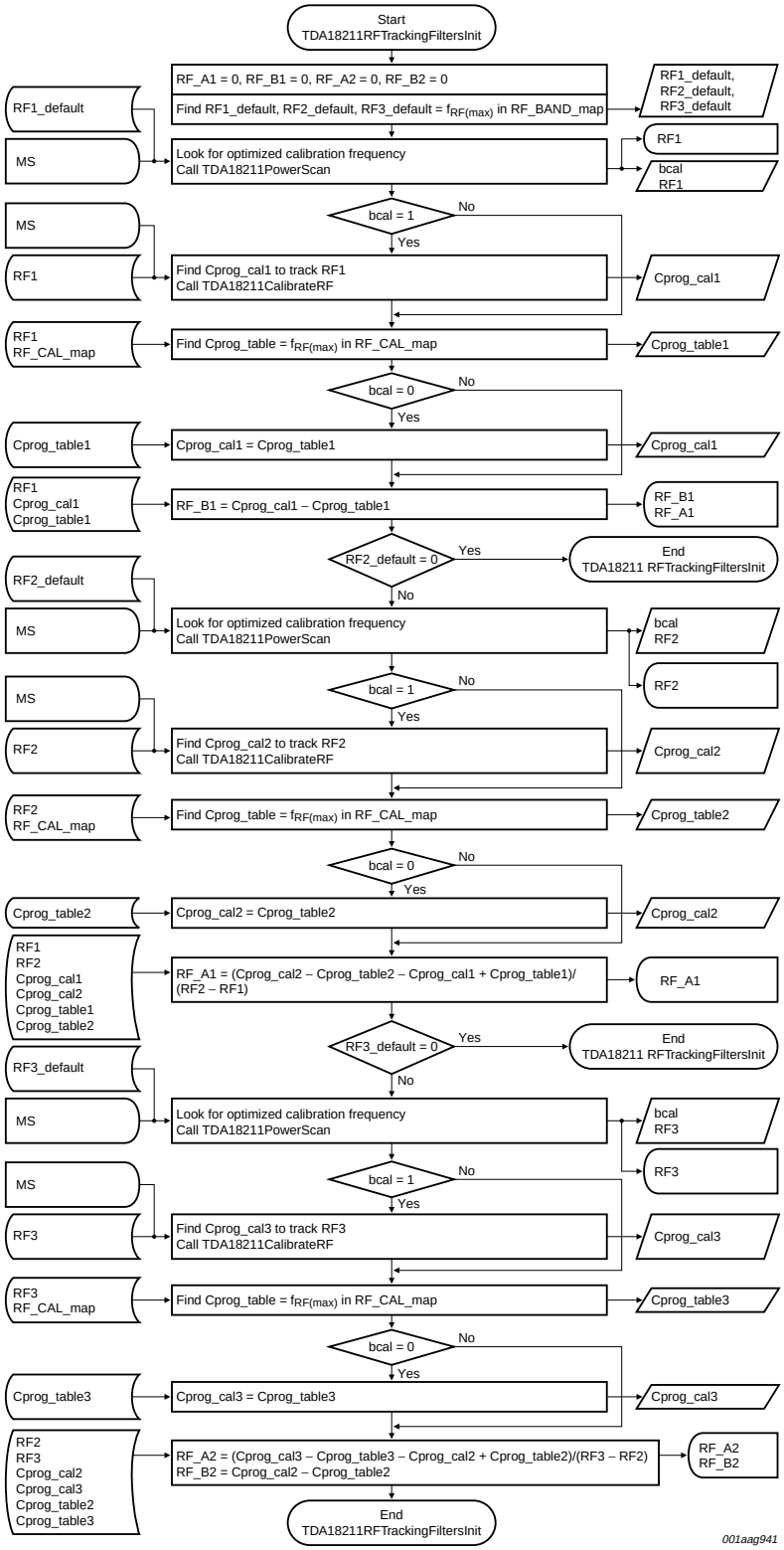


Fig 11. Flowchart TDA18211RFTrackingFiltersInit

9.4.7 Flowchart TDA18211PowerScanInit

Table 30. TDA18211PowerScanInit

Function	Description	Reference
Description	fixed settings of the TDA18211PowerScan	
Input	MS	
Table		
Output		

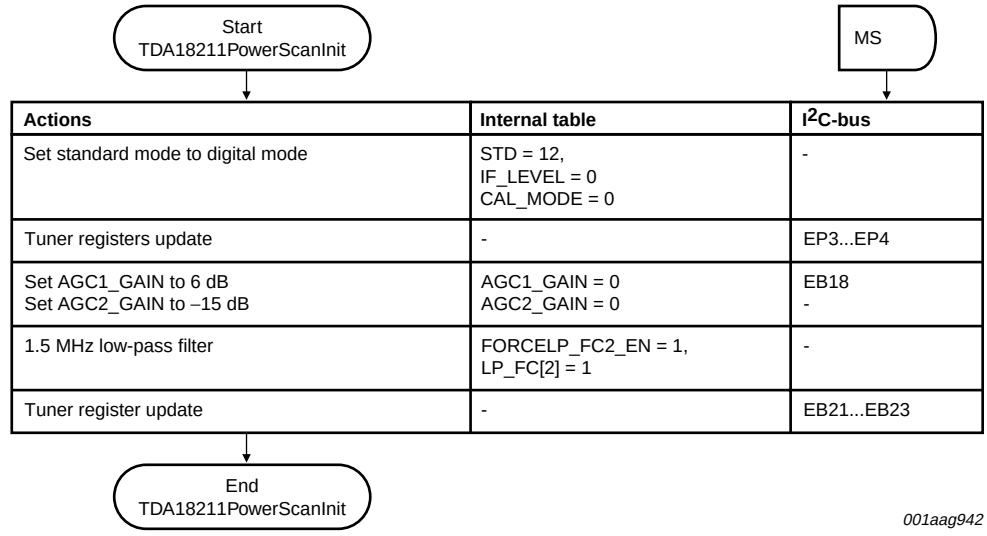


Fig 12. Flowchart TDA18211PowerScanInit

9.4.8 Flowchart TDA18211PowerScan

Table 31. TDA18211PowerScan

Function	Description	Reference
Description	find an interferer free calibration frequency	
Input	freq_input, MS	
Table	RF_BAND_map,	Table 43 “RF_BAND_map”
	RF_CAL_map,	Table 49 “RF_CAL_map”
	CID_TARGET_map	Table 52 “CID_TARGET_map”
Output	bcal, freq_output	

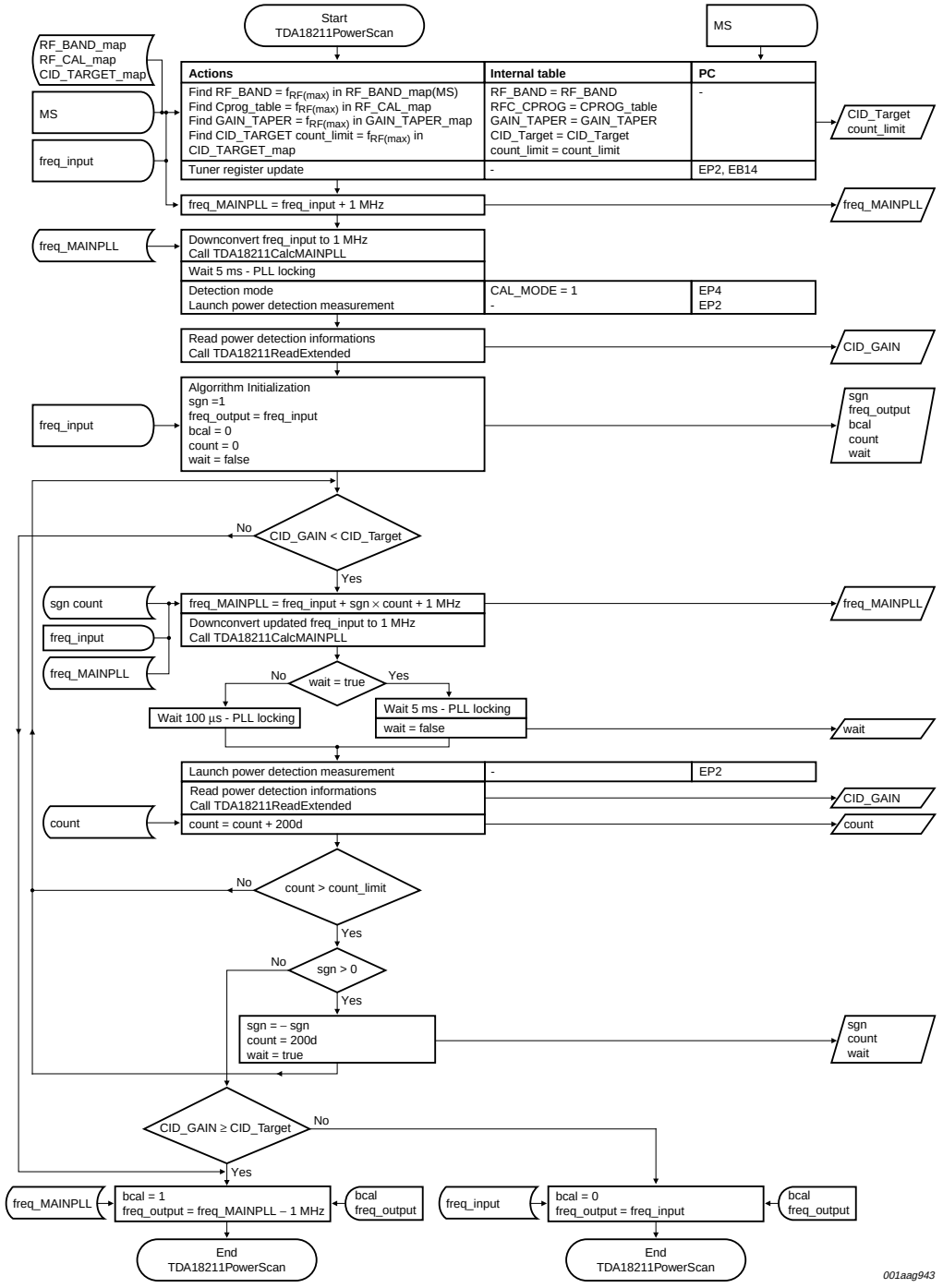


Fig 13. Flowchart TDA18211PowerScan

9.4.9 Flowchart TDA18211CalibrateRF

Table 32. TDA18211CalibrateRF

Function	Description	Reference
Description	find the Cprog for which freq_input is the central frequency of the RF tracking filters	
Input	freq_input, MS	
Table	BP_FILTER_map,	Table 42 “BP_FILTER_map”
	KM_map,	Table 44 “KM_map”
	GAIN_TAPER_map	Table 47 “GAIN_TAPER_map”
Output	RFC_CPROG	

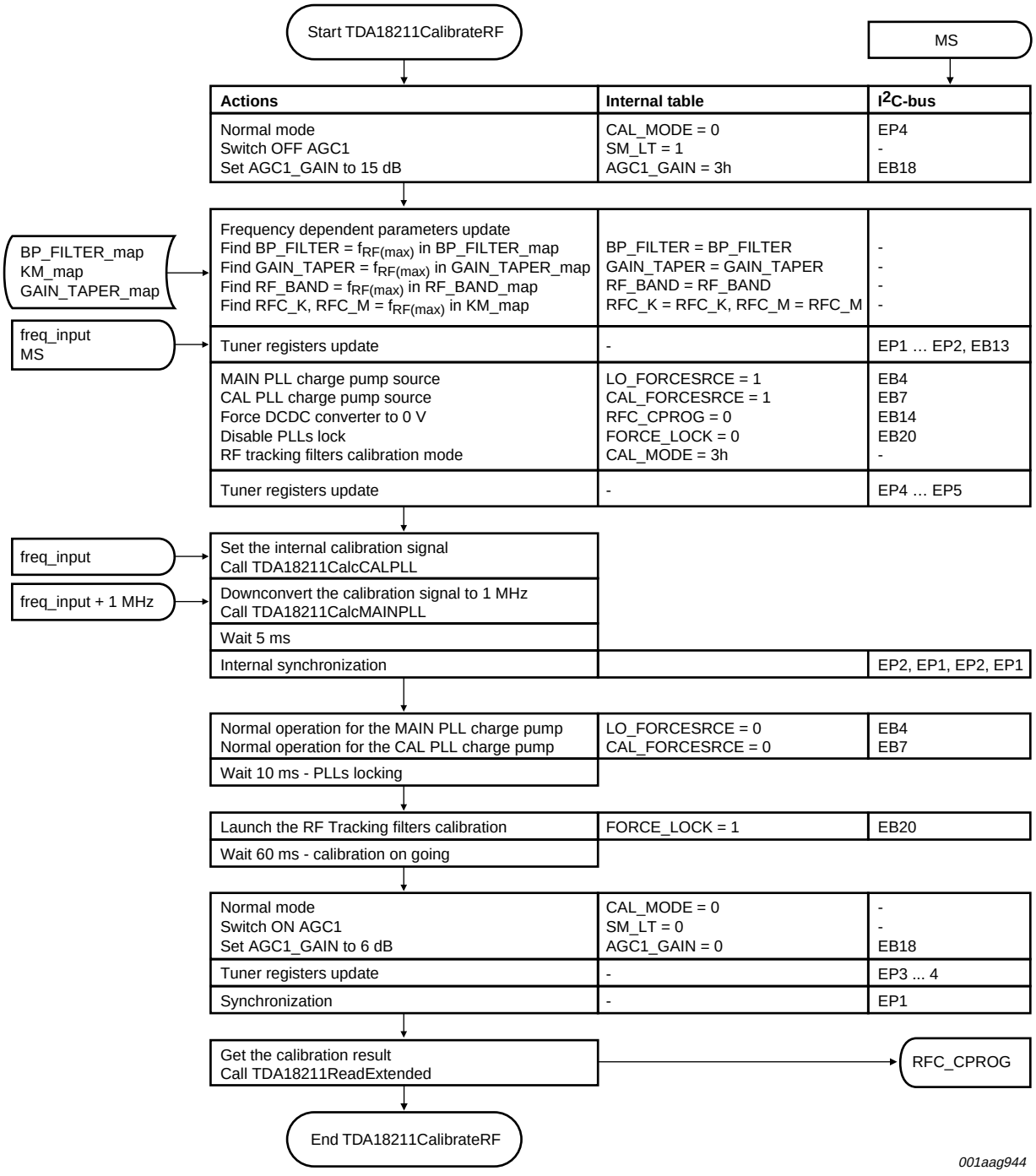


Fig 14. Flowchart TDA18211CalibrateRF

9.4.10 Flowchart TDA18211MSPOR

Table 33. TDA18211MSPOR

Function	Description	Reference
Description	master or slave tuner goes to Power-On Reset (POR) mode	
Input	MS	
Table	-	
Output	-	

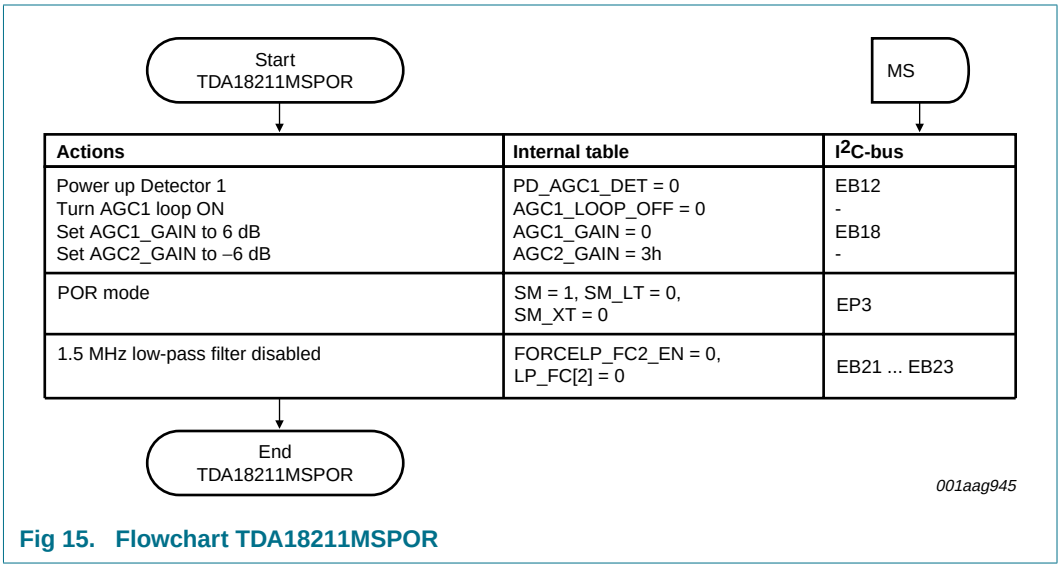


Fig 15. Flowchart TDA18211MSPOR

9.4.11 Flowchart TDA18211RFtrackingFiltersCorrection

Table 34. TDA18211RFtrackingFiltersCorrection

Function	Description	Reference
Description	find the Cprog corresponding to the programmed central frequency freq_input	
Input	freq_input, TMVALUE_RFCAL, MS	
Table	RF_BAND_map,	Table 43 “RF_BAND_map”
	RF_CAL_OVER_DT_map,	Table 48 “RF_CAL_DC_OVER_DT_map”
	RF_CAL_map	Table 49 “RF_CAL_map”
Output	-	

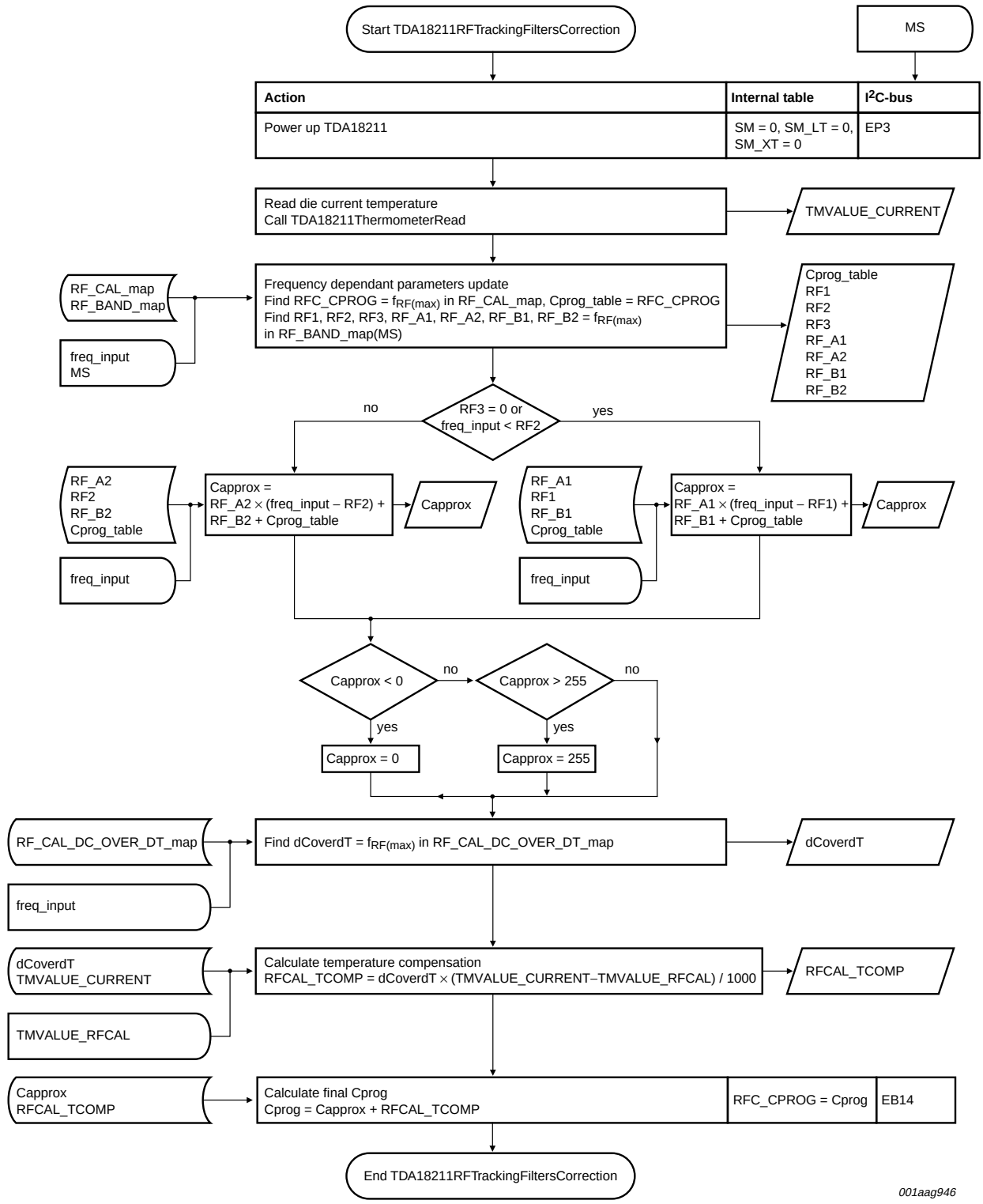


Fig 16. Flowchart TDA18211RFtrackingFiltersCorrection

9.4.12 Flowchart TDA18211ChannelConfiguration

Table 35. TDA18211ChannelConfiguration

Function	Description	Reference
Description	tune the tuner according to the channel and broadcast configuration	
Input	freq_input, MS, Standard	
Table	STANDARD_DESCRIPTION_map,	Table 41 “STANDARD_DESCRIPTION_map”
	BP_FILTER_map,	Table 42 “BP_FILTER_map”
	RF_BAND_map,	Table 43 “RF_BAND_map”
	CAL_PLL_map,	Table 46 “CAL_PLL_map”
	GAIN_TAPER_map,	Table 47 “GAIN_TAPER_map”
	IR_MEAS_map	Table 51 “IR_MEAS_map”
Output	-	

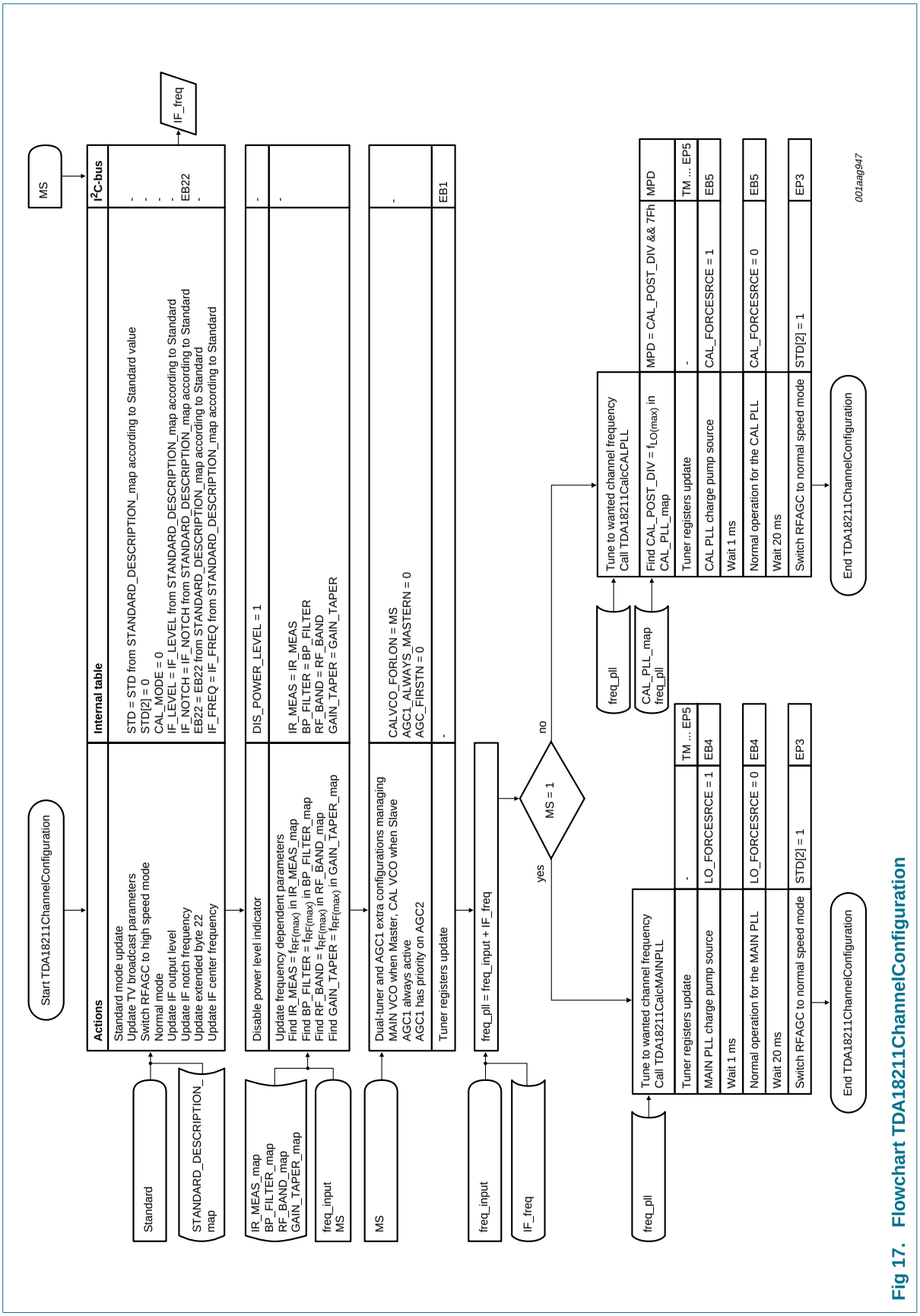


Fig 17. Flowchart TDA18211ChannelConfiguration

9.4.13 Flowchart TDA18211CalcMAINPLL

Table 36. TDA18211CalcMAINPLL

Function	Description	Reference
Description	find the correct values for the bytes MPD, MD1, MD2, MD3 and update the tuner registers	
Input	freq_input, MS	
Table	MAIN_PLL_map	Table 45 “MAIN_PLL_map”
Output	-	

MPD, MD1, MD2 and MD3 are 8-bit registers. Arithmetical and logical operations performed on those registers are considered binary operations. (Dividing is right shifting and multiplying is left shifting, etc.)

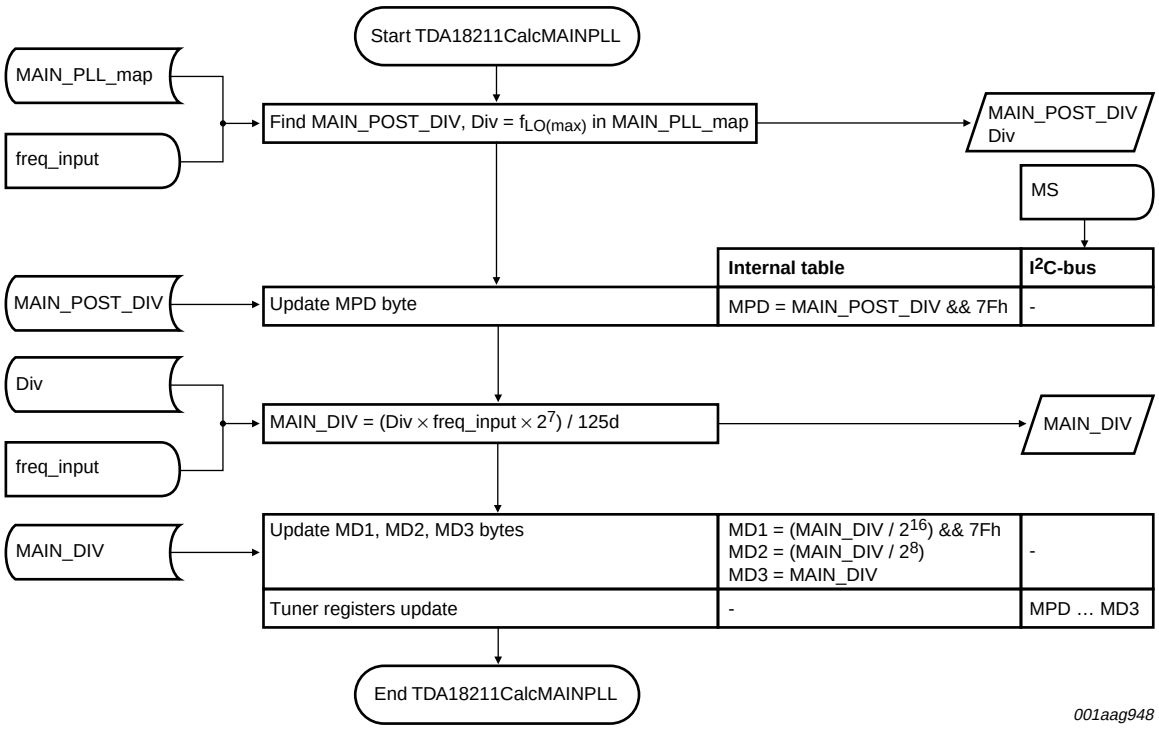


Fig 18. Flowchart TDA18211CalcMAINPLL

9.4.14 Flowchart TDA18211CalcCALPLL

CPD, CD1, CD2 and CD3 are 8-bit registers. Arithmetical and logical operations performed on those registers are considered binary operations. Dividing is right shifting and multiplying is left shifting.

Table 37. TDA18211CalcCALPLL

Function	Description	Reference
Description	find the correct values for the bytes CPD, CD1, CD2, CD3 and update the tuner registers	
Input	freq_input, MS	
Table	CAL_PLL_map	Table 46 “CAL_PLL_map”
Output		

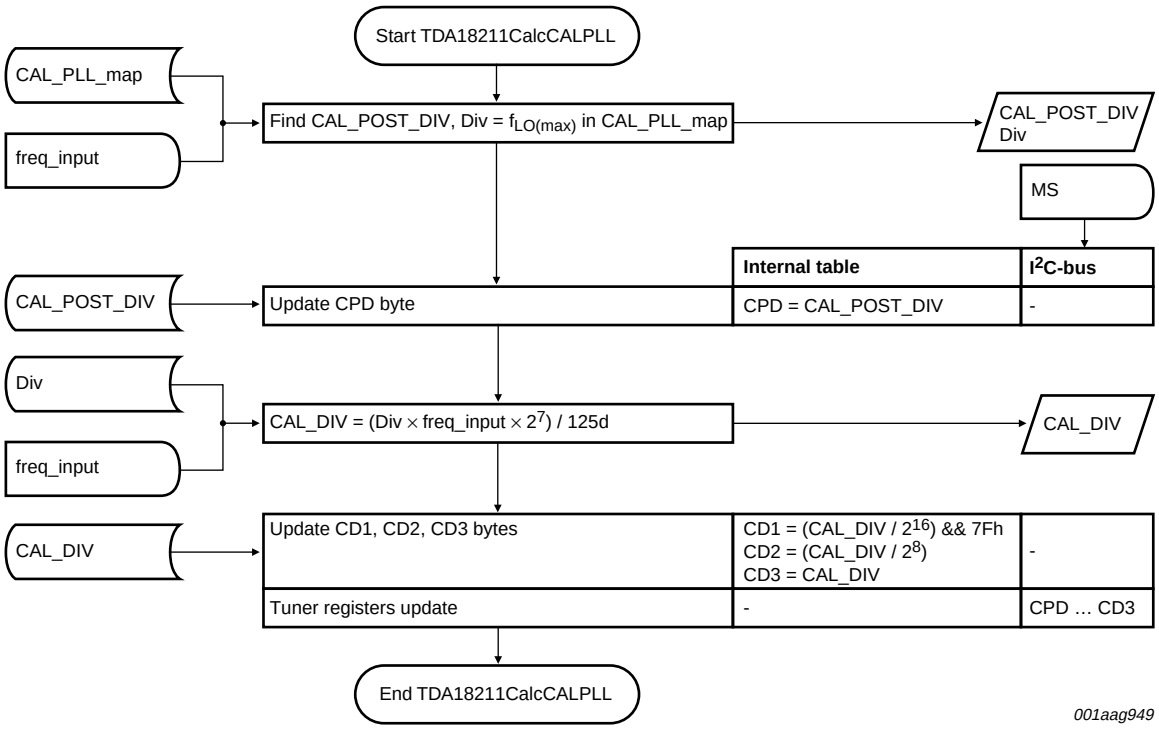


Fig 19. Flowchart TDA18211CalcCALPLL

9.4.15 Flowchart TDA18211ThermometerRead

Table 38. TDA18211ThermometerRead

Function	Description	Reference
Description	turns the on-chip thermometer ON, reads the current temperature on the die and then turns the thermometer OFF	
Input	MS	
Table	THERMOMETER_map	Table 50 “THERMOMETER_map[1]”
Output	TMVALUE (temperature in °C)	

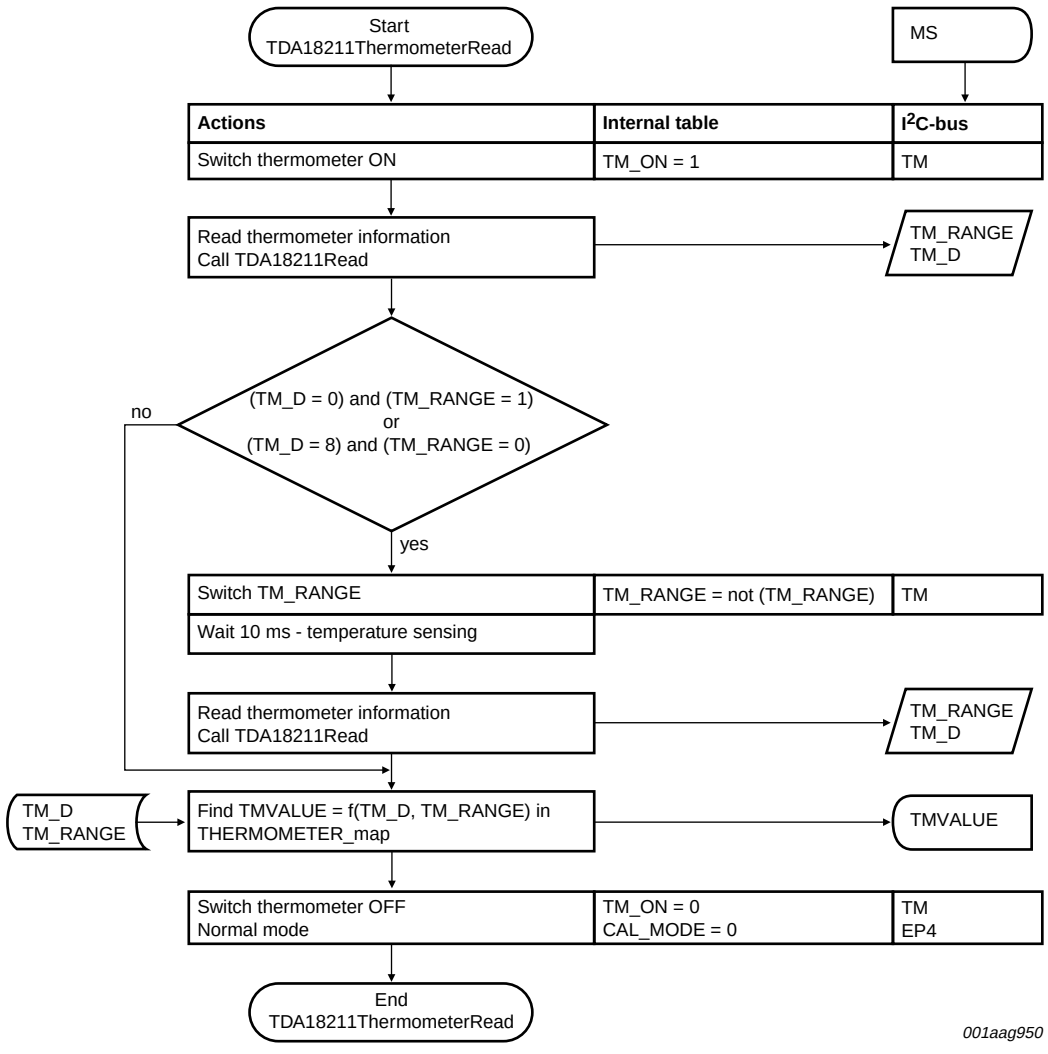


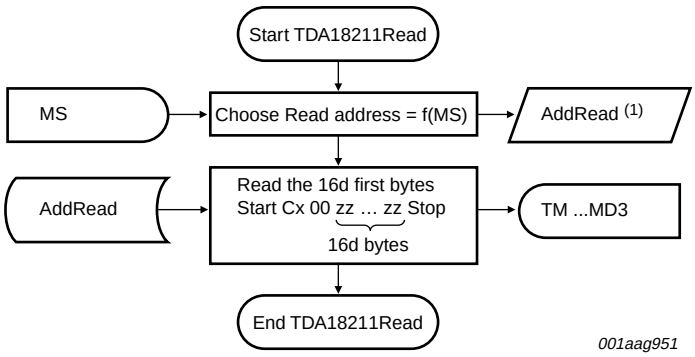
Fig 20. Flowchart TDA18211ThermometerRead

9.4.16 Flowchart TDA18211Read

Table 39. TDA18211Read

Function	Description	Reference
Description	read the 16 first bytes of the TDA18211HD	
Input	MS	
Table	-	
Output	an image of the tuner registers from TM to MD3	

The software internal table registers are not updated throughout a read procedure. The update is performed at the level of the call TDA18211Read.



AddRead = C1, C3, C5 or C7.

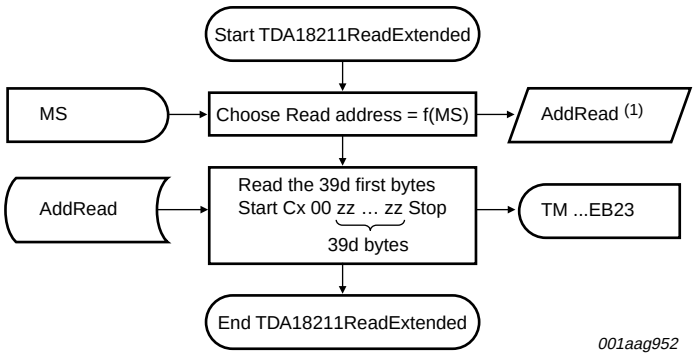
Fig 21. Flowchart TDA18211Read

9.4.17 Flowchart TDA18211ReadExtended

Table 40. TDA18211ReadExtended

Function	Description	Reference
Description	read the 39 first bytes of the TDA18211HD	
Input	MS	
Table	-	
Output	an image of the tuner registers from TM to EB23	

The software internal table registers are not updated throughout a read procedure. The update is performed at the level of the call TDA18211ReadExtended.



AddRead = C1, C3, C5 or C7.

Fig 22. Flowchart TDA18211ReadExtended

9.5 Maps

Table 41. STANDARD_DESCRIPTION_map

Standard[1]	Recommended value with a TDA10048HN channel decoder				
	STD[2:0]	IF_LEVEL[2:0]	IF_NOTCH	EB22[7:0]	f_{IF} (MHz)
ATSC 6 MHz	100	001	1	0011 0111	3.25
DVB-T 6 MHz	100	001	1	0011 0111	3.30
DVB-T 7 MHz	100	001	1	0011 0111	3.50
DVB-T 8 MHz	101	001	1	0011 0111	4.00
QAM 6 MHz	101	001	1	0011 0111	4
QAM 8 MHz	111	001	1	0011 0111	5

[1] Digital standard settings may vary, depending on channel decoder used.

Table 42. BP_FILTER_map

$f_{RF(max)}$ (kHz)	BP_FILTER[2:0]
180000	101
865000	110

Table 43. RF_BAND_map

$f_{RF(max)}$ (kHz)	RF_BAND [2:0]	Used in flowchart							RF1_ default (kHz)	RF2_ default (kHz)	RF3_ default (kHz)
		RF_A1	RF_B1	RF_A2	RF_B2	RF1	RF2	RF3			
203500	100	RF_A1_4	RF_B1_4	RF_A2_4	RF_B2_4	RF1_4	0	0	186250	0	0
457800	101	RF_A1_5	RF_B1_5	RF_A2_5	RF_B2_5	RF1_5	RF2_5	RF3_5	230000	345000	426000
865000	110	RF_A1_6	RF_B1_6	RF_A2_6	RF_B2_6	RF1_6	RF2_6	RF3_6	489500	697500	842000

Table 44. KM_map

$f_{RF(max)}$ (kHz)	RFC_K[2:0]	RFC_M[1:0]
350000	011	00
720000	010	01
865000	011	11

Table 45. MAIN_PLL_map

$f_{LO(max)}$ (kHz)	MAIN_POST_DIV[6:0]	Div[1]
180500	33h	2Ch
198750	32h	28h
220750	31h	24h
248500	30h	20h
265000	27h	1Eh
284000	26h	1Ch
305500	25h	1Ah
331000	24h	18h
361000	23h	16h
397500	22h	14h
441500	21h	12h
497000	20h	10h
530000	17h	0Fh
568000	16h	0Eh
611000	15h	0Dh
662000	14h	0Ch
722000	13h	0Bh
795000	12h	0Ah
883000	11h	09h
994000	10h	08h

[1] Used in Section 9.4.13 “Flowchart TDA18211CalcMAINPLL”.

Table 46. CAL_PLL_map

$f_{LO(max)}$ (kHz)	CAL_POST_DIV[7:0]	Div[1]
175750	BAh	28h
195250	B9h	24h
219750	B8h	20h
251250	B3h	1Ch
270500	ADh	1Ah
293000	ACh	18h
319500	ABh	16h
351500	AAh	14h
390500	A9h	12h
439500	A8h	10h
502500	A3h	0Eh
541000	9Dh	0Dh
586000	9Ch	0Ch
639000	9Bh	0Bh
703000	9Ah	0Ah
781000	99h	09h
879000	98h	08h

[1] Used in Section 9.4.14 “Flowchart TDA18211CalcCALPLL”.

Table 47. GAIN_TAPER_map

$f_{RF(max)}$ (kHz)	$f_{RF(max)}$ (kHz)	$f_{RF(max)}$ (kHz)	GAIN_TAPER[4:0][1]
-	-	476300	19h
-	-	494800	18h
-	-	513300	17h
175800	-	531800	16h
181300	-	550300	15h
186900	216200	568900	14h
192400	228900	587400	13h
198000	241600	605900	12h
203500	254400	624400	11h
-	267100	642900	10h
-	279800	661400	0Fh
-	292500	679900	0Eh
-	305200	698400	0Dh
-	317900	716900	0Ch
-	330700	735400	0Bh
-	343400	753900	0Ah
-	356100	772500	09h
-	368800	791000	08h
-	381500	809500	07h
-	394200	828000	06h

Table 47. GAIN_TAPER_map *...continued*

$f_{RF(max)}$ (kHz)	$f_{RF(max)}$ (kHz)	$f_{RF(max)}$ (kHz)	GAIN_TAPER[4:0][1]
-	406900	846500	05h
-	419700	865000	04h
-	432400	-	03h
-	445100	-	02h
-	457800	-	01h
-	-	-	00h

[1] The gain taper function compensates for any systematic RF gain ripple and makes it flat versus frequency.

Table 48. RF_CAL_DC_OVER_DT_map

$f_{RF(max)}$ (kHz)	dCoverdT[1]	$f_{RF(max)}$ (kHz)	dCoverdT[1]	$f_{RF(max)}$ (kHz)	dCoverdT[1]	$f_{RF(max)}$ (kHz)	dCoverdT[1]
203500	32h	417000	2Eh	524000	1Eh	774000	40h
353000	19h	419000	2Fh	534000	1Fh	779000	41h
356000	1Ah	422000	30h	549000	20h	784000	43h
359000	1Bh	424000	31h	554000	22h	789000	46h
363000	1Ch	427000	32h	584000	24h	794000	48h
366000	1Dh	429000	33h	589000	26h	799000	4Bh
369000	1Eh	432000	34h	658000	27h	804000	4Fh
373000	1Fh	434000	35h	664000	2Ch	809000	54h
376000	20h	437000	36h	669000	2Dh	814000	59h
379000	21h	439000	37h	699000	2Eh	819000	5Dh
383000	22h	442000	38h	704000	30h	824000	61h
386000	23h	444000	39h	709000	31h	829000	68h
389000	24h	447000	3Ah	714000	32h	834000	6Eh
393000	25h	449000	3Bh	724000	33h	839000	75h
396000	26h	457800	3Ch	729000	36h	844000	7Eh
399000	27h	465000	0Fh	739000	38h	849000	82h
402000	28h	477000	12h	744000	39h	854000	84h
404000	29h	483000	14h	749000	3Bh	859000	8Fh
407000	2Ah	502000	19h	754000	3Ch	865000	9Ah
409000	2Bh	508000	1Bh	759000	3Dh	-	-
412000	2Ch	519000	1Ch	764000	3Eh	-	-
414000	2Dh	522000	1Dh	769000	3Fh	-	-

[1] Used in flowcharts.

Table 49. RF_CAL_map

$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table
174000	18h	267000	29h	384000	5Fh	473000	14h	662000	4Ah	779000	80h
175000	1Ah	269000	2Ah	385000	60h	474000	15h	665000	4Bh	781000	81h
176000	1Bh	271000	2Bh	386000	61h	481000	16h	667000	4Ch	783000	82h
178000	1Dh	273000	2Ch	388000	62h	486000	17h	670000	4Dh	784000	83h
179000	1Eh	275000	2Dh	390000	63h	491000	18h	673000	4Eh	785000	84h
180000	1Fh	277000	2Eh	393000	64h	498000	19h	676000	4Fh	786000	85h
181000	20h	279000	2Fh	394000	65h	499000	1Ah	677000	50h	793000	86h
182000	21h	282000	30h	396000	66h	501000	1Bh	681000	51h	794000	87h
183000	22h	284000	31h	397000	67h	506000	1Ch	683000	52h	795000	88h
184000	24h	286000	32h	398000	68h	511000	1Dh	686000	53h	797000	89h
185000	25h	287000	33h	400000	69h	516000	1Eh	688000	54h	799000	8Ah
186000	26h	290000	34h	402000	6Ah	520000	1Fh	689000	55h	801000	8Bh
187000	27h	293000	35h	403000	6Bh	521000	20h	691000	56h	802000	8Ch
188000	29h	295000	36h	407000	6Ch	525000	21h	695000	57h	803000	8Dh
189000	2Ah	297000	37h	408000	6Dh	529000	22h	698000	58h	804000	8Eh
190000	2Ch	300000	38h	409000	6Eh	533000	23h	703000	59h	810000	90h
191000	2Dh	303000	39h	410000	6Fh	539000	24h	704000	5Ah	811000	91h
192000	2Eh	305000	3Ah	411000	70h	541000	25h	705000	5Bh	812000	92h
193000	2Fh	306000	3Bh	412000	71h	547000	26h	707000	5Ch	814000	93h
194000	30h	307000	3Ch	413000	72h	549000	27h	710000	5Dh	816000	94h
195000	33h	310000	3Dh	414000	73h	551000	28	712000	5Eh	817000	96h
196000	35h	312000	3Eh	417000	74h	556000	29h	717000	5Fh	818000	97h
198000	36h	315000	3Fh	418000	75h	561000	2Ah	718000	60h	820000	98h
200000	38h	318000	40h	420000	76h	563000	2Bh	721000	61h	821000	99h
201000	3Ch	320000	41h	422000	77h	565000	2Ch	722000	62h	822000	9Ah
202000	3Dh	323000	42h	423000	78h	569000	2Dh	723000	63h	828000	9Bh
203500	3Eh	324000	43h	424000	79h	571000	2Eh	725000	64h	829000	9Dh
206000	0Eh	325000	44h	427000	7Ah	577000	2Fh	727000	65h	830000	9Fh
208000	0Fh	327000	45h	428000	7Bh	580000	30h	730000	66h	831000	A0h
212000	10h	331000	46h	429000	7Dh	582000	31h	732000	67h	833000	A1h
216000	11h	334000	47h	432000	7Fh	584000	32h	735000	68h	835000	A2h
217000	12h	337000	48h	434000	80h	588000	33h	740000	69h	836000	A3h
218000	13h	339000	49h	435000	81h	591000	34h	741000	6Ah	837000	A4h
220000	14h	340000	4Ah	436000	83h	596000	35h	742000	6Bh	838000	A6h
222000	15h	341000	4Bh	437000	84h	598000	36h	743000	6Ch	840000	A8h
225000	16h	343000	4Ch	438000	85h	603000	37h	745000	6Dh	842000	A9h
228000	17h	345000	4Dh	439000	86h	604000	38h	747000	6Eh	845000	AAh
231000	18h	349000	4Eh	440000	87h	606000	39h	748000	6Fh	846000	ABh
234000	19h	352000	4Fh	441000	88h	612000	3Ah	750000	70h	847000	ADh
235000	1Ah	353000	50h	442000	89h	615000	3Bh	752000	71h	848000	AEh

Table 49. RF_CAL_map *…continued*

$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table	$f_{RF(max)}$ (kHz)	Cprog_ table
236000	1Bh	355000	51h	445000	8Ah	617000	3Ch	754000	72h	852000	AFh
237000	1Ch	357000	52h	446000	8Bh	621000	3Dh	757000	73h	853000	B0h
240000	1Dh	359000	53h	447000	8Ch	622000	3Eh	758000	74h	858000	B1h
242000	1Eh	361000	54h	448000	8Eh	625000	3Fh	760000	75h	860000	B2h
244000	1Fh	362000	55h	449000	8Fh	632000	40h	763000	76h	861000	B3h
247000	20h	364000	56h	450000	90h	633000	41h	764000	77h	862000	B4h
249000	21h	368000	57h	452000	91h	634000	42h	766000	78h	863000	B6h
252000	22h	370000	58h	453000	93h	642000	43h	767000	79h	864000	B8h
253000	23h	372000	59h	454000	94h	643000	44h	768000	7Ah	865000	B9h
254000	24h	375000	5Ah	456000	96h	647000	45h	773000	7Bh	-	-
256000	25h	376000	5Bh	457800	98h	650000	46h	774000	7Ch	-	-
259000	26h	377000	5Ch	461000	11h	652000	47h	776000	7Dh	-	-
262000	27h	379000	5Dh	468000	12h	657000	48h	777000	7Eh	-	-
264000	28h	382000	5Eh	472000	13h	661000	49h	778000	7Fh	-	-

Table 50. THERMOMETER_map[1]

TM_D[3:0]	TMVALUE (die temperature)	
	TM_RANGE = 0	TM_RANGE = 1
0000	60 °C	92 °C
0001	62 °C	94 °C
0010	66 °C	98 °C
0011	64 °C	96 °C
0100	74 °C	106 °C
0101	72 °C	104 °C
0110	68 °C	100 °C
0111	70 °C	102 °C
1000	90 °C	122 °C
1001	88 °C	120 °C
1010	84 °C	116 °C
1011	86 °C	118 °C
1100	76 °C	108 °C
1101	78 °C	110 °C
1110	82 °C	114 °C
1111	80 °C	112 °C

[1] Bit TM_ON must be set to logic 1.

Table 51. IR_MEAS_map

$f_{RF(max)}$ (kHz)	IR_MEAS[2:0]
200	101
600	110
865	111

Table 52. CID_TARGET_map

$f_{RF(max)}$	CID_Target	count_limit
186250	10	4000
230000	10	4000
345000	24	4000
426000	14	4000
489500	30	4000
697500	50	4000
842000	58	4000

10. Internal circuitry

Table 53. Internal circuits

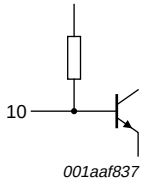
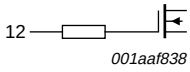
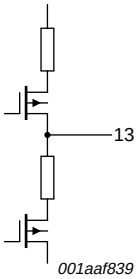
Symbol	Pin	Description[1]	Average DC voltage
RF_IN	10		0.8 V
CAPRFAGC	12		2.8 V
LT	13		0.85 V

Table 53. Internal circuits *...continued*

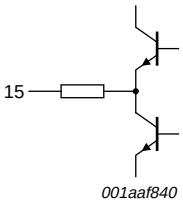
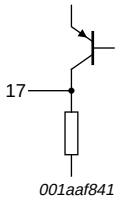
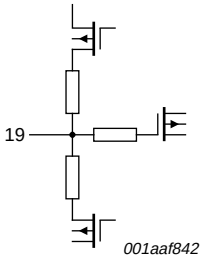
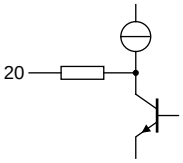
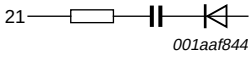
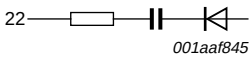
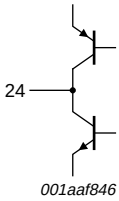
Symbol	Pin	Description[1]	Average DC voltage
STO	15		0.85 V
CAPREGVCO	17		2.8 V (Normal mode) 0 V (Standby mode)
MASTERSYNC	19		$0.5 \times V_{CC}$
CAPFILTVCO	20		1.6 V (Normal mode) 0 V (Standby mode)
VT_COARSE	21		$0.5 \times V_{CC}$
VT_FINE	22		$0.5 \times V_{CC}$
CP_LO	24		$0.5 \times V_{CC}$

Table 53. Internal circuits *...continued*

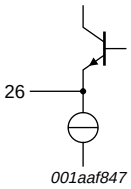
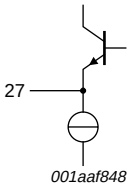
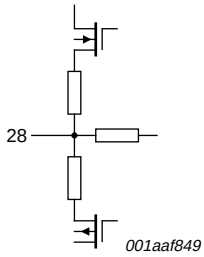
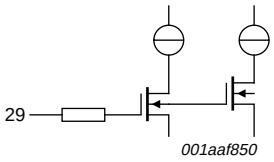
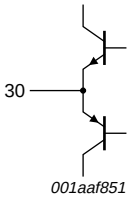
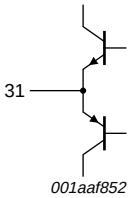
Symbol	Pin	Description[1]	Average DC voltage
XTALP	26		1.45 V
XTALN	27		1.45 V
FREEZE	28		3.3 V
XTOUT_MS	29		high-Z
XTOUTP	30		2.4 V
XTOUTN	31		2.4 V

Table 53. Internal circuits *...continued*

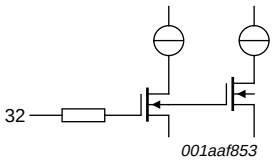
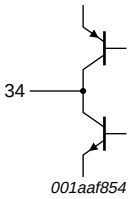
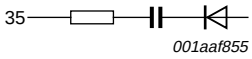
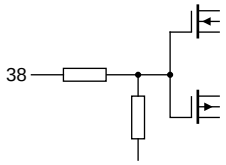
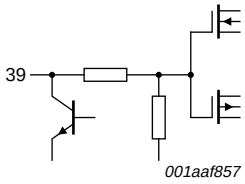
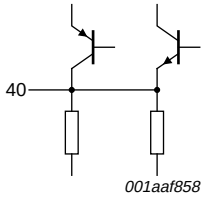
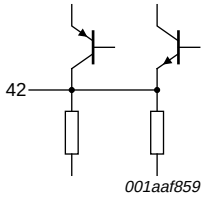
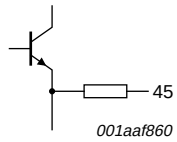
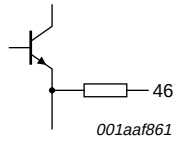
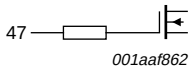
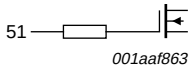
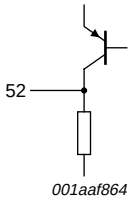
Symbol	Pin	Description[1]	Average DC voltage
AS	32		high-Z
CP_CAL	34		3.3 V (Normal mode) 0.5 × V_{CC} (Calibration mode)
VT_CAL	35		3.3 V (Normal mode) 0.5 × V_{CC} (Calibration mode)
SCL	38		high-Z
SDA	39		high-Z
CAPREG18	40		1.8 V (Normal mode) 2.0 V (Sleep mode)
CAPREG28	42		2.8 V (Normal mode) 2.4 V (Sleep mode)

Table 53. Internal circuits *...continued*

Symbol	Pin	Description[1]	Average DC voltage
IFOUTN	45		1.35 V
IFOUTP	46		1.35 V
V_IFAGC	47		high-Z
VSYNC	51		high-Z
CAPREGFILTRF	52		2.8 V (Normal mode) 0 V (Sleep mode)

[1] ESD protection components are not shown.

11. Limiting values

Table 54. Limiting values[1]

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+3.6	V
V_I	input voltage	pins SDA and SCL	–0.3	+5.5	V
		all other pins			
		V_{CC} < 3.3 V	–0.3	V_{CC} + 0.3	V
		V_{CC} > 3.3 V	–0.3	+3.6	V
T_{stg}	storage temperature		–40	+150	°C
T_j	junction temperature		-	110	°C
V_{esd}	electrostatic discharge voltage	EIA/JESD22-A114 (human body model)	±2000	-	V
		EIA/JESD22-A115 (machine model)	±200	-	V

[1] The TDA18211HD withstands the latch-up specifications of JEDEC (JESD78A), with the specific recommendation using coupling capacitors on pins RF_IN, LT, STO, XTOUTP and XTOUTN.

12. Thermal characteristics

Table 55. Thermal characteristics[1]

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	according to JEDEC specification	19.6	K/W

[1] The junction temperature can be obtained with the formula $T_j = T_{amb} + R_{th(j-a)} \times V_{CC} \times I_{CC}$, where $R_{th(j-a)}$ is the thermal resistance of the application. $R_{th(j-a)}$ must be such that the resulting T_j does not exceed the maximum value defined in Table 54.

13. Characteristics

All data in this section refers to Master mode operation.

Table 56. Loop-through characteristics (RF input to loop-through output)

T_{amb} = 25 °C; V_{CC} = 3.3 V; for test circuit see Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{RF(lt)}$	loop-through RF frequency	center of channel		45	-	864	MHz
VSWR	voltage standing wave ratio	loop-through output; 75 Ω nominal impedance		-	-	3	-
$G_{v(lt)}$	loop-through voltage gain	75 Ω load		-	1.5	-	dB
ΔG_{lt}	loop-through gain variation	in the RF frequency range; 75 Ω load		-	3	-	dB
NF_{lt}	loop-through noise figure	Normal mode		-	5.5	-	dB
CSO	composite second-order distortion		[1]	-	–60	-	dBc
CTB	composite triple beat		[1]	-	–63	-	dBc
$\alpha_{isol(bp)}$	bypass isolation	from loop-through output to RF input		-	24	-	dB
$V_{L(tun-lto)}$	leakage voltage between tuner and loop-through output	in RF TV band		-	10	-	dBµV

[1] Channel loading assumptions: 129 channels (NTSC 129 frequency plan) at 75 dBµV.

Table 57. Slave tuner output characteristics (pin STO)

T_{amb} = 25 °C; V_{CC} = 3.3 V; for test circuit see Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{RF(STO)}$	RF frequency on pin STO		45	-	864	MHz
$Z_{o(STO)}$	output impedance on pin STO		30	35	40	Ω
$G_{v(STO)}$	voltage gain on pin STO	75 Ω source resistance on RF input; Z_i = 35 Ω (75 Ω, VSWR = 2)				
		POWER_LEVEL[6:5] = 00	-	6	-	dB
		POWER_LEVEL[6:5] = 01	-	9	-	dB
		POWER_LEVEL[6:5] = 10	-	12	-	dB
		POWER_LEVEL[6:5] = 11	-	15	-	dB

Table 58. General characteristics for TV reception (RF input to IF output)

T_{amb} = 25 °C; V_{CC} = 3.3 V; IF output level option = 2 V (p-p); IF output load = 1 kΩ on each terminal; for test circuit see Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{CC}	supply voltage		3.13	3.30	3.47	V
I_{CC}	supply current	Normal mode	180	235	290	mA
		Standby mode with loop-through and crystal oscillator on (default at POR)	40	51	65	mA
		Standby mode with only crystal oscillator on	10	15	20	mA
		Device off mode	1	2	5	mA
P	power dissipation		-	780	-	mW
T_{amb}	ambient temperature		0	-	70	°C
Input						
f_{RF}	RF frequency	center of channel	174	-	864	MHz
VSWR	voltage standing wave ratio	RF input; 75 Ω nominal impedance	-	2	3	-
NF_{tun}	tuner noise figure	maximum gain	-	5.5	6	dB
$G_{v(tun)max}$	maximum tuner voltage gain	2 V (p-p) IF output selection	71	83	90	dB
$\Delta G_{AGC(tun)}$	tuner AGC gain range		68	71	80	dB
$V_{i(max)}$	maximum input voltage	1 dB gain compression, one analog TV signal at RF input (–5 dBm)	-	103	-	dBµV
$V_{L(tun-RF)}$	leakage voltage between tuner and RF	at RF input; in RF band	-	0	-	dBµV

Table 58. General characteristics for TV reception (RF input to IF output) *...continued*

T_{amb} = 25 °C; V_{CC} = 3.3 V; IF output level option = 2 V (p-p); IF output load = 1 kΩ on each terminal; for test circuit see Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output						
$V_{o(IF)dif(p-p)}$	peak-to-peak differential IF output voltage	IF_LEVEL[2:0] = 000	-	2	-	V
		IF_LEVEL[2:0] = 001	-	1.25	-	V
		IF_LEVEL[2:0] = 010	-	1	-	V
		IF_LEVEL[2:0] = 111	-	0.5	-	V
$Z_{o(IF)}$	IF output impedance	differential mode; magnitude value	-	100	-	Ω
$\Delta G_{AGC(IF)}$	IF AGC GAIN range	2 V (p-p) IF output voltage selection	-	30	-	dB
G_{tlt}	tilt gain	RF frequency range; 6/7/8 MHz channel	-	2	4	dB
$f_{IF(stpb)lp}$	low-pass stop-band IF frequency	60 dB attenuation				
		6 MHz IF filter	-	14	-	MHz
		7 MHz IF filter	-	16	-	MHz
		8 MHz IF filter	-	18	-	MHz
α_{image}	image rejection		53	65	-	dB
t_{ripple}	ripple time	digital TV; difference between f_1 and f_2 in digital channel				
		ATSC 6 MHz; f_1 = 0.75 MHz; f_2 = 5.75 MHz	-	395	-	ns
		DVB-T 6 MHz; f_1 = 0.8 MHz and f_2 = 5.8 MHz	-	365	-	ns
		DVB-T 7 MHz; f_1 = 0.5 MHz and f_2 = 6.5 MHz	-	478	-	ns
		DVB-T 8 MHz; f_1 = 0.5 MHz and f_2 = 7.5 MHz	-	515	-	ns
		QAM 6 MHz; f_1 = 1.5 MHz and f_2 = 6.5 MHz	-	155	-	ns
		QAM 8 MHz; f_1 = 1.5 MHz and f_2 = 8.5 MHz	-	180	-	ns
φ_n	phase noise	1 kHz and 10 kHz, details see Figure 23	-	–89	-	dBc/Hz
α_{IF}	IF rejection	9 MHz Low-pass filter			-	
		13.75 MHz	35	42		dB
		18 MHz	56	66		dB
Various						
$t_{startup(tun)}$	tuner start-up time	at power-up	-	1.5	-	s
t_{set}	setting time	PLL setting time; channel change	-	-	5	ms
S_{dig}	digital sensitivity	DVB-T (64 QAM 2/3); BER = 2.10^{-4} [1]	-	–82	-	dBm

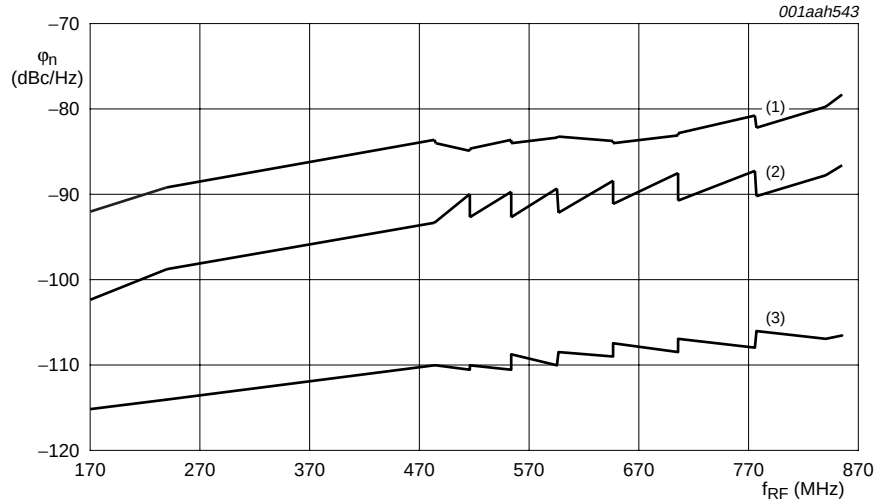
[1] Measured with TDA10048HN channel decoder.

Table 59. Characteristics of terminals

T_{amb} = 25 °C; V_{CC} = 3.3 V; 2.2 nF on input pin V_IFAGC; for test circuit see Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IF AGC input: pin V_IFAGC						
V_{AGC}	AGC voltage		0	-	V_{CC}	V
Z_i	input impedance		-	high-Z	-	Ω
dG_{AGC}/dV	rate of change of AGC gain with voltage		-	30	55	dB/V
Crystal oscillator						
f_{xtal}	crystal frequency		15.99	16	16.01	MHz
Z_i	input impedance	magnitude value	-	500	-	Ω
Crystal oscillator output buffer; pins XTOUTP and XTOUTN						
R_o	output resistance	16 MHz output frequency	-	460	-	Ω
$V_{o(p-p)}$	peak-to-peak output voltage	10 kΩ//10 pF AC load	-	0.4	-	V
SR_r	slew rate of rising signal	10 kΩ//10 pF AC load	-	40	-	V/µs
SR_f	slew rate of falling signal	10 kΩ//10 pF AC load	-	40	-	V/µs
I²C-bus[1]						
Pin SCL						
V_{IL}	LOW-level input voltage	fixed input levels	-	-	1.5	V
		V_{DD} related input levels	-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	fixed input levels	3	-	-	V
		V_{DD} related input levels	$0.7V_{DD}$	-	-	V
f_{SCL}	SCL clock frequency		-	-	400	kHz
Pin SDA						
V_{OH}	HIGH-level output voltage	I_{SDA} = 3 mA (sink current)	-	-	0.4	V
V_{IL}	LOW-level input voltage	fixed input levels	-	-	1.5	V
		V_{DD} related input levels	-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage	fixed input levels	3	-	-	V
		V_{DD} related input levels	$0.7V_{DD}$	-	-	V

[1] Devices that use non-standard supply voltages, which do not conform the intended I²C-bus system levels, must relate their input levels to the supply voltage to which the pull-up resistors are connected.

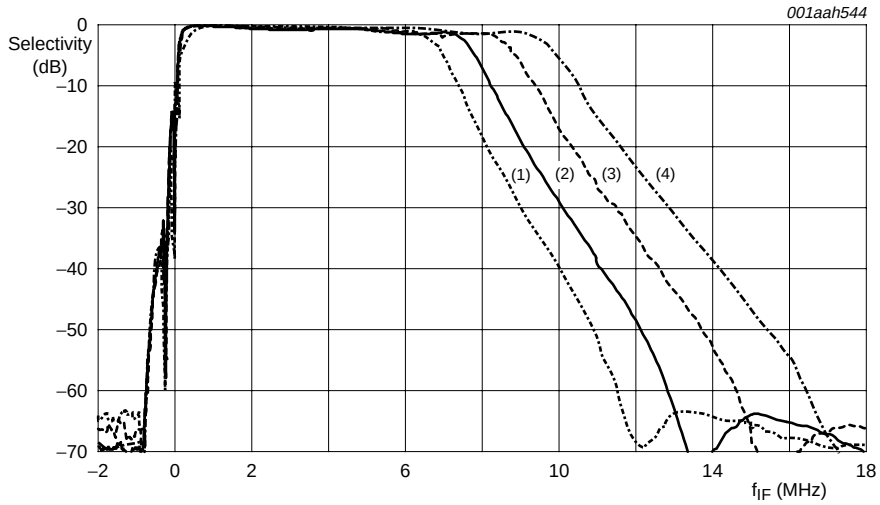


(1) Offset is 1 kHz.

(2) Offset is 10 kHz.

(3) Offset is 100 kHz.

Fig 23. Typical phase noise curve



(1) 6 MHz bandwidth filter.

(2) 7 MHz bandwidth filter.

(3) 8 MHz bandwidth filter.

(4) 9 MHz bandwidth filter.

Fig 24. Typical IF selectivity curves

14. Application information

14.1 Application example

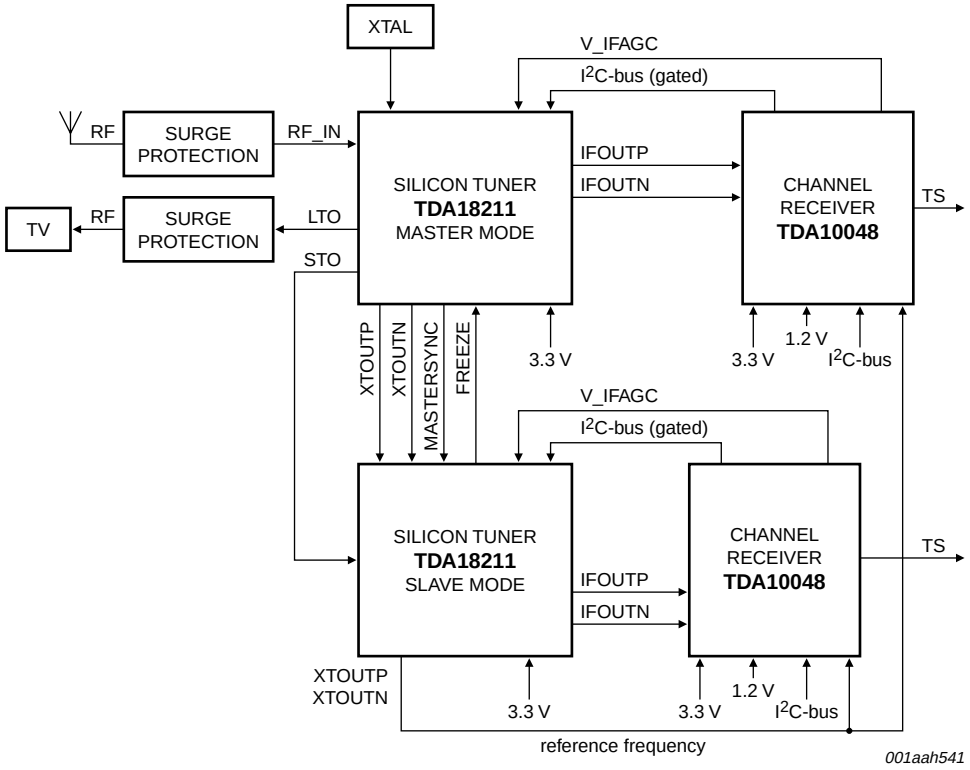


Fig 25. Example for TDA18211HD of DVB-T dual-tuner reception

14.2 Application notes

Please contact the NXP sales office for additional information on dual-tuner DVB-T applications.

15. Test information

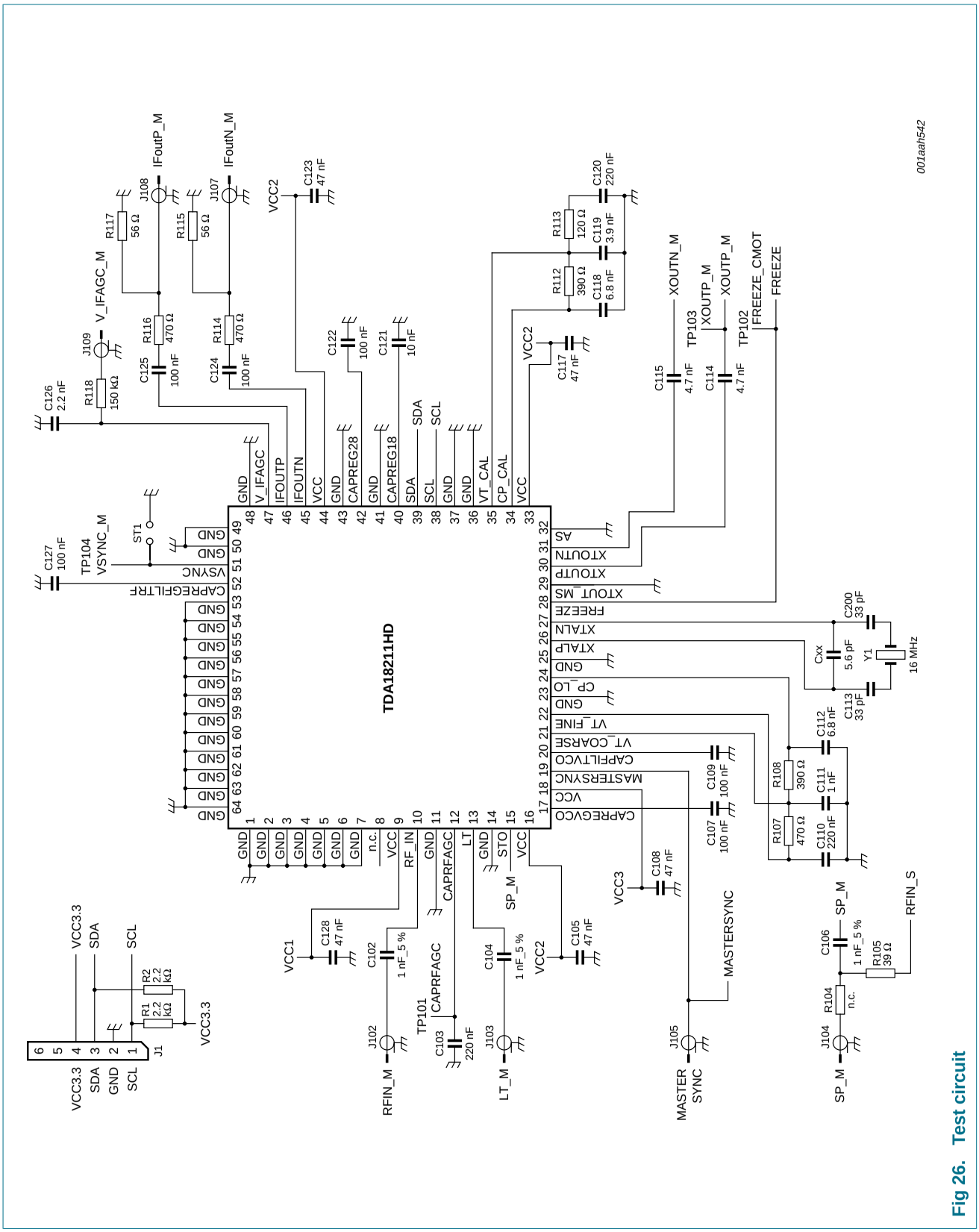
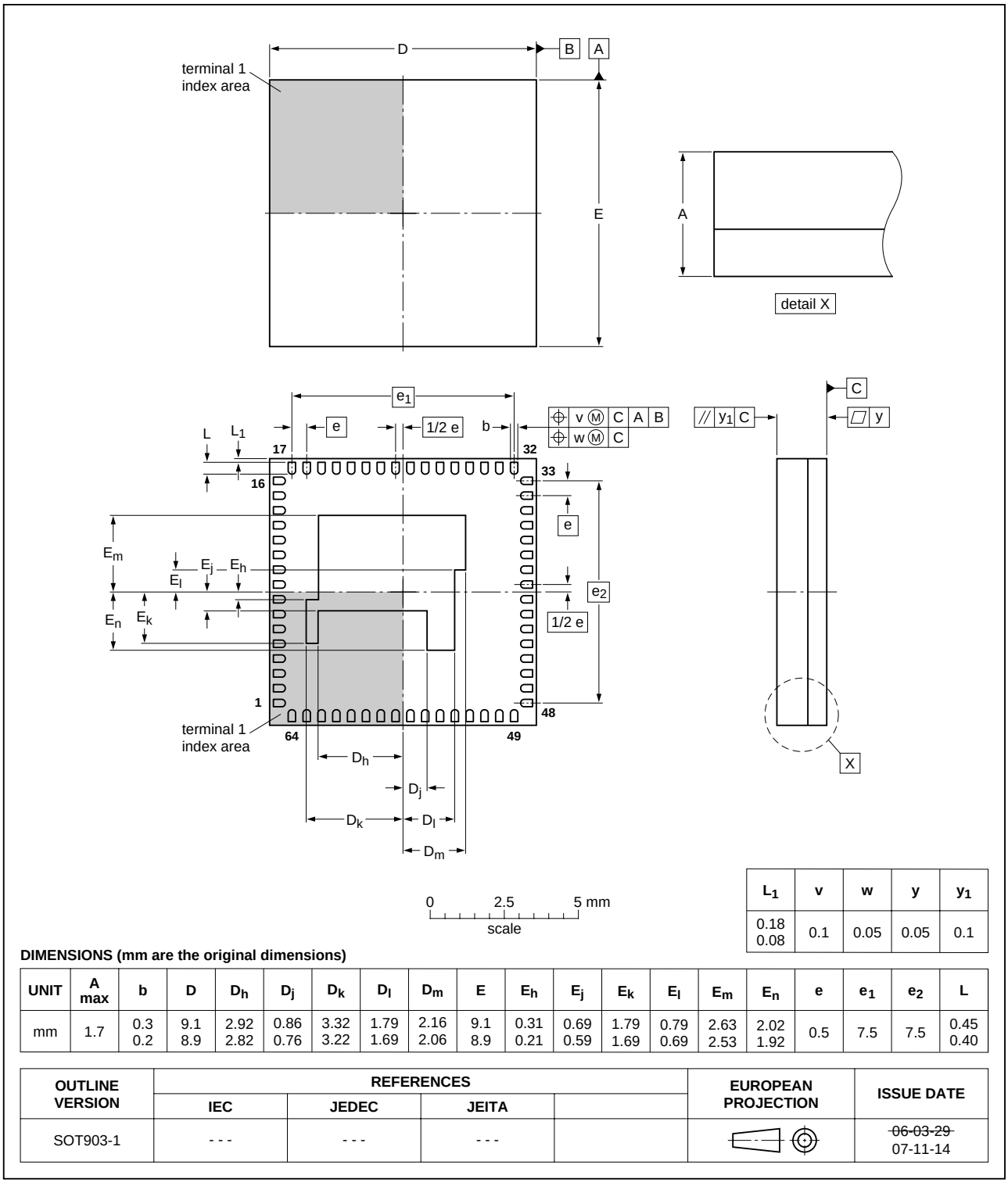


Fig 26. Test circuit

16. Package outline

HLQFN64R; plastic thermal enhanced low profile quad flat package; no leads; 64 terminals; resin based; body 9 × 9 × 1.6 mm **SOT903-1**



L_1	v	w	y	y_1
0.18 0.08	0.1	0.05	0.05	0.1

DIMENSIONS (mm are the original dimensions)

UNIT	A max	b	D	D_h	D_j	D_k	D_l	D_m	E	E_h	E_j	E_k	E_l	E_m	E_n	e	e_1	e_2	L
mm	1.7	0.3 0.2	9.1 8.9	2.92 2.82	0.86 0.76	3.32 3.22	1.79 1.69	2.16 2.06	9.1 8.9	0.31 0.21	0.69 0.59	1.79 1.69	0.79 0.69	2.63 2.53	2.02 1.92	0.5	7.5	7.5	0.45 0.40

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT903-1	- - -	- - -	- - -			~~06-03-29~~ 07-11-14

Fig 27. Package outline SOT903-1 (HLQFN64R)

17. Printed-circuit board

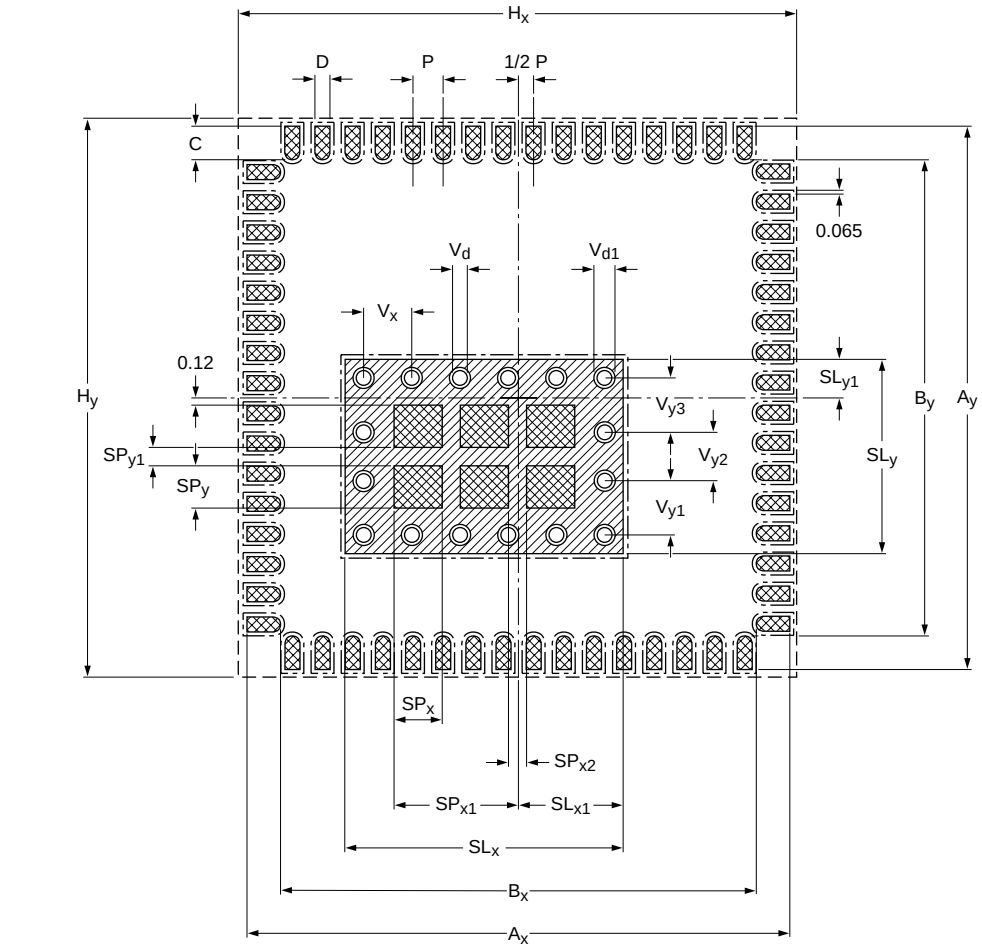
17.1 Reflow profile

See application note *AN10366*.

17.2 Desoldering recommendation

See application notes *AN10366*.

17.3 Footprint layout



SP_{y1}	V_d	V_{d1}	V_x	V_{y1}	V_{y2}	V_{y3}
0.3	0.35	0.5	0.8	0.9	0.8	0.9

DIMENSIONS in mm

P	A_x	A_y	B_x	B_y	C	D	H_x	H_y	SL_x	SL_{x1}	SL_y	SL_{y1}	SP_x	SP_{x1}	SP_{x2}	SP_y
0.500	9.000	9.000	7.880	7.880	0.555	0.250	9.500	9.500	4.610	1.740	3.220	0.640	0.800	2.065	0.3	0.7

Fig 28. Footprint HLQFN64R (SOT903-1)

18. Abbreviations

Table 60. Abbreviations

Acronym	Description
AGC	Automatic Gain Control
DVB-T	Digital Video Broadcasting - Terrestrial
DVR	Digital Video Recorder
ESD	ElectroStatic Discharge
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
PLL	Phase-Lock Loop
QAM	Quadrature Amplitude Modulation
RoHS	Restriction of Hazardous Substances
SAW	Surface Acoustic Wave
STB	Set-Top Box
VCO	Voltage-Controlled Oscillator

19. Revision history

Table 61. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA18211HD_5	20090602	Product data sheet	-	TDA18211HD_4
Modifications:	• Figure 21 “Flowchart TDA18211Read” updated			
TDA18211HD_4	20090505	Product data sheet	-	TDA18211HD_3
TDA18211HD_3	20080304	Product data sheet	-	TDA18211HD_2
TDA18211HD_2	20071121	Product data sheet	-	TDA18211HD_1
TDA18211HD_1	20070802	Product data sheet	-	-

20. Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 2 June 2009
Document identifier: TDA18211HD_5