

TDA1308; TDA1308A

Class-AB stereo headphone driver

Rev. 04 — 25 January 2007

Product data sheet

1. General description

The TDA1308; TDA1308A is an integrated class-AB stereo headphone driver contained in an SO8, DIP8 or a TSSOP8 plastic package. The TDA1308AUK is available in an 8 bump wafer level chip-size package (WLCSP8). The device is fabricated in a 1 μm Complementary Metal Oxide Semiconductor (CMOS) process and has been primarily developed for portable digital audio applications.

The difference between the TDA1308 and the TDA1308A is that the TDA1308A can be used at low supply voltages.

2. Features

- Wide temperature range
- No switch ON/OFF clicks
- Excellent power supply ripple rejection
- Low power consumption
- Short-circuit resistant
- High performance
 - ◆ High signal-to-noise ratio
 - ◆ High slew rate
 - ◆ Low distortion
- Large output voltage swing

3. Quick reference data

Table 1. Quick reference data

$V_{DD} = 5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $f_i = 1\text{ kHz}$; $R_L = 32\ \Omega$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage	TDA1308				
		single supply	3.0	5.0	7.0	V
		dual supply	1.5	2.5	3.5	V
		TDA1308A				
		single supply	2.4	5.0	7.0	V
	dual supply	1.2	2.5	3.5	V	
V_{SS}	negative supply voltage	TDA1308; dual supply	-1.5	-2.5	-3.5	V
		TDA1308A; dual supply	-1.2	-2.5	-3.5	V
I_{DD}	supply current	no load	-	3	5	mA

Table 1. Quick reference data ...continued

$V_{DD} = 5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $f_i = 1\text{ kHz}$; $R_L = 32\text{ }\Omega$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_{tot}	total power dissipation	no load	-	15	25	mW
P_o	maximum output power	(THD + N)/S < 0.1 %	[1] -	40	80	mW
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio		[1] -	0.03	0.06	%
			[1] -	-70	-65	dB
		$R_L = 5\text{ k}\Omega$	[2] -	-92	-89	dB
		$R_L = 5\text{ k}\Omega$	[3] -	-52	-40	dB
		$R_L = 5\text{ k}\Omega$	-	-101	-	dB
S/N	signal-to-noise ratio		100	110	-	dB
α_{cs}	channel separation		-	70	-	dB
		$R_L = 5\text{ k}\Omega$	[1] -	105	-	dB
PSRR	power supply ripple rejection	$f_i = 100\text{ Hz}$; $V_{ripple(p-p)} = 100\text{ mV}$	-	90	-	dB
T_{amb}	ambient temperature		-40	-	+85	$^\circ\text{C}$

[1] $V_{DD} = 5\text{ V}$; $V_{O(p-p)} = 3.5\text{ V}$ (at 0 dB).

[2] $V_{DD} = 2.4\text{ V}$; $V_{O(p-p)} = 1.62\text{ V}$ (at -4.8 dBV); for TDA1308A only.

[3] $V_{DD} = 2.4\text{ V}$; $V_{O(p-p)} = 1.19\text{ V}$ (at -7.96 dBV); for TDA1308A only.

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA1308	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TDA1308T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TDA1308AT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TDA1308AUK	WLCSP8	wafer level chip-size package; 8 bumps; 0.61 × 0.84 × 0.38 mm	TDA1308AUK
TDA1308TT	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

5. Block diagram

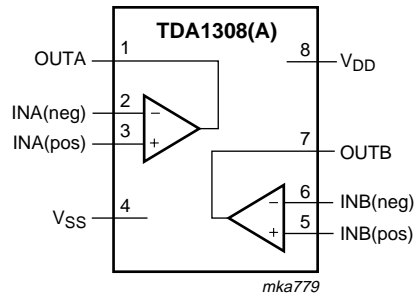


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

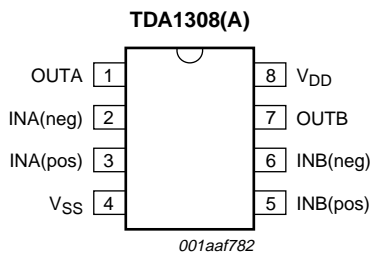


Fig 2. Pin configuration TDA1308(A)

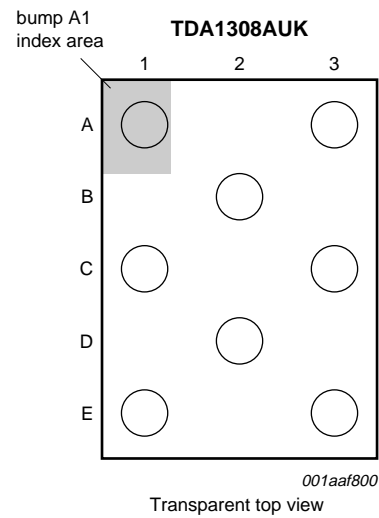


Fig 3. Pin configuration TDA1308AUK

6.2 Pin description

Table 3. Pin description TDA1308(A)

Symbol	Pin	Description
OUTA	1	output A
INA(neg)	2	inverting input A
INA(pos)	3	non-inverting input A
V _{SS}	4	negative supply
INB(pos)	5	non-inverting input B

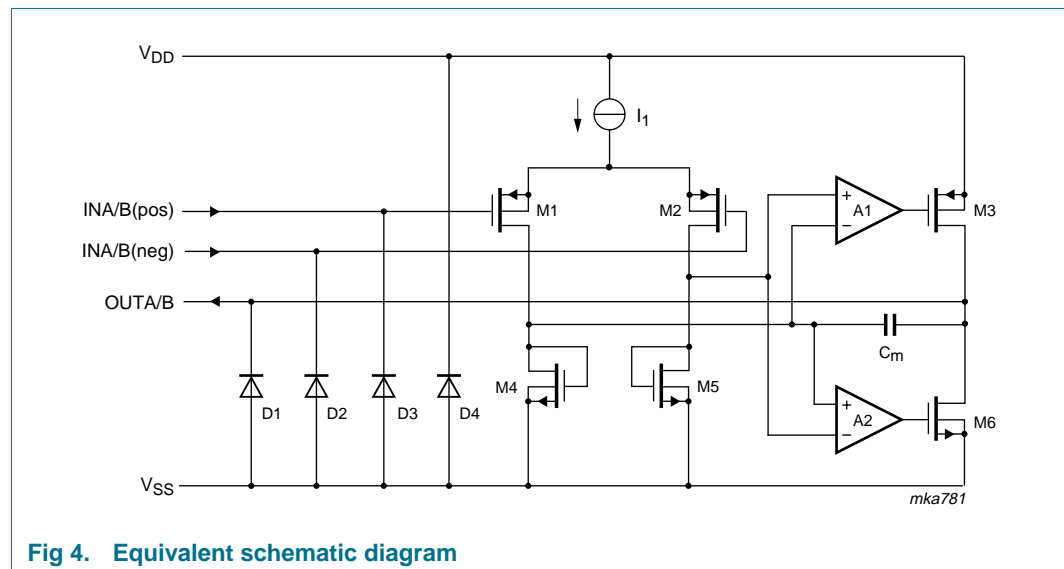
Table 3. Pin description TDA1308(A) ...continued

Symbol	Pin	Description
INB(neg)	6	inverting input B
OUTB	7	output B
V _{DD}	8	positive supply

Table 4. Pin description TDA1308AUK

Symbol	Pin	Description
OUTA	A1	output A
V _{SS}	A3	negative supply
INA(pos)	B2	non-inverting input A
OUTB	C1	output B
INA(neg)	C3	inverting input A
INB(neg)	D2	inverting input B
V _{DD}	E1	positive supply
INB(pos)	E3	non-inverting input B

7. Internal circuitry



8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		0	8.0	V
$t_{SC(O)}$	output short-circuit duration	$T_{amb} = 25\text{ °C};$ $P_{tot} = 1\text{ W}$	20	-	s
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
V_{esd}	electrostatic discharge voltage	HBM	[1] -2	+2	kV
		MM	[2] -200	+200	V

[1] Human body model (HBM): C = 100 pF; R = 1500 Ω ; 3 pulses positive plus 3 pulses negative.

[2] Machine model (MM): C = 200 pF; L = 0.5 mH; R = 0 Ω ; 3 pulses positive plus 3 pulses negative.

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient			
	DIP8		109	K/W
	SO8		210	K/W
	TSSOP8		220	K/W
	WLCSP8		1000	K/W

10. Characteristics

Table 7. Characteristics

$V_{DD} = 5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $f_i = 1\text{ kHz}$; $R_L = 32\text{ }\Omega$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	supply voltage	TDA1308				
		single supply	3.0	5.0	7.0	V
		dual supply	1.5	2.5	3.5	V
		TDA1308A				
		single supply	2.4	5.0	7.0	V
		dual supply	1.2	2.5	3.5	V
V_{SS}	negative supply voltage	TDA1308; dual supply	-1.5	-2.5	-3.5	V
		TDA1308A; dual supply	-1.2	-2.5	-3.5	V
I_{DD}	supply current	no load	-	3	5	mA
P_{tot}	total power dissipation	no load	-	15	25	mW
Static characteristics						
$V_{I(0s)}$	input offset voltage		-	10	-	mV
I_{bias}	input bias current		-	10	-	pA
V_{CM}	common mode voltage		0	-	3.5	pA
G_V	open-loop voltage gain	$R_L = 5\text{ k}\Omega$	-	70	-	dB
I_O	maximum output current		-	60	-	mA
R_O	output resistance	$(THD + N)/S < 0.1\%$	-	0.25	-	Ω
V_O	output voltage swing		[1] 0.75	-	4.25	V
		$R_L = 16\text{ }\Omega$	[1] 1.5	-	3.5	V
		$R_L = 5\text{ k}\Omega$	[1] 0.1	-	4.9	V
α_{cs}	channel separation		-	70	-	dB
		$R_L = 5\text{ k}\Omega$	[1] -	105	-	dB
PSRR	power supply ripple rejection	$f_i = 100\text{ Hz}$; $V_{ripple(p-p)} = 100\text{ mV}$	-	90	-	dB
C_L	load capacitance		-	-	200	pF
Dynamic characteristics						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio		[2] -	0.03	0.06	%
			[2] -	-70	-65	dB
		$R_L = 5\text{ k}\Omega$	[3] -	-92	-89	dB
		$R_L = 5\text{ k}\Omega$	[3] -	-52	-40	dB
		$R_L = 5\text{ k}\Omega$	[3] -	0.25	1.0	%
		$R_L = 5\text{ k}\Omega$	[2] -	-101	-	dB
		$R_L = 5\text{ k}\Omega$	[2] -	0.0009	-	%
S/N	signal-to-noise ratio		100	110	-	dB
f_G	unity gain frequency	open-loop; $R_L = 5\text{ k}\Omega$	-	5.5	-	MHz
P_O	maximum output power	$(THD + N)/S < 0.1\%$	-	40	80	mW

Table 7. Characteristics ...continued

$V_{DD} = 5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $f_i = 1\text{ kHz}$; $R_L = 32\text{ }\Omega$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance		-	3	-	pF
SR	slew rate	unity gain inverting	-	5	-	V/ μs
B	bandwidth	unity gain inverting	-	20	-	kHz

- [1] Values are proportional to V_{DD} ; $(\text{THD} + \text{N})/\text{S} < 0.1\%$.
- [2] $V_{DD} = 5\text{ V}$; $V_{O(p-p)} = 3.5\text{ V}$ (at 0 dB).
- [3] $V_{DD} = 2.4\text{ V}$; $V_{O(p-p)} = 1.19\text{ V}$ (at -7.96 dBV); for TDA1308A only.

11. Application information

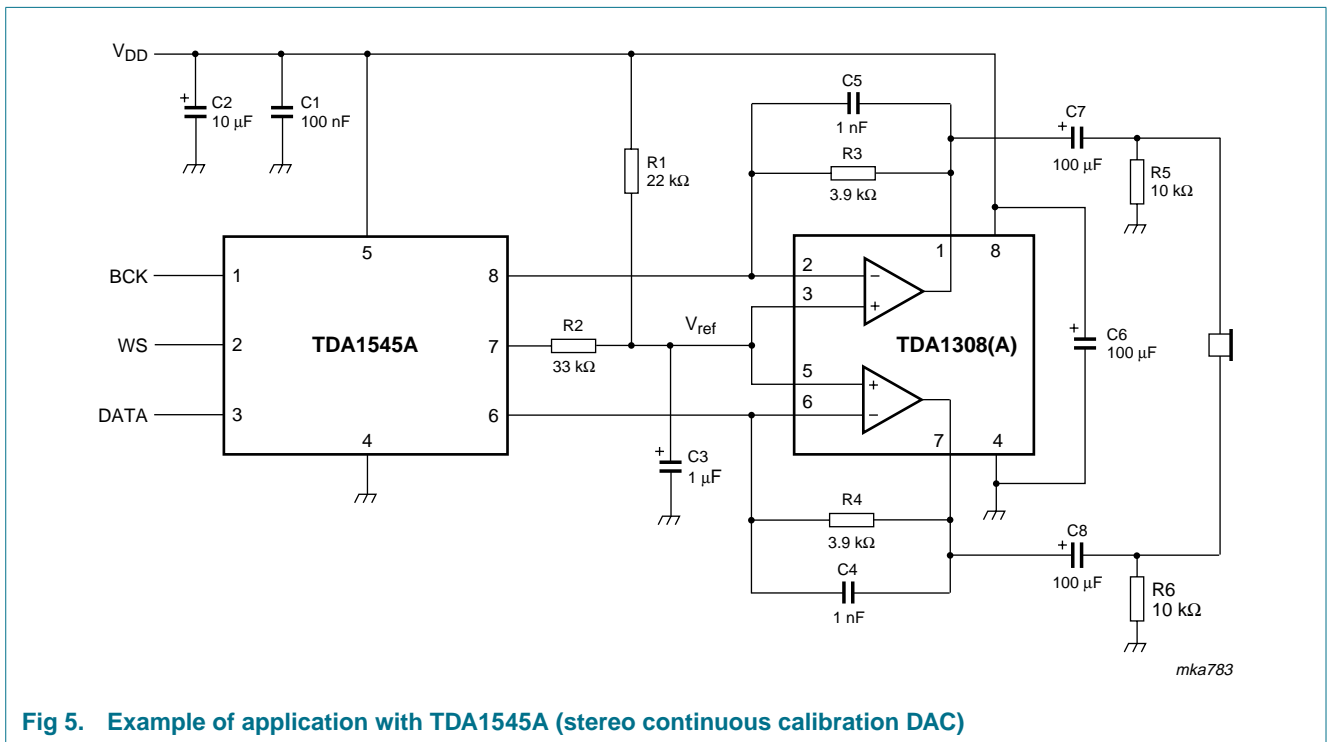


Fig 5. Example of application with TDA1545A (stereo continuous calibration DAC)

12. Test information

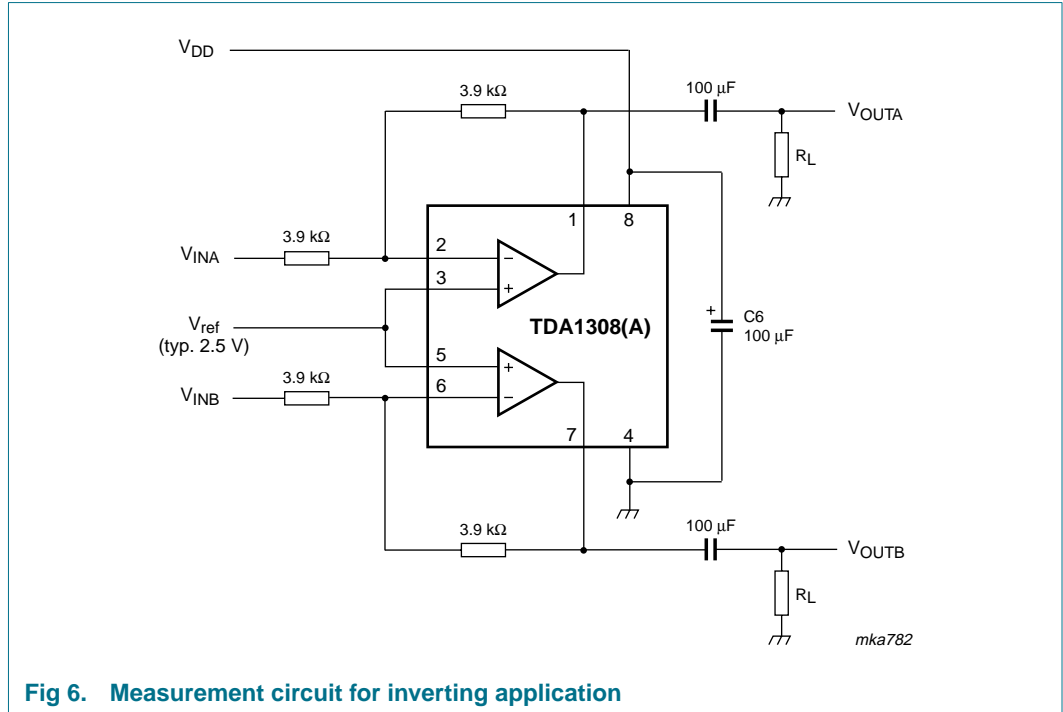


Fig 6. Measurement circuit for inverting application

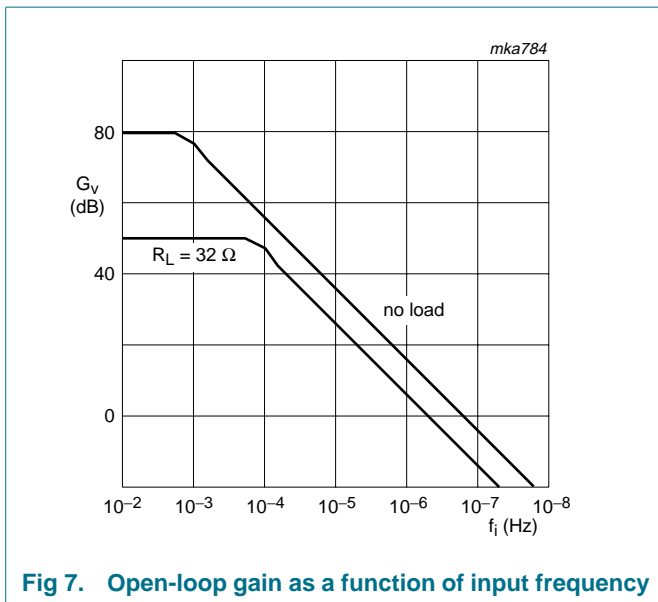


Fig 7. Open-loop gain as a function of input frequency

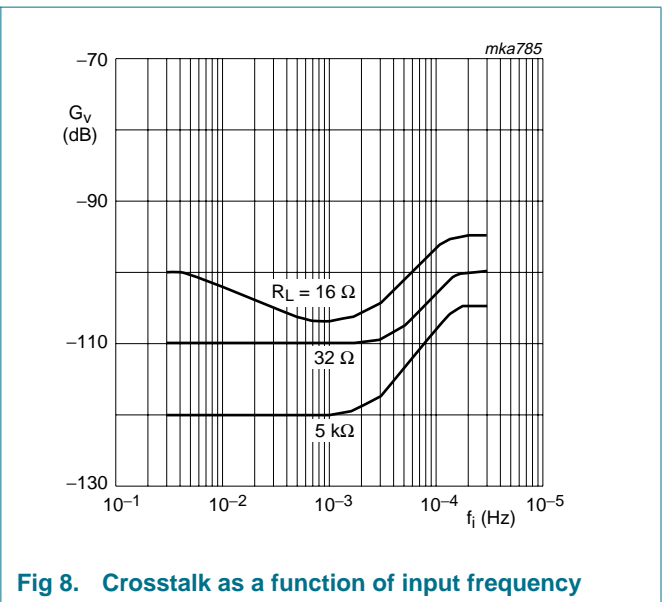


Fig 8. Crosstalk as a function of input frequency

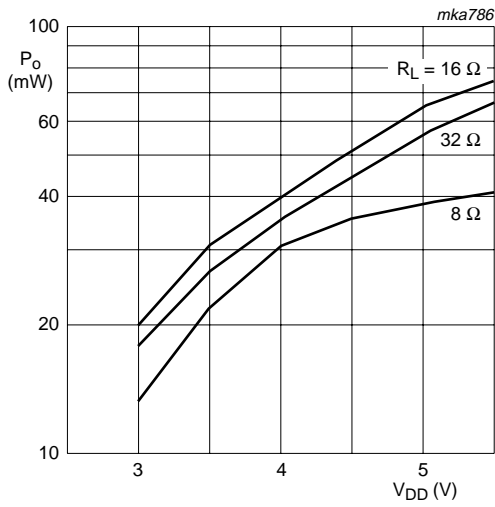


Fig 9. Output power as a function of supply voltage

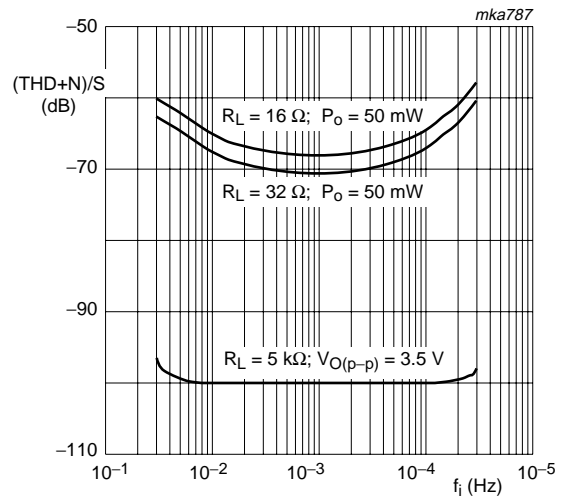


Fig 10. Total harmonic distortion plus noise-to-signal ratio as a function of input frequency

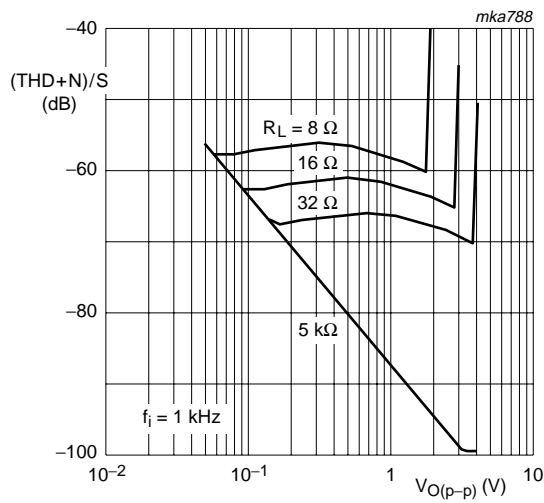


Fig 11. Total harmonic distortion plus noise-to-signal ratio as a function of output voltage level

12.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

13. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1

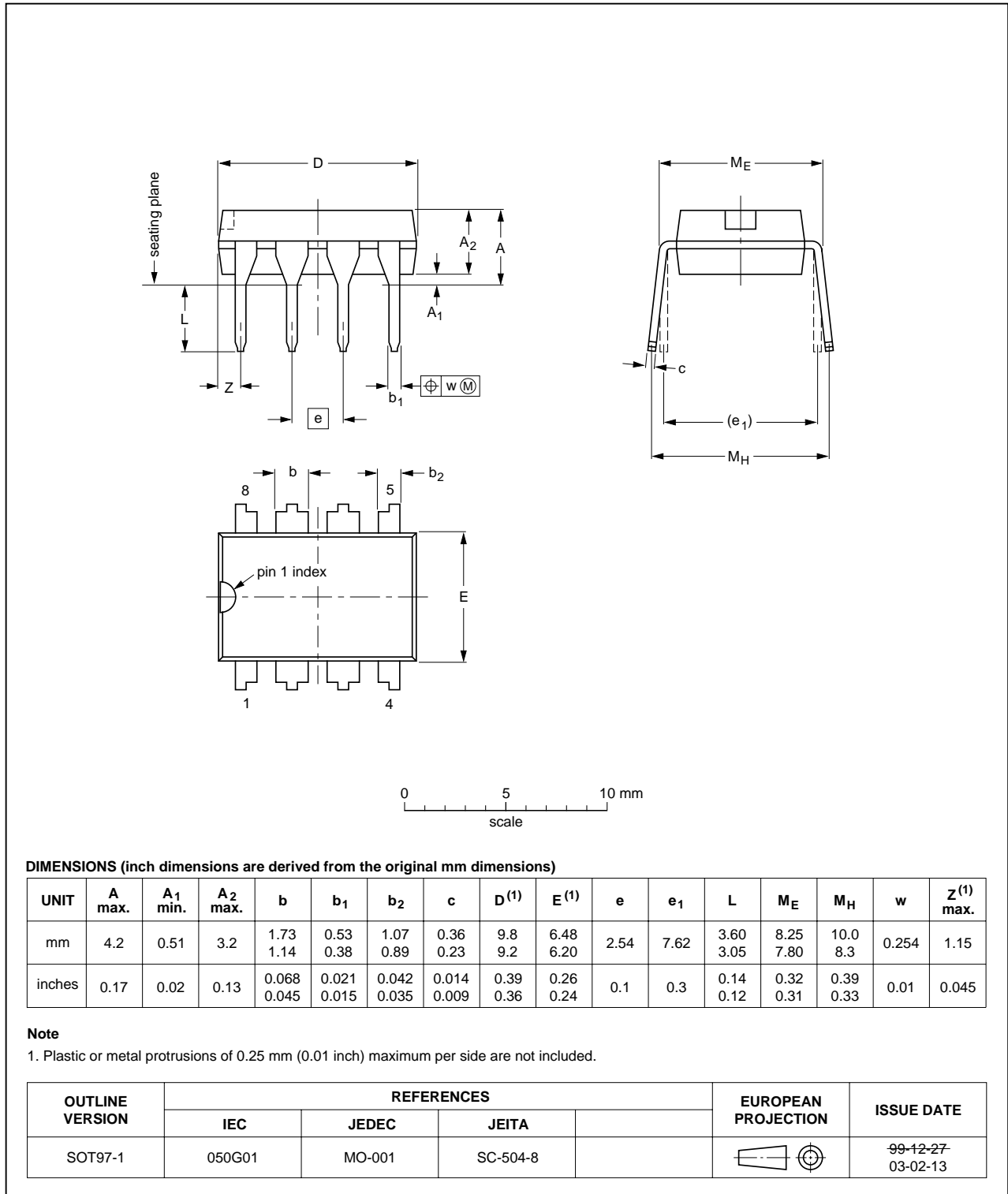


Fig 12. Package outline SOT97-1 (DIP8)

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

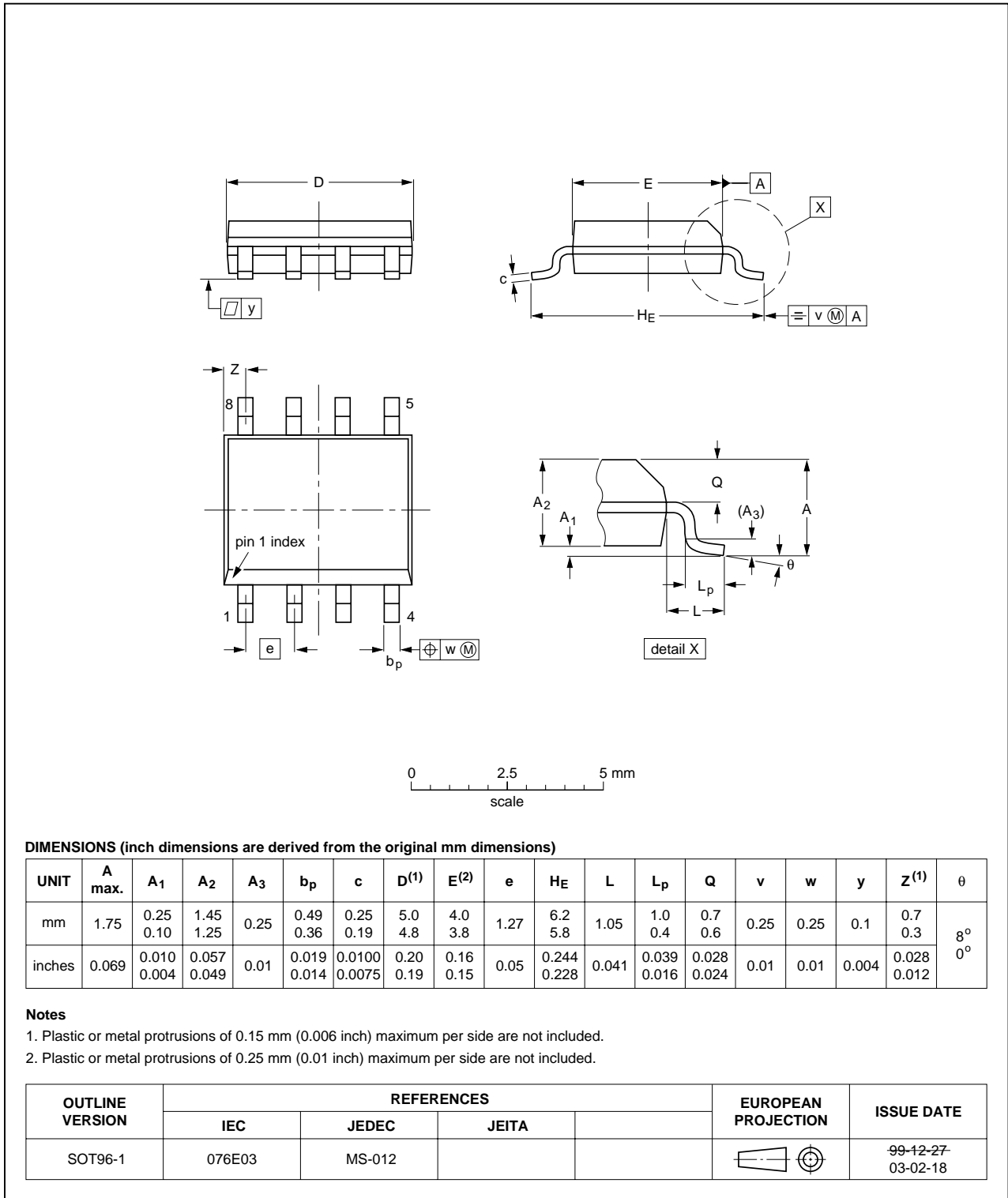


Fig 13. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1

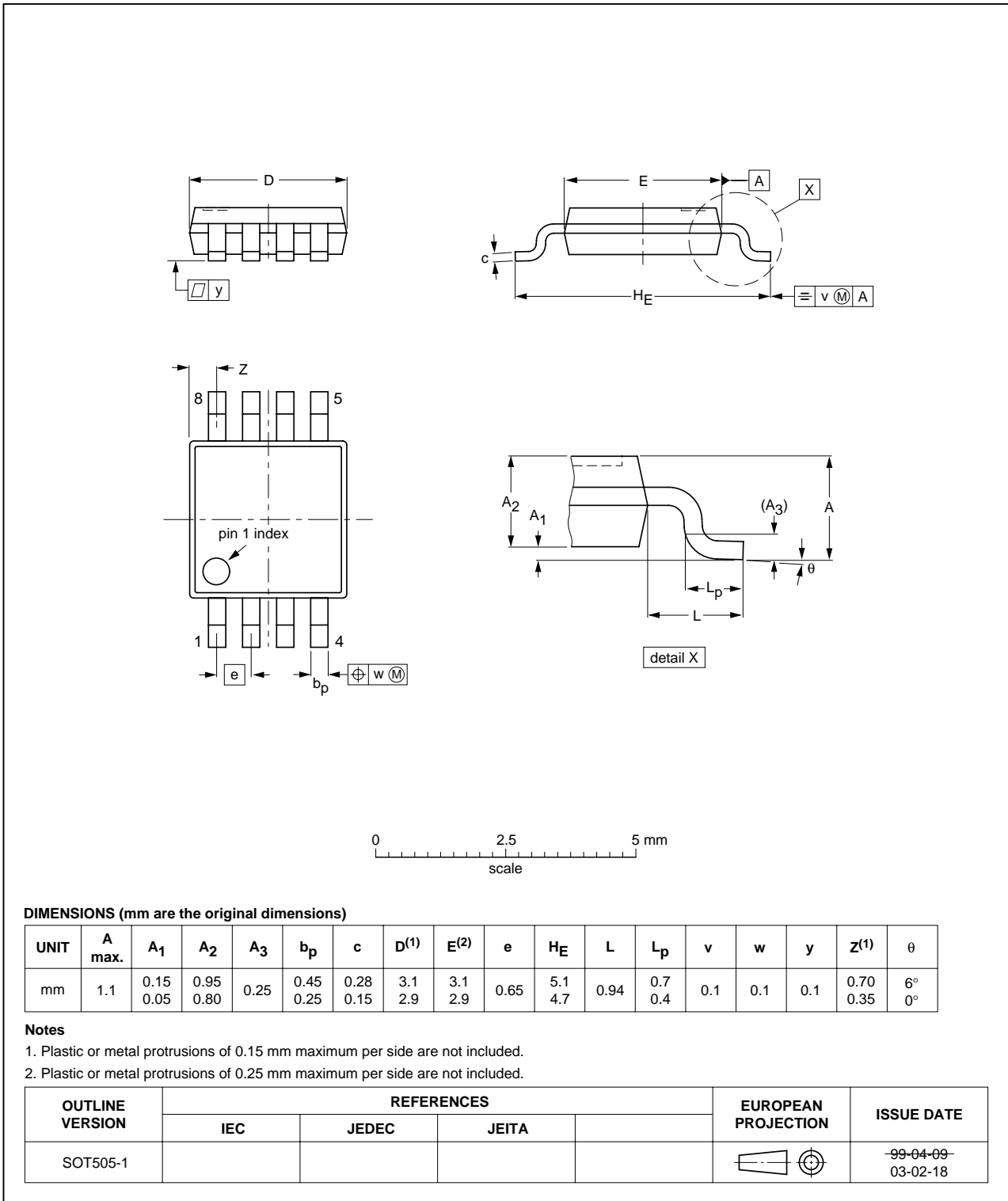


Fig 14. Package outline SOT505-1 (TSSOP8)

WL CSP8: wafer level chip-size package; 8 bumps; 0.61 x 0.84 x 0.38 mm

TDA1308AUK

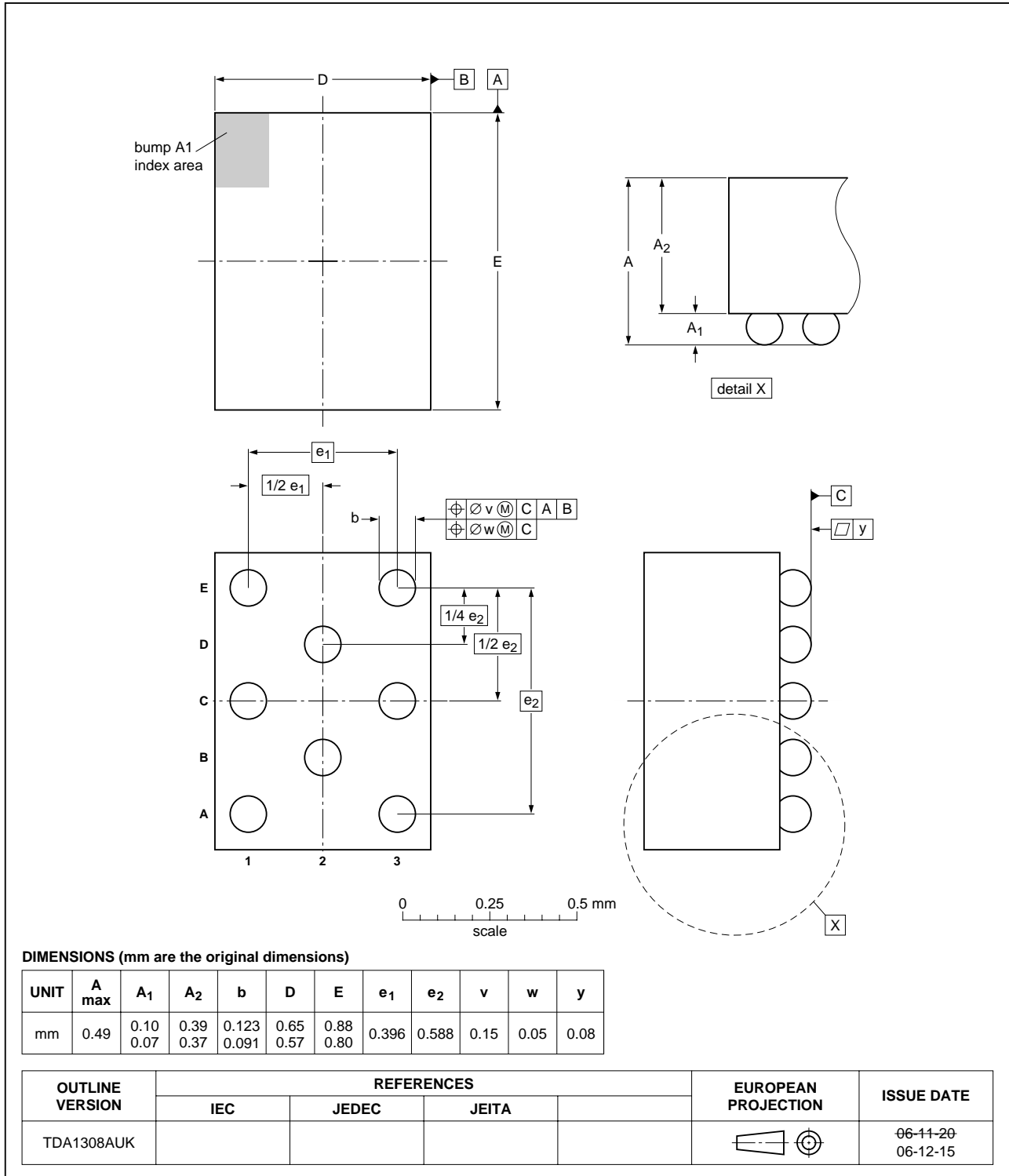


Fig 15. Package outline TDA1308AUK (WL CSP8)

14. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 16](#)) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 8](#) and [9](#)

Table 8. SnPb eutectic process (from J-STD-020C)

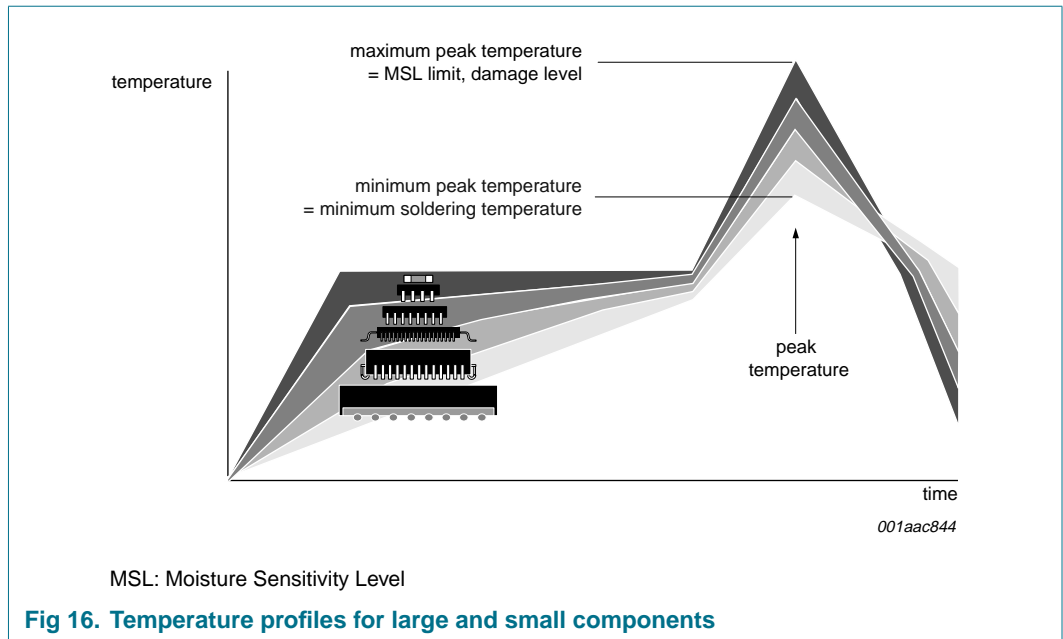
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 9. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 16](#).



For further information on temperature profiles, refer to Application Note AN10365 "Surface mount reflow soldering description".

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA1308_A_4	20070125	Product data sheet	-	TDA1308_A_3
Modifications:		<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors• Legal texts have been adapted to the new company name where appropriate• Type number TDA1308AUK has been added		
TDA1308_A_3	20020719	Product specification	-	TDA1308_A_2
TDA1308_A_2	20020227	Product specification	-	TDA1308_1
TDA1308_1	19940905	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

16.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, send an email to: salesaddresses@nxp.com

18. Contents

1	General description	1
2	Features	1
3	Quick reference data	1
4	Ordering information	2
5	Block diagram	3
6	Pinning information	3
6.1	Pinning	3
6.2	Pin description	3
7	Internal circuitry	4
8	Limiting values	5
9	Thermal characteristics	5
10	Characteristics	6
11	Application information	7
12	Test information	8
12.1	Quality information	9
13	Package outline	10
14	Soldering	14
14.1	Introduction to soldering	14
14.2	Wave and reflow soldering	14
14.3	Wave soldering	14
14.4	Reflow soldering	15
15	Revision history	17
16	Legal information	18
16.1	Data sheet status	18
16.2	Definitions	18
16.3	Disclaimers	18
16.4	Trademarks	18
17	Contact information	18
18	Contents	19

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2007.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 25 January 2007

Document identifier: TDA1308_A_4