## MB90480B/485B Series

## - PRODUCT LINEUP

## MB90480B series

| Part number |  | MB90F481B | MB90F482B | MB90V480B |
| :---: | :---: | :---: | :---: | :---: |
| Classification |  | Flash memory product |  | Evaluation product |
| ROM size |  | 192 Kbytes | 256 Kbytes |  |
| RAM size |  | 4 Kbytes | 6 Kbytes | 16 Kbytes |
| CPU function |  | Number of instructions $: 351$ <br> Instruction bit length $: 8$-bit, 16 -bit <br> Instruction length $: 1$ byte to 7 bytes <br> Data bit length $: 1$-bit, 8 -bit, 16 -bit <br> Minimum instruction execution time $: 40 \mathrm{~ns} \mathrm{(25} \mathrm{MHz} \mathrm{machine} \mathrm{clock)}$  |  |  |
| Ports |  | General-purpose I/O ports: up to 84 <br> General-purpose I/O ports (CMOS output) <br> General-purpose I/O ports (with pull-up resistance) <br> General-purpose I/O ports (N-ch open drain output) |  |  |
| UART |  | 1 channel, start-stop synchronized |  |  |
| 8/16-bit PPG |  | 8-bit 6 channels/16-bit 3 channels |  |  |
| 8/16-bit up/down counter/timer |  | Event input pins : 6, 8-bit up/down counters : 2 8-bit reload/compare registers : 2 |  |  |
| 16-bit I/O timers | $\begin{aligned} & \text { 16-bit } \\ & \text { free-run timer } \end{aligned}$ | Number of channels : 1 Overflow interrupt |  |  |
|  | Output compare (OCU) | Number of channels : 6 <br> Pin input factor : A match signal of compare register |  |  |
|  | Input capture (ICU) | Number of channels : 2 <br> Rewriting a register value upon a pin input (rising, falling, or both edges) |  |  |
| DTP/external interrupt circuit |  | Number of external interrupt pin channels : 8 (edge or level detection) |  |  |
| Extended I/O serial interface |  | Embedded 2 channels |  |  |
| Timebase timer |  | 18-bit counter Interrupt cycles: $1.0 \mathrm{~ms}, 4.1 \mathrm{~ms}, 16.4 \mathrm{~ms}, 131.1 \mathrm{~ms}$ (at 4 MHz base oscillator) |  |  |
| A/D converter |  | Conversion resolution : 8/10-bit, switchable <br> One-shot conversion mode (converts selected channel 1 time only) <br> Scan conversion mode (conversion of multiple consecutive channels, programmable up to 8 channels) <br> Continuous conversion mode (repeated conversion of selected channels) Stop conversion mode (conversion of selected channels with repeated pause) |  |  |
| Watchdog timer |  | Reset generation interval : $3.58 \mathrm{~ms}, 14.33 \mathrm{~ms}, 57.23 \mathrm{~ms}, 458.75 \mathrm{~ms}$(minimum value, at 4 MHz base oscillator) |  |  |
| Low-power consumption (standby) modes |  | Stop mode, sleep mode, CPU intermittent operation mode, watch mode, timebase timer mode |  |  |
| Process |  | CMOS |  |  |
| Type |  | Not included security function |  | User pin ${ }^{* 1}$, $3 \mathrm{~V} / 5 \mathrm{~V}$ versions |
| Emulator power supply*2 |  |  |  | Included |

*1: User pin : P20 to P27, P30 to P37, P40 to P47, P70 to P77
*2 : It is setting of Jumper switch (TOOL VCC) when emulator (MB2147-01) is used.
Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply switching) about details.
Note : Ensure that you must write to Flash at Vcc 3.13 V to $3.60 \mathrm{~V}(3.3 \mathrm{~V} 10$, 5 ).

## MB90480B/485B Series

(Continued)

| Part number <br> Item | MB90487B | MB90488B | MB90F488B | MB90V485B | MB90F489B | MB90483C |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Watchdog timer | Reset generation interval: $3.58 \mathrm{~ms}, 14.33 \mathrm{~ms}, 57.23 \mathrm{~ms}, 458.75 \mathrm{~ms}$ (minimum value, at 4 MHz base oscillator) |  |  |  |  |  |
| Low-power consumption (standby) modes | Stop mode, sleep mode, CPU intermittent operation mode, watch timer mode, timebase timer mode |  |  |  |  |  |
| Process | CMOS |  |  |  |  |  |
| Type | 3 V/5 V power supply*1 | 3 V/5 V power supply* | $3 \mathrm{~V} / 5 \mathrm{~V}$ power supply*1 Included security function | 3 V/5 V power supply* | $3 \mathrm{~V} / 5 \mathrm{~V}$ power supply* ${ }^{* 1}$ Included security function | $3 \mathrm{~V} / 5 \mathrm{~V}$ power supply* |
| Emulator power supply*3 |  |  |  | Included |  |  |

*1: $3 \mathrm{~V} / 5 \mathrm{~V}$ I/F pin : All pins should be for 3 V power supply without P20 to P27, P30 to P37, P40 to P47, and P70 to P77.
*2 : P76/P77 pins are N-ch open drain pins (without P-ch) at built-in $I^{2} \mathrm{C}$. However, MB90V485B uses the N -ch open drain pin (with P-ch).
*3 : It is setting of Jumper switch (TOOL VCC) when emulator (MB2147-01) is used.
Please refer to the MB2147-01 or MB2147-20 hardware manual (3.3 Emulator-dedicated Power Supply Switching) about details.
Notes: As for MB90V485B, input pins (PWC0, PWC1, PWC2/EXTC/SCL and SDA pins) for PWC/ PG//2C become CMOS input.
Ensure that you must write to Flash at $\mathrm{V}_{\mathrm{cc}} 3.13 \mathrm{~V}$ to $3.60 \mathrm{~V}(3.3 \mathrm{~V} 10,5)$.

## MB90480B/485B Series

## PIN ASSIGNMENT

(TOP VIEW)

(FPT-100P-M06)

* : These are the pins for MB90485B series. The pins for MB90480B series are P36/A06, P37/A07, P43/A11, P44/A12, P45/A13, P75 to P77.

Note: MB90485B series only
${ }^{12} \mathrm{C}$ pin P77 and P76 are N-ch open drain pin (without P-ch). However, MB90V485B uses the N -ch open drain pin (with P -ch) .
P20 to P27, P30 to P37, P40 to P47 and P70 to P77 are also used as $3 \mathrm{~V} / 5 \mathrm{~V}$ I/F pin. As for MB90V485B, input pins (PWC0, PWC1, PWC2/EXTC/SCL and SDA pins) for PWC/ PG// ${ }^{2}$ C become CMOS input.

## MB90480B/485B Series


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## MB90480B/485B Series

(Continued)

| Pin No. |  | Pin name | I/O circuit type*3 | Function |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| QFP*1 | LQFP* ${ }^{\text {2 }}$ |  |  |  |  |
| 10 | 8 | P31 | $\begin{gathered} E \\ (\text { CMOS/H }) \end{gathered}$ | This is a general purpose I/O port. |  |
|  |  | A01 |  | In non-multiplex mode, this pin functions as an external address pin. |  |
|  |  | BIN0 |  | 8/16-bit up/down timer input pin (ch.0) . |  |
| 12 | 10 | P32 | $\begin{gathered} \mathrm{E} \\ (\mathrm{CMOS} / \mathrm{H}) \end{gathered}$ | This is a general purpose I/O port. |  |
|  |  | A02 |  | In non-multiplex mode, this pin functions as an external address pin. |  |
|  |  | ZINO |  | 8/16-bit up/down timer input pin (ch.0) |  |
| 13 | 11 | P33 | $\begin{gathered} \mathrm{E} \\ (\mathrm{CMOS} / \mathrm{H}) \end{gathered}$ | This is a general purpose I/O port. |  |
|  |  | A03 |  | In non-multiplex mode, this pin functions as an external address pin. |  |
|  |  | AIN1 |  | 8/16-bit up/down timer input pin (ch.1) . |  |
| 14 | 12 | P34 | $\begin{gathered} E \\ (\text { CMOS/H) } \end{gathered}$ | This is a general purpose I/O port. |  |
|  |  | A04 |  | In non-multiplex mode, this pin functions as an external address pin. |  |
|  |  | BIN1 |  | 8/16-bit up/down timer input pin (ch.1). |  |
| 15 | 13 | P35 | $\begin{gathered} E \\ (\text { CMOS/H) } \end{gathered}$ | This is a general purpose I/O port. |  |
|  |  | A05 |  | In non-multiplex mode, this pin functions as an external address pin. |  |
|  |  | ZIN1 |  | 8/16-bit up/down timer input pin (ch.1) |  |
| 16, 17 | 14, 15 | P36, P37 | $\stackrel{\mathrm{D}}{(\mathrm{CMOS})}$ | MB90480B series | This is a general purpose I/O port. |
|  |  | A06, A07 |  |  | In non-multiplex mode, these pins function as external address pins. |
|  |  | P36, P37 | $\underset{\text { (CMOS/H) }}{\text { E }}$ | MB90485Bseries | This is a general purpose I/O port. |
|  |  | A06, A07 |  |  | In non-multiplex mode, these pins function as external address pins. |
|  |  | PWCO, PWC1*4 |  |  | PWC input pins |
| 18 | 16 | P40 | $\begin{gathered} \mathrm{G} \\ (\mathrm{CMOS} / \mathrm{H}) \end{gathered}$ | This is a general purpose I/O port. |  |
|  |  | A08 |  | In non-multiplex mode, this pin functions as an external address pin. |  |
|  |  | SIN2 |  | Extended I/O serial interface input pin. |  |
| 19 | 17 | P41 | F (CMOS) | This is a general purpose I/O port. |  |
|  |  | A09 |  | In non-multiplex mode, this pin functions as an external address pin. |  |
|  |  | SOT2 |  | Extended I/O serial interface output pin. |  |
| 20 | 18 | P42 | $\begin{gathered} \mathrm{G} \\ (\mathrm{CMOS} / \mathrm{H}) \end{gathered}$ | This is a general purpose I/O port. |  |
|  |  | A10 |  | In non-multiplex mode, this pin functions as an external address pin. |  |
|  |  | SCK2 |  | Extended I/O serial interface clock input/output pin. |  |

(Continued)

## MB90480B/485B Series

| Pin No. |  | Pin name | I/O circuit type*3 | Function |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| QFP*1 | LQFP*2 |  |  |  |  |
| 21, 22 | 19, 20 | P43, P44 | F(CMOS) | $\begin{gathered} \text { MB90480B } \\ \text { series } \end{gathered}$ | This is a general purpose I/O port. |
|  |  | A11, A12 |  |  | In non-multiplex mode, these pins function as external address pins. |
|  |  | P43, P44 | F(CMOS) | $\begin{gathered} \text { MB90485B } \\ \text { series } \end{gathered}$ | This is a general purpose I/O port. |
|  |  | A11, A12 |  |  | In non-multiplex mode, these pins function as external address pins. |
|  |  | MT00, MT01 |  |  | PG output pins |
| 24 | 22 | P45 | $\begin{gathered} \text { F } \\ (\mathrm{CMOS}) \end{gathered}$ | MB90480B | This is a general purpose I/O port. |
|  |  | A13 |  |  | In non-multiplex mode, this pin functions as an external address pin. |
|  |  | P45 | $\begin{gathered} \mathrm{G} \\ (\mathrm{CMOS} / \mathrm{H}) \end{gathered}$ | $\begin{aligned} & \text { MB90485B } \\ & \text { series } \end{aligned}$ | This is a general purpose I/O port. |
|  |  | A13 |  |  | In non-multiplex mode, this pin functions as an external address pin. |
|  |  | EXTC*4 |  |  | PG input pin. |
| 25, 26 | 23, 24 | P46, P47 | $\begin{gathered} \text { F } \\ \text { (CMOS) } \end{gathered}$ | This is a general purpose I/O port. |  |
|  |  | A14, A15 |  | In non-multiplex mode, these pins function as external address pins. |  |
|  |  | $\begin{aligned} & \text { OUT4, } \\ & \text { OUT5 } \end{aligned}$ |  | Output compare event output pins. |  |
| 70 | 68 | P50 | $\begin{gathered} \mathrm{D} \\ \text { (CMOS) } \end{gathered}$ | This is a general purpose I/O port. In external bus mode, this pin functions as the ALE pin. |  |
|  |  | ALE |  | In external bus mode, this pin functions as the address load enable (ALE) signal pin. |  |
| 71 | 69 | P51 | $\begin{gathered} \text { D } \\ \text { (CMOS) } \end{gathered}$ | This is a general purpose I/O port. In external bus mode, this pin functions as the RD pin. |  |
|  |  | $\overline{\mathrm{RD}}$ |  | In external bus mode, this pin functions as the read strobe output ( $\overline{\mathrm{RD}})$ signal pin. |  |
| 72 | 70 | P52 | $\begin{gathered} \mathrm{D} \\ \text { (CMOS) } \end{gathered}$ | This is a general purpose I/O port. In external bus mode, when the WRE bit in the EPCR register is set to " 1 ", this pin functions as the WRL pin. |  |
|  |  | WRL |  | In external bus mode, this pin functions as the lower data write strobe output (WRL) pin. When the WRE bit in the EPCR register is set to " 0 ", this pin functions as a general purpose I/O port. |  |
|  | 71 | P53 | $\begin{gathered} \text { D } \\ \text { (CMOS) } \end{gathered}$ | This is a general purpose I/O port. In external bus mode with 16-bit bus width, when the WRE bit in the EPCR register is set to " 1 ", this pin functions as the WRH pin. |  |
| 73 |  | WRH |  | In external bus mode with 16 -bit bus width, this pin functions as the upper data write strobe output (WRH) pin. When the WRE bit in the EPCR register is set to " 0 ", this pin functions as a general purpose I/O port. |  |

(Continued)

## MB90480B/485B Series

| Pin No. |  | Pin name | circuittypety | Function |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| QFP*1 | LQFP*2 |  |  |  |  |
| 32 | 30 | P75 | $\begin{gathered} \hline \mathrm{F} \\ (\mathrm{CMOS}) \end{gathered}$ | $\begin{aligned} & \text { MB90480B } \\ & \text { series } \end{aligned}$ | This is a general purpose I/O port. |
|  |  | P75 | $\underset{(\mathrm{CMOS} / \mathrm{H})}{\mathrm{G}}$ | MB90485B series | This is a general purpose I/O port. |
|  |  | PWC2*4 |  |  | This is a PWC input pin. |
| 33 | 31 | P76 | $\begin{gathered} \mathrm{F} \\ \text { (CMOS) } \end{gathered}$ | $\begin{array}{\|c\|} \hline \text { MB90480B } \\ \text { series } \end{array}$ | This is a general purpose I/O port. |
|  |  | P76 | $\stackrel{\mathrm{I}}{(\mathrm{NMOS} / \mathrm{H})}$ | $\begin{array}{\|c} \text { MB90485B } \\ \text { series } \end{array}$ | This is a general purpose I/O port. |
|  |  | SCL*4 |  |  | Serves as the $I^{2} \mathrm{C}$ interface data I/O pin. During operation of the $I^{2} \mathrm{C}$ interface, leave the port output in a high impedance state. |
| 34 | 32 | P77 | $\underset{(\mathrm{CMOS})}{\mathrm{F}}$ | $\begin{gathered} \text { MB90480B } \\ \text { series } \end{gathered}$ | This is a general purpose I/O port. |
|  |  | P77 | (NMOS/H) | $\begin{aligned} & \text { MB90485B } \\ & \text { series } \end{aligned}$ | This is a general purpose I/O port. |
|  |  | SDA*4 |  |  | Serves as the $I^{2} \mathrm{C}$ interface data I/O pin. During operation of the $I^{2} \mathrm{C}$ interface, leave the port output in a high impedance state. |
| 47, 48 | 45, 46 | P80, P81 | $\begin{gathered} \mathrm{E} \\ (\mathrm{CMOS} / \mathrm{H}) \end{gathered}$ | These are general purpose I/O ports. |  |
|  |  | IRQ0, IRQ1 |  | External interrupt input pins. |  |
| 52 to 57 | 50 to 55 | P82 to P87 | $\begin{gathered} E \\ (\mathrm{CMOS} / \mathrm{H}) \end{gathered}$ | These are | general purpose I/O ports. |
|  |  | IRQ2 to IRQ7 |  | External interrupt input pins. |  |
| 58 | 56 | P90 | $\begin{gathered} \mathrm{E} \\ (\mathrm{CMOS} / \mathrm{H}) \end{gathered}$ | This is a ge | eneral purpose I/O port. |
|  |  | SIN1 |  | Extended I | /O serial interface data input pin. |
|  |  | CSO |  | Chip select |  |
| 59 | 57 | P91 | $\begin{gathered} \text { D } \\ \text { (CMOS) } \end{gathered}$ | This is a general purpose I/O port. |  |
|  |  | SOT1 |  | Extended I/O serial interface data output pin. |  |
|  |  | CS1 |  | Chip select 1. |  |
| 60 | 58 | P92 | $\underset{(\mathrm{CMOS} / \mathrm{H})}{\mathrm{E}}$ | This is a general purpose I/O port. |  |
|  |  | SCK1 |  | Extended I/O serial interface clock input/output pin. |  |
|  |  | CS2 |  | Chip select 2. |  |
| 61 | 59 | P93 | $\underset{(\mathrm{CMOS} / \mathrm{H})}{\mathrm{E}}$ | This is a general purpose I/O port. |  |
|  |  | FRCK |  | When the free-run timer is in use, this pin functions as the external clock input pin. |  |
|  |  | ADTG |  | When the A/D converter is in use, this pin functions as the external trigger input pin. |  |
|  |  | CS3 |  | Chip select 3. |  |
| 62 | 60 | P94 | $\begin{gathered} \text { (CMOS) } \end{gathered}$ | This is a general purpose I/O port. |  |
|  |  | PPG4 |  | PPG timer output pin. |  |

(Continued)

## MB90480B/485B Series

(Continued)

| Pin No. |  | Pin name | I/O circuit type ${ }^{* 3}$ | Function |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| QFP** | LQFP*2 |  |  |  |  |
| 63 | 61 | P95 | $\begin{gathered} \text { D } \\ \text { (CMOS) } \end{gathered}$ | This is a general purpose I/O port. |  |
|  |  | PPG5 |  | PPG timer output pin. |  |
| 64 | 62 | P96 | $\begin{gathered} \mathrm{E} \\ (\mathrm{CMOS} / \mathrm{H}) \end{gathered}$ | This is a general purpose I/O port. |  |
|  |  | IN0 |  | Input capture ch. 0 trigger input pin. |  |
| 65 | 63 | P97 | $\underset{(\mathrm{CMOS} / \mathrm{H})}{\mathrm{E}}$ | This is a general purpose I/O port. |  |
|  |  | IN1 |  | Input capture ch. 1 trigger input pin. |  |
| 66 to 69 | 64 to 67 | PA0 to PA3 | $\begin{gathered} \text { D } \\ \text { (CMOS) } \end{gathered}$ | These are general purpose I/O ports. |  |
| 66 to 69 | 64 to 67 | OUT0 to OUT3 |  | Output compare event output pins. |  |
| 35 | 33 | AVcc |  | A/D converter analog power supply input pin. |  |
| 36 | 34 | AVRH |  | A/D converter reference voltage input pin. |  |
| 37 | 35 | AVss |  | A/D converter GND pin. |  |
| 49 to 51 | 47 to 49 | MD0 to MD2 | $\underset{(\mathrm{CMOS} / \mathrm{H})}{\mathrm{J}}$ | Operating mode selection input pins. |  |
| 84 | 82 | Vcc3 |  | 3.3 V 0.3 V power supply pins ( V cc3) . |  |
|  | 21 | Vcc5 |  | $\begin{array}{c\|} \hline \text { MB90480B } \\ \text { series } \end{array}$ | $3.3 \mathrm{~V} \quad 0.3 \mathrm{~V}$ power supply pin. Usually, use Vcc Vcc3 Vcc5 as a 3 V power supply. |
| 23 |  |  |  | $\begin{gathered} \text { MB90485B } \\ \text { series } \end{gathered}$ | 3 V/5 V power supply pin. <br> 5 V power supply pin when P20 to P27, P30 to P37, P 40 to $\mathrm{P} 47, \mathrm{P} 70$ to P 77 are used as $5 \mathrm{~V} \mathrm{I} / \mathrm{F}$ pins. Usually, use Vcc Vcc3 Vcc5 as a 3 V power supply (when the 3 V power supply is used alone). |
| $\begin{gathered} 11,42, \\ 81 \end{gathered}$ | $\begin{aligned} & 9,40, \\ & 79 \end{aligned}$ | Vss |  | GND pins. |  |

*1: QFP : FPT-100P-M06
*2 : LQFP : FPT-100P-M20
*3 : For the I/O circuit type, refer to "■ I/O CIRCUIT TYPES".
*4 : As for MB90V485B, input pins become CMOS input.

## MB90480B/485B Series

## HANDLING DEVICES

## 1. Be careful never to exceed maximum rated voltages (preventing latch-up)

In CMOS IC devices, a condition known as latch-up may occur if voltages higher than Vcc or lower than Vss are applied to input or output pins other than medium-or high-voltage pins, or if the voltage applied between Vcc and Vss pins exceeds the rated voltage level.
When latch-up occurs, the power supply current increases rapidly causing the possibility of thermal damage to circuit elements. Therefore it is necessary to ensure that maximum ratings are not exceeded in circuit operation. Similarly, when turning the analog power supply on or off, it is necessary to ensure that the analog power supply voltages ( AV cc and AVRH ) and analog input voltages do not exceed the digital power supply ( Vcc ) .

## 2. Treatment of unused pins

Leaving unused input pins unconnected can cause abnormal operation or latch-up, leading to permanent damage. Unused input pins should always be pulled up or down through resistance of at least 2 k . Any unused input/output pins may be set to output mode and left open, or set to input mode and treated the same as unused input pins.

## 3. Treatment of Power Supply Pins ( $\mathrm{Vcc}_{\mathrm{c}} / \mathrm{Vss}_{\mathrm{ss}}$ )

When multiple $\mathrm{Vcc} / \mathrm{Vss}$ pins are present, device design considerations for prevention of latch-up and unwanted electromagnetic interference, abnormal strobe signal operation due to ground level rise, and conformity with total output current ratings require that all power supply pins must be externally connected to power supply or ground.
Consideration should be given to connecting power supply sources to the $\mathrm{Vcc} / \mathrm{Vss}$ pins of this device with as low impedance as possible. It is also recommended that a bypass capacitor of approximately 0.1 F be placed between the Vcc and Vss lines as close to this device as possible.

## 4. Crystal Oscillator Circuits

Noise around the $\mathrm{X} 0 / \mathrm{X} 1$, or $\mathrm{X} 0 \mathrm{~A} / \mathrm{X} 1 \mathrm{~A}$ pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit board artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

## 5. Precautions when turning the power supply on

In order to prevent abnormal operation in the chip's internal step-down circuits, a voltage rise time during poweron of $50 \mathrm{~s}(0.2 \mathrm{~V}$ to 2.7 V$)$ or greater should be assured.

## 6. Supply Voltage Stabilization

Even within the operating range of Vcc supply voltage, rapid voltage fluctuations may cause abnormal operation. As a standard for power supply voltage stability, it is recommended that the peak-to-peak Vcc ripple voltage at commercial supply frequency $\left(50 / 60 \mathrm{~Hz}\right.$ ) be 10 or less of $\mathrm{V}_{\mathrm{cc}}$, and that the transient voltage fluctuation be no more than $0.1 \mathrm{~V} / \mathrm{ms}$ or less when the power supply is turned on or off.

## 7. Proper power-on/off sequence

The A/D converter power (AVcc, AVRH) and analog input (ANO to AN7) must be turned on after the digital power supply ( Vcc ) is turned on. The $\mathrm{A} / \mathrm{D}$ converter power ( $\mathrm{AVcc}, \mathrm{AVRH}$ ) and analog input (ANO to AN7) must be shut off before the digital power supply ( V cc) is shut off. Care should be taken that AVRH does not exceed $A V c c$. Even when pins used as analog input pins are doubled as input ports, be sure that the input voltage does not exceed AV cc.

## MB90480B/485B Series

## BLOCK DIAGRAM



P00 to P07 (8 pins) : with an input pull-up resistance setting register.
P10 to P17 (8 pins) : with an input pull-up resistance setting register.
P40 to P47 (8 pins) : with an open drain setting register.
P70 to P77 (8 pins) : with an open drain setting register.
MB90485B series only
$1^{2} \mathrm{C}$ pin P77 and P76 are N-ch open drain pin (without P-ch). However, MB90V485B uses the N-ch open drain pin (with P-ch).
P20 to P27, P30 to P37, P40 to P47 and P70 to P77 are also used as $3 \mathrm{~V} / 5 \mathrm{~V}$ I/F pin.
As for MB90V485B, input pins (PWC0, PWC1, PWC2/EXTC/SCL and SDA pins) for PWC/ $\mathrm{PG} /{ }^{2} \mathrm{C}$ become CMOS input.
Note : In the above diagram, I/O ports share internal function blocks and pins. However, when a set of pins is used with an internal module, it cannot also be used as an I/O port.

## MB90480B/485B Series

- MB90F489B




## MB90480B/485B Series

I/O MAP

| Address | Register name | Abbreviated <br> register name | Read/ Write | Resource name | Initial value |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 00H | Port 0 data register | PDR0 | R/W | Port 0 | ХХХХХХХХХв |
| 01н | Port 1 data register | PDR1 | R/W | Port 1 | ХХХХХХХХХв |
| 02H | Port 2 data register | PDR2 | R/W | Port 2 | XXXXXXXX |
| 03н | Port 3 data register | PDR3 | R/W | Port 3 | ХХХХХХХХв |
| 04 | Port 4 data register | PDR4 | R/W | Port 4 | ХХХХХХХХв |
| 05н | Port 5 data register | PDR5 | R/W | Port 5 | ХХХХХХХХв |
| 06 | Port 6 data register | PDR6 | R/W | Port 6 | ХХХХХХХХв |
| 07\% | Port 7 data register | PDR7 | R/W | Port 7 | $\begin{gathered} \text { ХХХXXXXXв } \\ \text { (MB90480B series) } \end{gathered}$ |
|  |  |  |  |  | 11 XXXXXX (MB90485B series) |
| 08H | Port 8 data register | PDR8 | R/W | Port 8 | ХХХХХХХХХ |
| 09н | Port 9 data register | PDR9 | R/W | Port 9 | ХХХХХХХХХв |
| OAн | Port A data register | PDRA | R/W | Port A | ----XXXX |
| OBн | Up/down timer input enable register | UDRE | R/W | Up/down timer input control | XX000000в |
| 0С | Interrupt/DTP enable register | ENIR | R/W | DTP/external interrupts | 00000000в |
| ODH | Interrupt/DTP source register | EIRR | R/W |  | ХХХХХХХХХ |
| ОЕн | Request level setting register | ELVR | R/W |  | 00000000в |
| OFH | Request level setting register |  | R/W |  | 00000000в |
| 10H | Port 0 direction register | DDR0 | R/W | Port 0 | 00000000 в |
| 11H | Port 1 direction register | DDR1 | R/W | Port 1 | 00000000в |
| 12H | Port 2 direction register | DDR2 | R/W | Port 2 | 00000000 ${ }_{\text {B }}$ |
| 13н | Port 3 direction register | DDR3 | R/W | Port 3 | 00000000в |
| 14H | Port 4 direction register | DDR4 | R/W | Port 4 | 00000000в |
| 15 | Port 5 direction register | DDR5 | R/W | Port 5 | 00000000в |
| 16н | Port 6 direction register | DDR6 | R/W | Port 6 | 00000000 в |
| 17H | Port 7 direction register | DDR7 | R/W | Port 7 |  |
|  |  |  |  |  | XX000000в (MB90485B series) |
| 18H | Port 8 direction register | DDR8 | R/W | Port 8 | 00000000в |
| 19н | Port 9 direction register | DDR9 | R/W | Port 9 | 00000000в |
| $1 \mathrm{~A}^{\prime}$ | Port A direction register | DDRA | R/W | Port A | ----0000в |
| 1Вн | Port 4 output pin register | ODR4 | R/W | Port 4 (Open-drain control) | 00000000в |
| 1 Cr | Port 0 input resistance register | RDR0 | R/W | Port 0 (resistance control) | 00000000в |
| 1D ${ }_{\text {H }}$ | Port 1 input resistance register | RDR1 | R/W | Port 1 (resistance control) | 00000000в |
| 1Ен | Port 7 output pin register | ODR7 | R/W | Port 7 <br> (Open-drain control) | $\begin{gathered} 00000000 \text { в } \\ \text { (MB90480B series) } \end{gathered}$ |
|  |  |  |  |  | XX000000в (MB90485B series) |
| $1 \mathrm{~F}_{\mathrm{H}}$ | Analog input enable register | ADER | R/W | Port 6, A/D | 11111111B |

(Continued)

## MB90480B/485B Series

| Address | Register name | Abbreviated register name | Read/ Write | Resource name | Initial value |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 20 H | Serial mode register | SMR | R/W | UART | 00000X00в |
| 21н | Serial control register | SCR | W, R/W |  | 00000100в |
| 22н | Serial input/output register | SIDR/SODR | R/W |  | ХХХХХХХХв |
| 23н | Serial status register | SSR | R, R/W |  | 00001000в |
| 24 H | (Reserved area) |  |  |  |  |
| 25 | Communication prescaler control register | CDCR | R/W | Communication prescaler (UART) | 00--0000в |
| 26н | Serial mode control status register 0 | SMCSO | R, R/W | SIO1 (ch.0) | ----0000в |
| 27 |  |  |  |  | 00000010в |
| 28н | Serial data register 0 | SDR0 | R/W |  | ХХХХХХХХХ |
| 29н | Communication prescaler control register 0 | SDCR0 | R/W | Communication prescaler SIO1 (ch.0) | 0---0000в |
| $2 \mathrm{~A}_{\boldsymbol{H}}$ | Serial mode control status register 1 | SMCS1 | R, R/W | SIO2 (ch.1) | ----0000в |
| 2Вн |  |  |  |  | 00000010в |
| 2 CH | Serial data register 1 | SDR1 | R/W |  | ХХХХХХХХв |
| 2Dн | Communication prescaler control register 1 | SDCR1 | R/W | Communication prescaler SIO2 (ch.1) | 0---0000в |
| 2Ен | Reload register L (ch.0) | PRLLO | R/W | 8/16-bit PPG (ch. 0 to ch.5) | ХХХХХХХХв |
| 2 FH | Reload register H (ch.0) | PRLH0 | R/W |  | ХХХХХХХХв |
| 30н | Reload register L (ch.1) | PRLL1 | R/W |  | ХХХХХХХХв |
| 31н | Reload resister H (ch.1) | PRLH1 | R/W |  | ХХХХХХХХХ |
| 32н | Reload register L (ch.2) | PRLL2 | R/W |  | ХХХХХХХХв |
| 33н | Reload register H (ch.2) | PRLH2 | R/W |  | ХХХХХХХХв |
| 34 | Reload register L (ch.3) | PRLL3 | R/W |  | ХХХХХХХХв |
| 35н | Reload register H (ch.3) | PRLH3 | R/W |  | ХХХХХХХХв |
| 36н | Reload register L (ch.4) | PRLL4 | R/W |  | ХХХХХХХХв |
| 37 | Reload register H (ch.4) | PRLH4 | R/W |  | ХХХХХХХХв |
| 38H | Reload register L (ch.5) | PRLL5 | R/W |  | ХХХХХХХХв |
| 39н | Reload register H (ch.5) | PRLH5 | R/W |  | ХХХХХХХХХв |
| ЗАн | PPG0 operating mode control register | PPGC0 | R/W |  | 0X000XX1в |
| ЗВн | PPG1 operating mode control register | PPGC1 | R/W |  | 0X000001в |
| $3 \mathrm{CH}_{\mathrm{H}}$ | PPG2 operating mode control register | PPGC2 | R/W |  | 0X000XX1в |
| 3D ${ }_{\text {H }}$ | PPG3 operating mode control register | PPGC3 | R/W |  | 0X000001в |
| ЗЕн | PPG4 operating mode control register | PPGC4 | R/W |  | 0X000XX1в |
| $3 \mathrm{FH}^{\text {¢ }}$ | PPG5 operating mode control register | PPGC5 | R/W |  | 0X000001в |
| 40H | PPG0, PPG1 output control register | PPG01 | R/W | 8/16-bit PPG | 00000000в |
| 41н | (Reserved area) |  |  |  |  |
| 42н | PPG2, PPG3 output control register | PPG23 | R/W | 8/16-bit PPG | 00000000в |
| 43н | (Reserved area) |  |  |  |  |

(Continued)

## MB90480B/485B Series

| Address | Register name | Abbreviated register name | Read/ Write | Resource name | Initial value |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 884* | Bus status register | IBSR | R |  | 00000000в |
| 89н* | Bus control register | IBCR | R/W |  | 00000000в |
| 8Ан* | Clock control register | ICCR | R/W | $1^{2} \mathrm{C}$ | --0ХХХХХв |
| 8В ${ }^{*}$ | Address register | IADR | R/W |  | -ХХХХХХХв |
| $8 \mathrm{CH}^{*}$ | Data register | IDAR | R/W |  | ХХХХХХХХв |
| 8D | (Reserved area) |  |  |  |  |
| 8E ${ }^{*}$ | PG control status register | PGCSR | R/W | PG | 00000---в |
| 8Fн to 9Bн | (Disabled) |  |  |  |  |
| 9С | DMAC status register lower digits | DSRL | R/W | DMAC | 00000000в |
| 9Dн | DMAC status register upper digits | DSRH | R/W | DMAC | 00000000в |
| 9Ен | Program address detection control status resister | PACSR | R/W | Address match detection function | 00000000в |
| 9F\% | Delayed interrupt source general/ cancel register | DIRR | R/W | Delayed interrupt generator module | -------0в |
| AOH | Low-power consumption mode control register | LPMCR | W, R/W | Low-power consumption | 00011000в |
| A1н | Clock select register | CKSCR | R, R/W | Low-power consumption | 11111100в |
| А2н, АЗн | (Reserved area) |  |  |  |  |
| А4 ${ }_{\text {H }}$ | DMAC stop status register | DSSR | R/W | DMAC | 00000000в |
| A5 | Automatic ready function select register | ARSR | W | External pins | 0011--00в |
| A6н | External address output control register | HACR | W | External pins | ******** |
| A7\% | Bus control signal select register | EPCR | W | External pins | 1000*10-в |
| A8H | Watchdog timer control register | WDTC | R, W | Watchdog timer | XXXXX111в |
| А9н | Timebase timer control register | TBTC | W, R/W | Timebase timer | 1ХХ00100в |
| ААн | Watch timer control register | WTC | R, R/W | Watch timer | 10001000в |
| $\mathrm{ABH}^{\text {¢ }}$ | (Reserved area) |  |  |  |  |
| $\mathrm{ACH}^{\text {H}}$ | DMAC enable register lower digits | DERL | R/W | DMAC | 00000000в |
| AD | DMAC enable register upper digits | DERH | R/W | DMAC | 00000000в |
| АЕн | Flash memory control status register | FMCS | W, R/W | Flash memory interface | 000Х0000в |
| AFH | (Disabled) |  |  |  |  |
| BOH | Interrupt control register 00 | ICR00 | W, R/W | Interrupt controller | XXXX0111в |
| В1н | Interrupt control register 01 | ICR01 | W, R/W |  | XXXX0111в |
| В2н | Interrupt control register 02 | ICR02 | W, R/W |  | XXXX0111в |
| В3н | Interrupt control register 03 | ICR03 | W, R/W |  | XXXX0111в |
| В4н | Interrupt control register 04 | ICR04 | W, R/W |  | XXXX0111в |
| В5н | Interrupt control register 05 | ICR05 | W, R/W |  | XXXX0111в |
| B6н | Interrupt control register 06 | ICR06 | W, R/W |  | XXXX0111в |
| B7\% | Interrupt control register 07 | ICR07 | W, R/W |  | XXXX0111в |
| B8\% | Interrupt control register 08 | ICR08 | W, R/W |  | XXXX0111в |

(Continued)

## MB90480B/485B Series

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

| Interrupt source | Clear of El2OS | DMAC channel number | Interrupt vector |  | Interrupt control register |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Number | Address | Number | Address |
| Reset |  |  | \#08 | FFFFDCH |  |  |
| INT9 instruction |  |  | \#09 | FFFFD8н |  |  |
| Exception |  |  | \#10 | FFFFD4н |  |  |
| INT0 (IRQ0) | $\bigcirc$ | 0 | \#11 | FFFFD0н | ICR00 | 0000В号 |
| INT1 (IRQ1) | $\bigcirc$ |  | \#12 | FFFFCCH |  |  |
| INT2 (IRQ2) | $\bigcirc$ |  | \#13 | FFFFC8н | ICR01 | 0000B1н |
| INT3 (IRQ3) | $\bigcirc$ |  | \#14 | FFFFC4H |  |  |
| INT4 (IRQ4) | $\bigcirc$ |  | \#15 | FFFFC0н | ICR02 | 0000B2н |
| INT5 (IRQ5) | $\bigcirc$ |  | \#16 | FFFFBC ${ }_{\text {н }}$ |  |  |
| INT6 (IRQ6) | $\bigcirc$ |  | \#17 | FFFFB8 | ICR03 | 0000В3н |
| INT7 (IRQ7) | $\bigcirc$ |  | \#18 | FFFFB4н |  |  |
| PWC1 (MB90485B series only) | $\bigcirc$ |  | \#19 | FFFFB0н | ICR04 | 0000B4н |
| PWC2 (MB90485B series only) | $\bigcirc$ |  | \#20 | FFFFACH |  |  |
| PWC0 (MB90485B series only) | $\bigcirc$ | 1 | \#21 | FFFFA8н | ICR05 | 0000B5 ${ }^{\text {H }}$ |
| PPG0/PPG1 counter borrow |  |  | \#22 | FFFFA4н |  |  |
| PPG2/PPG3 counter borrow |  |  | \#23 | FFFFA0н | ICR06 | 0000B6н |
| PPG4/PPG5 counter borrow |  |  | \#24 | FFFF9C ${ }_{\text {н }}$ |  |  |
| 8/16-bit up/down counter/ timer (ch.0, ch.1) compare/ underflow/overflow/up/down inversion | $\bigcirc$ |  | \#25 | FFFF98 | ICR07 | 0000B7 ${ }^{\text {H }}$ |
| Input capture (ch.0) load | $\bigcirc$ | 5 | \#26 | FFFF94 ${ }_{\text {н }}$ |  |  |
| Input capture (ch.1) load | $\bigcirc$ | 6 | \#27 | FFFF90 ${ }_{\text {н }}$ | ICR08 | 0000B8н |
| Output compare (ch.0) match | $\bigcirc$ | 8 | \#28 | FFFF8C ${ }_{\text {H }}$ |  |  |
| Output compare (ch.1) match | $\bigcirc$ | 9 | \#29 | FFFF88 | ICR09 | 0000B9н |
| Output compare (ch.2) match | $\bigcirc$ | 10 | \#30 | FFFF84 ${ }_{\text {¢ }}$ |  |  |
| Output compare (ch.3) match | $\bigcirc$ |  | \#31 | FFFF80 ${ }_{\text {н }}$ | ICR10 | 0000ВАн |
| Output compare (ch.4) match | $\bigcirc$ |  | \#32 | FFFF7C ${ }_{\text {н }}$ |  |  |
| Output compare (ch.5) match | $\bigcirc$ |  | \#33 | FFFF78н | ICR11 | 0000ВВн |
| UART sending completed | $\bigcirc$ | 11 | \#34 | FFFF74н |  |  |
| 16-bit free-run timer overflow, 16-bit reload timer underflow*2 | $\bigcirc$ | 12 | \#35 | FFFF70 ${ }_{\text {H }}$ | ICR12 | 0000BCH |
| UART receiving completed | © | 7 | \#36 | FFFF6CH |  |  |
| SIO1 (ch.0) | $\bigcirc$ | 13 | \#37 | FFFF68 | ICR13 | 0000BDн |
| SIO2 (ch.1) | $\bigcirc$ | 14 | \#38 | FFFF64 ${ }_{\text {н }}$ |  |  |

(Continued)

## MB90480B/485B Series

## (2) Port Direction Registers

| DDR0 |  |  |  |  |  |  |  |  | Initial value 00000000в | Access <br> R/W |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Address : 000010 ${ }^{\text {H }}$ |  |  |  |  |  |  |  |  |  |  |
| DDR1 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| Address: 000011н | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | 00000000в | R/W |
| DDR2 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| Address : 000012H | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | 00000000в | R/W |
| DDR3 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| Address : 000013H | D37 | D36 | D35 | D34 | D33 | D32 | D31 | D30 | 00000000в | R/W |
| DDR4 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| Address : 000014H | D47 | D46 | D45 | D44 | D43 | D42 | D41 | D40 | 00000000в | R/W |
| DDR5 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| Address : 000015H | D57 | D56 | D55 | D54 | D53 | D52 | D51 | D50 | 00000000в | R/W |
| DDR6 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| Address : 000016н | D67 | D66 | D65 | D64 | D63 | D62 | D61 | D60 | 00000000в | R/W |
| DDR7 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| Address : 000017H | D77*1 | D76*1 | D75 | D74 | D73 | D72 | D71 | D70 | $00000000 \mathrm{~B}^{* 2}$ | R/W |
| DDR8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| Address: 000018H | D87 | D86 | D85 | D84 | D83 | D82 | D81 | D80 | 00000000в | R/W |
| DDR9 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| Address: 000019н | D97 | D96 | D95 | D94 | D93 | D92 | D91 | D90 | 00000000в | R/W |
| DDRA | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| Address: 00001Ан |  |  |  |  | DA3 | DA2 | DA1 | DAO | ----0000в | R/W |

*1: The value is set to " " on MB90485B series only.
*2 : The initial value of this bit is "XX000000b" on MB90485B series only.
When a set of pins is functioning as a port, the corresponding signal pins are controlled as follows.
0 : Input mode.
1 : Output mode. Reset to "0".
Notes: When any of these registers are accessed using a read-modify-write type instruction (such as a bit set instruction), the bit specified in the instruction will be set to the indicated value. However, the contents of output registers corresponding to any other bits having input settings will be rewritten to the input values of those pins at that time.
For this reason, when changing any pin that has been used for input to output, first write the desired value to the PDR register before setting the DDR register for output.
P76, P77 (MB90485B series only)
This port has no DDR. To use P77 and P76 as $I^{2} \mathrm{C}$ pins, set the PDR value to " 1 " so that port data remains enabled (to use P77 and P76 for general purposes, disable $\mathrm{I}^{2} \mathrm{C}$ ). The port is an open drain output (with no P-ch).
To use it as an input port, therefore, set the PDR to "1" to turn off the output transistor and add a pull-up resistor to the external output.

## MB90480B/485B Series

## 2. UART

The UART is a serial I/O port for asynchronous (start-stop synchronized) communication as well as CLK synchronized communication.

- Full duplex double buffer
- Transfer modes : asynchronous (start-stop synchronized) , or CLK synchronized (no start bit or stop bit) .
- Multi-processor mode supported.
- Embedded proprietary baud rate generator

Asynchronous : 76923/38461/19230/9615/500 k/250 kbps
CLK synchronized : 16 M/8 M/4 M/2 M/1 M/500 kbps

- External clock setting available, allows use of any desired baud rate.
- Can use internal clock feed from PPG1.
- Data length : 7-bit (asynchronous normal mode only) or 8-bit.
- Master/slave type communication functions (in multi-processor mode).
- Error detection functions (parity, framing, overrun)
- Transfer signals are NRZ encoded.
- DMAC supported (for receiving/sending)


## MB90480B/485B Series

## (1) Register List

| 15 | 8 |
| :---: | :---: |
| CDCR | 0 |
| SCR | SMR |
| SSR | SIDR (R)/SODR (W) |
| -8 bits $\longrightarrow 8$ bits $\longrightarrow$ |  |

Serial mode register (SMR)
000020 н

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MD1 | MDO | CS2 | CS1 | CSO | Reserved | SCKE | SOE |  |
| $\begin{gathered} \text { R/W } \\ 0 \end{gathered}$ | $\begin{gathered} \text { R/W } \\ 0 \end{gathered}$ | $\begin{gathered} \text { R/W } \\ 0 \end{gathered}$ | $\begin{gathered} \text { R/W } \\ 0 \end{gathered}$ | $\begin{gathered} \text { R/W } \\ 0 \end{gathered}$ | $\begin{gathered} \text { R/W } \\ \mathrm{X} \end{gathered}$ | $\begin{gathered} \mathrm{R} / \mathrm{W} \\ 0 \end{gathered}$ | $\begin{gathered} \text { R/W } \\ 0 \end{gathered}$ | Initial value |

Serial control register (SCR)
$000021_{\text {H }}$


Initial value
Serial I/O register (SIDR/SODR)
000022н


Initial value
Serial status register (SSR)
000023н


Initial value
Communication prescaler control register (CDCR)
000025


Initial value

## MB90480B/485B Series

## 3. Expanded I/O Serial Interface

The expanded I/O serial interface is an 8-bit 1-channel serial I/O interface for clock synchronized data transfer. A selection of LSB-first or MSB-first data transfer is provided.

There are two serial I/O operation modes.

- Internal shift clock mode : Data transfer is synchronized with the internal clock signal.
- External shift clock mode : Data transfer is synchronized with a clock signal input from the external clock signal pin (SCK). In this mode the general-purpose port that shares the external clock signal pin (SCK) can be used for transfer according to CPU instructions.
(1) Register List

Serial mode control status register 0/1 (SMCS0, SMCS1)
Address: 000027н

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SMD2 | SMD1 | SMDO | SIE | SIR | BUSY | STOP | STRT | 00000010в |
| R/W | R/W | R/W | R/W | R/W | R | R/W | R/W |  |

Address : 000026 00002Ан

----0000 в

Serial data register 0/1 (SDR0, SDR1)


Communication prescaler control register 0/1 (SDCR0, SDCR1)


## MB90480B/485B Series

(2) Block Diagram


## MB90480B/485B Series

## 4. 8/10-bit A/D Converter

The A/D converter converts analog input voltage to digital values, and provides the following features.

- Conversion time : minimum 3.68 s per channel
( 92 machine cycles at 25 MHz machine clock, including sampling time)
- Sampling time : minimum 1.92 s per channel
( 48 machine cycles at 25 MHz machine clock)
- RC sequential comparison conversion method, with sample \& hold circuit.
- 8 -bit or 10-bit resolution
- Analog input selection of 8 channels

Single conversion mode : Conversion from one selected channel.
Scan conversion mode : Conversion from multiple consecutive channels, programmable selection of up to 8 channels.
Continuous conversion mode : Repeated conversion of specified channels.
Stop conversion mode : Conversion from one channel followed by a pause until the next activation allows to synchronize with conversion start.

- At the end of $A / D$ conversion, an A/D conversion completed interrupt request can be generated to the CPU. The interrupt can be used activate the DMAC in order to transfer the results of A/D conversion to memory for efficient continuous processing.
- The starting factor conversion may be selected from software, external trigger (falling edge) , or timer (rising edge).


## (1) Register List

ADCS2, ADCS1 (Control status register)

| ADCS1 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial value Bit attributes |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Address : 000046н | MD1 | MD0 | ANS2 | ANS1 | ANSO | ANE2 | ANE1 | ANEO |  |
|  | $\begin{gathered} 0 \\ \text { R/W } \end{gathered}$ | $\begin{gathered} 0 \\ \text { R/W } \end{gathered}$ | $\begin{gathered} 0 \\ \text { R/W } \end{gathered}$ | $\begin{gathered} 0 \\ \text { R/W } \end{gathered}$ | $\begin{gathered} 0 \\ \text { R/W } \end{gathered}$ | $\begin{gathered} 0 \\ \text { R/W } \end{gathered}$ | $\begin{gathered} 0 \\ \text { R/W } \end{gathered}$ | $\begin{gathered} 0 \\ \text { R/W } \end{gathered}$ |  |
| ADCS2 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial value Bit attributes |
| Address : 000047H | BUSY | INT | INTE | PAUS | STS1 | STSO | STRT | Reserved |  |
|  | $\begin{gathered} 0 \\ \text { R/W } \end{gathered}$ | $\begin{gathered} 0 \\ \text { R/W } \end{gathered}$ | $\begin{gathered} 0 \\ \text { R/W } \end{gathered}$ | $\begin{gathered} 0 \\ \text { R/W } \end{gathered}$ | $\begin{gathered} 0 \\ \text { R/W } \end{gathered}$ | $\begin{gathered} 0 \\ \text { R/W } \end{gathered}$ | $\begin{gathered} 0 \\ \text { W } \end{gathered}$ | $\begin{gathered} 0 \\ \text { R/W } \end{gathered}$ |  |
| ADCR2, ADCR1 (Data register) |  |  |  |  |  |  |  |  |  |
| ADCR1 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial value Bit attributes |
| Address : 000048H | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |  |
|  | X R | X R | X R | X R | X R | X | X R | X R |  |

ADCR2

Address :000049н |  |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |

Initial value Bit attributes

## MB90480B/485B Series

(2) Block Diagram


## MB90480B/485B Series

## 5. 8/16-bit PPG

The $8 / 16$-bit PPG is an 8 -bit reload timer module that produces a PPG output using a pulse from the timer operation. Hardware resources include 6 -bit down counters, 128 -bit reload timers, 316 -bit control registers, 6 external pulse output pins, and 6 interrupt outputs. Note that MB90480B/485B series has six channels for 8-bit PPG use, which can also be combined as PPG0 PPG1, PPG2 PPG3, and PPG4 PPG5 to operate as a three-channel 16-bit PPG. The following is a summary of functions.

- 8-bit PPG output 6-channel independent mode : Provides PPG output operation on six independent channels.
- 16-bit PPG output operation mode : Provides 16-bit PPG output on three channels. The six original channels are used in combination as PPG0 PPG1, PPG2 PPG3, and PPG4 PPG5.
- 8 8-bit PPG output operation mode : Output from PPG0 (PPG2/PPG4) is used as clock input to PPG1 (PPG3/ PPG5) to provide to 8-bit PPG output at any desired period length.
- PPG output operation : Produces pulse waves at any desired period and duty ratio. The PPG module can also be used with external circuits as a D/A converter.
(1) Register List

PPGC0/PPGC2/PPGC4 (PPG0/PPG2/PPG4 operation mode control register)


PPGC1/PPGC3/PPGC5 (PPG1/PPG3/PPG5 operation mode control register)
00003Вн
00003Dн $00003 \mathrm{FH}_{\mathrm{H}}$


Read/write Initial value
PPG01/PPG23/PPG45 (PPG0 to PPG5 output control register)

|  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 000040 H | PCS2 | PCS1 | PCS0 | PCM2 | PCM1 | PCM0 | Reserved | Reserved |
| 000042 H | PCS/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 000044 H | R/ |  |  |  |  |  |  |  |
|  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Read/write Initial value

PRLL0 to PRLL5 (Reload register L) 00002Ен 000030н
000032н
000034н
000036н

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| X | X | X | X | X | X | X |  |

Read/write Initial value 000038н
PRLH0 to PRLH5 (Reload register H)
00002Fн 000031н 000033н 000035 000037н

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| D15 | D14 | D13 | D12 | D11 | D10 | D09 | D08 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| X | X | X | X | X | X | X | X |

Read/write Initial value

## MB90480B/485B Series

## (2) Block Diagram

-8-bit PPG ch.0/2/4 block Diagram


## MB90480B/485B Series

- 8-bit PPG ch. 1/3/5 Block Diagram



## MB90480B/485B Series

## 6. 8/16-bit up/down Counter/Timer

8/16-bit up/down counter/timer consists of up/down counter/timer circuits including six event input pins, two 8 -bit up/down counters, two 8 -bit reload/compare registers, as well as the related control circuits.

## (1) Principal Functions

- 8 -bit count register enables counting in the range 0 to 256 .
(In 16-bit 1 mode, counting is enabled in the range 0 to 65535)
- Count clock selection provides four count modes.

Count modes
 Timer mode Up/down count mode Phase differential down count mode (

- In timer mode, there is a choice of two internal count clock signals.
Count clock
(at 16 MHz operation)
 $125 \mathrm{~ns}(8 \mathrm{MHz}$ :

2) 
3) 

- In up/down count mode, there is a choice of trigger edge detection for the input signal from external pins.

- In phase differential count mode, to handle encoder counting for motors, the encoder A-phase, B-phase, and Z-phase are each input, enabling easy and highly accurate counting of angle of rotation, speed of rotation, etc.
- The ZIN pin provides a selection of two functions.

ZIN pin
 Counter clear function Gate functions

- A compare function and reload function are provided, each for use separately or in combination. Both functions can be activated together for up/down counting in any desired bandwidth.
Compare/reload function
 Compare function (output interrupt at compare events) Compare function (output interrupt and clear counter at compare events)
Reload function (output interrupt and reload at underflow events)
Compare/reload function
(output interrupt and clear counter at compare events, output interrupt and reload at underflow events)
Compare/reload disabled
- Individual control over interrupts at compare, reload (underflow) and overflow events.
- Count direction flag enables identification of the last previous count direction.
- Interrupt generated when count direction changes.


## MB90480B/485B Series

## (2) Register List

| 15 | 87 |  |
| :---: | :---: | :---: |
| UDCR1 | UDCR0 |  |
| RCR1 | RCR0 |  |
| Reserved area | CSR0 |  |
| CCRH0 | CCRL0 |  |
| Reserved area | CSR1 |  |
| CCRH1 | CCRL1 |  |
| 8-bit | 8-bit $\longrightarrow$ |  |

CCRHO (Counter Control Register High ch.0)

Address : 00006DH \begin{tabular}{c}
H

 

15 \& 14 \& 13 \& 12 \& 11 \& 10 \& 9 \& 8 <br>
\cline { 2 - 9 } \& M16E \& CDCF \& CFIE \& CLKS \& CMS1 \& CMS0 \& CES1 <br>
CES0 <br>
\hline
\end{tabular}

Initial value 00000000в

CCRH1 (Counter Control Register High ch.1)
Address : 000071H


CCRLO/1 (Counter Control Register Low ch.0/ch.1)

Address : 00006CH | 7 |
| :---: |

CSRO/1 (Counter Status Register ch.0/ch.1)


UDCR0/1 (Up Down Count Register ch.0/ch.1)

| Address : 000069н | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 |
|  |  |  |  |  | R | R | R | R |

Address : 000068 ${ }^{\text {H }}$


RCR0/1 (Reload/Compare Register ch.0/ch.1)


Address : 00006Ан


Initial value 00000000в

Initial value 00000000в

## MB90480B/485B Series

(3) Block Diagram


## MB90480B/485B Series

## 7. DTP/External Interrupt

The DTP (Data Transfer Peripheral) is a peripheral block that interfaces external peripherals to the F${ }^{2} \mathrm{MC}$-16LX CPU. The DTP receives DMA and interrupt processing requests from external peripherals and passes the requests to the $\mathrm{F}^{2} \mathrm{MC}-16 \mathrm{LX}$ CPU to activate the extended intelligent DMAC or interrupt processing.
(1) Detailed Register Descriptions

| Interrupt/DTP Enable Register (ENIR : Enable Interrupt Request Register) |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ENIR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial value |
| Address : 00000С ${ }_{\text {H }}$ | EN7 | EN6 | EN5 | EN4 | EN3 | EN2 | EN1 | ENO | 00000000в |
|  | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |  |
| Interrupt/DTP Source Register (EIRR : External Interrupt Request Register) |  |  |  |  |  |  |  |  |  |
| EIRR | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial value |
| Address : 00000D ${ }^{\text {н }}$ | ER7 | ER6 | ER5 | ER4 | ER3 | ER2 | ER1 | ER0 | XXXXXXXX ${ }_{\text {B }}$ |
|  | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |  |
| Interrupt Level Setting Register (ELVR : External Level Register) |  |  |  |  |  |  |  |  |  |
|  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Initial value |
| Address : 00000Ен | LB3 | LA3 | LB2 | LA2 | LB1 | LA1 | LB0 | LAO | 00000000в |
|  | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |  |
|  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | Initial value |
| Address : 00000Fh | LB7 | LA7 | LB6 | LA6 | LB5 | LA5 | LB4 | LA4 | 00000000в |
|  | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |  |

## (2) Block Diagram

$F^{2}$ MC-16 bus


Request input

## MB90480B/485B Series

## 8. 16-bit Input/Output Timer

The 16-bit input/output timer module is composed of one 16-bit free-run timer, six output compare and two input capture modules. These functions can be used to output six independent wave form based on the 16-bit freerun timer, enabling input pulse width measurement and external clock frequency measurement.

- Register List
- 16-bit free-run timer

- 16-bit output compare


Output compare registers


Output compare control registers

- 16-bit input capture


Input capture data registers


Input capture control status register

## MB90480B/485B Series



## MB90480B/485B Series

## (1) 16-bit Free Run Timer

The 16-bit free-run timer is composed of a 16-bit up-down counter and control status register.
The counter value of this timer is used as the base timer for the input capture and output compare.

- The counter operation provides a choice of eight clock types.
- A counter overflow interrupt can be produced.
- A mode setting is available to initialize the counter value whenever the output compare value matches the value in the compare clear register.
- Register List

Compare clear register (CPCLR)


Initial value ХХХХХХХХв 000066H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CL07 | CL06 | CL05 | CL04 | CL03 | CL02 | CL01 | CL00 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Initial value
XXXXXXXXв

Timer counter data register (TCDT)


Initial value 00000000 в

000062н


Initial value 00000000в

Timer counter control status register (TCCS)
000065


Initial value 0--00000в

000064

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IVF | IVFE | STOP | MODE | SCLR | CLK2 | CLK1 | CLK0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Initial value
00000000в

## MB90480B/485B Series

## - Block Diagram



## MB90480B/485B Series

## (2) Output Compare

The output compare module is composed of a 16-bit compare register, compare output pin unit, and control register. When the value in the compare register in this module matches the 16 -bit free-run timer, the pin output levels can be inverted and an interrupt generated.

- There are six compare registers in all, each operating independently. A setting is available to allow two compare registers to be used to control output.
- Interrupts can be set in terms of compare match events.


## - Register List

Output compare registers (OCCPO to OCCP5)

|  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 00004Вн | C15 | C14 | C13 | C12 | C11 | C10 | C09 | C08 |
| 00004Fн | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Initial value $00000000_{B}$ 0000 000053 000055

|  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 00004Ан | C07 | C06 | C05 | C04 | C03 | C02 | C01 | C00 |
| 00004Eн | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 000050н |  |  |  |  |  |  |  |  |
| 000052н |  |  |  |  |  |  |  |  |
| 000054н |  |  |  |  |  |  |  |  |

Initial value $00000000_{B}$

Output compare control registers (OCS1/OCS3/OCS5)
000057
000059
00005 B

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | CMOD | OTE1 | OTEO | OTD1 | OTDO |
| R/W |  |  |  |  |  |  | R/W |
| R/W | R/W | R/W |  |  |  |  |  |

Initial value ---00000в

Output compare control registers (OCS0/OCS2/OCS4)
Initial values 0000--00в
000056н
$\square$ 00005A

## MB90480B/485B Series



## MB90480B/485B Series

## (3) Input Capture

The input capture module performs the functions of detecting the rising edge, falling edge, or both edges of signal input from external circuits, and saving the 16 -bit free-run timer value at that moment to a register. An interrupt can also be generated at the instant of edge detection.
The input capture module consists of input capture registers and a control register. Each input capture module has its own external input pin.

- Selection of three types of valid edge for external input signals.

Rising edge, falling edge, both edges.

- An interrupt can be generated when a valid edge is detected in the external input signal.
- Register List

Input capture data registers (IPCP0, IPCP1)


Initial value
XXXXXXXX


Initial value
XXXXXXXX

Input capture control status register (ICS01)
000060H


Initial value
00000000в

- Block Diagram



## MB90480B/485B Series

## 9. $I^{2} C$ Interface (MB90485B series only)

The $I^{2} \mathrm{C}$ interface is a serial I/O port supporting the Inter IC BUS. Serves as a master/slave device on the $I^{2} \mathrm{C}$ bus.
The $I^{2} \mathrm{C}$ interface has the following functions.
Master/slave transmit/receive
Arbitration function
Clock synchronization
Slave address/general call address detection function
Forwarding direction detection function
Start condition repeated generation and detection
Bus error detection function

## (1) Register List

Bus Status Register (IBSR)


Initial value 00000000 B

Bus control register (IBCR)
$000089^{\text {H }}$


Initial value

Clock control register (ICCR)
00008Ан


Initial value
--0XXXXX

Address register (IADR)
00008Вн


Initial value

- XXXXXXX

Data register (IDAR)
00008 CH $_{\text {н }}$

|  | 7 |  |  |  | 6 | 5 | 4 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| --- | D7 | D6 | D5 | D4 | D | D2 | D1 | D0 |
| -- R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |  |

Initial value
XXXXXXXX

## MB90480B/485B Series

(2) Block Diagram


## MB90480B/485B Series

## 10. 16-bit Reload Timer

The 16-bit reload timer provides a choice of functions, including internal clock signals that count down in synchronization with three types of internal clock, as well as an event count mode that counts down at specified edge detection events in pulse signals input from external pins. This timer defines an underflow as a change in count value from 0000 н to FFFFн. Thus an underflow will occur when counting from the value "reload register setting value 1 ". The choice of counting operations includes reload mode, in which the count setting values is reloaded and counting continues following an underflow event, and one-shot mode, in which an underflow event causes counting to stop. An interrupt can be generated at counter underflow, and the timer is DTC compatible.

## (1) Register List

- TMCSR (Timer control status register)

Timer control status register (high) (TMCSR)
0000 CB н


Read/Write Initial value

Timer control status register (low) (TMCSR)


Read/Write Initial value

- 16-bit timer register/16-bit reload register TMR/TMRLR (high)

| 0000СDн | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | D15 | D14 | D13 | D12 | D11 | D10 | D09 | D08 |
|  | $\begin{gathered} \text { R/W } \\ \mathrm{X} \end{gathered}$ | $\begin{gathered} \text { R/W } \\ \mathrm{X} \end{gathered}$ | $\begin{gathered} \text { R/W } \\ \text { X } \end{gathered}$ | $\begin{gathered} \text { R/W } \\ \text { X } \end{gathered}$ | $\begin{gathered} \text { R/W } \\ \mathrm{X} \end{gathered}$ | R/W X | $\begin{gathered} \text { R/W } \\ \mathrm{X} \end{gathered}$ | $\begin{gathered} \text { R/W } \\ \mathrm{X} \end{gathered}$ |

Read/Write Initial value

TMR/TMRLR (low)
0000CCH

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| X | X | X | X | X | X | X | X |

Read/Write Initial value

## MB90480B/485B Series

(2) Block Diagram


## MB90480B/485B Series

## 11. PG Timer (MB90485B series only)

The PG timer performs pulse output in response to the external input.
(1) Register List

PG control status register (PGCSR)
00008Ен


Initial value
00000---в
(2) Block Diagram


## MB90480B/485B Series

## 12. PWC Timer (MB90485B series only)

The PWC timer is a 16 -bit multifunction up-count timer capable of measuring the pulse width of the input signal. A total of three channels are provided, each consisting of a 16-bit up-count timer, an input pulse divider \& divide ratio control register, a measurement input pin, and a 16-bit control register. These components provide the following functions.
Timer function: Capable of generating an interrupt request at fixed intervals specified.
The internal clock used as the reference clock can be selected from among three types.

Pulse width measurement function: Measures the time between arbitrary events based on external pulse inputs.
The internal clock used as the reference clock can be selected from among three types.
Measurement modes

- " H " pulse width ( to )/"L" pulse width ( to )
- Rising cycle ( to )/Falling cycle ( to )
- Measurement between edges ( or to or )

The 8 -bit input divider can be used for division measurement by dividing the input pulse by $22 n(n \quad 1,2,3,4)$.
An interrupt can be generated upon completion of measurement.
One-time measurement or fast measurement can be selected.

## MB90480B/485B Series

(1) Register list

PWC control/status registers (PWCSR0 to PWCSR2)
000077H 00007Вн 00007 FH

| 15 | 14 | 1 | 12 | 11 | 10 | 9 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| TRT | TOP | EDIR | EDIE | OVIR | OVIE | ERR | Re erved |
| R/W | R/W | R | R/W | R/W | R/W | R | - |

PWC control/status registers (PWCSR0 to PWCSR2)
000076н 00007 Ан 00007Ен

| 7 | 6 | 5 | 4 |  |  | $c$ | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CK 1 | CK | 0 | PI 1 | PI 0 | /C | MOD2 | MOD1 | MOD0 |  |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |  |  |

Initial value 0000000 Х $_{\text {в }}$

PWC data buffer registers (PWCR0 to PWCR2)

> 000079н 00007Dн 000081 н

| 15 | 14 | 1 | 12 | 11 | 10 | 9 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| D15 | D14 | D1 | D12 | D11 | D10 | D9 | D |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

PWC data buffer registers (PWCR0 to PWCR2)

| 000078 | 7 | 6 | 5 | 4 | 2 |  | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 00007Сн | D7 | D6 | D5 | D4 | D | D2 | D1 | D0 |
| 000080н | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Initial value 00000000в

Dividing ratio control registers (DIVR0 to DIVR2)
000082н 000084н 000086н


Initial value 00000000 в

## MB90480B/485B Series

(2) Block Diagram


## MB90480B/485B Series

## 13. Watch Timer

The watch timer is a 15 -bit timer using the sub clock. This circuit can generate interrupts at predetermined intervals. Also a setting is available to enable it to be used as the clock source for the watchdog timer.
(1) Register List

Watch timer control register (WTC)
0000ААн

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| WDCS | SCE | WTIE | WTOF | WTR | WTC2 | WTC1 | WTC0 |
| R/W | R | R/W | R/W | R/W | R/W | R/W | R/W |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

Read/write
Initial value
(2) Block Diagram


To watchdog timer

## MB90480B/485B Series

## 14. Watchdog timer

The watchdog timer is a 2-bit counter that uses the output from the timebase timer or watch timer as a count clock signal, and will reset the CPU if not cleared within a predetermined time interval after it is activated.
(1) Register List

Watchdog timer control register (WDTC)
0000А8

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| PONR | Reserved | WRST | ERST | SRST | WTE | WT1 | WT0 |
| R |  | R | R | R | W | W | W |
| X | X | X | X | X | 1 | 1 | 1 |

Read/write
Initial value
(2) Block Diagram


## MB90480B/485B Series

## 15. Timebase Timer

The timebase timer is an 18-bit free run counter (timebase counter) that counts up in synchronization with the internal count clock signal (base oscillator 2), and functions as an interval timer with a choice of four types of time intervals. Other functions provided by this module include timer output for the oscillator stabilization wait period, and operating clock signal feed for other timer circuits such as the watchdog timer.

## (1) Register List

Timebase timer control register (TBTC)
0000A9н

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| RESV |  |  | TBIE | TBOF | TBR | TBC1 | TBC0 |
| R/W |  |  | R/W | R/W | W | R/W | R/W |
| 1 | X | X | 0 | 0 | 1 | 0 | 0 |

Read/write
Initial value
(2) Block Diagram


## MB90480B/485B Series

## 16. Clock

The clock generator module controls the operation of the internal clock circuits that serve as the operating clock for the CPU and peripheral devices. This internal clock is referred to as the machine clock, and one cycle is referred to as a machine cycle. Also, the clock signals from the base oscillator are called the oscillator clock, and those from the PLL oscillator are called the PLL clock.
(1) Register List

Clock select register (CKSCR)

0000A1н

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SCM | MCM | WS1 | WS0 | SCS | MCS | CS1 | CS0 |
| R | R | R/W | R/W | R/W | R/W | R/W | R/W |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

Read/write

PLL output select register (PLLOS)


Read/write
Initial value

## MB90480B/485B Series

(2) Block Diagram


HCLK : Oscillator clock
MCLK : Main clock
SCLK : Sub clock

## MB90480B/485B Series

(3) Clock Feed Map


## MB90480B/485B Series

## 17. Low-power Consumption Mode

The MB90480B/485B series uses operating clock selection and clock operation controls to provide the following CPU operating modes :

- Clock modes
(PLL clock mode, main clock mode, sub clock mode)
- CPU intermittent operating modes (PLL clock intermittent mode, main clock intermittent mode, sub clock intermittent mode)
- Standby modes
(Sleep mode, timebase timer mode, stop mode, watch mode)
(1) Register List

Low-power consumption mode control register (LPMCR)


Read/write Initial value

## MB90480B/485B Series

(2) Block Diagram


## MB90480B/485B Series

(3) Status Transition Chart


## MB90480B/485B Series

## 18. External Bus Pin Control Circuit

The external bus pin control circuit controls the external bus pins used to expand the CPU address/data bus connections to external circuits.
(1) Register List

- Auto ready function select register (ARSR)

- External address output control register (HACR)

Address : 0000А6 ${ }^{\text {н }}$


Initial value
********B

- Bus control signal select register (EPCR)


W : Write only
: Not used

* : May be either "1" or " 0 "
(2) Block Diagram



## MB90480B/485B Series

## 19. Chip Select Function Description

The chip select module generates a chip select signals, which are used to facilitate connections to external memory devices. The MB90480B/485B series has four chip select output pins, each having a chip select area register setting that specifies the corresponding hardware area and select signal that is output when access to the corresponding external address is detected.

- Chip select function features

The chip select function uses two 8 -bit registers for each output pin. One of these registers (CARx) is able to detect memory areas in 64 Kbytes units by specifying the upper 8 -bit of the address for match detection. The other register (CMRx) can be used to expand the detection area beyond 64 Kbytes by masking bits for match detection.
Note that during external bus holds, the CS output is set to high impedance.

## (1) Register List



Chip select area mask registers (CMRx)

| 0000СОн | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0000С2н | M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 |
| 0000С4н | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0000С6н | 0 | 0 | 0 | 0 | 1 | 1 | 1 | I |

Read/write Initial value

Chip select area registers (CARx)
0000 C 1 н
0000 C 3 н
0000 C 5 н
0000 C 7 н

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Read/write Initial value

Chip select control register (CSCR)


Read/write Initial value

Chip select active level register (CALR)


Read/write Initial value
*: The initial value of this bit is " 1 " or " 0 ".
The value depends on the mode pin (MD2, MD1 and MDO) .

## MB90480B/485B Series

(2) Block Diagram


## MB90480B/485B Series

## 20. ROM Mirror Function Select Module

The ROM mirror function selection module sets the data in ROM assigned to FF bank so that the data is read by access to 00 bank.
(1) Register List

ROM mirror function select register (ROMM)
Initial value
Address : 00006FH

------+1в
( ) : MB90F489B: Read only, fixed at "1"
()

Other: Selectable, Initial value 0

- : Not used
(2) Block Diagram


Note : Do not access ROM mirror function selection register (ROMM) on using the area of address 004000H to 00FFFFH (008000 н to 00FFFFH) .

## MB90480B/485B Series

## 21. Interrupt Controller

The interrupt control register is built in interrupt controller, and is supported for all I/O of interrupt function. This register sets corresponding peripheral interrupt level.
(1) Register List

Interrupt control registers



Read/write Initial value

| $W$ | $W$ | $W$ | $W$ | $R / W$ | $R / W$ | $R / W$ | $R / W$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $X$ | $X$ | $X$ | $X$ | 0 | 1 | 1 | 1 |

Interrupt control registers
Address: ICROO 0000ВОн
ICR02 0000В2н
ICR04 0000B4н
ICR06 0000B6н
ICR08 0000B8н
ICR10 0000ВАн


ICR12 0000BC
ICR14 0000BEн
Read/write Initial value


Note : The use of access involving read-modify-write instructions may lead to abnormal operation, and should be avoided.

## MB90480B/485B Series

(2) Block Diagram


## MB90480B/485B Series

## 22. DMAC

The DMAC is a simplified DMA module with functions equivalent to $\mathrm{EI}^{2} \mathrm{OS}$. The DMAC has 16 DMA data transfer channels, and provides the following functions.

- Automatic data transfer between peripheral resources (I/O) and memory.
- CPU program execution stops during DMA operation.
- Incremental addressing for transfer source and destination can be turned on/off.
- DMA transfer control from the DMAC enable register, DMAC stop status register, DMAC status register, and descriptor.
- Stop requests from resources can stop DMA transfer.
- When DMA transfer is completed, the DMAC status register sets a flag in the bit for the corresponding channel on which transfer was completed, and outputs a completion interrupt to the interrupt controller.


## (1) Register List

DMAC enable register


Initial value
00000000в

DMAC enable register


DMAC stop status register

| DSSR : 0000A4н | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | STP7 | STP6 | STP5 | STP4 | STP3 | STP2 | STP1 | STPO |
|  | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

DMAC status register
DSRH : 00009D

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DE15 | DE14 | DE13 | DE12 | DE11 | DE10 | DE9 | DE8 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

DMAC status register
DSRL: 00009CH


## MB90480B/485B Series

(2) Block Diagram


## MB90480B/485B Series

## 23. Address Match Detection Function

When the address is equal to a value set in the address detection register, the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code (01H). As a result, when the CPU executes a set instruction, the INT9 instruction is executed. Processing by the INT\#9 interrupt routine allows the program patching function to be implemented.
Two address detection registers are supported. An interrupt enable bit is prepared for each register. If the value set in the address detection register matches an address and if the interrupt enable bit is set at " 1 ", the instruction code loaded into the CPU is replaced forcibly with the INT9 instruction code.

## (1) Register List

- Program address detection register 0 (PADRO)


Initial value XXXXXXXXB


- Program address detection register 1 (PADR1)

- Program address detection control status register (PACSR)

Address
00009Ен

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| RESV | RESV | RESV | RESV | AD1E | RESV | AD0E | RESV |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Initial value 00000000 в

R/W : Readable and writable
X : Undefined
RESV : Reserved bit

## MB90480B/485B Series

(2) Block Diagram


## MB90480B/485B Series

## ■ ELECTRICAL CHARACTERISTICS

## 1. Absolute Maximum Ratings

| Parameter | Symbol | Rating |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max |  |  |
| Power supply voltage*1 | Vcc3 | Vss 0.3 | Vss 4.0 | V |  |
|  | Vcc5 | Vss 0.3 | Vss 7.0 | V |  |
|  | AVcc | Vss 0.3 | Vss 4.0 | V | *2 |
|  | AVRH | Vss 0.3 | Vss 4.0 | V | *2 |
| Input voltage*1 | V | Vss 0.3 | Vss 4.0 | V | *3 |
|  |  | Vss 0.3 | Vss 7.0 | V | *3, *8, *9 |
| Output voltage*1 | Vo | Vss 0.3 | Vss 4.0 | V | *3 |
|  |  | Vss 0.3 | Vss 7.0 | V | *3, *8, *9 |
| Maximum clamp current | Iclamp | 2.0 | 2.0 | mA | *7 |
| Total maximum clamp current | Iclamp |  | 20 | mA | *7 |
| "L" level maximum output current | loL |  | 10 | mA | *4 |
| "L" level average output current | lolav |  | 3 | mA | *5 |
| "L" level maximum total output current | lol |  | 60 | mA |  |
| "L" level total average output current | lolav |  | 30 | mA | *6 |
| "H" level maximum output current | Іон |  | 10 | mA | *4 |
| "H" level average output current | Іоhav |  | 3 | mA | *5 |
| "H" level maximum total output current | Іон |  | 60 | mA |  |
| "H" level total average output current | lohav |  | 30 | mA | *6 |
| Power consumption | Pd |  | 320 | mW |  |
| Operating temperature | TA | 40 | 85 | C |  |
| Storage temperature | Tstg | 55 | 150 | C |  |

*1 : This parameter is based on $\mathrm{V}_{\text {ss }} \mathrm{AV}$ ss 0.0 V .
*2 : AVcc and AVRH must not exceed Vcc. Also, AVRH must not exceed AVcc.
*3: $\mathrm{V}_{1}$ and $\mathrm{V}_{0}$ must not exceed $\mathrm{V}_{\mathrm{cc}} \quad 0.3 \mathrm{~V}$. However, if the maximum current to/from and input is limited by some means with external components, the lclamp rating supersedes the $\mathrm{V}_{1}$ rating.
*4 : Maximum output current is defined as the peak value for one of the corresponding pins.
*5 : Average output current is defined as the average current flow in a 100 ms interval at one of the corresponding pins.
*6 : Average total output current is defined as the average current flow in a 100 ms interval at all corresponding pins.
*7 : Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA3
Use within recommended operating conditions.
Use at DC voltage (current).
The $\quad B$ signal should always be applied with a limiting resistance placed between the $B$ signal and the microcontroller.
The value of the limiting resistance should be set so that when the B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
(Continued)

## MB90480B/485B Series

## (Continued)

Note that when the microcontroller drive current is low, such as in the power saving modes, the B input potential may pass through the protective diode and increase the potential at the $\mathrm{V}_{\mathrm{cc}}$ pin, and this may affect other devices.
Note that if a B signal is input when the microcontroller power supply is off (not fixed at 0 V ), the power supply is provided from the pins, so that incomplete operation may result.
Note that if the B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
Care must be taken not to leave the $B$ input pin open.
Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept B signal input.
Sample recommended circuits:

- Input/Output Equivalent circuits

*8: MB90485B series only
P20 to P27, P30 to P37, P40 to P47, P70 to P77 pins can be used as 5 V I/F pin on applied 5 V to Vcc 5 pin. P 76 and P 77 is N -ch open drain pin.
*9: As for P76 and P77 ( N -ch open drain pin), even if using at 3 V simplicity ( $\mathrm{V} c \mathrm{c} 3 \mathrm{Vcc5}$ ), the ratings are applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## MB90480B/485B Series

2. Recommended Operating Conditions
(Vss AVss 0.0 V )

| Parameter | Symbol | Value |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max |  |  |
| Power supply voltage | Vcc3 | 2.7 | 3.6 | V | During normal operation |
|  |  | 1.8 | 3.6 | V | To maintain RAM state in stop mode |
|  | Vcc5 | 2.7 | 5.5 | V | During normal operation* |
|  |  | 1.8 | 5.5 | V | To maintain RAM state in stop mode* |
| " H " level input voltage | V ${ }_{\text {H }}$ | 0.7 Vcc | Vcc 0.3 | V | All pins other than $\mathrm{V}_{\mathbf{I н}}$, $\mathrm{V}_{\text {неs }}$, $\mathrm{V}_{\text {ннм }}$ and VHX $^{\prime}$ |
|  | $\mathrm{V}_{\mathbf{H} 2}$ | 0.7 Vcc | Vss 5.8 | V | MB90485B series only P76, P77 pins (N-ch open drain pins) |
|  | V ${ }_{\text {HS }}$ | 0.8 Vcc | $\begin{array}{ll}\text { Vcc } & 0.3\end{array}$ | V | Hysteresis input pins |
|  | Vimm | V cc 0.3 | $\begin{array}{lll}\text { Vcc } & 0.3\end{array}$ | V | MD pin input |
|  | VIHx | 0.8 Vcc | Vcc 0.3 | V | X0A pin, X1A pin |
| "L" level input voltage | VIL | Vss 0.3 | 0.3 Vcc | V | All pins other than VILs, VıLм and VILx |
|  | VILs | $\begin{array}{ll}\text { Vss } & 0.3\end{array}$ | 0.2 Vcc | V | Hysteresis input pins |
|  | VILm | $\begin{array}{ll}\text { Vss } & 0.3\end{array}$ | Vss 0.3 | V | MD pin input |
|  | VILx | Vss 0.3 | 0.1 | V | X0A pin, X1A pin |
| Operating temperature | TA | 0 | 70 | C | At external bus operation |

*: MB90485B series only
P20 to P27, P30 to P37, P40 to P47, P70 to P77 pins can be used as $5 \mathrm{~V} / / \mathrm{F}$ pin on applied 5 V to V Cc 5 pin.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## MB90480B/485B Series

## 3. DC Characteristics



## Notes: MB90485B series only

P40 to P47 and P70 to P77 are N-ch open drain pins with control, which are usually used as CMOS.
P76 and P77 are open drain pins without P-ch.
For use as a single 3 V power supply products, set $\mathrm{V}_{c c}$ Vcc3 $\mathrm{V}_{\mathrm{cc}} 5$.
When the device is used with dual power supplies, P20 to P27, P30 to P37, P40 to P47 and
P 70 to P 77 serve as 5 V pins while the other pins serve as $3 \mathrm{~V} / \mathrm{O}$ pins.




## MB90480B/485B Series

(2) Clock Output Timing

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Parameter |  | Symbol | Pin name | Conditions |  | Value |  |  |  |  |  | Unit | Remarks |  |
|  |  | Min |  |  |  | Max |  |  |  |  |  |
| Cycle |  |  | torc | CLK |  |  | tcp* |  |  |  |  |  | ns |  |  |
|  | CLK | tchcı | CLK | Vcc | 3.0 V to 3.6 V | tcp* | 2 | 15 | tcp* | 2 | 15 | ns | at fcp | 25 MHz |
|  |  |  |  |  | 2.7 V to 3.3 V | tcp* | 2 | 20 |  | 2 | 20 | ns | at fcp | 16 MHz |
|  |  |  |  |  | 2.7 V to 3.3 V | tcp* | 2 | 64 | tcp* | 2 | 64 | ns | at fcp | 5 MHz |

* : tcp is internal operating clock cycle time. Refer to " (1) Clock Timing".



## MB90480B/485B Series

(3) Reset Input Standards

|  |  |  |  | (Vcc 2.7 V to 3.6 V, Vss | $0.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}$ |  | 40 C to 85 C |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Parameter | Symbol | $\underset{\text { Pin }}{\text { name }}$ | Conditions | Value |  | Unit | Remarks |
|  |  |  |  | Min | Max |  |  |
| Reset input time | $\mathrm{t}_{\text {fsti }}$ | $\overline{\text { RST }}$ |  | 16 tcp*1 |  | ns | Normal operation |
|  |  |  |  | Oscillator oscillation time ${ }^{\star 2}$ 4 tcp $^{* 1}$ |  | ms | Stop mode |

*1: tcp is internal operating clock cycle time. Refer to " (1) Clock Timing".
*2 : Oscillator oscillation time is the time to 90 of amplitude. For a crystal oscillator this is on the order of several milliseconds to tens of milliseconds. For a ceramic oscillator, this is several hundred microseconds to several milliseconds. For an external clock signal the value is 0 ms .

- In stop mode

- Condition for measurement of AC standards

$C_{\llcorner }$: Load capacitance applied to pins during testing
CLK, ALE : Cl 30 pF
AD15 to AD00 (address data bus) , $\overline{\mathrm{RD}}, \overline{\mathrm{WR}}$,
A23 to A00/D15 to D00: CL 30 pF


## MB90480B/485B Series

(5) Bus Read Timing
(Vcc 2.7 V to 3.6 V , $\mathrm{V}_{\mathrm{ss}} \quad 0.0 \mathrm{~V}$, $\mathrm{T}_{\mathrm{A}} 0 \mathrm{C}$ to 70 C )

| Parameter | Symbol | Pin name | Conditions | Value |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |  |
| ALE pulse width | tLHLL | ALE |  | tcp* 215 |  | ns | $\begin{aligned} & 16 \mathrm{MHz}<\mathrm{fcp} \\ & 25 \mathrm{MHz} \end{aligned}$ |
|  |  |  |  | tcp* 220 |  | ns | $\begin{aligned} & 8 \mathrm{MHz}<\mathrm{fcp} \\ & 16 \mathrm{MHz} \end{aligned}$ |
|  |  |  |  | tcp* 235 |  | ns | fcp 8 MHz |
| Valid address ALE time | tavll | Address, ALE |  | $\begin{array}{lcl}\text { tcp* } & 2 & 17\end{array}$ |  | ns |  |
|  |  |  |  | tcp* 240 |  | ns | fcp 8 MHz |
| ALE address valid time | tlıax | ALE, <br> Address |  | tcp* 215 |  | ns |  |
| Valid address <br> RD time | tavgl | $\overline{\mathrm{RD}}$, <br> Address |  | tcp* 25 |  | ns |  |
| Valid address valid data input | tavov | Address, Data |  |  | 5 tcp* 255 | ns |  |
|  |  |  |  |  | 5 top* $^{*} 280$ | ns | fop 8 MHz |
| $\overline{\mathrm{RD}}$ pulse width | trLRH | $\overline{\mathrm{RD}}$ |  | 3 tcp* 225 |  | ns | $\begin{aligned} & 16 \mathrm{MHz}<\mathrm{fcp} \\ & 25 \mathrm{MHz} \end{aligned}$ |
|  |  |  |  | 3 tcp* 220 |  | ns | 8 MHz < fcp 16 MHz |
| $\overline{R D}$ valid data input | trLDv | $\overline{\mathrm{RD}}$, Data |  |  | 3 tcp* 255 | ns |  |
|  |  |  |  |  | 3 tcp* $^{*} 280$ | ns | fcp 8 MHz |
| $\overline{\mathrm{RD}}$ data hold time | trhdx | $\overline{\mathrm{RD}}$, Data |  | 0 |  | ns |  |
| $\overline{\mathrm{RD}}$ ALE time | trнцн | RD, ALE |  | tcp* 215 |  | ns |  |
| $\begin{aligned} & \overline{\overline{R D}} \\ & \text { address valid time } \end{aligned}$ | trhax | Address, $\overline{\mathrm{RD}}$ |  | tcp* 210 |  | ns |  |
| Valid address <br> CLK time | tavch | Address, CLK |  | tcp* 217 |  | ns |  |
| $\overline{\mathrm{RD}}$ CLK time | trLCH | $\overline{\mathrm{RD}}, \mathrm{CLK}$ |  | tcp* 217 |  | ns |  |
| ALE $\overline{\mathrm{RD}}$ time | tLlRL | $\overline{\mathrm{RD}}, \mathrm{ALE}$ |  | tcp* 215 |  | ns |  |

* : tcp is internal operating clock cycle time. Refer to " (1) Clock Timing".


## MB90480B/485B Series



## MB90480B/485B Series

(6) Bus Write Timing

| Parameter | $\begin{gathered} \text { Sym- } \\ \text { bol } \end{gathered}$ | Pin name | Condition | Value |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |
|  |  |  |  | Min | Max |  |  |
| Valid address $\overline{\mathrm{WR}}$ time | tavwL | Address, $\overline{\mathrm{WR}}$ |  | tcp* 15 |  | ns |  |
| $\overline{\text { WR }}$ pulse width | twLwh | $\overline{\text { WRL, }} \overline{\text { WRH }}$ |  | 3 tcp* 225 |  | ns | $\begin{aligned} & 16 \mathrm{MHz}<\mathrm{fcp} \\ & 25 \mathrm{MHz} \end{aligned}$ |
|  |  |  |  | 3 tcp* 220 |  | ns | $\begin{aligned} & 8 \mathrm{MHz}<\mathrm{fcp} \\ & 16 \mathrm{MHz} \end{aligned}$ |
| Valid data output $\overline{\mathrm{WR}}$ time | tovw | Data, $\overline{\mathrm{WR}}$ |  | 3 tcp** 215 |  | ns |  |
| $\overline{W R}$ data hold time | twhox | $\overline{\mathrm{WR}}$, Data |  | 10 |  | ns | $\begin{array}{\|l\|l\|} \hline 16 \mathrm{MHz}<\mathrm{fcp} \\ 25 \mathrm{MHz} \\ \hline \end{array}$ |
|  |  |  |  | 20 |  | ns | $\begin{aligned} & 8 \mathrm{MHz}<\mathrm{fcp} \\ & 16 \mathrm{MHz} \end{aligned}$ |
|  |  |  |  | 30 |  | ns | fcp 8 MHz |
| WR $\quad$ address valid time | twhax | $\overline{\text { WR, Address }}$ |  | tcp* 210 |  | ns |  |
| $\overline{\overline{W R}}$ ALE time | twHLL | $\overline{\text { WR, ALE }}$ |  | tcp* 215 |  | ns |  |
| $\overline{\overline{W R}}$ CLK time | twLCH | $\overline{\text { WR, CLK }}$ |  | tcp* 217 |  | ns |  |

*: tcp is internal operating clock cycle time. Refer to " (1) Clock Timing".

## MB90480B/485B Series

(7) Ready Input Timing

| Parameter | Symbol | Pin name | Conditions | Value |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |  |
| RDY setup time | tryHs | RDY |  | 35 |  | ns |  |
|  |  |  |  | 70 |  | ns | at fcp 8 MHz |
| RDY hold time | trYнн |  |  | 0 |  | ns |  |



## MB90480B/485B Series

- Internal shift clock mode

- External shift clock mode



## MB90480B/485B Series

- Internal shift clock mode

- External shift clock mode


|  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |



|  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |



## MB90480B/485B Series

(14) Trigger Input Timing
(Vcc 2.7 V to 3.6 V , $\mathrm{V}_{\mathrm{ss}} \quad 0.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}} \quad 40 \mathrm{C}$ to 85 C )

| Parameter | Symbol | Pin name | Conditions | Value |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :--- |
|  |  |  |  | Max |  |  |  |
| Input pulse width | tTRGH <br> tTRGL | ADTG, <br> IRQ0 to IRQ7 |  | 5 ttp** $^{*}$ |  | ns | Normal operation |
|  |  | 1 |  | s | Stop mode |  |  |

* : tcp is internal operating clock cycle time. Refer to " (1) Clock Timing".

(15) Up-down Counter Timing

| (Vcc |  |  | 2.7V to 3.6 V, Vss | $0.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}$ | 40 C to | $85 \mathrm{C})$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Parameter | Symbol | Pin name | Conditions | Value |  | Unit |
|  |  |  |  | Min | Max |  |
| AIN input "H" pulse width | tahl | AINO, AIN1, BINO, BIN1 | Load conditions 80 pF | 8 tcp* |  | ns |
| AIN input "L" pulse width | tall |  |  | 8 tcp* |  | ns |
| BIN input "H" pulse width | tвнL |  |  | 8 tcp* |  | ns |
| BIN input "L" pulse width | tвLL |  |  | 8 tcp* |  | ns |
| AIN BIN time | taubu |  |  | 4 tcp* |  | ns |
| BIN AIN time | teuad |  |  | 4 tcp* |  | ns |
| AIN BIN time | tabbi |  |  | 4 tcp* |  | ns |
| BIN AIN time | tbdau |  |  | 4 tcp* |  | ns |
| BIN AIN time | teuau |  |  | 4 tcp* |  | ns |
| AIN BIN time | taubd |  |  | 4 tcp* |  | ns |
| BIN AIN time | tbdad |  |  | 4 tcp* |  | ns |
| AIN BIN time | tadbu |  |  | 4 tcp* |  | ns |
| ZIN input "H" pulse width | tzHL | ZINO, ZIN1 |  | 4 tcp* |  | ns |
| ZIN input "L" pulse width | tzuL |  |  | 4 tcp* |  | ns |

* : tcp is internal operating clock cycle time. Refer to " (1) Clock Timing".


## MB90480B/485B Series

(16) Chip Select Output Timing

|  |  | (Vcc 2.7 V to 3.6 V, V |  | ss $0.0 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}$ | 40 C to | $85 \mathrm{C})$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Parameter | Symbol | Pin name | Conditions | Val |  |  |
| Parameter | Symbol | Pin name | Conditions | Min | Max |  |
| Chip select output valid time RD | tsvaL | $\mathrm{CSO} \frac{\text { to }}{\frac{\mathrm{RD}}{}}$ |  | tcp* 27 |  | ns |
| Chip select output valid time WR | tsvwL | $\begin{aligned} & \text { CSO to CS3, } \\ & \hline \text { WRH, WRL } \end{aligned}$ |  | tcp* 27 |  | ns |
| $\overline{\mathrm{RD}} \quad$ chip select output valid time | trhsv | $\begin{gathered} \overline{\mathrm{RD}}, \\ \text { CSO to } \mathrm{CS} 3 \end{gathered}$ |  | tcp* 217 |  | ns |
| WR chip select output valid time | twhsv | $\overline{\mathrm{WRH}}, \overline{\mathrm{WRL}}$, CSO to CS3 |  | tcp* 217 |  | ns |

* : tcp is internal operating clock cycle time. Refer to " (1) Clock Timing".


Note : Due to the configuration of the internal bus, the chip select output signals are changed simultaneously and therefore may cause the bus conflict conditions. AC cannot be warranted between the ALE output signal and the chip select output signal.

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## MB90480B/485B Series

## About the external impedance of the analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.
- Analog input equivalent circuit

Analog input


MB90487B
R

MB90F481B/F482B 1.9 k
MB90F488B/F489B 1.9 k
(N
C

Note: The values are reference values.

- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.
The relationship between external impedance and minimum sampling time

- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 F to the analog input pin.


## About errors

As |AVRH AVss| becomes smaller, values of relative errors grow larger.
Note : Concerning sampling time, and compare time when $3.6 \mathrm{~V} \quad \mathrm{AV}$ cc 2.7 V , then
Sampling time : 1.92 s , compare time: 1.1 s
Settings should ensure that actual values do not go below these values due to operating frequency changes.
$\square$

## MB90480B/485B Series

(Continued)


## MB90480B/485B Series





## MB90480B/485B Series

(Continued)




## MB90480B/485B Series

■ ORDERING INFORMATION

| Part number | Package |
| :--- | :---: |
| MB90F481BPF |  |
| MB90F482BPF |  |
| MB90487BPF | 100-pin plastic QFP |
| MB90488BPF | (FPT-100P-M06) |
| MB90F488BPF |  |
| MB90483CPF |  |
| MB90F489BPF |  |
| MB90483CPMC | 100-pin plastic LQFP |
| MB904878PMC | (FPT-100P-M20) |
| MB90488BPMC |  |
| MB90F481BPMC |  |
| MB90F482BPMC |  |
| MB90F488BPMC |  |
| MB90F489BPMC |  |

## MB90480B/485B Series

## PACKAGE DIMENSIONS




Please check the latest package dimension at the following URL. http://edevice.fujitsu.com/package/en-search/

## MB90480B/485B Series

(Continued)

| (100-pin plastic QFP | Lead pitch | 0.65 mm |
| :---: | :---: | :---: |
|  | Package width $\times$ package length | $14.00 \times 20.00 \mathrm{~mm}$ |
|  | Lead shape | Gullwing |
|  | Sealing method | Plastic mold |
|  | Mounting height | 3.35 mm MAX |
|  | Code (Reference) | P-QFP100-14×20-0.65 |
| 100P-M06) |  |  |



Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

## MB90480B/485B Series

MEMO

