International
IOR Rectifier

PD-60319

iP1206PbF

iPOWIR™ TECHNOLOGY

Synchronous Buck Multiphase Optimized LGA Power Block

Integrated Power Semiconductors, PWM Control, & Passives

Features

- Input voltage range of 7.5V to 14.5V
- Output voltage range of 0.8V to 5.5V
- Output voltage accuracy of +/-1%
- Output current range of 0A to 30A
- Operation up to 600kHz
- Lossless current limit
- Output overvoltage protection
- Pre-Bias start-up
- External synchronization
- Output voltage tracking
- Output voltage sequencing
- Over temperature protection

Applications

- Embedded Telecom Systems
- Distributed Point of Load Power Architectures
- Powering Dual Voltage ASICs
- Microprocessor Power Supplies
- General DC/DC Converters

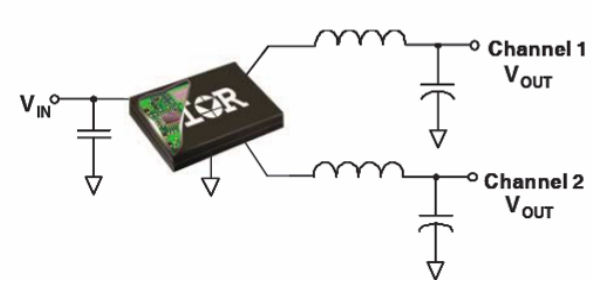
Package Description	Interface Connection	Parts Per Bag	Parts Per Reel	T & R Orientation
iP1206PbF	LGA	10	-	Fig. 29
iP1206TRPbF	LGA	-	750	

Description

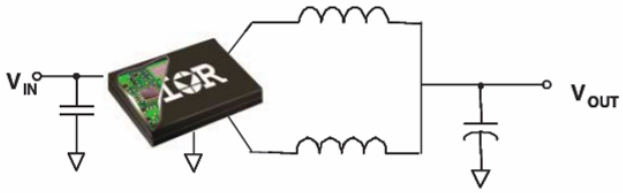
The iP1206 is a fully optimized solution for medium current synchronous buck applications. The iP1206 can be configured as a dual output voltage power supply delivering up to 15A of current per output. Alternatively, the iP1206 can be configured as a single output voltage power supply delivering up to 30A of current. In both cases, the power stages are operated 180º out of phase. This reduces the amount of input RMS current and lessens the quantity of input capacitors needed.

iPOWIR Technology offers designers an innovative board space saving solution for applications requiring high power densities. iPOWIR technology eases design for applications where component integration offers benefits in performance and functionality. iPOWIR technology solutions are also optimized internally for layout, heat transfer, and component selection.

Typical Application



Dual Output



Single Output

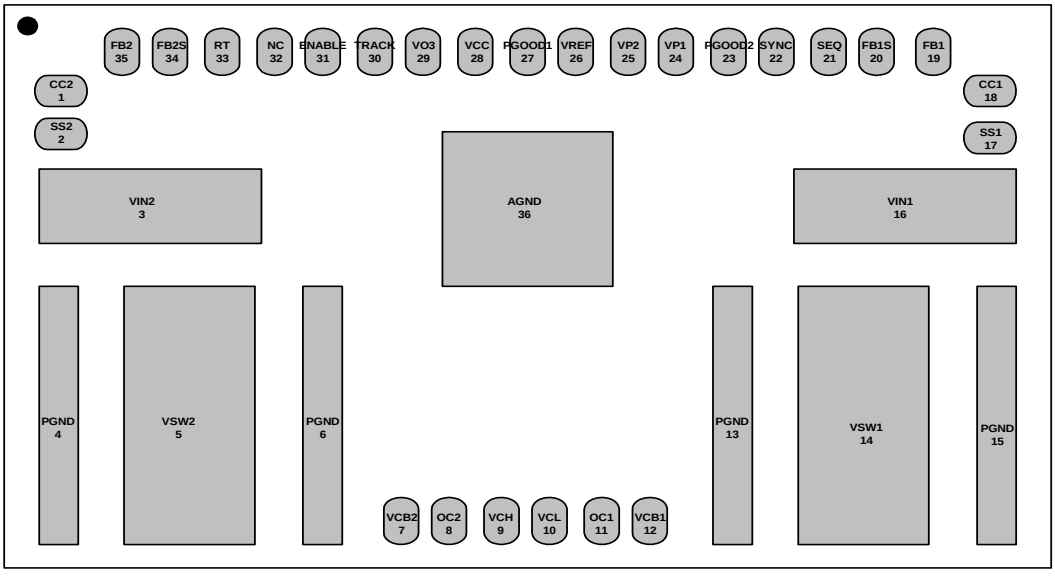
ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND)

- V_{IN1}, V_{IN2}, V_{CC}, V_{CL} Supply Voltage ..... -0.3V to 16V
- V_{CH} ..... -0.3V to 30V
- $V_{SW1,2}$ ..... -0.3V to 30V
- $FB_{1,2}$ ..... -0.3V to 3V
- V_P-V_{REF} ..... -0.3V to 3V
- ENABLE ..... -0.3V to Vcc
- $OC_{1,2}$ ..... -0.3V to 3V
- $SS_{1,2}$ ..... -0.3V to 3V
- TRACK, SEQ ..... -0.3V to Vcc
- R_T ..... -0.3V to 3V
- P_{GOOD1}, P_{GOOD2} .... -0.3V to Vcc
- AGND to PGND ..... +/- 0.3V
- Storage Temperature Range ..... -65°C To 150°C
- Block Temperature..... ..... -20°C To 125°C (Note 4)
- ESD Classification ..... JEDEC, JESD22-A114 (HBM[1KV], Class 1C)
  ..... JEDEC, JESD22-A115 (MM[50V], Class A)
- MSL Rating 3

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those listed in the "Recommended Operating Conditions" section of this specification is not implied.

Package Pinout Diagram



Recommended Operating Conditions

Symbol	Definition	Min	Max	Units
V_{IN1}, V_{IN2}	Input Supply Voltage	7.5	14.5	V
V_{CC}	Bias Supply Voltage	7.5	14.5	V
Io *(Note1)*	Output current per Phase	0	15	A
Fs	Operating frequency	200	600	kHz
Tj	Junction temperature	-40	125	°C

Electrical Specifications

Unless otherwise specified, these specification apply over Vcc=12V, 0ºC<Tj<105ºC

PARAMETER	Min	Typ	Max	Units	Conditions
Supply Power					
Power Loss	-	5	6.5	W	V_{IN} = 12V, V_{O1} = V_{02} = 1.5V, I_{O1} = I_{O2} = 15A, f_{SW} = 300kHz, T_{BLK} = 25ºC
V_{IN} Supply Current (Static)	-	0.5	2	mA	V_{IN} = 12V, ENABLE = 0V
V_{CC} Supply Current (Static)	-	25	30	mA	SS=0V ; no switching; V_{cc} tied to V_{CL}
V_{CH} Supply Current (Static)	-	10	12	mA	SS=0V ; no switching
Power-On Reset (POR)					
V_{CC} Rising	6.9	-	7.5	V	
V_{CC} Falling	6.1	-	6.75	V	
Hysteresis	500	-	-	mV	V_{IN} Rising & Falling
DC Output Regulation					
System Set Point Accuracy	0.792	0.8	0.808	V	T_J = 0ºC to 105ºC (Note 2)
	0.784	0.8	0.810	V	T_J = -40C to 125 (Note 2)
Enable					
Turn-on Threshold (V_{IH})	1.14	-	1.34	V	
Hysteresis	150	-	-	mV	Rising & Falling
Soft Start 1,2					
Voltage Level	-	3.0	-	V	V_{IN} = ENABLE = 12V
Disable Voltage Level	-	-	0.25	V	
Sink/Source Current	18	23	28	µA	

Electrical Specifications

PARAMETER	Min	Typ	Max	Units	Conditions
Error Amplifier 1,2					
Input Bias Current	-	-0.1	-0.5	µA	Soft Start Pin = 3V
Sink/Source Current	120	200	280	µA	
Transconductance	3000	-	5000	µmho	
Input Offset Voltage	-3.5	-	3.5	mV	FB to Vref
VP pin Voltage Range	0.4	-	V_{CC} - 2	V	(Note 3)
TRACK pin Voltage Range	0	-	V_O3	V	(Note 3)
Oscillator					
Frequency Range	200	-	600	kHz	
Frequency Accuracy	88	-	112	%	F_S = 300kHz
Ramp Amplitude	-	1.25	-	V	
Minimum Duty Cycle	-	-	0	%	FB = 1V
Maximum Duty Cycle	84	-	-	%	F_S = 300kHz, FB = 0V
Minimum Pulse Width	-	-	150	ns	F_S = 300kHz
SYNC Frequency Range	-	-	1200	kHz	20% above Free Running Freq
SYNC Pulse Duration	200	300	-	ns	
SYNC HIGH Level Threshold (V_{IH})	2	-	-	V	
SYNC LOW Level Threshold (V_{IL})	-	-	0.6	V	
Sequence					
Turn on Threshold	-	-	5	V	
Turn off Threshold	0.3	-	-	V	
POWER GOOD Monitor					
FB1/2S Threshold	80	90	95	%	Percentage of Voltage Reference
PGOOD1/2 Output Low Voltage	-	0.1	0.5	V	I_{SINK} = 2mA
Over Voltage Protection					
Start Threshold	110	115	120	%	Percentage of Voltage Reference
Propagation Delay to Shutdown	-	-	5	µs	Output Voltage set to 1.25Vref (Note3)

Electrical Specifications

PARAMETER	Min	Typ	Max	Units	Conditions
Over Current Protection					
Start Threshold	20	24.5	29	A	V_{IN} = 12V, R_{OCSET} = 7.5KΩ
Hiccup Duty Cycle	-	5	-	%	(Note 3)
Thermal Shutdown					
Start Threshold	130	145	-	ºC	(Note 3)
Temperature Hysteresis	-	20	-	ºC	
Internal Regulator (V_{O3})					
Output Accuracy	6.7	7.2	7.7	V	V_{CC} = 12V, I_{LOAD} = 50mA
Dropout Voltage			2	V	V_{CC} = 9V, I_{LOAD} = 100mA
Current Limit	110			mA	

Note1: Continuous output current determined by input and output voltage setting. Refer to SOA curve.

Note2: FB1,2 connected to CC1,2. Measured at the CC1,2 pin. Production tested at 25ºC. Other temperatures guaranteed by design.

Note3: Guaranteed by design but not tested in production.

Note4: Block Temperature is defined as any Die temperature within the package.

Pin Description

Pin Number	Pin Name	Description
1	CC2	Compensation pin for Error Amplifier 2
2	SS2	Soft Start/Shutdown pin for output 2
3	VIN2	Input supply voltage connection to output 2
4, 6, 13, 15	PGND	Power Ground
5	VSW2	Voltage Switching Node for output 2 – pin connection to the output inductor
7	VCB2	Boot strap capacitor pin for output 2 - connect a 0.1µF from this pin to VSW2
8	OC2	Over current threshold setting pin for output 2
9	VCH	Supply voltage for internal high side FET drivers of both outputs
10	VCL	Supply voltage for internal low side FET drivers of both outputs
11	OC1	Over current threshold setting pin for output 1
12	VCB1	Boot strap capacitor pin for output 1 - connect a 0.1µF from this pin to VSW1
14	VSW1	Voltage Switching Node for output 1 – pin connection to the output inductor
16	VIN1	Input supply voltage connection to output 1
17	SS1	Soft Start/Shutdown pin for output 1
18	CC1	Compensation pin for Error Amplifier 1
19	FB1	Inverting input for Error Amplifier 1
20	FB1S	Output over voltage protection sense pin for output 1
21	SEQ	Sequence Enable pin
22	SYNC	External clock synchronization pin – when not in use, leave pin floating
23	PGOOD2	Power Good status pin of output 2 – output is open collector
24	VP1	Non-inverting input of error amplifier 1
25	VP2	Non-inverting input of error amplifier 2
26	VREF	Internal voltage reference pin - connect a 100pF from this pin to AGND
27	PGOOD1	Power Good status pin of output 1 – output is open collector
28	VCC	Input supply voltage of internal control IC - connect a 1.0µF from this pin to AGND
29	VO3	Output of internal regulator used to supply VCH – connect a 1.0µF from this pin to PGND
30	TRACK	Secondary non-inverting input to Error Amplifier 2 – used to set the type of power up/down sequence of the output voltages
31	ENABLE	Master enable pin. Recycling this pin will reset OV, SS, and Pre-Bias latch for both outputs.
32	NC	No connect. This pin is not for electrical connection.
33	RT	Switching frequency setting pin
34	FB2S	Output over voltage protection sense pin for output 2
35	FB2	Inverting input for Error Amplifier 2
36	AGND	Analog Ground

Block Diagram

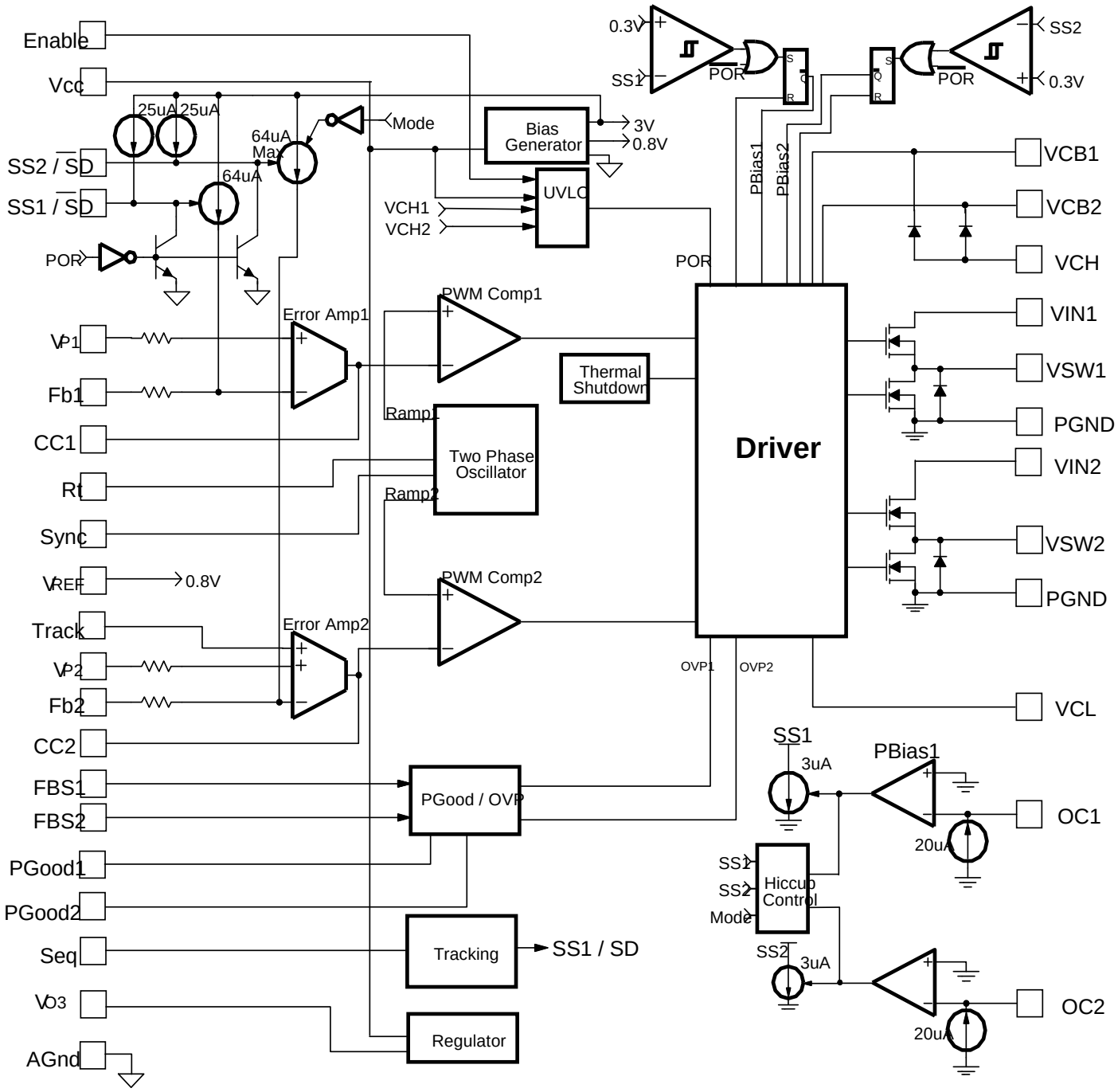


Fig. 2: Simplified block diagram of the iP1206

TYPICAL OPERATING CHARACTERISTICS

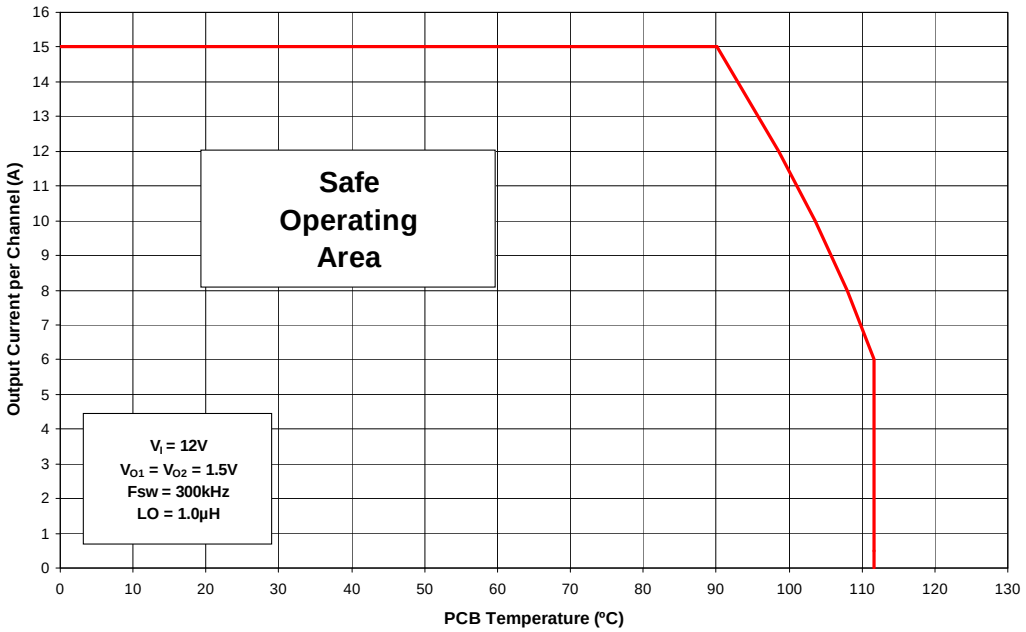


Fig. 3: Safe Operating Curve

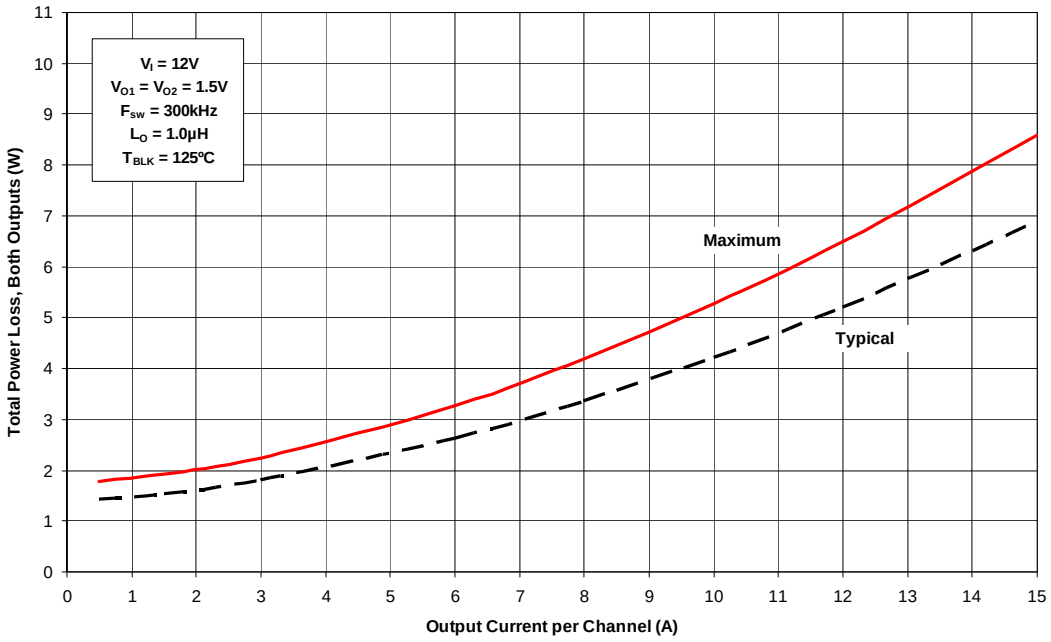


Fig. 4: Power Loss vs. Output Current

TYPICAL OPERATING CHARACTERISTICS

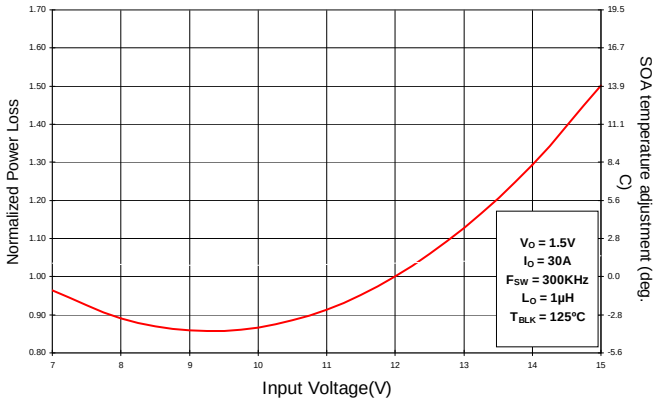


Fig. 4a: Power Loss vs. Input Voltage

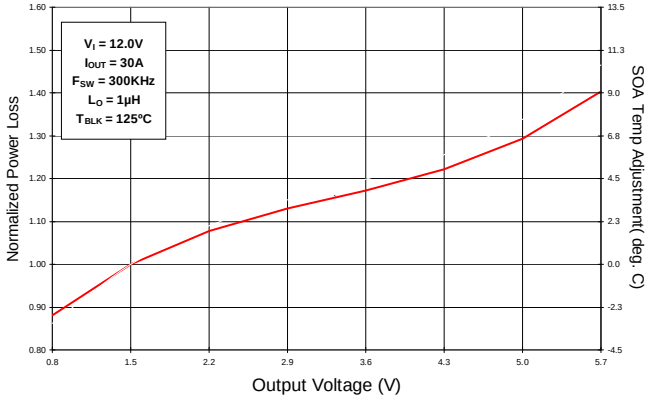


Fig. 4b: Power Loss vs. Output Voltage

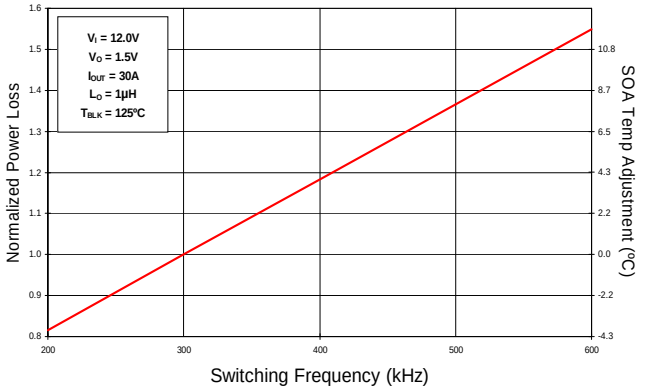


Fig. 4c: Power Loss vs. Switching Frequency

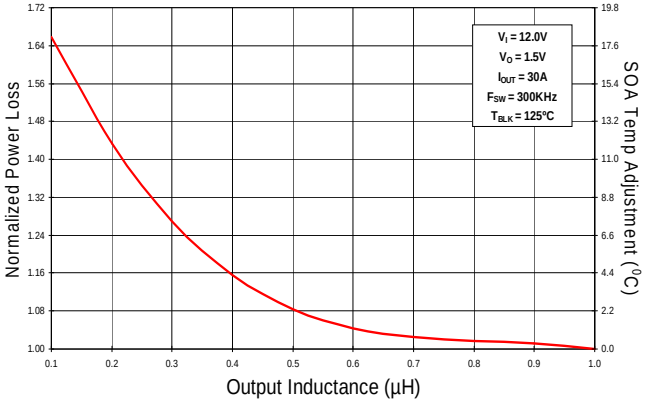


Fig. 4d: Power Loss vs. Output Inductor

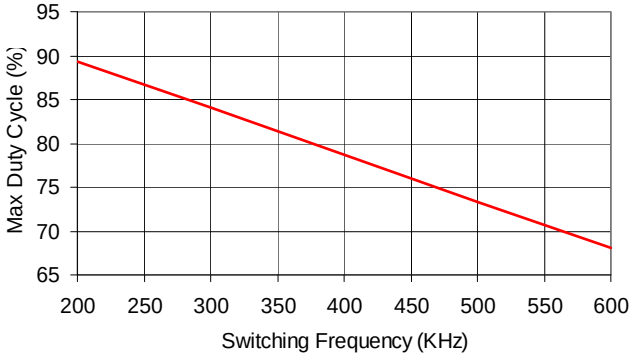


Fig. 5 Maximum Duty Cycle vs. Switching Frequency

Circuit Description

THEORY OF OPERATION

Introduction

The iP1206 is a versatile device for high performance buck converters. It consists of two synchronous buck controllers which can be operated either in a two independent outputs mode or in a current share single output mode for high current applications.

The timing of the IC is provided by an internal oscillator circuit which generates two-180º-out-of-phase clock that can be externally programmed up to 600kHz per phase.

Under-Voltage Lockout

The under-voltage lockout circuit monitors four signals (Vcc, Enable, V_{CH1}, V_{CH2}). This ensures the correct operation of the converter during power up and power down sequence. The driver outputs remain in the off state whenever one of these signals drops below set thresholds. Normal operation resumes once these signals rise above the set values. Fig. 6 shows a typical start up sequence.

Enable

The enable features another level of flexibility for start up. The Enable has precise threshold which is internally monitored by an under-voltage lockout circuit.

It's threshold can be externally programmed to desired level by using two external resistors, so the converter doesn't start up until the input voltage has reached the specified threshold level (see Fig. 6).

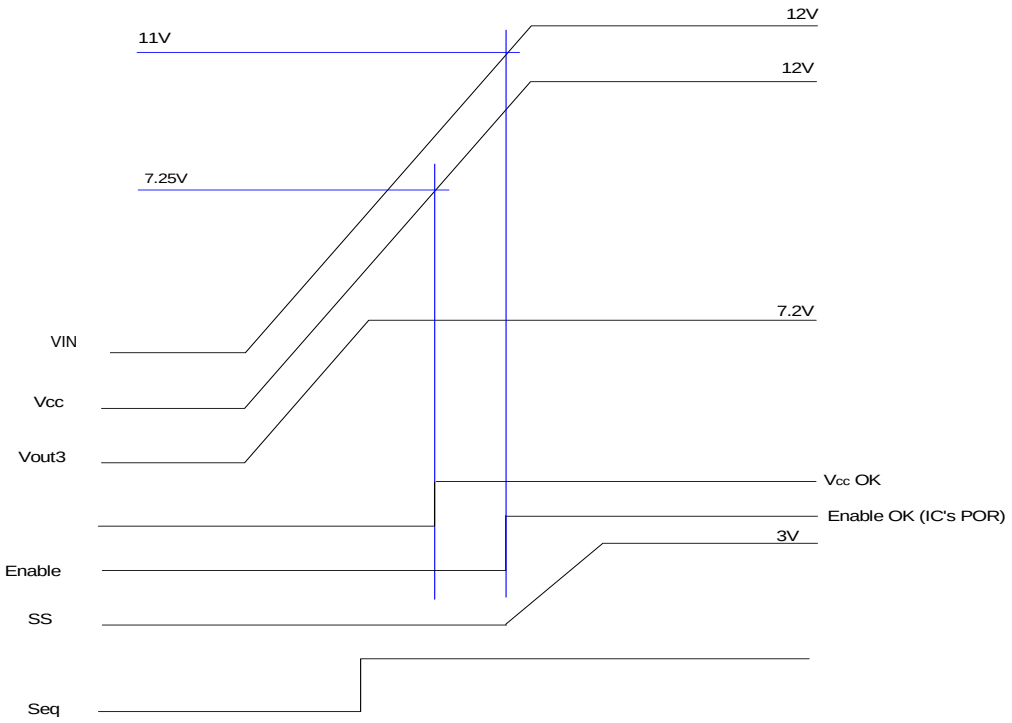


Fig. 6: Normal Start up, Enable threshold is externally set to 11V
Seq pin is pulled high prior to start up

Internal Regulator

iP1206 features an on-board regulator capable of sourcing current up to 100mA. This integrated regulator can be used to generate the necessary bias voltage for drivers. An example of how this can be used is shown in Fig. 25. The output of the regulator is protected for short circuit and thermal shutdown.

Out-of-Phase Operation

The iP1206 drives its two output stages 180º out-of-phase. In current share mode (single output), the two inductor ripple currents cancel each other and result in a reduction of the output current ripple and yield a smaller output capacitor for the same ripple voltage requirement. Fig. 7 shows two channels inductor current and the resulting voltage ripple at output.

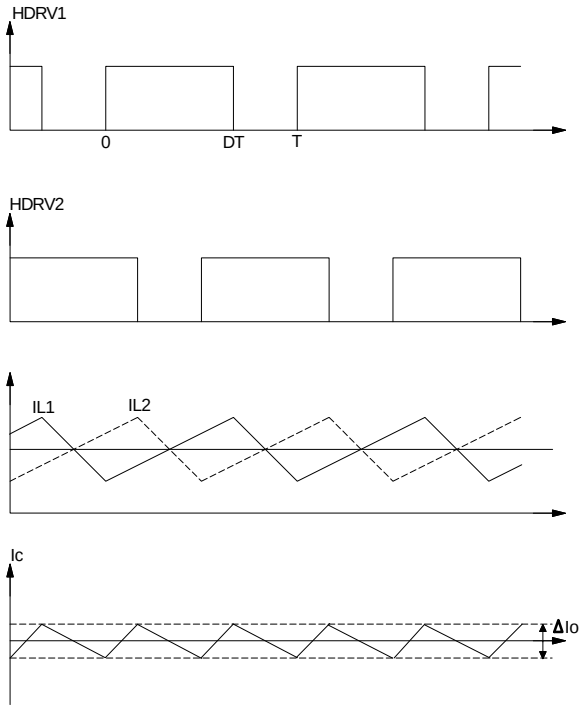


Fig. 7: Current ripple cancellation for output

In addition, the 180º out of phase operation contributes to input current cancellation. This results in a much smaller input capacitor - RMS current thereby reducing the input capacitor quantity. Fig. 8 shows the equivalent RMS current.

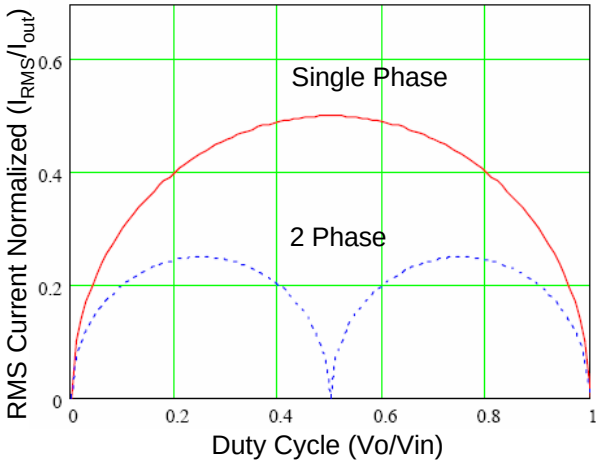


Fig. 8: Input RMS value vs. Duty Cycle

Mode Selection

The iP1206 can operate as a dual output independently regulated buck converter, or as a 2 phase single output buck converter (in current share mode). The SS2 pin is used for mode selection. In current share mode this pin should be floating and in dual output mode a soft start capacitor must be connected from this pin to ground to program the start time for the second output.

Independent Mode

In this mode the iP1206 provides control to two independent output power supplies with either common or different input voltages. The output voltage of each individual channel is set and controlled by the output of the error amplifier, which is the amplified error signal from the sensed output voltage and the reference voltage. The error amplifier output voltage is compared to the ramp signal thus generating fixed frequency pulses of variable duty-cycle, (PWM) which are applied to the internal MOSEFT drivers. Fig. 25b shows a typical schematic for such an application.

Current Share Mode

This feature allows the connection of both outputs together to increase current handling capability of the converter to support a common load. In current sharing mode, error amplifier 1 becomes the master which regulates the common output voltage and the error amplifier 2 performs the current sharing function, Fig. 9 shows the configuration of error amplifiers. See Fig 25a for a typical application.

In this mode iP1206 makes sure the master channel starts first followed by slave channel to prevent any glitch during start up. This is done by clamping the output of slave's error amplifier until the master channel generates the first PWM signal.

At no load condition the slave channel may be kept off depending on the offset of error amplifier.

Lossless Inductor Current Sensing

The iP1206 uses a lossless current sensing technique for current share purposes. The inductor current is sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor, this voltage is proportional to the inductor current. As shown in Fig. 9 the voltage across the inductor's DCR can be expressed by:

$$V_{RL1}(s) = (V_{in} - V_{out}) * \frac{R_{L1}}{R_{L1} + sL_1} \qquad ----(1)$$

$$V_{RL1}(s) = I_{L1} * R_{L1} \qquad ----(2)$$

The voltage across the C_1 can expressed by:

$$V_{C1}(s) = (V_{in} - V_{out}) * \frac{1/sC_1}{R_1 + 1/sC_1} \qquad ----(3)$$

Combining equations (1),(2) and (3) result in the following expression for V_{C1}:

$$V_{C1}(s) = I_{L1} * \frac{R_{L1} + sL_1}{1 + sR_1 * C_1} \qquad ----(4)$$

Usually the resistor R_1 and C_1 are chosen so that the time constant of R_1 and C_1 equals the time constant of the inductor which is the inductance L_1 over the inductor's DCR (R_{L1}). If the two time constants match, the voltage across C_1 is proportional to the current through L_1, and

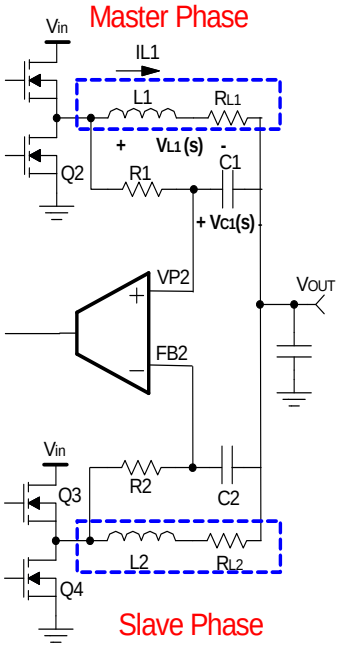


Fig. 9: Loss Less inductor current sensing and current sharing

the sense circuit can be treated as if only a sense resistor with the value R_{L1} was used.

$$If: R_1 * C_1 = \frac{L_1}{R_{L1}}$$

$$V_C(s) \approx I_{L1} * R_{L1}$$

The mismatch of the time constants does not affect the measurements of inductor DC current, but affects the AC component of the inductor current.

Soft-Start

The iP1206 has a programmable soft-start to control the output voltage rise and limit the inrush current during start-up. It provides a separate Soft-start function for each output. This enables the user to sequence the outputs by controlling the rise time of each output through the selection of different value soft-start capacitors.

To ensure correct start-up, the soft-start sequence initiates when the Vcc and Enable rise above their threshold and generate the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the error amplifier's output of the PWM converter.

Soft-Start (cont.)

During power up, the converter output starts at zero and thus the voltage at Fb is about 0V. A current (64µA) injects into the Fb pin and generates a voltage about 1.6V (64µAx25K) across the negative input of error amplifier, see Fig. 10.

The magnitude of this current is inversely proportional to the voltage at the soft-start pin. The 28µA current source starts to charge up the external capacitor. In the mean time, the soft-start voltage ramps up, the current flowing into Fb pin starts to decrease linearly and so does the voltage at negative input of error amplifier.

When the soft-start capacitor is around 1V, the voltage at the negative input of the error amplifier is approximately 0.8V.

As the soft-start capacitor voltage charges up, the current flowing into the Fb pin keeps decreasing.

The feedback voltage increases linearly as the injecting current decreases. The injecting current drops to zero when soft-start voltage is around 1.8V and the output voltage goes into steady state. Fig. 11 shows the theoretical operational waveforms during soft-start.

The output start-up time is the time period when soft-start capacitor voltage increases from 1V to 2V. The start-up time will be dependent on the size of the external soft-start capacitor. The start-up time can be estimated by:

$$28\mu A * \frac{T_{start}}{C_{ss}} = 1.8V - 1V$$

For a given start up time, the soft-start capacitor (nF) can be estimated as:

$$C_{ss} \cong \frac{20(\mu A) * T_{start}(ms)}{0.8(V)} \qquad ----(5)$$

For normal start up the **Seq** pin should be pulled high (usually can be connected to Vout3).

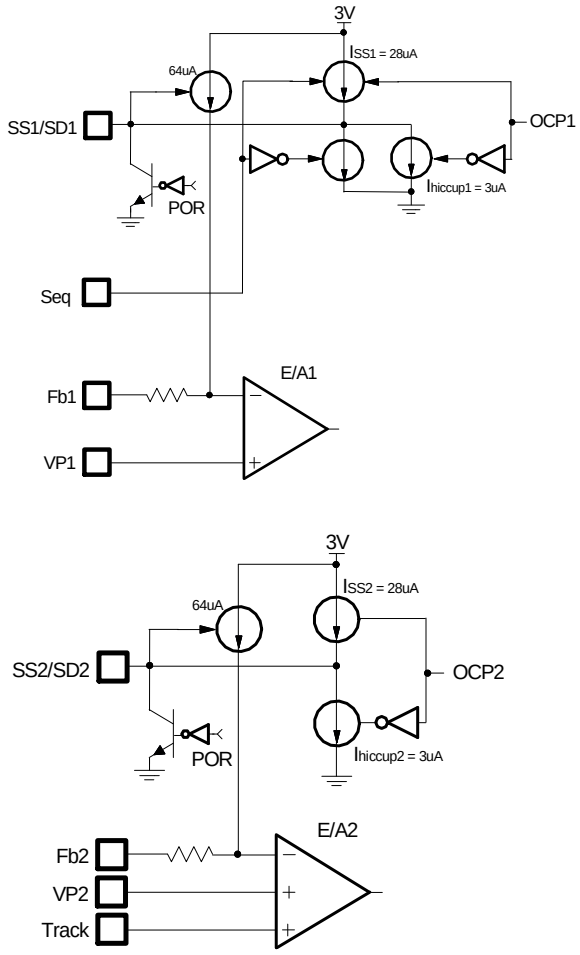


Fig. 10: Soft-Start circuit for iP1206

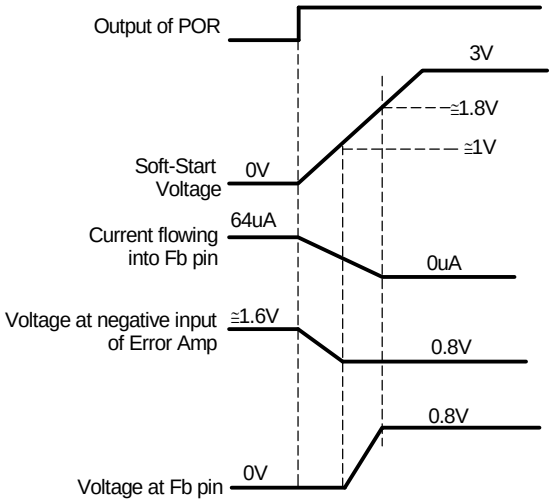


Fig. 11: Theoretical operation waveforms during soft-start

Output Voltage Tracking and Sequencing

The iP1206 can accommodate a full spectrum of user programmable tracking and sequencing options using Track, Seq, Enable and Power Good pins.

Through these pins both simple voltage tracking such as that required by the DDR memory application and more sophisticated sequencing such ratiometric or simultaneously can be implemented.

The Seq pin controls the internal current sources to set the power up or down sequencing, toggle this pin high for power up and toggle this pin low for power down.

The Track pin is used to determine the second channel output for either ratiometric or simultaneously by using two external resistors. Fig. 12 shows how these pins are configured for different sequencing mode.

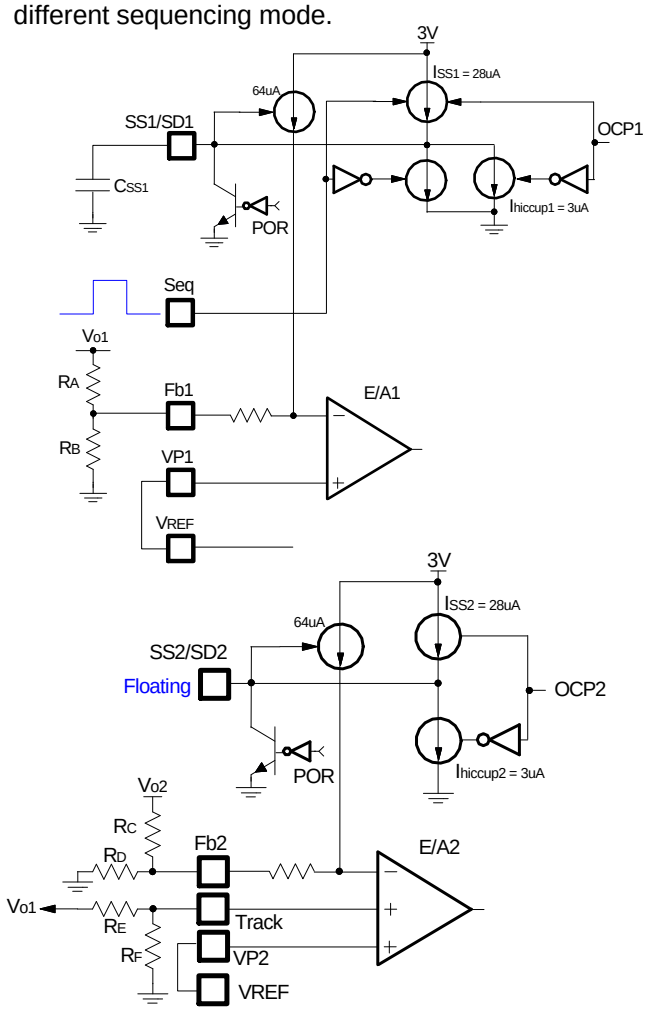


Fig.12: Using Seq and Track pin for different sequencing

In general the R_A and R_B set the output voltage for the first output and R_C and R_D set the output voltage for the second output.

For simultaneously vs. ratiometric, RE and RF can be selected according to the table below:

simultaneously	ratiometric
Set $R_E = R_C$	Set $R_E = R_A$
And $R_F = R_D$	And $R_F = R_B$

Fig. 13: Ratiometric Power up /down

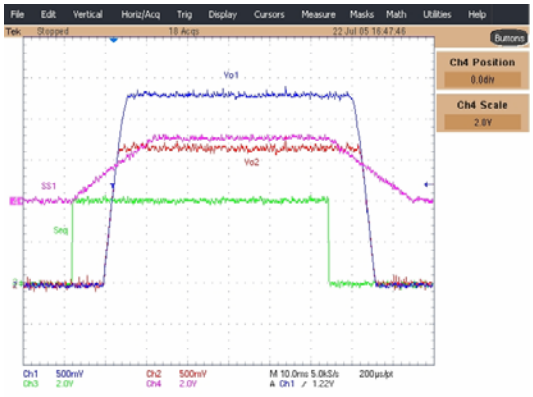


Fig. 14: Simultaneously Power Up / down

Fault Protection

The iP1206 monitors the output voltage for over voltage protection and power good indication. It senses the $R_{ds(on)}$ of low side MOSFET for over current protection. It also protects the output for prebias conditions. Fig. 15 below shows the IC's operating waveforms under different fault conditions.

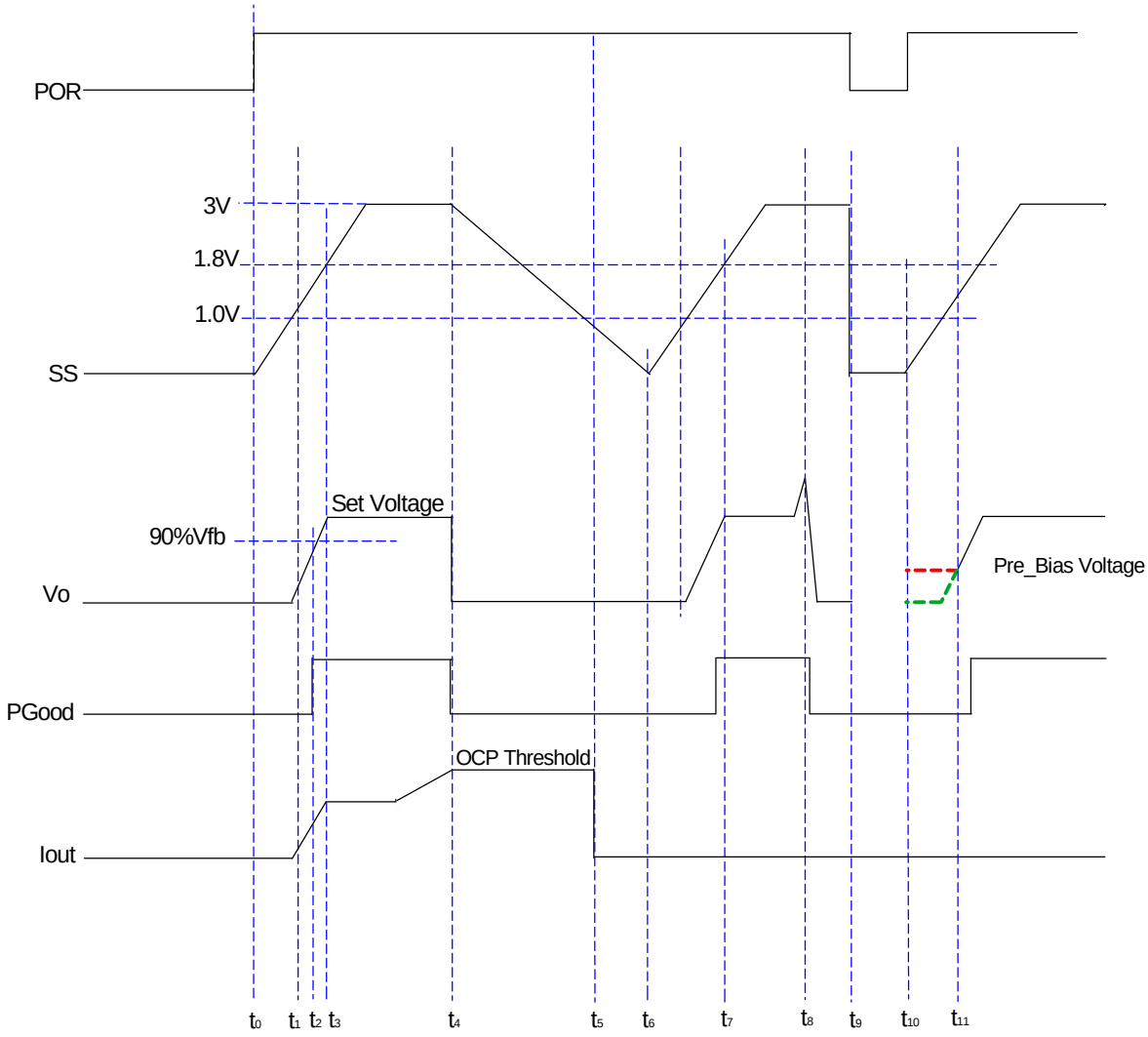


Fig. 15: Fault Conditions

$t_0 - t_1$: Vcc, VCH and Enable signals passed their respective UVLO threshold. Soft start sequence starts.

$t_1 - t_2$: Power Good signal flags high.

$t_1 - t_3$: Output voltage ramps up and reaches the set voltage.

$t_4 - t_5$: OC event, SS ramps down. IC in Hiccup mode.

$t_5 - t_6$: OC is removed, recovery sequence, fresh SS.

$t_6 - t_7$: Output voltage reaches the set voltage.

t_8: OVP event. HDrv turns off and LDrv Turns on. The IC latches off.

$t_9 - t_{10}$: Manually recycled the Vcc after latched OVP.

t_{11}: PreBias start up.

Over-Current Protection

The over current protection is performed by sensing current through the $R_{DS(on)}$ of low side MOSFET. This method enhances the converter's efficiency and reduce cost by eliminating a current sense resistor. As shown in Fig. 16, an external resistor (R_{OCSET}) is connected between OCSet pin and the drain of low side MOSFET (Q2) which sets the current limit set point.

When the overcurrent trip threshold is reached, the power supply output shuts down and attempts to restart, entering into the hiccup mode. The time duration between the shutdown of the output and the restart is determined by the time it takes to discharge the soft start capacitor.

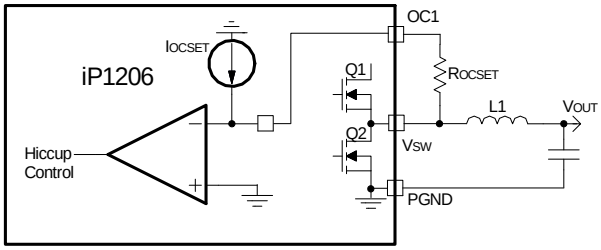


Fig. 16: Connection of over current sensing resistor

The duty cycle of the hiccup process is typically 5%. The hiccup is performed by charging and discharging the soft-start capacitor at a certain slope rate. As shown in Fig. 17 a 3µA current source is used to discharge the soft-start capacitor. The OCP comparator resets after every soft start cycle, the converter stays in this mode until the overload or short circuit is removed. Once the condition is removed the converter will automatically recover. Refer to Fig. 24 for R_{OCSET} selection.

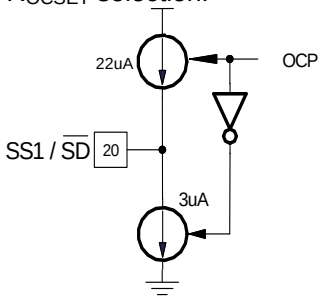


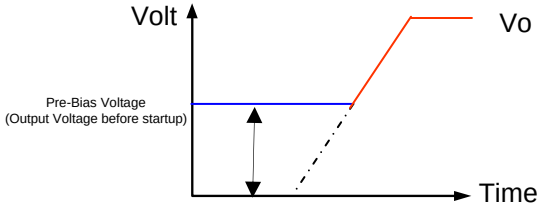
Fig. 17: 3uA current source for discharging soft-start capacitor during hiccup

Pre-Bias

iP1206 is able to start up into a pre-charged output, which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET off until the first gate signal for control MOSFET is generated. The figure below shows a typical Pre-Bias condition at start up.

Depending on the system configuration, specific amount of output capacitors may be required to prevent discharging the output voltage.



Over Voltage Protection

Over-voltage is sensed through two dedicated sense pins FBS1, FBS2. A separate OVP circuit is provided for each channel.

The OVP threshold is user programmable and can be set by two external resistors. Upon over-voltage condition of either one of the outputs, the OVP forces a latched shutdown on the fault output and pulls low the low side driver.

Reset is performed by recycling the Vcc or Enable. Overvoltage can be sensed either by connecting FB1s and FB2s to their corresponding outputs through separate output voltage divider resistor networks, or they can be connected directly to their corresponding feedback pins FB1 and FB2. For Type III compensation, FB1s and FB2s should be connected through voltage dividers only.

Power Good

The iP1206 provides two separate open collector power good signals which report the status of the outputs. The outputs are sensed through the two dedicated V_{SEN1} and V_{SEN2} pins.

Once the iP1206 is enabled and the outputs reach the set value (90% of set value) the power good signals go open and stay open as long as the outputs stay within the set values.These pins are open collector and need to be externally pulled high.

Shutdown using Soft Start pins

The outputs can be shutdown by pulling the soft-start pin below 0.25V. This can be easily done by using an external small signal transistor. During shutdown both MOSFET drivers will be turned off. Normal operation will resume by cycling soft start pin.

Operating Frequency Selection

The switching frequency is determined by connecting an external resistor (Rt) to ground. Fig. 18 provides a graph of oscillator frequency versus Rt. The maximum recommended channel frequency is 600kHz.

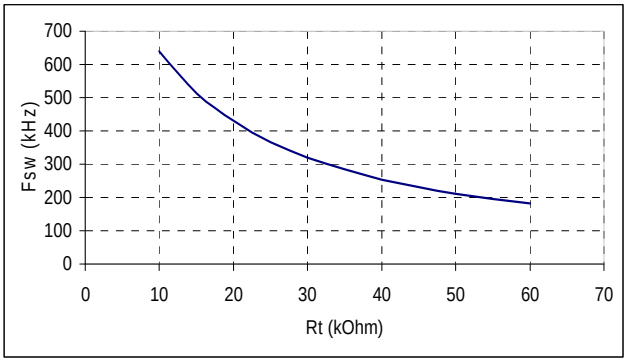


Fig. 18: Switching Frequency vs. External Resistor (R_t)

Frequency Synchronization

The iP1206 is capable of accepting an external digital synchronization signal. Synchronization will be enabled by the rising edge at an external clock. Per–channel switching frequency is set by external resistor (Rt). The free running frequency oscillator frequency is twice the per-channel frequency. During synchronization, Rt is selected such that the free running frequency is 20% below the synchronization frequency. Synchronization capability is provided for both single output current share mode and dual output configuration. When unused, the sync pin will remain floating and is noise immune.

Thermal Shutdown

Temperature sensing is provided inside iP1206. The trip threshold is typically set to 135ºC. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs. Thermal shutdown is not latched and automatic restart is initiated when the sensed temperature drops to normal range. There is a 20ºC hysteresis in the shutdown threshold.

Application Information

Design Example:

The following example is a typical application for iP1206. The application circuit is shown in page25.

$V_{in} = 12V, (13.2V, \max)$
$V_o = 1.2V$
$I_o = 30A$
$\Delta V_o \le 30mV$
$F_s = 300kHz$

Output Voltage Programming

Output voltage is programmed by the reference voltage and an external voltage divider. The Fb pin is the inverting input of the error amplifier, which is internally referenced to 0.8V. The divider ratio is chosen to provide 0.8V at the Fb pin when the output is at its desired value. The output voltage is defined by using the following equation:

$$V_o = V_{REF} * \left(1 + \frac{R_6}{R_5}\right) \quad ----(6)$$

When an external resistor divider is connected to the output as shown in Fig. 19.

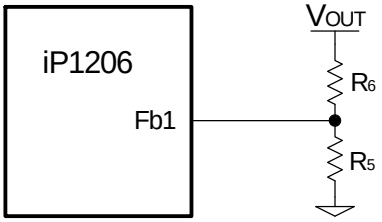


Fig. 19: Typical application of the iP1206 for programming the output voltage

Equation (6) can be rewritten as:

$$R_5 = R_6 * \left(\frac{V_{ref}}{V_o - V_{ref}}\right) \quad ----(7)$$

For the calculated values of R_5 and R_6 see feedback compensation section.

Soft-Start Programming

The soft-start timing can be programmed by selecting the soft-start capacitance value. The start-up time of the converter can be calculated by using:

$$C_{SS} \cong 20\mu A * T_{start} \quad ----(8)$$

Where T_{start} is the desired start-up time (ms)
For a start-up time of 5ms, the soft-start capacitor will be 0.1uF. Choose a ceramic capacitor at 0.1uF.

Input Capacitor Selection

The 180º out of phase feature will reduce the RMS value of the ripple current seen by input capacitors. This reduces numbers of input capacitors. The input capacitors selected must handle both the maximum ripple RMS at highest ambient temperature as well as the maximum input voltage. The RMS value of current ripple for duty cycle under 50% is expressed by:

$$I_{RMS} = \sqrt{\left(I_1^2 D_1(1-D_1) + I_2^2 D_2(1-D_2) - 2I_1 I_2 D_1 D_2\right)} \quad ----(9)$$

Where:
-I_{RMS} is the RMS value of the input capacitor current
-D_1 and D_2 are the duty cycle for each channel
-I_1 and I_2 are the output current for each channel

For Io=30A and D=0.10, the I_{RMS}= 12A.

Ceramic capacitors are recommended due to their peak current capabilities, they also feature low ESR and ESL at higher frequency which enhance better efficiency,
Use 8x22uF, 16V ceramic capacitor from TDK (C3225X5R1C226M).

For the single output application when the duty cycle is larger than 50% the following equation can be used to calculate the total RMS value input capacitor current:

$$I_{RMS} = I_o \sqrt{(2D(1-D) + (2-2D))} \qquad D > 0.5$$

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value causes a large ripple current, resulting in a smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to the choice of desired maximum ripple current (Δi) in the inductor. The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{in} - V_o = L * \frac{\Delta i}{\Delta t};\quad \Delta t = D * \frac{1}{F_s}$$

$$L = (V_{in} - V_o) * \frac{V_o}{V_{in} * \Delta i * F_s} \qquad ----(10)$$

Where:

V_{in} = *Maximum input voltage*

V_o = *Output Voltage*

Δi = *Inductor ripple current*

F_s = *Switching frequency*

Δt = *Turn on time*

D = *Duty cycle*

For 2-phase single output application the inductor ripple current is chosen between 10-40% of maximum phase current

If $\Delta i \approx 12\%(I_o)$, then the output inductor will be:

L = 1uH

The Delta MPL105-1R0IR (L_1=1uH, 25A, R_{L1}=2.3mOhm) provides a low profile inductor suitable for this application.
Use the following equation to calculate C_{12} and R_{12} for current sensing:

$$R_{12} * C_{12} = \frac{L_1}{R_{L1}}$$

This results to C_{12}=1uF and R_{12}=402Ohm

Output Capacitor Selection

The voltage ripple and transient requirements determine the output capacitors types and values. The criteria is normally based on the value of the Effective Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing components, these components can be described as:

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

$$\Delta V_{o(ESR)} = \Delta I_L * ESR \qquad ----(11)$$

$$\Delta V_{o(ESL)} = \left(\frac{V_{in}}{L}\right) * ESL$$

$$\Delta V_{o(C)} = \frac{\Delta I_L}{8 * C_o * F_s}$$

ΔV_o = *Output voltage ripple*

ΔI_L = *Inductor ripple current*

Since the output capacitor has a major role in overall performance of converter and determines the result of transient response, the selection of capacitors is critical. The iP1206 can perform well with all types of capacitors.

As a rule the capacitor must have low enough ESR to meet output ripple and load transient requirements, yet have high enough ESR to satisfy stability requirements.

The goal for this design is to meet the voltage ripple requirement in smallest possible capacitor size. Therefore ceramic capacitors are selected due to low ESR and small size.

Panasonic ECJ24YB0J107M (4*100uF, 6.3V, X5R and EIA 1210 case size) are a good choice.

In the case of tantalum or low ESR electrolytic capacitors, the ESR dominates the output voltage ripple, equation (13) can be used to calculate the required ESR for the specific voltage ripple.

Feedback Compensation

The iP1206 is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45º).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180º (see Fig. 20). The resonant frequency of the LC filter expressed as follows:

$$F_{LC} = \frac{1}{2*\pi\sqrt{L_o * C_o}} \qquad ----(12)$$

Since we already have 180º phase shift just from the output filter, the system risks being unstable.

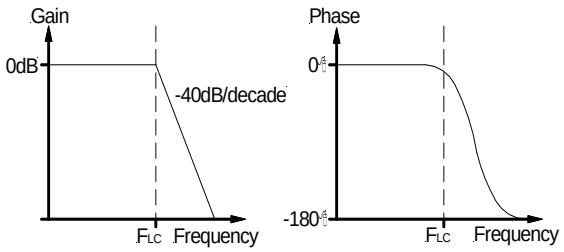


Fig. 20: Gain and Phase of LC filter

The iP1206's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control or AC phase compensation.

The E/A can be compensated either in type II or type III compensation. When it is used in type II compensation the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in Fig. 21.

This method requires that the output capacitor should have enough ESR to satisfy stability requirements. In general the output capacitor's ESR generates a zero typically at 5kHz to 50kHz which is essential for an acceptable phase margin. The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2*\pi*ESR*C_o} \qquad ----(13)$$

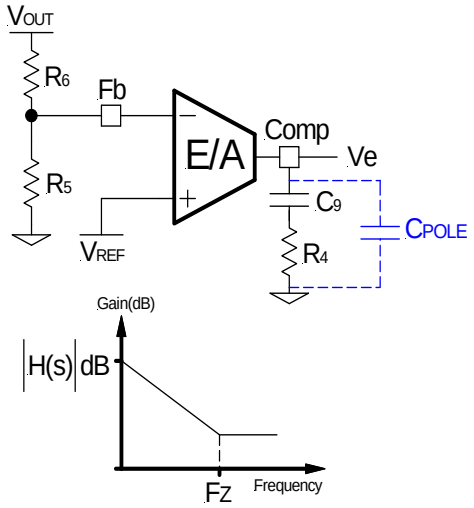


Fig. 21: TypeII compensation network and its asymptotic gain plot

The transfer function (Ve/Vo) is given by:

$$H(s) = \left(g_m * \frac{R_5}{R_5 + R_6}\right) * \frac{1 + sR_4C_9}{sC_9} \qquad ----(14)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$[H(s)] = \left(g_m * \frac{R_5}{R_5 + R_6}\right) * R_4 \qquad ----(15)$$

$$F_z = \frac{1}{2\pi * R_4 * C_9} \qquad ----(16)$$

The gain is determined by the voltage divider and E/A's transconductance gain.
First select the desired zero-crossover frequency (Fo):

$$F_o > F_{ESR} \text{ and } F_o \le (1/5 \sim 1/10) * F_s$$

Use the following equation to calculate R_4:

$$R_4 = \frac{V_{osc} * F_o * F_{ESR} * (R_5 + R_6)}{V_{in} * F_{LC}^2 * R_5 * g_m} \qquad ----(17)$$

Where:

V_{in} = Maximum Input Voltage
V_{osc} = Oscillator Ramp Voltage
F_o = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
g_m = Error Amplifier Transconductance

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_z = 75\% F_{LC}$$

$$F_z = 0.75 * \frac{1}{2\pi\sqrt{L_o * C_o}} \qquad ----(18)$$

Using equations (16) and (18) to calculate C9.

$$C_9 = \frac{1}{2\pi * R_4 * F_z}$$

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to suppress the switching noise.
The additional pole is given by:

$$F_P = \frac{1}{2\pi * R_4 * \frac{C_9 * C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi * R_4 * F_s - \frac{1}{C_9}} \cong \frac{1}{\pi * R_4 * F_s}$$

$$For\ F_P << \frac{F_s}{2}$$

For a general solution for unconditionally stability and any type of output capacitors, in a wide range of ESR values we should implement local feedback with a compensation network (typeIII). The typically used compensation network for voltage-mode controller is shown in Fig. 22.

In such configuration, the transfer function is given by:

$$\frac{V_e}{V_o} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m * Z_f >> 1 \ \ and \ \ g_m * Z_{in} >> 1 \qquad ----(19)$$

By replacing Z_{in} and Z_f according to figure 15, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{11} + C_{12})} * \frac{(1 + sR_7C_{11}) * [1 + sC_{10}(R_6 + R_8)]}{\left[1 + sR_7\left(\frac{C_{11} * C_{12}}{C_{11} + C_{12}}\right)\right] * (1 + sR_8C_{10})}$$

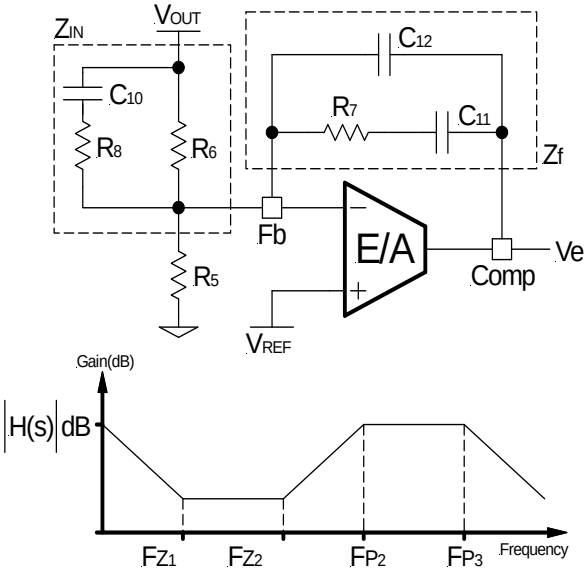


Fig. 22: Compensation network with local feedback and its asymptotic gain plot

As known, transconductance amplifiers have high impedance (current source) outputs, therefore, care should be taken when loading the E/A output. It may exceed its source/sink output current capability, so that the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi * R_8 * C_{10}}$$

$$F_{P3} = \frac{1}{2\pi * R_7\left(\frac{C_{11} * C_{12}}{C_{11} + C_{12}}\right)} \cong \frac{1}{2\pi * R_7 * C_{12}}$$

$$F_{z1} = \frac{1}{2\pi * R_7 * C_{11}}$$

$$F_{z2} = \frac{1}{2\pi * C_{10} * (R_6 + R_8)} \cong \frac{1}{2\pi * C_{10} * R_6}$$

Cross over frequency is expressed as:

$$F_o = R_7 * C_{10} * \frac{V_{in}}{V_{osc}} * \frac{1}{2\pi * L_o * C_o}$$

Based on the frequency of the zero generated by output capacitor and its ESR versus crossover frequency, the compensation type can be different. The table below shows the compensation types and location of crossover frequency.

Compensator type	F_{ESR} vs. F_o	Output capacitor
TypII(PI)	$F_{LC}<F_{ESR}<F_o<F_{s/2}$	Electrolytic , Tantalum
TypeIII(PID) **Method A**	$F_{LC}<F_o<F_{ESR}<F_{s/2}$	Tantalum, ceramic
TypeIII(PID) **Method B**	$F_{LC}<F_o<F_{s/2}<F_{ESR}$	Ceramic

Table1- The compensation type and location of F_{ESR} versus F_o

The details of these compensation types are discussed in application note AN-1043 which can be downloaded from the IR Web-Site.

For this design we have:

V_{in}=12V
V_o=1.2V
V_{osc}=1.25V
V_{ref}=0.8V
g_m=2800umoh
L_o=1uH, DCR=2.4mOhm
C_o=15x22uF, ESR= 0.33mOhm
F_s=300kHz

These result to:

F_{LC}=10.73kHz

(Replace L to L/2 in formula#14 for current share configuration)

F_{ESR}=1.46MHz

$F_{s/2}$=150kHz

Select crossover frequency:

$F_o < F_{ESR}$ and $F_o \le (1/5 \sim 1/10) * F_s$

F_o=40kHz

Since: $F_{LC}<F_o<F_{s/2}<F_{ESR}$, typeIII method B is selected to place the pole and zeros.

The following design rules will give a crossover frequency approximately one-sixth of the switching frequency. The higher the band width, the potentially faster the load transient response. The DC gain will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45º for overall stability.
Desired Phase Margin: $\Theta_{\max} = \frac{\pi}{3}$

$$F_{Z2} = F_o * \sqrt{\frac{1-Sin\Theta}{1+Sin\Theta}}$$
$$F_{Z2} = 10.72kHz$$

$$F_{P2} = F_o * \sqrt{\frac{1+Sin\Theta}{1-Sin\Theta}}$$
$$F_{P2} = 81.2kHz$$

$Select: F_{Z1} = 0.5 * F_{Z2}$ and $F_{P3} = 0.5 * F_s$

$$R_7 \ge \frac{2}{g_m}; R_7 \ge 0.72K\Omega; \quad Select: R_7 = 6.81K\Omega$$

Calculate C_{11}, C_{12} and C_{10} :

$$C_{11} = \frac{1}{2\pi * F_{Z1} * R_7}; C_{11} = 4.36nF, \quad Select: C_{11} = 5.6nF$$

$$C_{12} = \frac{1}{2\pi * F_{P3} * R_7}; C_{12} = 155pF, \quad Select: C_{12} = 100pF$$

$$C_{10} = \frac{2\pi * F_o * L_o * C_o * V_{osc}}{R_7 * V_{in}}; C_{10} = 0.85nF,$$

$Select: C_{10} = 1nF$

Calculate R_8, R_6 and R_5 :

$$R_8 = \frac{1}{2\pi * C_{10} * F_{P2}}; R_8 = 1.96K\Omega, \quad Select: R_8 = 2K\Omega$$

$$R_6 = \frac{1}{2\pi * C_{10} * F_{Z2}} - R_8; R_6 = 13.9K\Omega, \quad Select: R_6 = 16.9K\Omega$$

$$R_5 = \frac{V_{ref}}{V_o - V_{ref}} * R_6; R_5 = 39.2K\Omega, \quad Select: R_5 = 39.2K\Omega$$

Compensation for Current Loop (slave channel)

The slave error amplifier is differential transconductance amplifier, in 2-phase configuration the main goal for the slave channel feedback loop is to control the inductor current to match the master channel inductor current as well provides highest bandwidth and adequate phase margin for overall stability. The following analysis is valid for both using external current sense resistors and using DCR of inductor.

The transfer function of power stage is expressed by:

$$G(s)=\frac{I_{L2}(s)}{V_e}=\frac{V_{in}}{sL_2*V_{osc}} \qquad ----(20)$$

Where:
V_{in}=Input voltage
L_2=Output inductor
V_{osc}=Oscillator Peak Voltage

As shown the G(s) is a function of inductor current. The transfer function for compensation network is given by equation (21), when using a series RC circuit as shown in Fig 23.

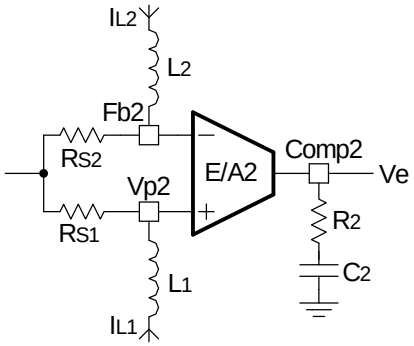


Fig. 23: The Compensation network for current loop

$$D(s)=\frac{V_e(s)}{R_{s2}}=\left(g_m*\frac{R_{s1}}{R_{s2}}\right)*\left(\frac{1+sC_2R_2}{sC_2}\right) \qquad ----(21)$$

The loop gain function is:

$$H(s)=[G(s)*D(s)*R_{s2}]$$

$$H(s)=R_{s2}*\left(g_m*\frac{R_{s1}}{R_{s2}}\right)*\left(\frac{1+sR_2C_2}{sC_2}\right)*\left(\frac{V_{in}}{sL_2*V_{osc}}\right)$$

Select a zero frequency for current loop (F_{o2}) 1.5 times larger than zero cross frequency for voltage loop (F_{o1}).

$$F_{O2}\cong 1.5*F_{O1}$$

$$H(F_{O2})=g_m*R_{s1}*R_2*\frac{V_{in}}{2\pi*F_{O2}*L_2*V_{osc}}=1 \qquad ----(22)$$

From (22), R2 can be expressed as:

$$R_2=\frac{1}{g_m*R_{s1}}*\frac{2\pi*F_{O2}*L_2*V_{osc}}{V_{in}} \qquad ----(23)$$

V_{in}=12V
V_{osc}=1.25V
g_m=2800umoh
L_2=1uH
R_{s1}=DCR=2.4mOhm
F_{o2}=60kHz

This results to : R_2=5.84K

The power stage of current loop has a dominant pole (Fp) at frequency expressed by:

$$F_P=\frac{R_{eq}}{2\pi*L_2}$$

$$R_{eq}=R_{ds(on1)}*D+R_{ds(on2)}*(1-D)+R_L$$

Where Rds(on1) is the on-resistance of control FET, Rds(on2) is the on-resistance of synchronous FET, RL is the DCR of output inductance and D is the duty cycle

Req=9.48mOhm

$$R_{eq}=R_{ds(on)}+R_L+R_s$$

Set the zero of compensator at 10 times the dominant pole frequency FP, the compensator capacitor, C2 can be expressed as:

$$F_z=10*F_P$$

$$C_2=\frac{1}{2\pi*R_2*F_z}$$

C2=1nF
All designs should be tested for stability to verify the calculated values.

Programming the Current-Limit

The Current-Limit threshold can be set by connecting a resistor (R_{OCSET}) from drain of low side MOSFET to the OCSet pin. The resistor value can be obtained by using Fig. 24.

It is important to pay careful attention to the layout of this resistor. It is recommended to place this resistor close to the IC and away from possible noisy traces. A small ceramic capacitor from this pin to ground can also be place for noise rejection purposes.

The trip current Itrip is given by:

$$I_{trip} = I_{\max} + I_{L,Peak} \quad ----(7)$$

where

$I_{\max}$ = *Maximum DC load current* 1.5*

$I_{L,Peak=}$ *Peak Inductor Current*

For a maximum DC load current of 8.5A and an inductor ripple of 3A

$I_{L,Peak} = 1.5A$

$\Rightarrow I_{trip} = 8.5*1.5+1.5A = 14.25A$

From Fig. 24 we get $R_{OCSET} = 5.23K\Omega$

Note: $I_{L,Peak} = \frac{\Delta i}{2} = \frac{(V_{in} - V_o) * \frac{V_o}{V_{in} * L * F_s}}{2}$

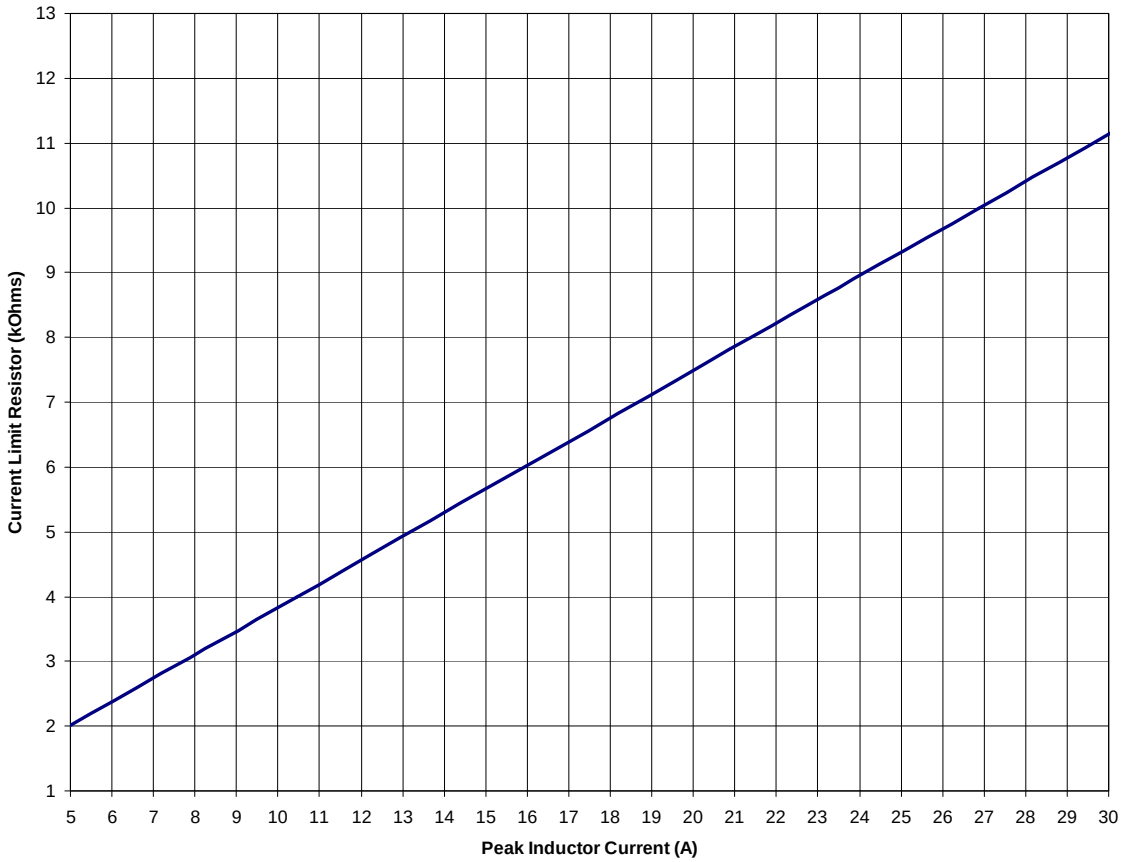


Fig. 24: R_{OCSET} selection from Peak Inductor Current

Typical Application Circuit

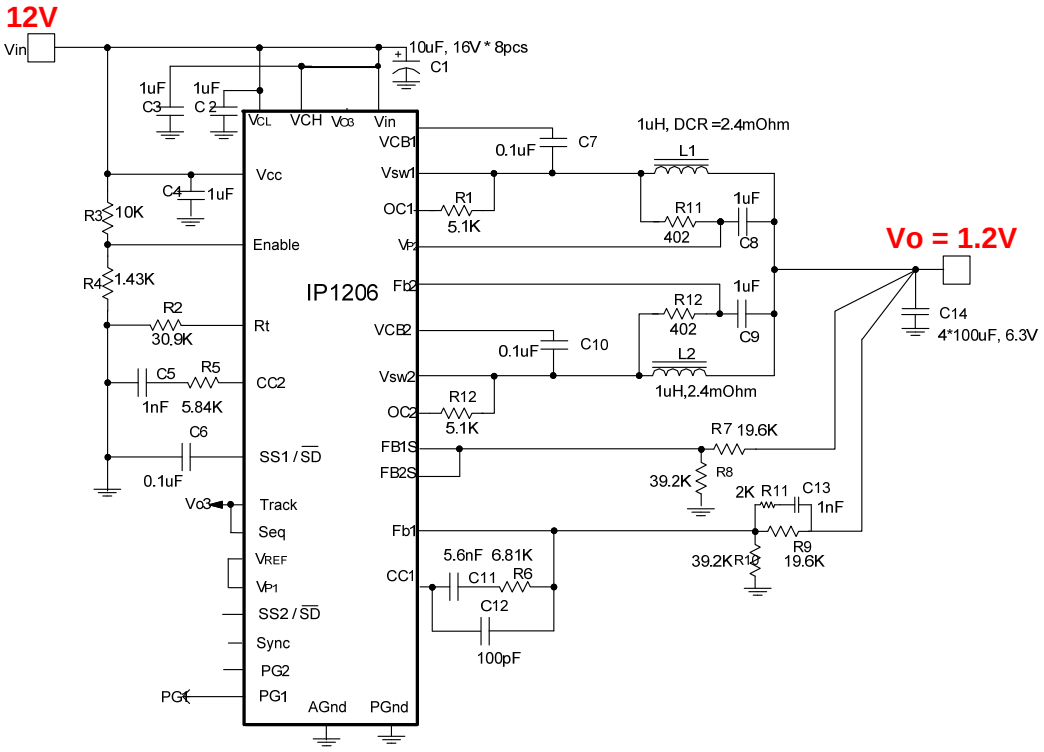


Fig. 25a: Typical Single Output Application circuit for 12V to 1.2V @ 30A

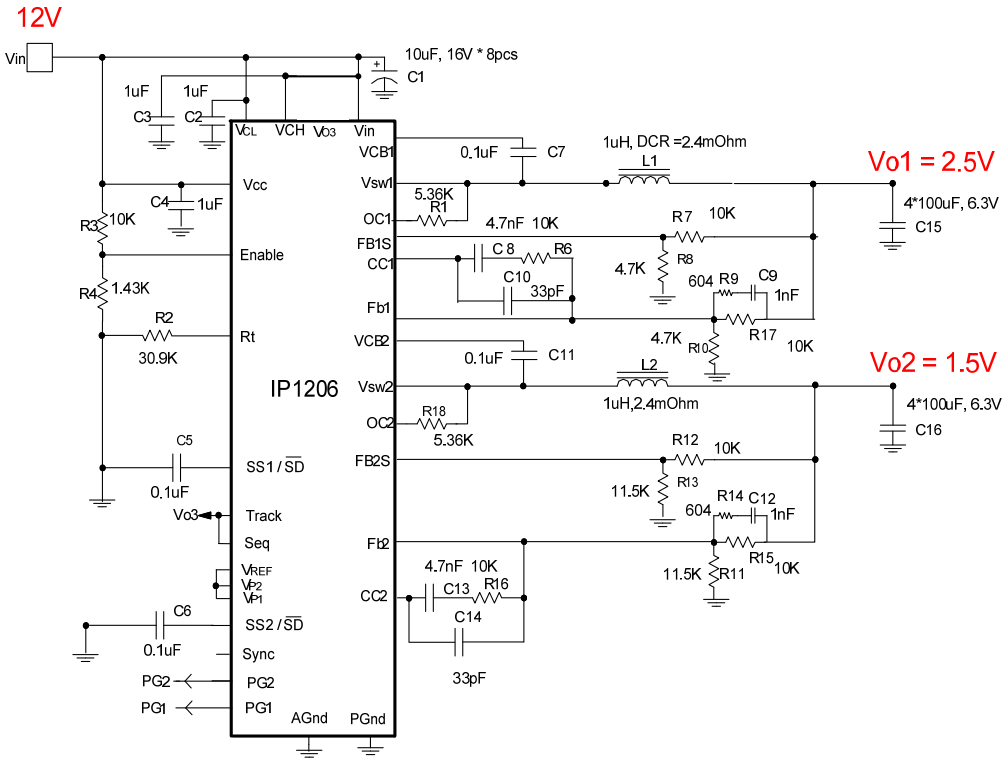


Fig. 25b: Typical Dual Output Application circuit for 12V to 2.5V @ 15A , 12V to 1.5V@ 15A

Recommended PCB Footprint

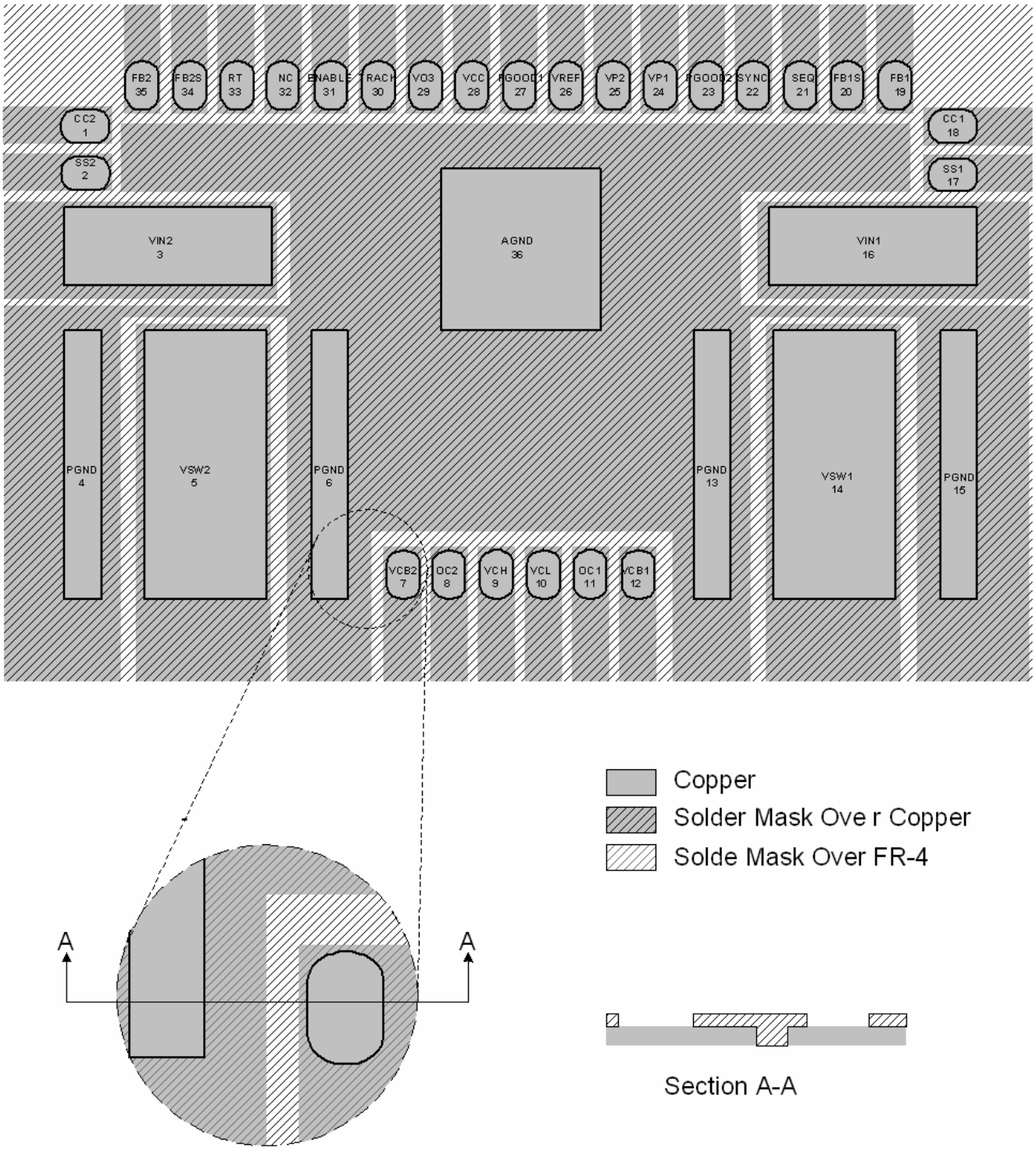


Fig. 26

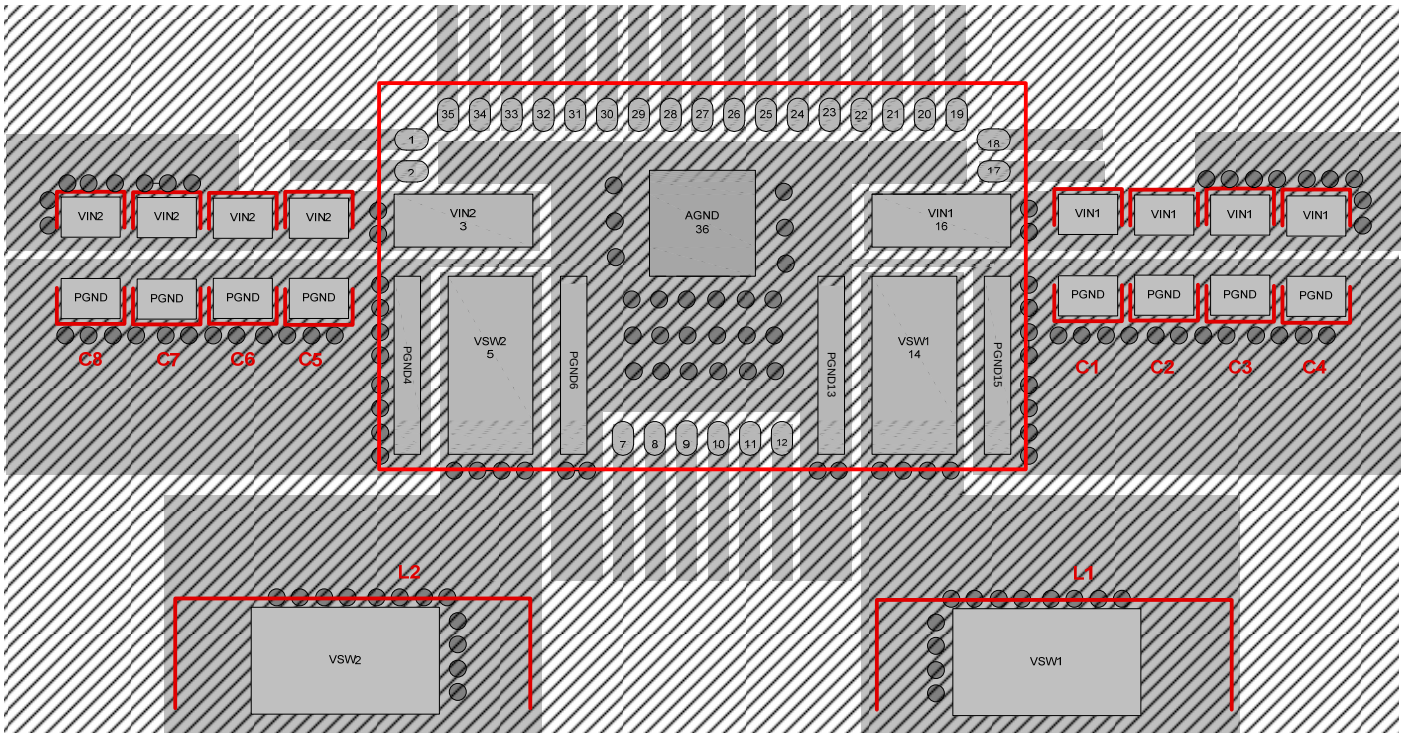


Fig. 27 Top component and via placement (Topside, transparent view down)

PCB Layout Guidelines

The following guidelines are recommended to reduce the parasitic values and optimize overall performance.

• All pads on the iP1206 footprint design need to be Solder-mask defined (see Figure 26). Also refer to International Rectifier application notes AN1028 and AN1029 for further footprint design guidance.

• Place as many vias around the Power pads (VIN, VSW, and PGND) for both electrical and optimal thermal performance.

• Vias in between the different power pads may overlap the pad opening and solder mask edge without the need to plug the via hole. Vias with a 13mil drill hole and 25mil capture pad were used in this example.

• A minimum of six 10µF, X5R, 16V ceramic capacitors per iP1206 are recommended for the lowest loss due to input capacitor ESR.

• Placement of the ceramic input capacitors is critical to optimize switching performance. In cases where there is a space constraint on the top layer capacitors C3,C4, C7 and C8 can be placed on the bottom layer directly below the footprints of C1, C2, C5 and C6.

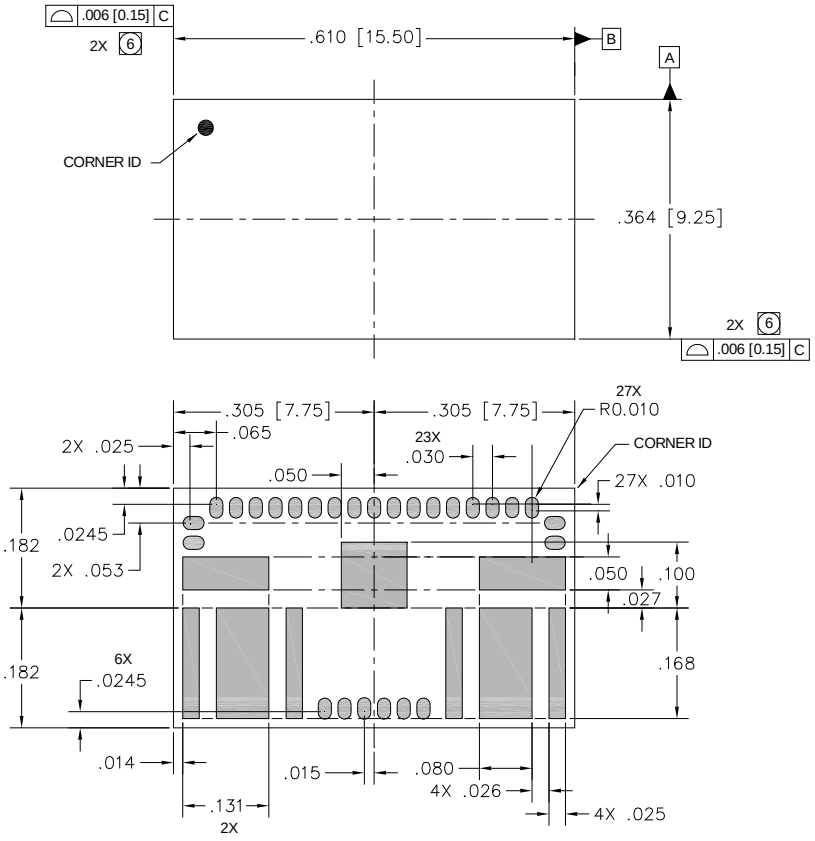
• Dedicate at least two layers for PGND only.

• Duplicate the Power Nodes on multiple layers (refer to AN1029).

• Refer to AN-1030 for information on applying IPOWIR products in your thermal environment for Safe Operation.

Mechanical Outline

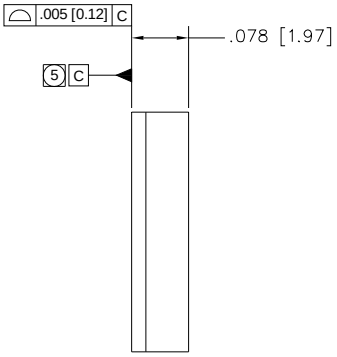
TOP VIEW



IR CONFIDENTIAL DOCUMENT

NOTES:

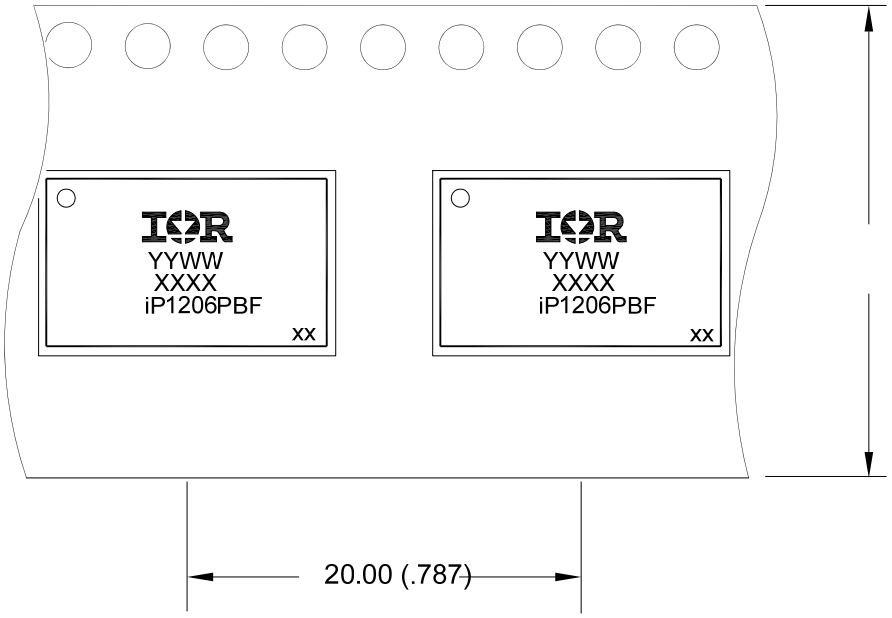
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN INCHES[MILLIMETERS].
3. CONTROLLING DIMENSION: INCHES
4. LAND PAD OPENINGS.
5. PRIMARY DATUM C (SEATING PLANE) IS DEFINED BY THE LAND PAD OPENINGS.
6. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
7. NOT TO SCALE.



SIDE VIEW

Fig. 28

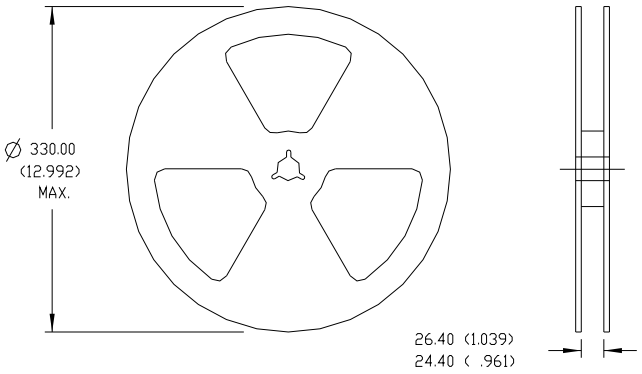
Tape and Reel Information



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.

iP1206, LGA



NOTES:

1. CONTROLLING DIMENSION: MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Fig. 29

Recommended Solder Paste Stencil Design

The recommended reflow peak temperature is 260ºC. The total furnace time is approximately 5 minutes with approximately 10 seconds at peak temperature.

SQUEEGE VIEW
RECOMMENDATED STENCIL OPENNING
ALL DIMENSION IN MM

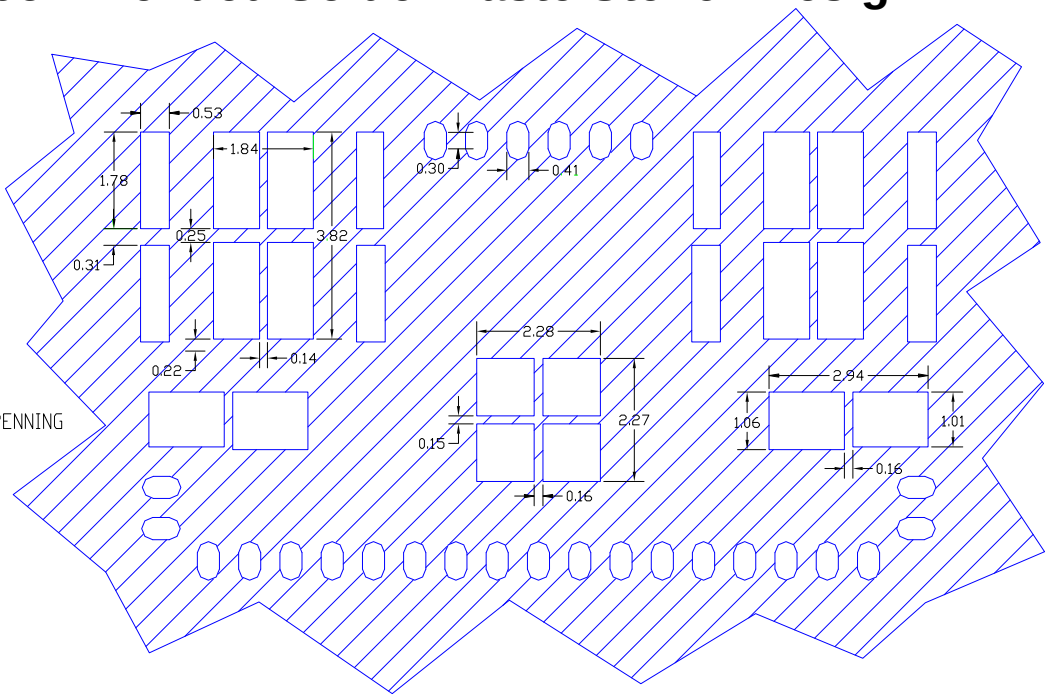


Fig. 30

Part Marking

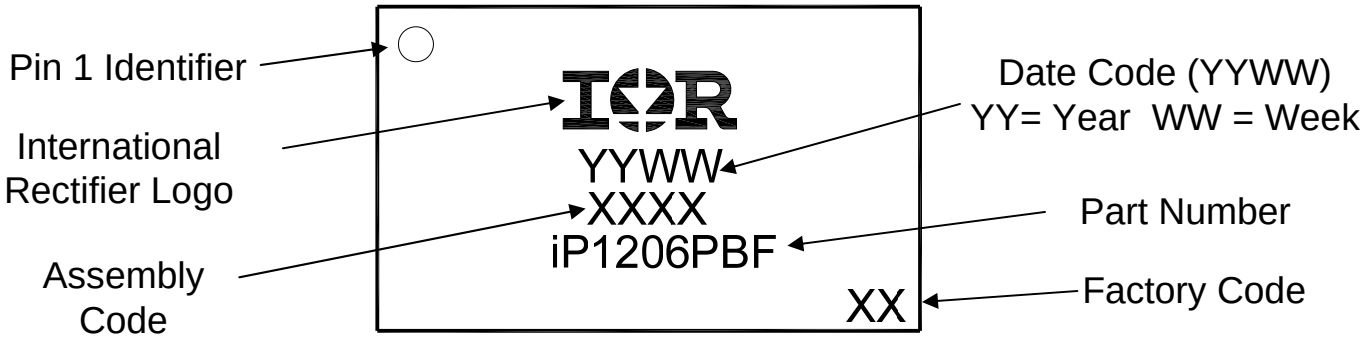


Fig. 31

International
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TAC Fax: (310) 252-7903

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