iC-HQ
HIGH-PERFORMANCE QUAD OPAMP

preliminary

iC-Haus

## FEATURES

♦ Ultra low offset (< 1 µV) and offset drift
♦ Very low load dependent offset shift
♦ Built-in offset measurement for each OPAMP
♦ 5 V single supply
♦ Low supply current, typ. 350 µA/OPAMP
♦ Unity gain stability
♦ Input common mode range down to 0 V
♦ 1 mA rail-to-rail output
♦ Very low 1/f noise
♦ 140 dB open loop gain
♦ 130 dB common mode rejection ratio
♦ 135 dB power supply rejection ratio
♦ 2.5 V/µs slew rate
♦ 3.5 MHz gain-bandwidth product
♦ Tight matching of bandwidth and slew rate among all 4 OPAMPs
♦ Short circuit proof outputs
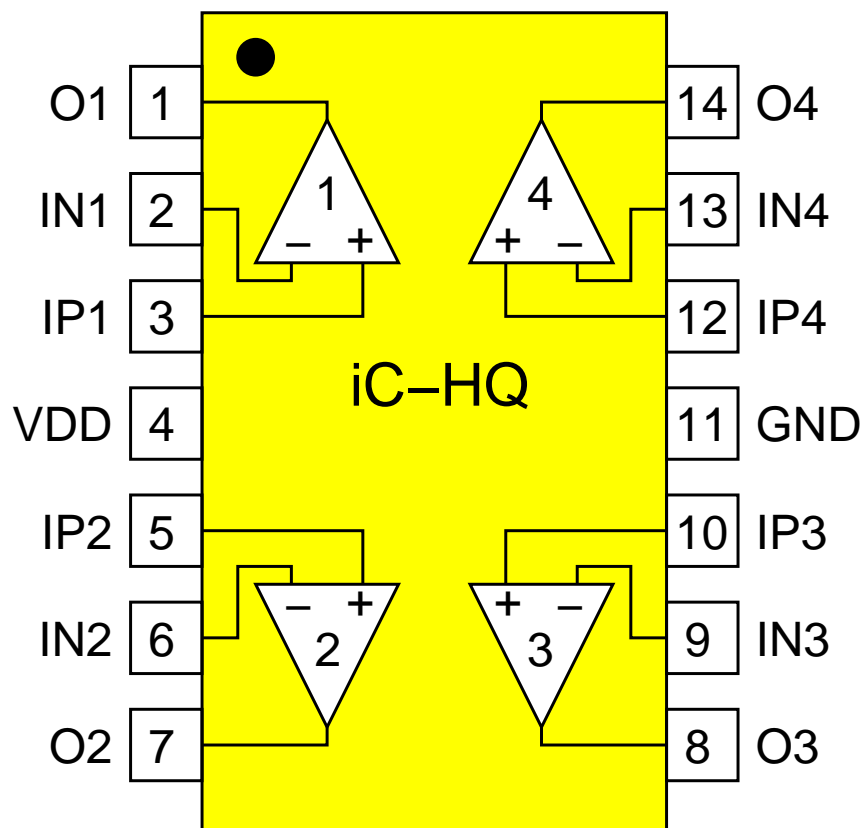
♦ **Option:** iC-HQL (< 10 µV Offset)

APPLICATIONS

♦ Measuring amplifiers
♦ Instrumentation amplifiers
♦ Signal conditioners
♦ Encoder applications
♦ Audio applications
♦ High-impedance buffers
♦ A/D and D/A converters
♦ Battery operated devices
♦ GND-sensing applications

PACKAGES

TSSOP14

BLOCK DIAGRAM
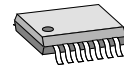
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DESCRIPTION

The iC-HQ contains four precision OPAMPs, operated from a common 5 V supply. The offset of less than 1 µV allows operation with a very high gain. The continuous offset cancellation principle results in ultra low offset temperature drift as well as exceptional suppression of the 1/f noise below 1 kHz. The validation of the specified offset voltage of each OPAMP is performed with built-in test circuitry as part of functional testing and quality assurance.

All parameters influencing precision, like open loop gain, power supply rejection ratio, common mode rejection ratio and load rejection are extremely high and add to the offset voltage only in the sub-µV range.

The 3.5 MHz gain-bandwidth makes this quad OPAMP ideally suited for signal processing tasks, where high frequencies have to be processed at a high gain. Unity gain stability is provided, thus the OPAMPs can also operate as buffers.

The low supply current of 1.4 mA is particularly advantageous in battery operated devices. The input common mode range includes GND. The rail-to-rail outputs are capable of 1 mA and are unlimited short-circuit proof.

The input current I(IPx), I(INx) is typically below 5 pA at room temperature and below 100 pA throughout the whole temperature range.

PACKAGES TSSOP14 to JEDEC

PIN CONFIGURATION TSSOP14
(top view)
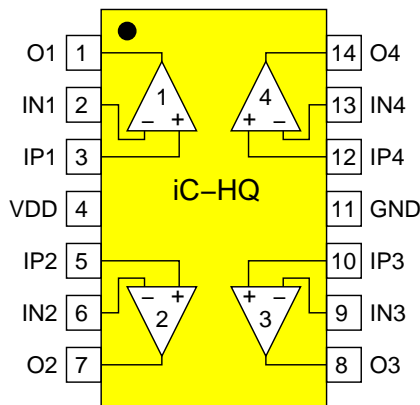
PIN FUNCTIONS

No.	Name	Function
1	O1	Output OPAMP1
2	IN1	Neg. input OPAMP1
3	IP1	Pos. input OPAMP1
4	VDD	Voltage supply
5	IP2	Pos. input OPAMP2
6	IN2	Neg. input OPAMP2
7	O2	Output OPAMP2
8	O3	Output OPAMP3
9	IN3	Neg. input OPAMP3
10	IP3	Pos. input OPAMP3
11	GND	Ground
12	IP4	Pos. input OPAMP4
13	IN4	Neg. input OPAMP4
14	O4	Output OPAMP4

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ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Supply Voltage		-0.5	6	V
G002	I(VDD)	Current in VDD		-10	80	mA
G003	V()	Voltage at IPx, INx		-0.5	VDD + 0.5	V
G004	I()	Current in IPx, INx		-5	5	mA
G005	V()	Voltage at Ox	Referenced to GND, V(Ox) < VDD + 0.5 V	-0.5	6	V
G006	I()	Current in Ox		-30	30	mA
G007	VDiff()	Input Difference Voltage	$V(IPx) - V(INx)$	-6	6	V
G008	Vd()	Susceptibility to ESD at all pins	HBM, 100 pF discharged through 1.5 kΩ		1	kV
G009	Ts	Storage Temperature Range		-40	150	°C
G010	Tj	Operating Junction Temperature		-40	150	°C

THERMAL DATA

Operation Conditions: VDD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C
T02	Rthja	Thermal Resistance Chip/Ambient	SMD assembly, no additional cooling areas			140	K/W

All voltages are referenced to ground unless otherwise stated.
All currents into the device pins are positive; all currents out of the device pins are negative.

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ELECTRICAL CHARACTERISTICS

Operation Conditions: VDD = 5 V ±10 %, Tj = -40...125 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Supply Voltage		4.5		5.5	V
002	I(VDD)	Supply Current in VDD	Total iC, all 4 OPAMPs without load	1.2	1.5	2	mA
003	Vc(hi)	Clamp Voltage hi at Ox	VDD = 0 V, I() = 10 mA	0.3		1.5	V
004	Vc(lo)	Clamp Voltage lo at Ox	VDD = 0 V, I() = -10 mA	-1.5		-0.3	
005	Vc(hi)	Clamp Voltage hi IPx, INx	VDD = 0 V, I() = 1 mA	0.3		1.8	V
006	Vc(lo)	Clamp Voltage lo IPx, INx	VDD = 0 V, I() = -1 mA	-1.5		-0.3	V
007	CMRR	Common Mode Rejection Ratio	$\Delta V_{os}/\Delta V_{cm}$ bei ΔV_{cm} = 3.5 V	125	130		dB
008	PSRR	Power Supply Rejection Ratio		125*	135		dB
009	A_{V0}	Open Loop Gain	RL = 1 kΩ	130	140		dB
010	LRR	Offset Shift vs. Power Dissipation	ΔV_{os} at ΔP_v(O1...4) = 1 mW	-0.3	0	0.3	µV
Inputs IN1...4, IP1...4							
101	V_{os}	Offset Voltage	V()cm = 1.5 V, closed loop operation; iC-HQ Tj = -40...27 °C iC-HQ Tj = -40...125 °C iC-HQL	-1 -1 -10	0 0 	1 1.6 10	µV µV µV
102	dV_{os}/dT	Offset Voltage Drift	Tj = -40...125 °C	-0.01*		0.01*	µV/°C
103	Ib()	Input Current I(IPx), I(INx)			5	400	pA
104	I_{os}()	Input Offset Current		-400		400	pA
105	V_{cm}()	Input Voltage Range		-0.1		VDD − 1.1	V
Outputs O1...4							
201	V()hi	Output Voltage hi at Ox	VDD = 5 V, RL = 100 kΩ vs. GND	4.95	4.987		V
202	V()lo	Output Voltage lo at Ox	RL = 100 kΩ vs. VDD		11	30	mV
203	Vs()hi	Saturation Voltage hi at Ox	Vs()hi = VDD − V(Ox), I() = -1.2 mA		250	600	mV
204	Vs()lo	Saturation Voltage lo at Ox	I() = 1.2 mA		125	250	mV
205	Isc()hi	Short Circuit Current from Ox	Short circuit Ox to GND	-30	-12	-5	mA
206	Isc()lo	Short Circuit Current in Ox	Short circuit Ox to VDD	1.5	3.4	8	mA
Dynamic Parameters							
301	SR	Slew Rate at Ox	RL = 10 kΩ, Av = -1, CL = 15 pF	1.75	2.5	3.6	V/µs
302	GBP	Gain bandwidth product	RL = 10 kΩ, CL = 15 pF		3.5		MHz
303	t_{set14}	Settling time 14 Bit	1 V step, Av ≤ 100, 14 Bit		350	500*	µs
304	t_{set10}	Settling time 10 Bit	1 V step, Av ≤ 100, 10 Bit		150	300	µs
305	t_{on}	Start-up time			100	200	µs
306	V_{noise}	Noise voltage	Referenced to the input up to 1 Hz		600		nV_{SS}
307	e_n	Noise density	f = 3.5 kHz...3.5 MHz f = 2...10 kHz f = 100 Hz...5 kHz f = 1...100 Hz		38 70 134 160		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$

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* Projected values by sample characterization.

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ELECTRICAL CHARACTERISTICS: Diagrams

Figure 1: Noise spectra at Av = 100

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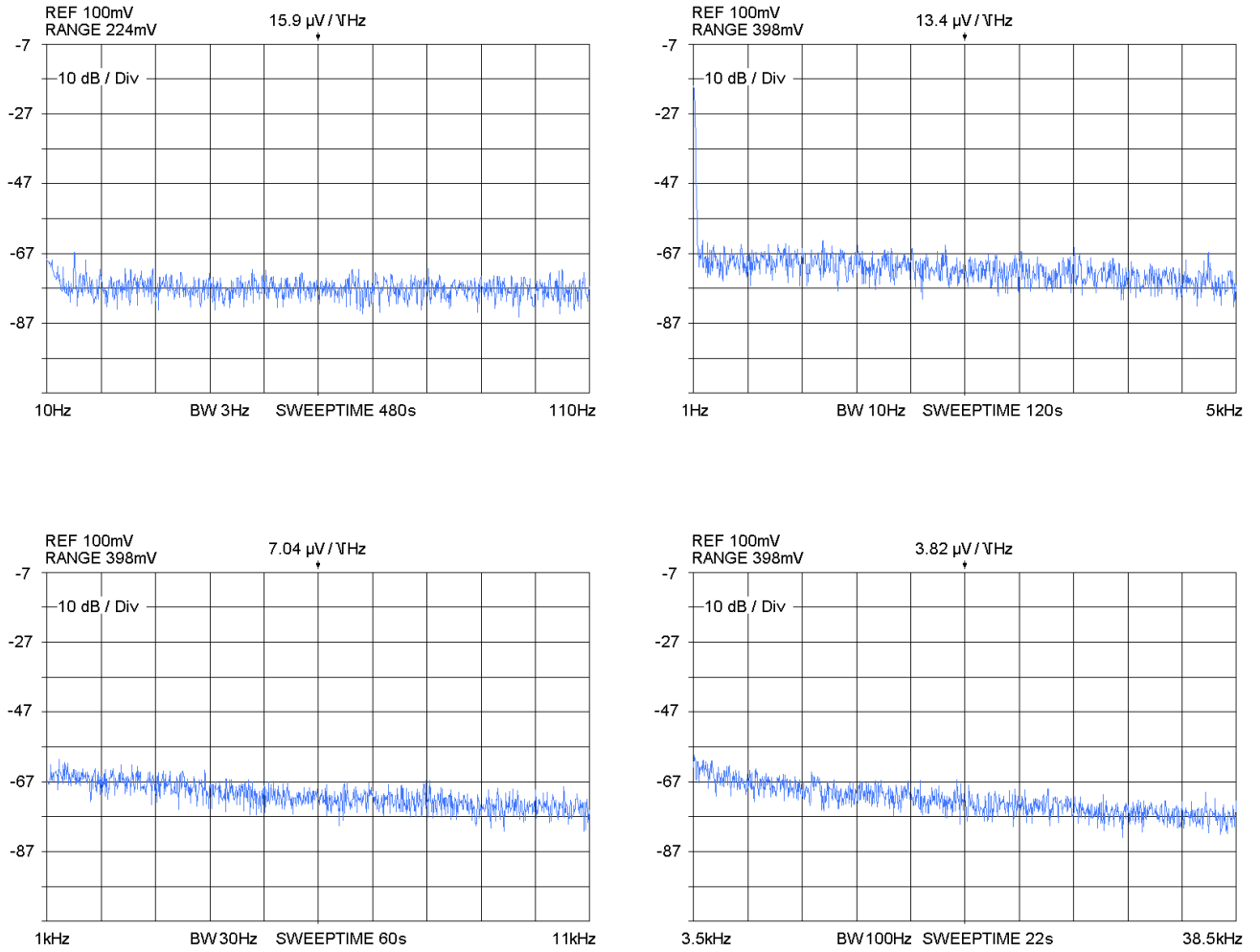
APPLICATIONS INFORMATION

To preserve the offset specification of a precision device like the iC-HQ, the soldering points of both the iC and the external circuitry must not be exposed to different temperatures. Such sensitive devices must not be positioned near heat sources. Temperature differences at metallic junctions cause contact electrification which appears like offset voltage. In the worst case, this contact voltage may even exceed the OPAMP's intrinsic offset by a wide margin.

Under no circumstances should the temperature behaviour of such a module (designed for 1 µV offset) be tested using e.g. a hot air blower. Even measurements conducted in a climatic test cabinet require a steady, constant temperature.

The offset specification of the iC-HQ is – due to the offset cancellation principle – only valid for closed loop operation. Therefore, the comparator mode requires a feedback to maintain its precision. A signal, which drives the OPAMP out of its control range for a short time, e.g. a steep input transition, in a follower configuration, is tolerable and will show the desired output response with high slew rate. In an open loop configuration, the continuous offset cancellation does not work.

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ORDERING INFORMATION

Type	Package	Order Designation
iC-HQ (1 µV)	TSSOP14	iC-HQ TSSOP14
iC-HQL (10 µV)	TSSOP14	iC-HQL TSSOP14

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