

## Summary

The Xilinx Automotive (XA) Spartan®-3A DSP family of FPGAs solves the design challenges in most high-volume, cost-sensitive, high-performance DSP automotive applications. The two-member family offers densities ranging from 1.8 to 3.4 million system gates, as shown in [Table 1](#).

## Introduction

XA devices are available in both extended-temperature Q-Grade (–40°C to +125°C T<sub>J</sub>) and I-Grade (–40°C to +100°C T<sub>J</sub>) and are qualified to the industry recognized AEC-Q100 standard.

The XA Spartan-3A DSP family builds on the success of the earlier XA Spartan-3E and XA Spartan-3 FPGA families by adding hardened DSP MACs with pre-adders, significantly increasing the throughput and performance of this low-cost family. These XA Spartan-3A DSP family enhancements, combined with proven 90 nm process technology, deliver more functionality and bandwidth per dollar than ever before, setting the new standard in the programmable logic industry.

Because of their exceptionally low cost, XA Spartan-3A DSP FPGAs are ideally suited to a wide range of automotive electronics applications, including infotainment, driver information, and driver assistance modules.

The XA Spartan-3A DSP family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial mask set costs and lengthy development cycles, while also permitting design upgrades in the field with no hardware replacement necessary because of its inherent programmability, an impossibility with conventional ASICs and ASSPs with their inflexible architecture.

## Features

- Very low cost, high-performance DSP solution for high-volume, cost-conscious applications
- 250 MHz DSP48A slices using XtremeDSP™ solution
  - ◆ Dedicated 18-bit by 18-bit multiplier
  - ◆ Available pipeline stages for enhanced performance of at least 250 MHz in the standard -4 speed grade
  - ◆ 48-bit accumulator for multiply-accumulate (MAC) operation
- ◆ Integrated adder for complex multiply or multiply-add operation
- ◆ Integrated 18-bit pre-adder
- ◆ Optional cascaded Multiply or MAC
- Dual-range V<sub>CCAUX</sub> supply simplifies 3.3V-only design
- Suspend and Hibernate modes reduce system power
- Multi-voltage, multi-standard SelectIO™ interface pins
  - ◆ Up to 519 I/O pins or 227 differential signal pairs
  - ◆ LVCMOS, LVTTTL, HSTL, and SSTL single-ended I/O
  - ◆ 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
  - ◆ Selectable output drive, up to 24 mA per pin
  - ◆ QUIETIO standard reduces I/O switching noise
  - ◆ Full 3.3V ± 10% compatibility and hot-swap compliance
  - ◆ 622+ Mb/s data transfer rate per differential I/O
  - ◆ LVDS, RSDS, mini-LVDS, HSTL/SSTL differential I/O with integrated differential termination resistors
  - ◆ Enhanced Double Data Rate (DDR) support
  - ◆ DDR/DDR2 SDRAM support up to 266 Mb/s
  - ◆ Fully compliant 32-bit, 33 MHz PCI® technology support
- Abundant, flexible logic resources
  - ◆ Densities up to 53,712 logic cells, including optional shift register
  - ◆ Efficient wide multiplexers, wide logic
  - ◆ Fast look-ahead carry logic
  - ◆ IEEE 1149.1/1532 JTAG programming/debug port
- Hierarchical SelectRAM™ memory architecture
  - ◆ Up to 2,268 Kbits of fast block RAM with byte write enables for processor applications
  - ◆ Up to 373 Kbits of efficient distributed RAM
  - ◆ Registered outputs on the block RAM with operation of at least 280 MHz in the standard -4 speed grade
- Eight Digital Clock Managers (DCMs)
  - ◆ Clock skew elimination (delay locked loop)
  - ◆ Frequency synthesis, multiplication, division
  - ◆ High-resolution phase shifting
  - ◆ Wide frequency range (5 MHz to over 320 MHz)
- Eight low-skew global clock networks, eight additional clocks per half device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
  - ◆ Low-cost, space-saving SPI serial Flash PROM
  - ◆ x8 or x8/x16 parallel NOR Flash PROM
  - ◆ Unique Device DNA identifier for design authentication
- Complete Xilinx [ISE®](#) and [WebPACK™](#) software support plus [Spartan-3A DSP FPGA Starter Kit](#)
- [MicroBlaze™](#) and [PicoBlaze™](#) embedded processor cores
- BGA packaging, Pb-free only
  - ◆ Common footprints support easy density migration

Table 1: Summary of XA Spartan-3A DSP FPGA Attributes

| Device     | System Gates | Equivalent Logic Cells | CLB Array (One CLB = Four Slices) |         |            |              | Distributed RAM Bits <sup>(1)</sup> | Block RAM Bits <sup>(1)</sup> | DSP48As | DCMs | Maximum User I/O | Maximum Differential I/O Pairs |
|------------|--------------|------------------------|-----------------------------------|---------|------------|--------------|-------------------------------------|-------------------------------|---------|------|------------------|--------------------------------|
|            |              |                        | Rows                              | Columns | Total CLBs | Total Slices |                                     |                               |         |      |                  |                                |
| XA3SD1800A | 1800K        | 37,440                 | 88                                | 48      | 4,160      | 16,640       | 260K                                | 1512K                         | 84      | 8    | 519              | 227                            |
| XA3SD3400A | 3400K        | 53,712                 | 104                               | 58      | 5,968      | 23,872       | 373K                                | 2268K                         | 126     | 8    | 469              | 213                            |

Notes: 1. By convention, one Kb is equivalent to 1,024 bits.

Refer to [DS610](#), *Spartan-3A DSP FPGA Family Data Sheet* for a full product description, AC and DC specifications, and package pinout descriptions. Any values shown specifically in this XA Spartan-3A DSP Automotive FPGA Family data sheet override those shown in DS610.

For information regarding reliability qualification, refer to RPT103, *Xilinx Spartan-3A Family Automotive Qualification Report* and RPT070, *Spartan-3A Commercial Qualification Report*. Contact your local Xilinx representative for more details on these reports.

## Key Feature Differences from Commercial XC Devices

- AEC-Q100 device qualification and full production part approval process (PPAP) documentation support available in both extended temperature I- and Q-Grades
- Guaranteed to meet full electrical specifications over the  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  temperature range (Q-Grade)
- XA Spartan-3A DSP devices are available in the -4 speed grade only
- PCI-66 and PCI-X are not supported in the XA Spartan-3A DSP FPGA product line
- Platform Flash is not supported within the XA family
- XA Spartan-3A DSP devices are available in Pb-free packaging only
- MultiBoot is not supported in XA versions of this product.
- The XA Spartan-3A DSP device must be power cycled prior to reconfiguration.

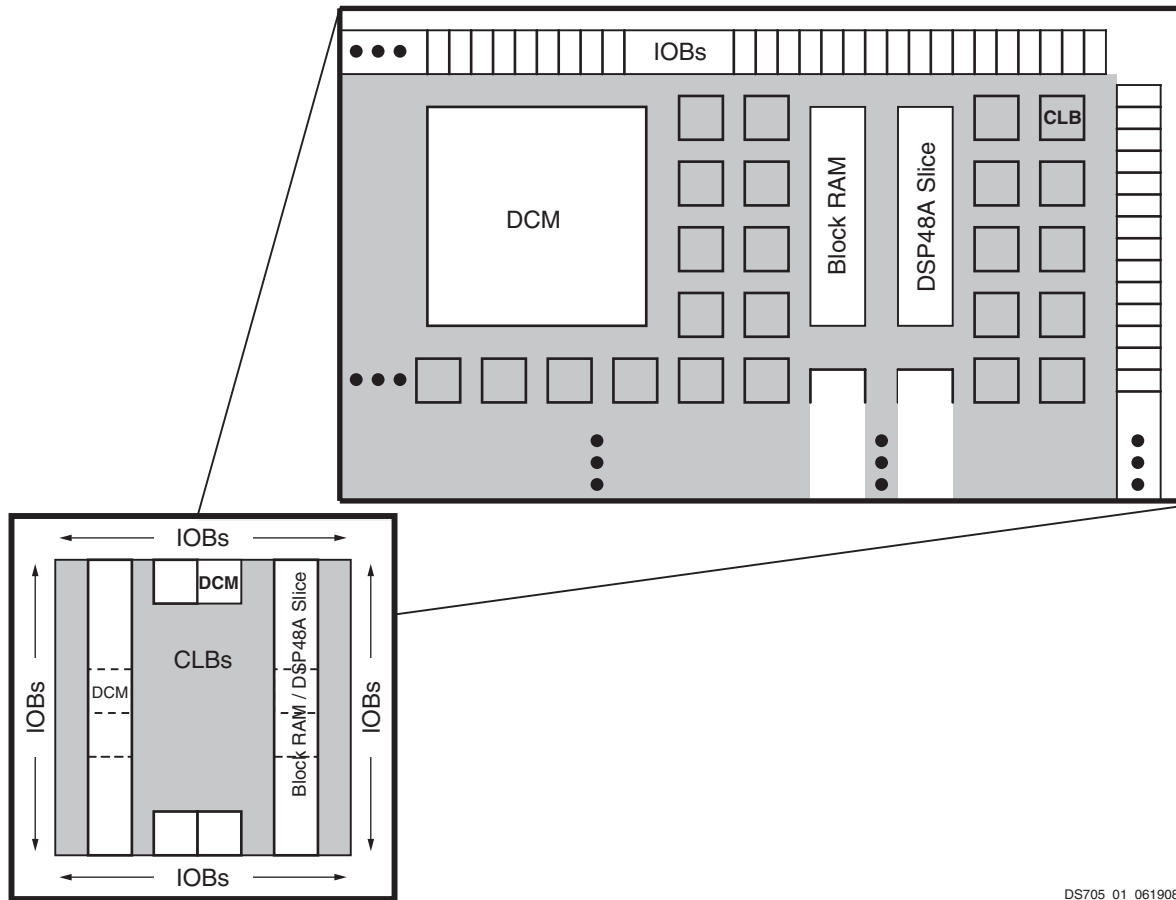
## Architectural Overview

The XA Spartan-3A DSP family architecture consists of five fundamental programmable functional elements:

- **XtremeDSP DSP48A Slice** provides an 18-bit x 18-bit multiplier, 18-bit pre-adder, 48-bit post-adder/accumulator, and cascade capabilities for various DSP applications.
- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in [Figure 1](#). A dual ring of staggered IOBs surrounds a regular array of CLBs. The XA3SD1800A has four columns of DSP48A slices, and the XA3SD3400A has five columns of DSP48A slices. Each DSP48A has an associated block RAM. The DCMs are positioned in the center with two at the top and two at the bottom of the device and in the two outer columns of the 4 or 5 columns of block RAM and DSP48As.

The XA Spartan-3A DSP family features a rich network of routing that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



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**Notes:**

1. The XA3SD1800A and XA3SD3400A have two DCMs on both the left and right sides, as well as the two DCMs at the top and bottom of the devices. The two DCMs on the left and right of the chips are in the middle of the outer block RAM/DSP48A columns of the 4 or 5 columns in the selected device, as shown in the diagram above.
2. A detailed diagram of the DSP48A can be found in [UG431, XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide](#).

Figure 1: XA Spartan-3A DSP Family Architecture

## Configuration

XA Spartan-3A DSP FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board.

After applying power, the configuration data is written to the FPGA using any of five different modes:

- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor

- Boundary-Scan (JTAG), typically downloaded from a processor or system tester

Additionally, each XA Spartan-3A DSP FPGA contains a unique, factory-programmed Device DNA identifier useful for tracking purposes, anti-cloning designs, or IP protection.

## I/O Capabilities

The XA Spartan-3A DSP FPGA SelectIO interface supports many popular single-ended and differential standards. [Table 2](#) shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional input-only pins as indicated in [Table 2](#).

XA Spartan-3A DSP FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz

- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications

XA Spartan-3A DSP FPGAs support the following differential standards:

- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

**Table 2: Available User I/Os and Differential (Diff) I/O Pairs**

| Device     | CSG484                    |                           | FGG676                     |                            |
|------------|---------------------------|---------------------------|----------------------------|----------------------------|
|            | User                      | Diff                      | User                       | Diff                       |
| XA3SD1800A | <b>309</b><br><i>(60)</i> | <b>140</b><br><i>(78)</i> | <b>519</b><br><i>(110)</i> | <b>227</b><br><i>(131)</i> |
| XA3SD3400A | <b>309</b><br><i>(60)</i> | <b>140</b><br><i>(78)</i> | <b>469</b><br><i>(60)</i>  | <b>213</b><br><i>(117)</i> |

**Notes:**

1. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in *(italics)* indicates the number of input-only pins. The differential (Diff) input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.

## Production Status

[Table 3](#) indicates the production status of each XA Spartan-3A DSP FPGA by temperature range and speed grade. The table also lists the earliest speed file version

required for creating a production configuration bitstream. Later versions are also supported.

**Table 3: XA Spartan-3A DSP FPGA Family Production Status (Production Speed File)**

| Temperature Range |            | I-Grade            | Q-Grade            |
|-------------------|------------|--------------------|--------------------|
| Speed Grade       |            | Standard (-4)      | Standard (-4)      |
| Part Number       | XA3SD1800A | Production (v1.32) | Production (v1.32) |
|                   | XA3SD3400A | Production (v1.32) | -                  |

## Package Marking

Figure 2 shows the top marking for XA Spartan-3A DSP FPGAs in BGA packages.

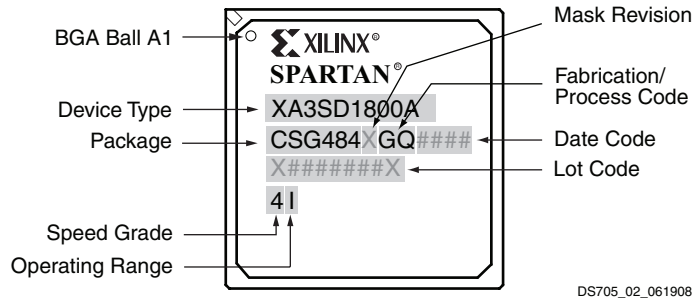
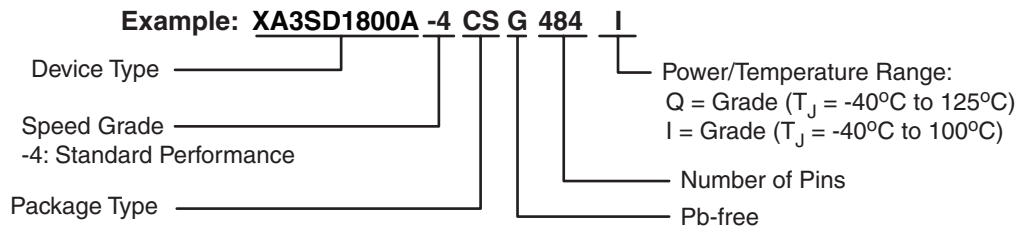


Figure 2: XA Spartan-3A DSP FPGA Package Marking Example

## Ordering Information

XA Spartan-3A DSP FPGAs are available in Pb-free packaging only for all device/package combinations.

### Pb-Free Packaging



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| Device     | Speed Grade             | Package Type / Number of Pins |   | Temperature Range ( $T_J$ ) |  |
|------------|-------------------------|-------------------------------|---|-----------------------------|--|
| XA3SD1800A | -4 Standard Performance | CSG484                        | 484-ball Chip-Scale Ball Grid Array (CSBGA) | I                           | I-Grade ( $-40^\circ\text{C}$ to $100^\circ\text{C}$ ) |
| XA3SD3400A |                         | FGG676                        | 676-ball Fine-Pitch Ball Grid Array (FBGA)  | Q                           | Q-Grade ( $-40^\circ\text{C}$ to $125^\circ\text{C}$ ) |

**Notes:**

1. The XA Spartan-3A DSP FPGA product line is available in -4 speed grade only.
2. The XA3SD3400A is available in I-Grade only.

## DC Electrical Characteristics

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all XA Spartan-3A DSP devices. AC and DC characteristics are specified using the same numbers for both I-Grade and Q-Grade.**

## Absolute Maximum Ratings

Stresses beyond those listed under [Table 4](#): Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 4: Absolute Maximum Ratings

| Symbol      | Description  | Conditions                       | Min   | Max             | Units              |
|-------------|--|----------------------------------|-------|-----------------|--------------------|
| $V_{CCINT}$ | Internal supply voltage                                    |                                  | -0.5  | 1.32            | V                  |
| $V_{CCAUX}$ | Auxiliary supply voltage                                   |                                  | -0.5  | 3.75            | V                  |
| $V_{CCO}$   | Output driver supply voltage                               |                                  | -0.5  | 3.75            | V                  |
| $V_{REF}$   | Input reference voltage                                    |                                  | -0.5  | $V_{CCO} + 0.5$ | V                  |
| $V_{IN}$    | Voltage applied to all User I/O pins and Dual-Purpose pins | Driver in a high-impedance state | -0.95 | 4.6             | V                  |
|             | Voltage applied to all Dedicated pins                      |                                  | -0.5  | 4.6             | V                  |
| $V_{ESD}$   | Electrostatic Discharge Voltage                            | Human body model                 | -     | $\pm 2000$      | V                  |
|             |  | Charged device model             | -     | $\pm 500$       | V                  |
|             |  | Machine model                    | -     | $\pm 200$       | V                  |
| $T_J$       | Junction temperature                                       |                                  | -     | 125             | $^{\circ}\text{C}$ |
| $T_{STG}$   | Storage temperature  |                                  | -65   | 150             | $^{\circ}\text{C}$ |

### Notes:

- For soldering guidelines, see [UG112](#), *Device Packaging and Thermal Characteristics* and [XAPP427](#), *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

## Power Supply Specifications

Table 5: Supply Voltage Thresholds for Power-On Reset

| Symbol       | Description                               | Min | Max | Units |
|--------------|---|-----|-----|-------|
| $V_{CCINTT}$ | Threshold for the $V_{CCINT}$ supply      | 0.4 | 1.0 | V     |
| $V_{CCAUXT}$ | Threshold for the $V_{CCAUX}$ supply      | 1.0 | 2.0 | V     |
| $V_{CCO2T}$  | Threshold for the $V_{CCO}$ Bank 2 supply | 1.0 | 2.0 | V     |

**Notes:**

- $V_{CCINT}$ ,  $V_{CCAUX}$ , and  $V_{CCO}$  supplies to the FPGA can be applied in any order. However, the FPGA configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply  $V_{CCINT}$  last for lowest overall power consumption (see the [UG331](#) chapter titled “Powering Spartan-3 Generation FPGAs” for more information).
- To ensure successful power-on,  $V_{CCINT}$ ,  $V_{CCO}$  Bank 2, and  $V_{CCAUX}$  supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 6: Supply Voltage Ramp Rate

| Symbol       | Description   | Min | Max | Units |
|--------------|---|-----|-----|-------|
| $V_{CCINTR}$ | Ramp rate from GND to valid $V_{CCINT}$ supply level      | 0.2 | 100 | ms    |
| $V_{CCAUXR}$ | Ramp rate from GND to valid $V_{CCAUX}$ supply level      | 0.2 | 100 | ms    |
| $V_{CCO2R}$  | Ramp rate from GND to valid $V_{CCO}$ Bank 2 supply level | 0.2 | 100 | ms    |

**Notes:**

- $V_{CCINT}$ ,  $V_{CCAUX}$ , and  $V_{CCO}$  supplies to the FPGA can be applied in any order. However, the FPGA configuration source (SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply  $V_{CCINT}$  last for lowest overall power consumption (see the [UG331](#) chapter titled “Powering Spartan-3 Generation FPGAs” for more information).
- To ensure successful power-on,  $V_{CCINT}$ ,  $V_{CCO}$  Bank 2, and  $V_{CCAUX}$  supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 7: Supply Voltage Levels Necessary for Preserving CMOS Configuration Latch (CCL) Contents and RAM Data

| Symbol      | Description  | Min | Units |
|-------------|--|-----|-------|
| $V_{DRINT}$ | $V_{CCINT}$ level required to retain CMOS Configuration Latch (CCL) and RAM data | 1.0 | V     |
| $V_{DRAUX}$ | $V_{CCAUX}$ level required to retain CMOS Configuration Latch (CCL) and RAM data | 2.0 | V     |

## General Recommended Operating Conditions

Table 8: General Recommended Operating Conditions

| Symbol          | Description                                 | Min                   | Nominal | Max  | Units         |    |
|-----------------|---|-----------------------|---------|------|---------------|----|
| $T_J$           | Junction temperature                        | I-Grade               | -40     | -    | 100           | °C |
|                 |   | Q-Grade               | -40     | -    | 125           | °C |
| $V_{CCINT}$     | Internal supply voltage                     | 1.14                  | 1.20    | 1.26 | V             |    |
| $V_{CCO}^{(1)}$ | Output driver supply voltage                | 1.10                  | -       | 3.60 | V             |    |
| $V_{CCAUX}$     | Auxiliary supply voltage                    | $V_{CCAUX} = 2.5$     | 2.25    | 2.50 | 2.75          | V  |
|                 |   | $V_{CCAUX} = 3.3$     | 3.00    | 3.30 | 3.60          | V  |
| $V_{IN}^{(2)}$  | Input voltage                               | PCI IOSTANDARD        | -0.5    | -    | $V_{CCO}+0.5$ | V  |
|                 |   | All other IOSTANDARDS | -0.5    | -    | 4.10          | V  |
| $T_{IN}$        | Input signal transition time <sup>(3)</sup> | -                     | -       | 500  | ns            |    |

### Notes:

1. This  $V_{CCO}$  range spans the lowest and highest operating voltages for all supported I/O standards. [Table 11](#) lists the recommended  $V_{CCO}$  range specific to each of the single-ended I/O standards, and [Table 13](#) lists that specific to the differential standards.
2. See [XAPP459](#), *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Generation FPGAs*.
3. Measured between 10% and 90%  $V_{CCO}$ . Follow [Signal Integrity](#) recommendations.



## General DC Characteristics for I/O Pins

Table 9: General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins

| Symbol          | Description   | Test Conditions  |   | Min                    | Typ  | Max   | Units     |
|-----------------|---|--|---|------------------------|------|-------|-----------|
| $I_L$           | Leakage current at User I/O, Input-only, Dual-Purpose, and Dedicated pins, FPGA powered   | Driver is in a high-impedance state, $V_{IN} = 0V$ or $V_{CCO}$ max, sample-tested |   | -10                    | -    | +10   | $\mu A$   |
| $I_{HS}$        | Leakage current on pins during hot socketing, FPGA unpowered  | All pins except INIT_B, PROG_B, DONE, and JTAG pins when PUDC_B = 1.               |   | -10                    | -    | +10   | $\mu A$   |
|                 |   | INIT_B, PROG_B, DONE, and JTAG pins or other pins when PUDC_B = 0.                 |   | Add $I_{HS} + I_{RPU}$ |      |       | $\mu A$   |
| $I_{RPU}^{(2)}$ | Current through pull-up resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins. Dedicated pins are powered by $V_{CCAUX}$ . | $V_{IN} = GND$   | $V_{CCO}$ or $V_{CCAUX} = 3.0V$ to $3.6V$ | -151                   | -315 | -710  | $\mu A$   |
|                 |   |  | $V_{CCO}$ or $V_{CCAUX} = 2.3V$ to $2.7V$ | -82                    | -182 | -437  | $\mu A$   |
|                 |   |  | $V_{CCO} = 1.7V$ to $1.9V$                | -36                    | -88  | -226  | $\mu A$   |
|                 |   |  | $V_{CCO} = 1.4V$ to $1.6V$                | -22                    | -56  | -148  | $\mu A$   |
|                 |   |  | $V_{CCO} = 1.14V$ to $1.26V$              | -11                    | -31  | -83   | $\mu A$   |
| $R_{PU}^{(2)}$  | Equivalent pull-up resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on $I_{RPU}$ per Note 2)             | $V_{IN} = GND$   | $V_{CCO} = 3.0V$ to $3.6V$                | 5.1                    | 11.4 | 23.9  | $k\Omega$ |
|                 |   |  | $V_{CCO} = 2.3V$ to $2.7V$                | 6.2                    | 14.8 | 33.1  | $k\Omega$ |
|                 |   |  | $V_{CCO} = 1.7V$ to $1.9V$                | 8.4                    | 21.6 | 52.6  | $k\Omega$ |
|                 |   |  | $V_{CCO} = 1.4V$ to $1.6V$                | 10.8                   | 28.4 | 74.0  | $k\Omega$ |
|                 |   |  | $V_{CCO} = 1.14V$ to $1.26V$              | 15.3                   | 41.1 | 119.4 | $k\Omega$ |
| $I_{RPD}^{(2)}$ | Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins  | $V_{IN} = V_{CCO}$   | $V_{CCAUX} = 3.0V$ to $3.6V$              | 167                    | 346  | 659   | $\mu A$   |
|                 |   |  | $V_{CCAUX} = 2.25V$ to $2.75V$            | 100                    | 225  | 457   | $\mu A$   |
| $R_{PD}^{(2)}$  | Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on $I_{RPD}$ per Note 2)           | $V_{CCAUX} = 3.0V$ to $3.6V$   | $V_{IN} = 3.0V$ to $3.6V$                 | 5.5                    | 10.4 | 20.8  | $k\Omega$ |
|                 |   |  | $V_{IN} = 2.3V$ to $2.7V$                 | 4.1                    | 7.8  | 15.7  | $k\Omega$ |
|                 |   |  | $V_{IN} = 1.7V$ to $1.9V$                 | 3.0                    | 5.7  | 11.1  | $k\Omega$ |
|                 |   |  | $V_{IN} = 1.4V$ to $1.6V$                 | 2.7                    | 5.1  | 9.6   | $k\Omega$ |
|                 |   |  | $V_{IN} = 1.14V$ to $1.26V$               | 2.4                    | 4.5  | 8.1   | $k\Omega$ |
|                 |   | $V_{CCAUX} = 2.25V$ to $2.75V$   | $V_{IN} = 3.0V$ to $3.6V$                 | 7.9                    | 16.0 | 35.0  | $k\Omega$ |
|                 |   |  | $V_{IN} = 2.3V$ to $2.7V$                 | 5.9                    | 12.0 | 26.3  | $k\Omega$ |
|                 |   |  | $V_{IN} = 1.7V$ to $1.9V$                 | 4.2                    | 8.5  | 18.6  | $k\Omega$ |
|                 |   |  | $V_{IN} = 1.4V$ to $1.6V$                 | 3.6                    | 7.2  | 15.7  | $k\Omega$ |
|                 |   |  | $V_{IN} = 1.14V$ to $1.26V$               | 3.0                    | 6.0  | 12.5  | $k\Omega$ |
| $I_{REF}$       | $V_{REF}$ current per pin   | All $V_{CCO}$ levels   |   | -10                    | -    | +10   | $\mu A$   |
| $C_{IN}$        | Input capacitance   | -  |   | -                      | -    | 10    | pF        |
| $R_{DT}$        | Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.              | $V_{CCO} = 3.3V \pm 10\%$  | LVDS_33, MINI_LVDS_33, RSDS_33            | 90                     | 100  | 115   | $\Omega$  |
|                 |   | $V_{CCO} = 2.5V \pm 10\%$  | LVDS_25, MINI_LVDS_25, RSDS_25            | 90                     | 110  | -     | $\Omega$  |

**Notes:**

- The numbers in this table are based on the conditions set forth in Table 8.
- This parameter is based on characterization. The pull-up resistance  $R_{PU} = V_{CCO} / I_{RPU}$ . The pull-down resistance  $R_{PD} = V_{IN} / I_{RPD}$ .

## Quiescent Current Requirements

Table 10: Quiescent Supply Current Characteristics

| Symbol              | Description                                 | Device     | Typical <sup>(2)</sup> | I-Grade Maximum <sup>(2)</sup> | Q-Grade Maximum <sup>(2)</sup> | Units |
|---------------------|---|------------|------------------------|--------------------------------|--------------------------------|-------|
| I <sub>CCINTQ</sub> | Quiescent V <sub>CCINT</sub> supply current | XA3SD1800A | 41                     | 500                            | 900                            | mA    |
|                     |   | XA3SD3400A | 64                     | 725                            | -                              | mA    |
| I <sub>CCOQ</sub>   | Quiescent V <sub>CCO</sub> supply current   | XA3SD1800A | 0.4                    | 5                              | 5                              | mA    |
|                     |   | XA3SD3400A | 0.4                    | 5                              | -                              | mA    |
| I <sub>CCAUXQ</sub> | Quiescent V <sub>CCAUX</sub> supply current | XA3SD1800A | 25                     | 110                            | 145                            | mA    |
|                     |   | XA3SD3400A | 39                     | 160                            | -                              | mA    |

### Notes:

- The numbers in this table are based on the conditions set forth in [Table 8](#).
- Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at ambient room temperature (T<sub>A</sub> of 25°C at V<sub>CCINT</sub> = 1.2V, V<sub>CCO</sub> = 3.3V, and V<sub>CCAUX</sub> = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V<sub>CCINT</sub> = 1.26V, V<sub>CCO</sub> = 3.6V, and V<sub>CCAUX</sub> = 3.6V. The FPGA is programmed with a “blank” configuration data file (that is, a design with no functional elements instantiated). For conditions other than those described above (for example, a design including functional elements), measured quiescent current levels will be different than the values in the table.
- There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The [Spartan-3A DSP FPGA XPower Estimator](#) provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
- The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
- For information on the power-saving Suspend mode, see [XAPP480, Using Suspend Mode in Spartan-3 Generation FPGAs](#). Suspend mode typically saves 40% total power consumption compared to quiescent current.

## Single-Ended I/O Standards

Table 11: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

| IOSTANDARD Attribute       | $V_{CCO}$ for Drivers <sup>(2)</sup> |         |         | $V_{REF}$                                     |         |         | $V_{IL}$            | $V_{IH}$            |
|----------------------------|--------------------------------------|---------|---------|---|---------|---------|---------------------|---------------------|
|                            | Min (V)                              | Nom (V) | Max (V) | Min (V)                                       | Nom (V) | Max (V) | Max (V)             | Min (V)             |
| LVTTL                      | 3.0                                  | 3.3     | 3.6     | $V_{REF}$ is not used for these I/O standards |         |         | 0.8                 | 2.0                 |
| LVC MOS33 <sup>(4)</sup>   | 3.0                                  | 3.3     | 3.6     |   |         |         | 0.8                 | 2.0                 |
| LVC MOS25 <sup>(4,5)</sup> | 2.3                                  | 2.5     | 2.7     |   |         |         | 0.7                 | 1.7                 |
| LVC MOS18 <sup>(4)</sup>   | 1.65                                 | 1.8     | 1.95    |   |         |         | 0.4                 | 0.8                 |
| LVC MOS15 <sup>(4)</sup>   | 1.4                                  | 1.5     | 1.6     |   |         |         | 0.4                 | 0.8                 |
| LVC MOS12 <sup>(4)</sup>   | 1.1                                  | 1.2     | 1.3     |   |         |         | 0.4                 | 0.7                 |
| PCI33_3 <sup>(6)</sup>     | 3.0                                  | 3.3     | 3.6     |   |         |         | $0.3 \cdot V_{CCO}$ | $0.5 \cdot V_{CCO}$ |
| HSTL_I                     | 1.4                                  | 1.5     | 1.6     | 0.68  | 0.75    | 0.9     | $V_{REF} - 0.1$     | $V_{REF} + 0.1$     |
| HSTL_III                   | 1.4                                  | 1.5     | 1.6     | -   | 0.9     | -       | $V_{REF} - 0.1$     | $V_{REF} + 0.1$     |
| HSTL_I_18                  | 1.7                                  | 1.8     | 1.9     | 0.8   | 0.9     | 1.1     | $V_{REF} - 0.1$     | $V_{REF} + 0.1$     |
| HSTL_II_18                 | 1.7                                  | 1.8     | 1.9     | -   | 0.9     | -       | $V_{REF} - 0.1$     | $V_{REF} + 0.1$     |
| HSTL_III_18                | 1.7                                  | 1.8     | 1.9     | -   | 1.1     | -       | $V_{REF} - 0.1$     | $V_{REF} + 0.1$     |
| SSTL18_I                   | 1.7                                  | 1.8     | 1.9     | 0.833   | 0.900   | 0.969   | $V_{REF} - 0.125$   | $V_{REF} + 0.125$   |
| SSTL18_II                  | 1.7                                  | 1.8     | 1.9     | 0.833   | 0.900   | 0.969   | $V_{REF} - 0.125$   | $V_{REF} + 0.125$   |
| SSTL2_I                    | 2.3                                  | 2.5     | 2.7     | 1.15  | 1.25    | 1.38    | $V_{REF} - 0.150$   | $V_{REF} + 0.150$   |
| SSTL2_II                   | 2.3                                  | 2.5     | 2.7     | 1.15  | 1.25    | 1.38    | $V_{REF} - 0.150$   | $V_{REF} + 0.150$   |
| SSTL3_I                    | 3.0                                  | 3.3     | 3.6     | 1.3   | 1.5     | 1.7     | $V_{REF} - 0.2$     | $V_{REF} + 0.2$     |
| SSTL3_II                   | 3.0                                  | 3.3     | 3.6     | 1.3   | 1.5     | 1.7     | $V_{REF} - 0.2$     | $V_{REF} + 0.2$     |

### Notes:

- Descriptions of the symbols used in this table are as follows:  
 $V_{CCO}$  – the supply voltage for output drivers  
 $V_{REF}$  – the reference voltage for setting the input switching threshold  
 $V_{IL}$  – the input voltage that indicates a Low logic level  
 $V_{IH}$  – the input voltage that indicates a High logic level
- In general, the  $V_{CCO}$  rails supply only output drivers, not input circuits. The exceptions are for LVC MOS25 inputs when  $V_{CCAUX} = 3.3V$  range and for PCI I/O standards.
- For device operation, the maximum signal voltage ( $V_{IH}$  max) can be as high as  $V_{IN}$  max. See Table 4.
- There is approximately 100 mV of hysteresis on inputs using LVC MOS33 and LVC MOS25 I/O standards.
- All Dedicated pins (PROG\_B, DONE, SUSPEND, TCK, TDI, TDO, and TMS) draw power from the  $V_{CCAUX}$  rail and use the LVC MOS25 or LVC MOS33 standard depending on  $V_{CCAUX}$ . The Dual-Purpose configuration pins use the LVC MOS25 standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the  $V_{CCO}$  lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
- For information on PCI IP solutions, see [www.xilinx.com/pci](http://www.xilinx.com/pci). The PCI IOSTANDARD is not supported on input-only pins.

Table 12: DC Characteristics of User I/Os Using Single-Ended Standards

| IOSTANDARD Attribute    | Test Conditions      |                      |                    | Logic Level Characteristics |                         |
|-------------------------|----------------------|----------------------|--------------------|-----------------------------|-------------------------|
|                         | I <sub>OL</sub> (mA) | I <sub>OH</sub> (mA) |                    | V <sub>OL</sub> Max (V)     | V <sub>OH</sub> Min (V) |
| LVTTTL <sup>(3)</sup>   | 2                    | 2                    | -2                 | 0.4                         | 2.4                     |
|                         | 4                    | 4                    | -4                 |                             |                         |
|                         | 6                    | 6                    | -6                 |                             |                         |
|                         | 8                    | 8                    | -8                 |                             |                         |
|                         | 12                   | 12                   | -12                |                             |                         |
|                         | 16                   | 16                   | -16                |                             |                         |
|                         | 24                   | 24 <sup>(6)</sup>    | -24                |                             |                         |
| LVCMOS33 <sup>(3)</sup> | 2                    | 2                    | -2                 | 0.4                         | V <sub>CCO</sub> - 0.4  |
|                         | 4                    | 4                    | -4                 |                             |                         |
|                         | 6                    | 6                    | -6                 |                             |                         |
|                         | 8                    | 8                    | -8                 |                             |                         |
|                         | 12                   | 12                   | -12                |                             |                         |
|                         | 16                   | 16                   | -16 <sup>(6)</sup> |                             |                         |
|                         | 24 <sup>(4)</sup>    | 24                   | -24 <sup>(6)</sup> |                             |                         |
| LVCMOS25 <sup>(3)</sup> | 2                    | 2                    | -2                 | 0.4                         | V <sub>CCO</sub> - 0.4  |
|                         | 4                    | 4                    | -4                 |                             |                         |
|                         | 6                    | 6                    | -6                 |                             |                         |
|                         | 8                    | 8                    | -8                 |                             |                         |
|                         | 12                   | 12                   | -12                |                             |                         |
|                         | 16 <sup>(4)</sup>    | 16                   | -16 <sup>(6)</sup> |                             |                         |
|                         | 24 <sup>(4)</sup>    | 24 <sup>(6)</sup>    | -24 <sup>(6)</sup> |                             |                         |
| LVCMOS18 <sup>(3)</sup> | 2                    | 2                    | -2                 | 0.4                         | V <sub>CCO</sub> - 0.4  |
|                         | 4                    | 4                    | -4                 |                             |                         |
|                         | 6                    | 6                    | -6 <sup>(6)</sup>  |                             |                         |
|                         | 8                    | 8                    | -8                 |                             |                         |
|                         | 12 <sup>(4)</sup>    | 12                   | -12 <sup>(6)</sup> |                             |                         |
|                         | 16 <sup>(4)</sup>    | 16                   | -16                |                             |                         |
| LVCMOS15 <sup>(3)</sup> | 2                    | 2                    | -2                 | 0.4                         | V <sub>CCO</sub> - 0.4  |
|                         | 4                    | 4                    | -4                 |                             |                         |
|                         | 6                    | 6                    | -6                 |                             |                         |
|                         | 8 <sup>(4)</sup>     | 8                    | -8                 |                             |                         |
| LVCMOS12 <sup>(3)</sup> | 2                    | 2                    | -2                 | 0.4                         | V <sub>CCO</sub> - 0.4  |
|                         | 4 <sup>(4)</sup>     | 4                    | -4                 |                             |                         |
|                         | 6 <sup>(4)</sup>     | 6                    | -6                 |                             |                         |
| PCI33_3 <sup>(5)</sup>  | 1.5                  | -0.5                 |                    | 10% V <sub>CCO</sub>        | 90% V <sub>CCO</sub>    |

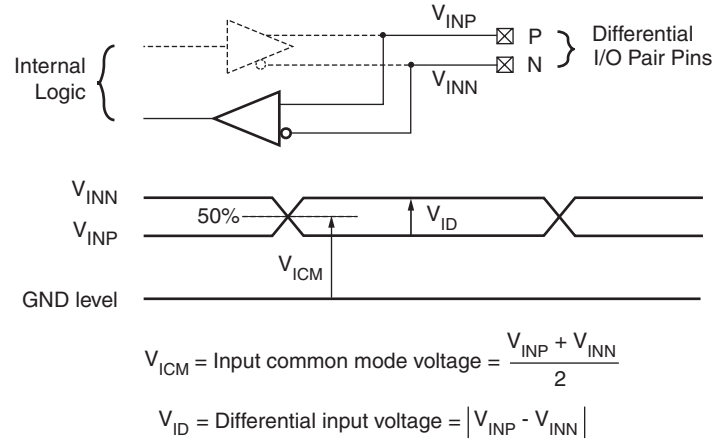
Table 12: DC Characteristics of User I/Os Using Single-Ended Standards (Cont'd)

| IOSTANDARD Attribute      | Test Conditions      |                      | Logic Level Characteristics |                         |
|---------------------------|----------------------|----------------------|-----------------------------|-------------------------|
|                           | I <sub>OL</sub> (mA) | I <sub>OH</sub> (mA) | V <sub>OL</sub> Max (V)     | V <sub>OH</sub> Min (V) |
| HSTL_I <sup>(4)</sup>     | 8                    | -8                   | 0.4                         | V <sub>CCO</sub> - 0.4  |
| HSTL_III <sup>(4)</sup>   | 24 <sup>(7)</sup>    | -8                   | 0.4                         | V <sub>CCO</sub> - 0.4  |
| HSTL_I_18                 | 8                    | -8                   | 0.4                         | V <sub>CCO</sub> - 0.4  |
| HSTL_II_18 <sup>(4)</sup> | 16                   | -16 <sup>(7)</sup>   | 0.4                         | V <sub>CCO</sub> - 0.4  |
| HSTL_III_18               | 24 <sup>(7)</sup>    | -8                   | 0.4                         | V <sub>CCO</sub> - 0.4  |
| SSTL18_I                  | 6.7                  | -6.7                 | V <sub>TT</sub> - 0.475     | V <sub>TT</sub> + 0.475 |
| SSTL18_II <sup>(4)</sup>  | 13.4                 | -13.4                | V <sub>TT</sub> - 0.475     | V <sub>TT</sub> + 0.475 |
| SSTL2_I                   | 8.1                  | -8.1                 | V <sub>TT</sub> - 0.61      | V <sub>TT</sub> + 0.61  |
| SSTL2_II <sup>(4)</sup>   | 16.2                 | -16.2                | V <sub>TT</sub> - 0.80      | V <sub>TT</sub> + 0.80  |
| SSTL3_I                   | 8                    | -8                   | V <sub>TT</sub> - 0.6       | V <sub>TT</sub> + 0.6   |
| SSTL3_II <sup>(4)</sup>   | 16                   | -16                  | V <sub>TT</sub> - 0.8       | V <sub>TT</sub> + 0.8   |

**Notes:**

- The numbers in this table are based on the conditions set forth in [Table 8](#) and [Table 11](#).
- Descriptions of the symbols used in this table are as follows:  
 I<sub>OL</sub> — the output current condition under which V<sub>OL</sub> is tested  
 I<sub>OH</sub> — the output current condition under which V<sub>OH</sub> is tested  
 V<sub>OL</sub> — the output voltage that indicates a Low logic level  
 V<sub>OH</sub> — the output voltage that indicates a High logic level  
 V<sub>IL</sub> — the input voltage that indicates a Low logic level  
 V<sub>IH</sub> — the input voltage that indicates a High logic level  
 V<sub>CCO</sub> — the supply voltage for output drivers  
 V<sub>REF</sub> — the reference voltage for setting the input switching threshold  
 V<sub>TT</sub> — the voltage applied to a resistor termination
- For the LVCMOS and LVTTTL standards: the same V<sub>OL</sub> and V<sub>OH</sub> limits apply for both the Fast and Slow slew attributes.
- These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in [UG331](#).
- Tested according to the relevant PCI specifications. For information on PCI IP solutions, see [www.xilinx.com/pci](http://www.xilinx.com/pci). The PCI IOSTANDARD is not supported on input-only pins.
- Derate by 20% for T<sub>J</sub> above 100°C.
- Derate by 5% for T<sub>J</sub> above 100°C.

Differential I/O Standards



DS705\_04\_061908

Figure 3: Differential Input Voltages

Table 13: Recommended Operating Conditions for User I/Os Using Differential Signal Standards

| IOSTANDARD Attribute           | V <sub>CCO</sub> for Drivers <sup>(1)</sup> |         |         | V <sub>ID</sub> |          |          | V <sub>ICM</sub> <sup>(2)</sup> |         |                    |
|--------------------------------|---|---------|---------|-----------------|----------|----------|---------------------------------|---------|--------------------|
|                                | Min (V)                                     | Nom (V) | Max (V) | Min (mV)        | Nom (mV) | Max (mV) | Min (V)                         | Nom (V) | Max (V)            |
| LVDS_25 <sup>(3)</sup>         | 2.25  | 2.5     | 2.75    | 100             | 350      | 600      | 0.3                             | 1.25    | 2.35               |
| LVDS_33 <sup>(3)</sup>         | 3.0   | 3.3     | 3.6     | 100             | 350      | 600      | 0.3                             | 1.25    | 2.35               |
| BLVDS_25 <sup>(4)</sup>        | 2.25  | 2.5     | 2.75    | 100             | 300      | –        | 0.3                             | 1.3     | 2.35               |
| MINI_LVDS_25 <sup>(3)</sup>    | 2.25  | 2.5     | 2.75    | 200             | –        | 600      | 0.3                             | 1.2     | 1.95               |
| MINI_LVDS_33 <sup>(3)</sup>    | 3.0   | 3.3     | 3.6     | 200             | –        | 600      | 0.3                             | 1.2     | 1.95               |
| LVPECL_25 <sup>(5)</sup>       | Inputs Only                                 |         |         | 100             | 800      | 1000     | 0.3                             | 1.2     | 1.95               |
| LVPECL_33 <sup>(5)</sup>       | Inputs Only                                 |         |         | 100             | 800      | 1000     | 0.3                             | 1.2     | 2.8 <sup>(6)</sup> |
| RSDS_25 <sup>(3)</sup>         | 2.25  | 2.5     | 2.75    | 100             | 200      | –        | 0.3                             | 1.2     | 1.5                |
| RSDS_33 <sup>(3)</sup>         | 3.0   | 3.3     | 3.6     | 100             | 200      | –        | 0.3                             | 1.2     | 1.5                |
| TMDS_33 <sup>(3,4,7)</sup>     | 3.14  | 3.3     | 3.47    | 150             | –        | 1200     | 2.7                             | –       | 3.23               |
| PPDS_25 <sup>(3)</sup>         | 2.25  | 2.5     | 2.75    | 100             | –        | 400      | 0.2                             | –       | 2.3                |
| PPDS_33 <sup>(3)</sup>         | 3.0   | 3.3     | 3.6     | 100             | –        | 400      | 0.2                             | –       | 2.3                |
| DIFF_HSTL_I_18                 | 1.7   | 1.8     | 1.9     | 100             | –        | –        | 0.8                             | –       | 1.1                |
| DIFF_HSTL_II_18 <sup>(8)</sup> | 1.7   | 1.8     | 1.9     | 100             | –        | –        | 0.8                             | –       | 1.1                |
| DIFF_HSTL_III_18               | 1.7   | 1.8     | 1.9     | 100             | –        | –        | 0.8                             | –       | 1.1                |
| DIFF_HSTL_I                    | 1.4   | 1.5     | 1.6     | 100             | –        | –        | 0.68                            | –       | 0.9                |
| DIFF_HSTL_III                  | 1.4   | 1.5     | 1.6     | 100             | –        | –        | –                               | 0.9     | –                  |
| DIFF_SSTL18_I                  | 1.7   | 1.8     | 1.9     | 100             | –        | –        | 0.7                             | –       | 1.1                |
| DIFF_SSTL18_II <sup>(8)</sup>  | 1.7   | 1.8     | 1.9     | 100             | –        | –        | 0.7                             | –       | 1.1                |
| DIFF_SSTL2_I                   | 2.3   | 2.5     | 2.7     | 100             | –        | –        | 1.0                             | –       | 1.5                |
| DIFF_SSTL2_II <sup>(8)</sup>   | 2.3   | 2.5     | 2.7     | 100             | –        | –        | 1.0                             | –       | 1.5                |
| DIFF_SSTL3_I                   | 3.0   | 3.3     | 3.6     | 100             | –        | –        | 1.1                             | –       | 1.9                |
| DIFF_SSTL3_II                  | 3.0   | 3.3     | 3.6     | 100             | –        | –        | 1.1                             | –       | 1.9                |

Notes:

1. The V<sub>CCO</sub> rails supply only differential output drivers, not input circuits.
2. V<sub>ICM</sub> must be less than V<sub>CCAUX</sub>.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the chapter “Using I/O Resources” in [UG331](#).
4. See “External Termination Requirements for Differential I/O.”
5. LVPECL is supported on inputs only, not outputs. Requires V<sub>CCAUX</sub> = 3.3V ± 10%.
6. LVPECL\_33 maximum V<sub>ICM</sub> = V<sub>CCAUX</sub> - (V<sub>ID</sub>/2).
7. Requires V<sub>CCAUX</sub> = 3.3V ± 10%. (V<sub>CCAUX</sub> - 300 mV) ≤ V<sub>ICM</sub> ≤ (V<sub>CCAUX</sub> - 37 mV).
8. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter “Using I/O Resources” in [UG331](#).
9. V<sub>REF</sub> inputs are used for the DIFF\_SSTL and DIFF\_HSTL standards. The V<sub>REF</sub> settings are the same as for the single-ended versions in [Table 11](#). Other differential standards do not use V<sub>REF</sub>.

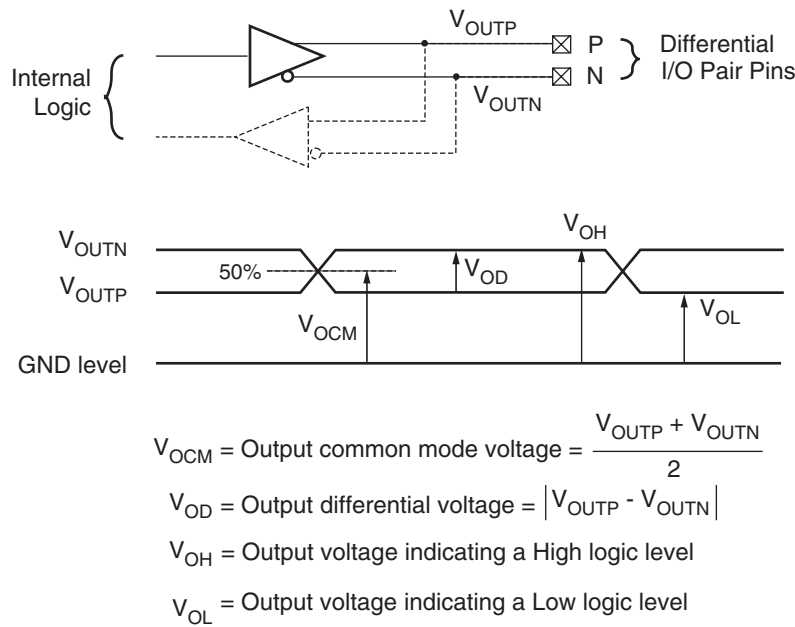


Figure 4: Differential Output Voltages

Table 14: DC Characteristics of User I/Os Using Differential Signal Standards

| IOSTANDARD Attribute | V <sub>OD</sub> |          |          | V <sub>OCM</sub>         |         |                          | V <sub>OH</sub>         | V <sub>OL</sub>         |
|----------------------|-----------------|----------|----------|--------------------------|---------|--------------------------|-------------------------|-------------------------|
|                      | Min (mV)        | Typ (mV) | Max (mV) | Min (V)                  | Typ (V) | Max (V)                  | Min (V)                 | Max (V)                 |
| LVDS_25              | 247             | 350      | 454      | 1.125                    | –       | 1.375                    | –                       | –                       |
| LVDS_33              | 247             | 350      | 454      | 1.125                    | –       | 1.375                    | –                       | –                       |
| BLVDS_25             | 240             | 350      | 460      | –                        | 1.30    | –                        | –                       | –                       |
| MINI_LVDS_25         | 300             | –        | 600      | 1.0                      | –       | 1.4                      | –                       | –                       |
| MINI_LVDS_33         | 300             | –        | 600      | 1.0                      | –       | 1.4                      | –                       | –                       |
| RSDS_25              | 100             | –        | 400      | 1.0                      | –       | 1.4                      | –                       | –                       |
| RSDS_33              | 100             | –        | 400      | 1.0                      | –       | 1.4                      | –                       | –                       |
| TMDS_33              | 400             | –        | 800      | V <sub>CCO</sub> – 0.405 | –       | V <sub>CCO</sub> – 0.190 | –                       | –                       |
| PPDS_25              | 100             | –        | 400      | 0.5                      | 0.8     | 1.4                      | –                       | –                       |
| PPDS_33              | 100             | –        | 400      | 0.5                      | 0.8     | 1.4                      | –                       | –                       |
| DIFF_HSTL_I_18       | –               | –        | –        | –                        | –       | –                        | V <sub>CCO</sub> – 0.4  | 0.4                     |
| DIFF_HSTL_II_18      | –               | –        | –        | –                        | –       | –                        | V <sub>CCO</sub> – 0.4  | 0.4                     |
| DIFF_HSTL_III_18     | –               | –        | –        | –                        | –       | –                        | V <sub>CCO</sub> – 0.4  | 0.4                     |
| DIFF_HSTL_I          | –               | –        | –        | –                        | –       | –                        | V <sub>CCO</sub> – 0.4  | 0.4                     |
| DIFF_HSTL_III        | –               | –        | –        | –                        | –       | –                        | V <sub>CCO</sub> – 0.4  | 0.4                     |
| DIFF_SSTL18_I        | –               | –        | –        | –                        | –       | –                        | V <sub>TT</sub> + 0.475 | V <sub>TT</sub> – 0.475 |
| DIFF_SSTL18_II       | –               | –        | –        | –                        | –       | –                        | V <sub>TT</sub> + 0.475 | V <sub>TT</sub> – 0.475 |
| DIFF_SSTL2_I         | –               | –        | –        | –                        | –       | –                        | V <sub>TT</sub> + 0.61  | V <sub>TT</sub> – 0.61  |
| DIFF_SSTL2_II        | –               | –        | –        | –                        | –       | –                        | V <sub>TT</sub> + 0.81  | V <sub>TT</sub> – 0.81  |
| DIFF_SSTL3_I         | –               | –        | –        | –                        | –       | –                        | V <sub>TT</sub> + 0.6   | V <sub>TT</sub> – 0.6   |
| DIFF_SSTL3_II        | –               | –        | –        | –                        | –       | –                        | V <sub>TT</sub> + 0.8   | V <sub>TT</sub> – 0.8   |

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8 and Table 13.
2. See "External Termination Requirements for Differential I/O."
3. Output voltage measurements for all differential standards are made with a termination resistor (R<sub>T</sub>) of 100Ω across the N and P pins of the differential signal pair.
4. At any given time, no more than two of the following differential output standards can be assigned to an I/O bank: LVDS\_25, RSDS\_25, MINI\_LVDS\_25, PPDS\_25 when V<sub>CCO</sub>=2.5V, or LVDS\_33, RSDS\_33, MINI\_LVDS\_33, TMDS\_33, PPDS\_33 when V<sub>CCO</sub> = 3.3V

## External Termination Requirements for Differential I/O

### LVDS, RSDS, MINI\_LVDS, and PPDS I/O Standards

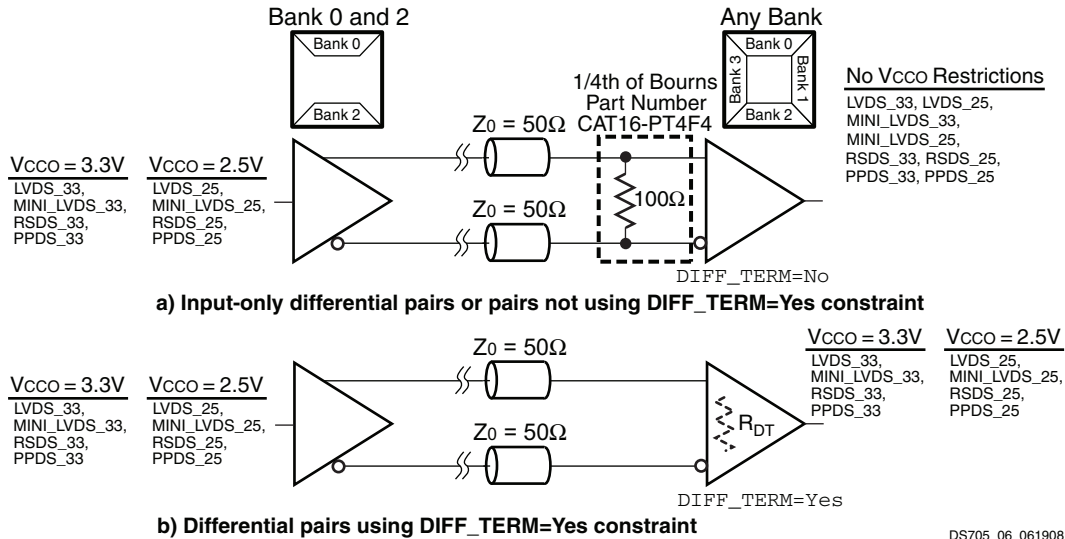


Figure 5: External Input Termination for LVDS, RSDS, MINI\_LVDS, and PPDS I/O Standards

### BLVDS\_25 I/O Standard

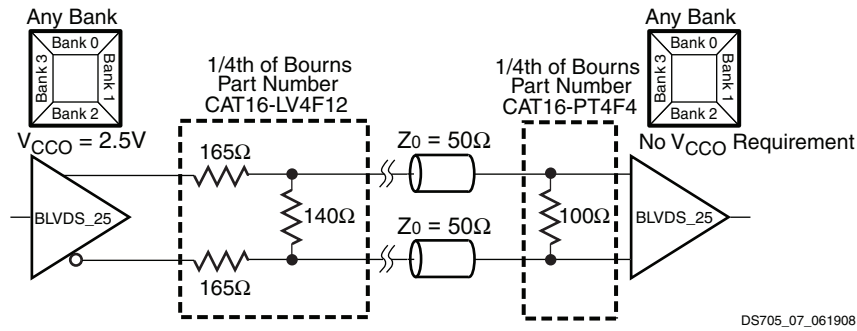


Figure 6: External Output and Input Termination Resistors for BLVDS\_25 I/O Standard

### TMDS\_33 I/O Standard

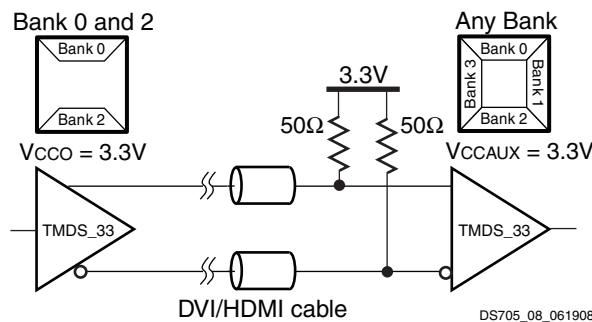


Figure 7: External Input Resistors Required for TMDS\_33 I/O Standard

## Device DNA Read Endurance

Table 15: Device DNA Identifier Memory Characteristics

| Symbol     | Description  | Minimum    | Units       |
|------------|--|------------|-------------|
| DNA_CYCLES | Number of READ operations or JTAG ISC_DNA read operations. Unaffected by HOLD or SHIFT operations. | 30,000,000 | Read cycles |

## Switching Characteristics

All XA Spartan-3A DSP FPGAs ship in the -4 speed grade. Switching characteristics in this document are designated as Production, as shown in [Table 16](#).

**Production:** These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes.

## Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Preview, Advance, or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all XA Spartan-3A DSP devices. AC and DC characteristics are specified using the same numbers for both I-Grade and Q-Grade.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The XA Spartan-3A DSP FPGA speed files (v1.32), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in [Table 16](#). For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

*Table 16: XA Spartan-3A DSP FPGA v1.32 Speed Grade Designations*

| Device     | Production |
|------------|------------|
| XA3SD1800A | -4         |
| XA3SD3400A | -4         |

[Table 17](#) provides the recent history of the XA Spartan-3A DSP FPGA speed files.

*Table 17: XA Spartan-3A DSP Speed File Version History*

| Version | ISE Software Release | Description             |
|---------|----------------------|-------------------------|
| 1.32    | ISE 10.1 SP2         | Support for Automotive. |



## I/O Timing

### Pin-to-Pin Clock-to-Output Times

Table 18: Pin-to-Pin Clock-to-Output Times for the IOB Output Path

| Symbol                       | Description   | Conditions  | Device     | Speed Grade | Units |
|------------------------------|---|---|------------|-------------|-------|
|                              |   |   |            | -4          |       |
|                              |   |   |            | Max         |       |
| <b>Clock-to-Output Times</b> |   |   |            |             |       |
| T <sub>ICKOFDCM</sub>        | When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use. | LVCMOS25 <sup>(2)</sup> , 12 mA output drive, Fast slew rate, with DCM <sup>(3)</sup> | XA3SD1800A | 3.51        | ns    |
|                              |   |   | XA3SD3400A | 3.82        | ns    |
| T <sub>ICKOF</sub>           | When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.                    | LVCMOS25 <sup>(2)</sup> , 12 mA output drive, Fast slew rate, without DCM             | XA3SD1800A | 5.58        | ns    |
|                              |   |   | XA3SD3400A | 6.13        | ns    |

**Notes:**

- The numbers in this table are tested using the methodology presented in [Table 27](#) and are based on the operating conditions set forth in [Table 8](#) and [Table 11](#).
- This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from [Table 23](#). If the latter is true, *add* the appropriate Output adjustment from [Table 26](#).
- DCM output jitter is included in all measurements.

### Pin-to-Pin Setup and Hold Times

Table 19: Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)

| Symbol             | Description  | Conditions   | Device     | Speed Grade | Units |
|--------------------|--|--|------------|-------------|-------|
|                    |  |  |            | -4          |       |
|                    |  |  |            | Min         |       |
| <b>Setup Times</b> |  |  |            |             |       |
| T <sub>PSDCM</sub> | When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed. | LVCMOS25 <sup>(2)</sup> , IFD_DELAY_VALUE = 0, with DCM <sup>(4)</sup> | XA3SD1800A | 3.11        | ns    |
|                    |  |  | XA3SD3400A | 2.49        | ns    |
| T <sub>PSFD</sub>  | When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.                 | LVCMOS25 <sup>(2)</sup> , IFD_DELAY_VALUE = 6, without DCM             | XA3SD1800A | 3.39        | ns    |
|                    |  |  | XA3SD3400A | 3.08        | ns    |
| <b>Hold Times</b>  |  |  |            |             |       |
| T <sub>PHDCM</sub> | When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.      | LVCMOS25 <sup>(3)</sup> , IFD_DELAY_VALUE = 0, with DCM <sup>(4)</sup> | XA3SD1800A | -0.38       | ns    |
|                    |  |  | XA3SD3400A | -0.26       | ns    |
| T <sub>PHFD</sub>  | When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed. | LVCMOS25 <sup>(3)</sup> , IFD_DELAY_VALUE = 6, without DCM             | XA3SD1800A | -0.71       | ns    |
|                    |  |  | XA3SD3400A | -0.65       | ns    |

**Notes:**

- The numbers in this table are tested using the methodology presented in [Table 27](#) and are based on the operating conditions set forth in [Table 8](#) and [Table 11](#).
- This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from [Table 23](#). If this is true of the data Input, add the appropriate Input adjustment from the same table.
- This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from [Table 23](#). If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
- DCM output jitter is included in all measurements.

**Input Setup and Hold Times**

Table 20: Setup and Hold Times for the IOB Input Path

| Symbol               | Description   | Conditions              | IFD_DELAY_VALUE | Device     | Speed Grade | Units |
|----------------------|---|-------------------------|-----------------|------------|-------------|-------|
|                      |   |                         |                 |            | -4<br>Min   |       |
| <b>Setup Times</b>   |   |                         |                 |            |             |       |
| T <sub>IOPICK</sub>  | Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.                 | LVCMOS25 <sup>(2)</sup> | 0               | XA3SD1800A | 1.81        | ns    |
|                      |   |                         |                 | XA3SD3400A | 1.88        | ns    |
| T <sub>IOPICKD</sub> | Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.                | LVCMOS25 <sup>(2)</sup> | 1               | XA3SD1800A | 2.24        | ns    |
|                      |   |                         |                 |            | 2.83        | ns    |
|                      |   |                         |                 |            | 3.64        | ns    |
|                      |   |                         |                 |            | 4.20        | ns    |
|                      |   |                         |                 |            | 4.16        | ns    |
|                      |   |                         |                 |            | 5.09        | ns    |
|                      |   |                         |                 |            | 6.02        | ns    |
|                      |   |                         |                 |            | 6.63        | ns    |
|                      |   |                         |                 | XA3SD3400A | 2.44        | ns    |
|                      |   |                         |                 |            | 3.02        | ns    |
|                      |   |                         |                 |            | 3.81        | ns    |
|                      |   |                         |                 |            | 4.39        | ns    |
|                      |   |                         |                 |            | 4.26        | ns    |
|                      |   |                         |                 |            | 5.08        | ns    |
|                      |   |                         |                 |            | 5.95        | ns    |
|                      |   |                         |                 |            | 6.55        | ns    |
| <b>Hold Times</b>    |   |                         |                 |            |             |       |
| T <sub>IOICKP</sub>  | Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. No Input Delay is programmed. | LVCMOS25 <sup>(2)</sup> | 0               | XA3SD1800A | -0.52       | ns    |
|                      |   |                         |                 | XA3SD3400A | -0.56       | ns    |

Table 20: Setup and Hold Times for the IOB Input Path (Cont'd)

| Symbol                       | Description  | Conditions              | IFD_DELAY_VALUE | Device     | Speed Grade | Units |
|------------------------------|--|-------------------------|-----------------|------------|-------------|-------|
|                              |  |                         |                 |            | -4          |       |
|                              |  |                         |                 |            | Min         |       |
| T <sub>IOICKPD</sub>         | Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. The Input Delay is programmed. | LVCMOS25 <sup>(2)</sup> | 1               | XA3SD1800A | -1.40       | ns    |
|                              |  |                         | 2               |            | -2.11       | ns    |
|                              |  |                         | 3               |            | -2.48       | ns    |
|                              |  |                         | 4               |            | -2.77       | ns    |
|                              |  |                         | 5               |            | -2.62       | ns    |
|                              |  |                         | 6               |            | -3.06       | ns    |
|                              |  |                         | 7               |            | -3.42       | ns    |
|                              |  |                         | 8               |            | -3.65       | ns    |
|                              |  |                         | 1               | XA3SD3400A | -1.31       | ns    |
|                              |  |                         | 2               |            | -1.88       | ns    |
|                              |  |                         | 3               |            | -2.44       | ns    |
|                              |  |                         | 4               |            | -2.89       | ns    |
|                              |  |                         | 5               |            | -2.83       | ns    |
|                              |  |                         | 6               |            | -3.33       | ns    |
|                              |  |                         | 7               |            | -3.63       | ns    |
|                              |  |                         | 8               |            | -3.96       | ns    |
| <b>Set/Reset Pulse Width</b> |  |                         |                 |            |             |       |
| T <sub>RPW_IOB</sub>         | Minimum pulse width to SR control input on IOB   | -                       | -               | All        | 1.61        | ns    |

**Notes:**

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 23.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 23. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 21: Sample Window (Source Synchronous)

| Symbol            | Description                                       | Max   | Units |
|-------------------|---|---|-------|
| T <sub>SAMP</sub> | Setup and hold capture window of an IOB flip-flop | The input capture sample window value is highly specific to a particular application, device, package, I/O standard, I/O placement, DCM usage, and clock buffer. Please consult the appropriate Xilinx Answer Record for application-specific values. <ul style="list-style-type: none"> <li>• Answer Record <a href="#">30879</a></li> </ul> | ps    |

## Input Propagation Times

Table 22: Propagation Times for the IOB Input Path

| Symbol              | Description   | Conditions              | IFD_DELAY_VALUE | Device     | Speed Grade              |      | Units |
|---------------------|---|-------------------------|-----------------|------------|--------------------------|------|-------|
|                     |   |                         |                 |            | -4                       | Max  |       |
|                     |   |                         |                 |            | <b>Propagation Times</b> |      |       |
| T <sub>IOPLI</sub>  | The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed  | LVCMOS25 <sup>(2)</sup> | 0               | XA3SD1800A | 2.04                     | ns   |       |
|                     |   |                         |                 | XA3SD3400A | 2.11                     | ns   |       |
| T <sub>IOPLID</sub> | The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed | LVCMOS25 <sup>(2)</sup> | 1               | XA3SD1800A | 2.47                     | ns   |       |
|                     |   |                         |                 |            | 2                        | 3.06 | ns    |
|                     |   |                         |                 |            | 3                        | 3.86 | ns    |
|                     |   |                         |                 |            | 4                        | 4.43 | ns    |
|                     |   |                         |                 |            | 5                        | 4.39 | ns    |
|                     |   |                         |                 |            | 6                        | 5.32 | ns    |
|                     |   |                         |                 |            | 7                        | 6.24 | ns    |
|                     |   |                         |                 |            | 8                        | 6.86 | ns    |
|                     |   |                         | 1               | XA3SD3400A | 2.67                     | ns   |       |
|                     |   |                         |                 |            | 2                        | 3.25 | ns    |
|                     |   |                         |                 |            | 3                        | 4.04 | ns    |
|                     |   |                         |                 |            | 4                        | 4.62 | ns    |
|                     |   |                         |                 |            | 5                        | 4.49 | ns    |
|                     |   |                         |                 |            | 6                        | 5.31 | ns    |
|                     |   |                         |                 |            | 7                        | 6.18 | ns    |
|                     |   |                         |                 |            | 8                        | 6.78 | ns    |

### Notes:

- The numbers in this table are tested using the methodology presented in [Table 27](#) and are based on the operating conditions set forth in [Table 8](#) and [Table 11](#).
- This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from [Table 23](#).

## Input Timing Adjustments

Table 23: Input Timing Adjustments by IOSTANDARD

| Convert Input Time from LVC MOS25 to the Following Signal Standard (IOSTANDARD) | Add the Adjustment Below | Units |
|---|--------------------------|-------|
|   | -4                       |       |
| <b>Single-Ended Standards</b>   |                          |       |
| LVTTTL  | 0.62                     | ns    |
| LVC MOS33   | 0.54                     | ns    |
| LVC MOS25   | 0.00                     | ns    |
| LVC MOS18   | 0.83                     | ns    |
| LVC MOS15   | 0.60                     | ns    |
| LVC MOS12   | 0.31                     | ns    |
| PCI33_3   | 0.45                     | ns    |
| HSTL_I  | 0.72                     | ns    |
| HSTL_III  | 0.85                     | ns    |
| HSTL_I_18   | 0.69                     | ns    |
| HSTL_II_18  | 0.83                     | ns    |
| HSTL_III_18   | 0.79                     | ns    |
| SSTL18_I  | 0.71                     | ns    |
| SSTL18_II   | 0.71                     | ns    |
| SSTL2_I   | 0.71                     | ns    |
| SSTL2_II  | 0.71                     | ns    |
| SSTL3_I   | 0.78                     | ns    |
| SSTL3_II  | 0.78                     | ns    |

Table 23: Input Timing Adjustments by IOSTANDARD (Cont'd)

| Convert Input Time from LVC MOS25 to the Following Signal Standard (IOSTANDARD) | Add the Adjustment Below | Units |
|---|--------------------------|-------|
|   | -4                       |       |
| <b>Differential Standards</b>   |                          |       |
| LVDS_25   | 0.79                     | ns    |
| LVDS_33   | 0.79                     | ns    |
| BLVDS_25  | 0.79                     | ns    |
| MINI_LVDS_25  | 0.84                     | ns    |
| MINI_LVDS_33  | 0.84                     | ns    |
| LVPECL_25   | 0.80                     | ns    |
| LVPECL_33   | 0.80                     | ns    |
| RSDS_25   | 0.83                     | ns    |
| RSDS_33   | 0.83                     | ns    |
| TMDS_33   | 0.80                     | ns    |
| PPDS_25   | 0.81                     | ns    |
| PPDS_33   | 0.81                     | ns    |
| DIFF_HSTL_I_18  | 0.80                     | ns    |
| DIFF_HSTL_II_18   | 0.98                     | ns    |
| DIFF_HSTL_III_18  | 1.05                     | ns    |
| DIFF_HSTL_I   | 0.77                     | ns    |
| DIFF_HSTL_III   | 1.05                     | ns    |
| DIFF_SSTL18_I   | 0.76                     | ns    |
| DIFF_SSTL18_II  | 0.76                     | ns    |
| DIFF_SSTL2_I  | 0.77                     | ns    |
| DIFF_SSTL2_II   | 0.77                     | ns    |
| DIFF_SSTL3_I  | 1.06                     | ns    |
| DIFF_SSTL3_II   | 1.06                     | ns    |

### Notes:

1. The numbers in this table are tested using the methodology presented in Table 27 and are based on the operating conditions set forth in Table 8, Table 11, and Table 13.
2. These adjustments are used to convert input path times originally specified for the LVC MOS25 standard to times that correspond to other signal standards.

## Output Propagation Times

Table 24: Timing for the IOB Output Path

| Symbol                       | Description   | Conditions  | Device | Speed Grade | Units |
|------------------------------|---|---|--------|-------------|-------|
|                              |   |   |        | -4          |       |
|                              |   |   |        | Max         |       |
| <b>Clock-to-Output Times</b> |   |   |        |             |       |
| $T_{IOCKP}$                  | When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin | LVC MOS25 <sup>(2)</sup> , 12 mA output drive, Fast slew rate | All    | 3.13        | ns    |
| <b>Propagation Times</b>     |   |   |        |             |       |
| $T_{IOOP}$                   | The time it takes for data to travel from the JOB's O input to the Output pin   | LVC MOS25 <sup>(2)</sup> , 12 mA output drive, Fast slew rate | All    | 2.91        | ns    |
| $T_{IOOLP}$                  | The time it takes for data to travel from the O input through the OFF latch to the Output pin   |   |        | 2.85        | ns    |
| <b>Set/Reset Times</b>       |   |   |        |             |       |
| $T_{IOSRP}$                  | Time from asserting the OFF's SR input to setting/resetting data at the Output pin  | LVC MOS25 <sup>(2)</sup> , 12 mA output drive, Fast slew rate | All    | 3.89        | ns    |
| $T_{IOGSRQ}$                 | Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3A primitive to setting/resetting data at the Output pin     |   |        | 9.65        | ns    |

### Notes:

1. The numbers in this table are tested using the methodology presented in [Table 27](#) and are based on the operating conditions set forth in [Table 8](#) and [Table 11](#).
2. This time requires adjustment whenever a signal standard other than LVC MOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from [Table 26](#).

### Three-State Output Propagation Times

Table 25: Timing for the IOB Three-State Path

| Symbol  | Description  | Conditions                                    | Device | Speed Grade |  | Units |
|---|--|---|--------|-------------|--|-------|
|   |  |   |        | -4          |  |       |
|   |  |   |        | Max         |  |       |
| <b>Synchronous Output Enable/Disable Times</b>  |  |   |        |             |  |       |
| $T_{IOCKHZ}$                                    | Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state     | LVC MOS25, 12 mA output drive, Fast slew rate | All    | 1.39        |  | ns    |
| $T_{IOCKON}^{(2)}$                              | Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data  |   | All    | 3.35        |  | ns    |
| <b>Asynchronous Output Enable/Disable Times</b> |  |   |        |             |  |       |
| $T_{GTS}$                                       | Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3A primitive to when the Output pin enters the high-impedance state | LVC MOS25, 12 mA output drive, Fast slew rate | All    | 10.36       |  | ns    |
| <b>Set/Reset Times</b>                          |  |   |        |             |  |       |
| $T_{IOSRHZ}$                                    | Time from asserting TFF's SR input to when the Output pin enters a high-impedance state  | LVC MOS25, 12 mA output drive, Fast slew rate | All    | 1.86        |  | ns    |
| $T_{IOSRON}^{(2)}$                              | Time from asserting TFF's SR input at TFF to when the Output pin drives valid data   |   | All    | 3.82        |  | ns    |

**Notes:**

1. The numbers in this table are tested using the methodology presented in [Table 27](#) and are based on the operating conditions set forth in [Table 8](#) and [Table 11](#).
2. This time requires adjustment whenever a signal standard other than LVC MOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from [Table 26](#).

## Output Timing Adjustments

Table 26: Output Timing Adjustments for IOB

| Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD) |         |       | Add the Adjustment Below | Units |
|---|---------|-------|--------------------------|-------|
|   |         |       | Speed Grade              |       |
|   |         |       | -4                       |       |
| <b>Single-Ended Standards</b>   |         |       |                          |       |
| LVTTTL  | Slow    | 2 mA  | 5.58                     | ns    |
|   |         | 4 mA  | 3.44                     | ns    |
|   |         | 6 mA  | 3.44                     | ns    |
|   |         | 8 mA  | 2.26                     | ns    |
|   |         | 12 mA | 1.66                     | ns    |
|   |         | 16 mA | 1.29                     | ns    |
|   |         | 24 mA | 2.97                     | ns    |
|   |         | Fast  | 2 mA                     | 3.37  |
|   | 4 mA    |       | 2.26                     | ns    |
|   | 6 mA    |       | 2.26                     | ns    |
|   | 8 mA    |       | 0.62                     | ns    |
|   | 12 mA   |       | 0.61                     | ns    |
|   | 16 mA   |       | 0.59                     | ns    |
|   | 24 mA   |       | 0.60                     | ns    |
|   | QuietIO |       | 2 mA                     | 27.67 |
|   |         | 4 mA  | 27.67                    | ns    |
|   |         | 6 mA  | 27.67                    | ns    |
|   |         | 8 mA  | 16.71                    | ns    |
|   |         | 12 mA | 16.67                    | ns    |
|   |         | 16 mA | 16.22                    | ns    |
|   |         | 24 mA | 12.11                    | ns    |

Table 26: Output Timing Adjustments for IOB (Cont'd)

| Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD) |         |       | Add the Adjustment Below | Units |
|---|---------|-------|--------------------------|-------|
|   |         |       | Speed Grade              |       |
|   |         |       | -4                       |       |
| LVC MOS33   | Slow    | 2 mA  | 5.58                     | ns    |
|   |         | 4 mA  | 3.30                     | ns    |
|   |         | 6 mA  | 3.30                     | ns    |
|   |         | 8 mA  | 2.26                     | ns    |
|   |         | 12 mA | 1.29                     | ns    |
|   |         | 16 mA | 1.21                     | ns    |
|   |         | 24 mA | 2.79                     | ns    |
|   |         | Fast  | 2 mA                     | 3.72  |
|   | 4 mA    |       | 2.04                     | ns    |
|   | 6 mA    |       | 2.08                     | ns    |
|   | 8 mA    |       | 0.53                     | ns    |
|   | 12 mA   |       | 0.59                     | ns    |
|   | 16 mA   |       | 0.59                     | ns    |
|   | 24 mA   |       | 0.51                     | ns    |
|   | QuietIO |       | 2 mA                     | 27.67 |
|   |         | 4 mA  | 27.67                    | ns    |
|   |         | 6 mA  | 27.67                    | ns    |
|   |         | 8 mA  | 16.71                    | ns    |
|   |         | 12 mA | 16.29                    | ns    |
|   |         | 16 mA | 16.18                    | ns    |
|   |         | 24 mA | 12.11                    | ns    |



Table 26: Output Timing Adjustments for IOB (Cont'd)

| Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD) |           |         | Add the Adjustment Below | Units |    |
|---|-----------|---------|--------------------------|-------|----|
|   |           |         | Speed Grade              |       |    |
|   |           |         | -4                       |       |    |
| LVC MOS25   | Slow      | 2 mA    | 5.33                     | ns    |    |
|   |           | 4 mA    | 2.90                     | ns    |    |
|   |           | 6 mA    | 2.91                     | ns    |    |
|   |           | 8 mA    | 1.22                     | ns    |    |
|   |           | 12 mA   | 1.22                     | ns    |    |
|   |           | 16 mA   | 0.90                     | ns    |    |
|   |           | 24 mA   | 2.31                     | ns    |    |
|   | Fast      | 2 mA    | 4.71                     | ns    |    |
|   |           | 4 mA    | 2.19                     | ns    |    |
|   |           | 6 mA    | 1.49                     | ns    |    |
|   |           | 8 mA    | 0.39                     | ns    |    |
|   |           | 12 mA   | 0.00                     | ns    |    |
|   |           | 16 mA   | 0.01                     | ns    |    |
|   |           | 24 mA   | 0.01                     | ns    |    |
|   | QuietIO   | 2 mA    | 25.92                    | ns    |    |
|   |           | 4 mA    | 25.92                    | ns    |    |
|   |           | 6 mA    | 25.92                    | ns    |    |
|   |           | 8 mA    | 15.57                    | ns    |    |
|   |           | 12 mA   | 15.59                    | ns    |    |
|   |           | 16 mA   | 14.27                    | ns    |    |
|   |           | 24 mA   | 11.37                    | ns    |    |
|   | LVC MOS18 | Slow    | 2 mA                     | 5.00  | ns |
|   |           |         | 4 mA                     | 3.69  | ns |
|   |           |         | 6 mA                     | 2.91  | ns |
| 8 mA  |           |         | 2.02                     | ns    |    |
| 12 mA   |           |         | 1.57                     | ns    |    |
| Fast  |           | 2 mA    | 4.12                     | ns    |    |
|   |           | 4 mA    | 2.62                     | ns    |    |
|   |           | 6 mA    | 1.91                     | ns    |    |
|   |           | 8 mA    | 1.06                     | ns    |    |
|   |           | 12 mA   | 0.83                     | ns    |    |
|   |           | 16 mA   | 0.63                     | ns    |    |
|   |           | QuietIO | 2 mA                     | 24.97 | ns |
| 4 mA  |           |         | 24.97                    | ns    |    |
| 6 mA  |           |         | 24.08                    | ns    |    |
| 8 mA  |           |         | 16.43                    | ns    |    |
| 12 mA   |           |         | 14.52                    | ns    |    |
|   |           |         | 16 mA                    | 13.41 | ns |

Table 26: Output Timing Adjustments for IOB (Cont'd)

| Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD) |           |       | Add the Adjustment Below | Units |    |
|---|-----------|-------|--------------------------|-------|----|
|   |           |       | Speed Grade              |       |    |
|   |           |       | -4                       |       |    |
| LVC MOS15   | Slow      | 2 mA  | 6.41                     | ns    |    |
|   |           | 4 mA  | 3.97                     | ns    |    |
|   |           | 6 mA  | 3.21                     | ns    |    |
|   |           | 8 mA  | 2.53                     | ns    |    |
|   |           | 12 mA | 2.06                     | ns    |    |
|   | Fast      | 2 mA  | 5.83                     | ns    |    |
|   |           | 4 mA  | 3.05                     | ns    |    |
|   |           | 6 mA  | 1.95                     | ns    |    |
|   |           | 8 mA  | 1.60                     | ns    |    |
|   | QuietIO   | 2 mA  | 34.11                    | ns    |    |
|   |           | 4 mA  | 25.66                    | ns    |    |
|   |           | 6 mA  | 24.64                    | ns    |    |
|   |           | 8 mA  | 22.06                    | ns    |    |
|   | LVC MOS12 | Slow  | 2 mA                     | 7.14  | ns |
|   |           |       | 4 mA                     | 4.87  | ns |
|   |           |       | 6 mA                     | 5.67  | ns |
|   |           | Fast  | 2 mA                     | 6.77  | ns |
|   |           |       | 4 mA                     | 5.02  | ns |
| 6 mA  |           |       | 4.09                     | ns    |    |
| QuietIO   |           | 2 mA  | 50.76                    | ns    |    |
|   |           | 4 mA  | 43.17                    | ns    |    |
|   |           | 6 mA  | 37.31                    | ns    |    |
| PCI33_3   |           |       | 0.34                     | ns    |    |
| HSTL_I  |           |       | 0.85                     | ns    |    |
| HSTL_III  |           |       | 1.16                     | ns    |    |
| HSTL_I_18   |           |       | 0.35                     | ns    |    |
| HSTL_II_18  |           |       | 0.30                     | ns    |    |
| HSTL_III_18   |           |       | 0.47                     | ns    |    |
| SSTL18_I  |           |       | 0.40                     | ns    |    |
| SSTL18_II   |           |       | 0.30                     | ns    |    |
| SSTL2_I   |           |       | 0.00                     | ns    |    |
| SSTL2_II  |           |       | -0.05                    | ns    |    |
| SSTL3_I   |           |       | 0.00                     | ns    |    |
| SSTL3_II  |           |       | 0.17                     | ns    |    |

Table 26: Output Timing Adjustments for IOB (Cont'd)

| Convert Output Time from LVC MOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD) | Add the Adjustment Below | Units |
|---|--------------------------|-------|
|   | Speed Grade              |       |
|   | -4                       |       |
| <b>Differential Standards</b>   |                          |       |
| LVDS_25   | 1.49                     | ns    |
| LVDS_33   | 0.46                     | ns    |
| BLVDS_25  | 0.11                     | ns    |
| MINI_LVDS_25  | 1.11                     | ns    |
| MINI_LVDS_33  | 0.41                     | ns    |
| LVPECL_25   | Input Only               |       |
| LVPECL_33   |                          |       |
| RS DS_25  | 1.72                     | ns    |
| RS DS_33  | 0.64                     | ns    |
| TMDS_33   | 0.46                     | ns    |
| PPDS_25   | 1.28                     | ns    |
| PPDS_33   | 0.88                     | ns    |
| DIFF_HSTL_I_18  | 0.43                     | ns    |
| DIFF_HSTL_II_18   | 0.41                     | ns    |
| DIFF_HSTL_III_18  | 0.36                     | ns    |
| DIFF_HSTL_I   | 1.01                     | ns    |
| DIFF_HSTL_III   | 1.16                     | ns    |
| DIFF_SSTL18_I   | 0.49                     | ns    |
| DIFF_SSTL18_II  | 0.41                     | ns    |
| DIFF_SSTL2_I  | 0.91                     | ns    |
| DIFF_SSTL2_II   | 0.10                     | ns    |
| DIFF_SSTL3_I  | 1.18                     | ns    |
| DIFF_SSTL3_II   | 0.28                     | ns    |

**Notes:**

1. The numbers in this table are tested using the methodology presented in [Table 27](#) and are based on the operating conditions set forth in [Table 8](#), [Table 11](#), and [Table 13](#).
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVC MOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.

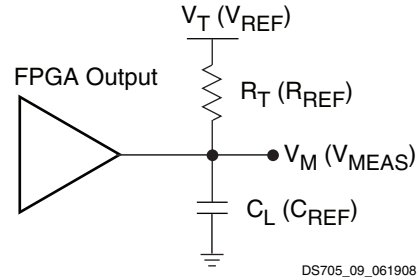
## Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 27 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of  $V_L$  and a High logic level of  $V_H$  is applied to the Input under test. Some standards also require the application of a bias voltage to the  $V_{REF}$  pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal ( $V_M$ ) is commonly located halfway between  $V_L$  and  $V_H$ .

The Output test setup is shown in Figure 8. A termination voltage  $V_T$  is applied to the termination resistor  $R_T$ , the other end of which is connected to the Output. For each standard,  $R_T$  and  $V_T$  generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (for example,

LVC MOS, LVTTTL), then  $R_T$  is set to 1 M $\Omega$  to indicate an open connection, and  $V_T$  is set to zero. The same measurement point ( $V_M$ ) that was used at the Input is also used at the Output.



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**Notes:**

1. The names shown in parentheses are used in the IBIS file.

Figure 8: Output Test Setup

Table 27: Test Methods for Timing Measurement at I/Os

| Signal Standard (IOSTANDARD) | Inputs        |                  |                  | Outputs            |           | Inputs and Outputs |
|------------------------------|---------------|------------------|------------------|--------------------|-----------|--------------------|
|                              | $V_{REF}$ (V) | $V_L$ (V)        | $V_H$ (V)        | $R_T$ ( $\Omega$ ) | $V_T$ (V) | $V_M$ (V)          |
| <b>Single-Ended</b>          |               |                  |                  |                    |           |                    |
| LVTTTL                       | -             | 0                | 3.3              | 1M                 | 0         | 1.4                |
| LVC MOS33                    | -             | 0                | 3.3              | 1M                 | 0         | 1.65               |
| LVC MOS25                    | -             | 0                | 2.5              | 1M                 | 0         | 1.25               |
| LVC MOS18                    | -             | 0                | 1.8              | 1M                 | 0         | 0.9                |
| LVC MOS15                    | -             | 0                | 1.5              | 1M                 | 0         | 0.75               |
| LVC MOS12                    | -             | 0                | 1.2              | 1M                 | 0         | 0.6                |
| PCI33_3                      | Rising        | Note 3           | Note 3           | 25                 | 0         | 0.94               |
|                              | Falling       |                  |                  | 25                 | 3.3       | 2.03               |
| HSTL_I                       | 0.75          | $V_{REF} - 0.5$  | $V_{REF} + 0.5$  | 50                 | 0.75      | $V_{REF}$          |
| HSTL_III                     | 0.9           | $V_{REF} - 0.5$  | $V_{REF} + 0.5$  | 50                 | 1.5       | $V_{REF}$          |
| HSTL_I_18                    | 0.9           | $V_{REF} - 0.5$  | $V_{REF} + 0.5$  | 50                 | 0.9       | $V_{REF}$          |
| HSTL_II_18                   | 0.9           | $V_{REF} - 0.5$  | $V_{REF} + 0.5$  | 25                 | 0.9       | $V_{REF}$          |
| HSTL_III_18                  | 1.1           | $V_{REF} - 0.5$  | $V_{REF} + 0.5$  | 50                 | 1.8       | $V_{REF}$          |
| SSTL18_I                     | 0.9           | $V_{REF} - 0.5$  | $V_{REF} + 0.5$  | 50                 | 0.9       | $V_{REF}$          |
| SSTL18_II                    | 0.9           | $V_{REF} - 0.5$  | $V_{REF} + 0.5$  | 25                 | 0.9       | $V_{REF}$          |
| SSTL2_I                      | 1.25          | $V_{REF} - 0.75$ | $V_{REF} + 0.75$ | 50                 | 1.25      | $V_{REF}$          |
| SSTL2_II                     | 1.25          | $V_{REF} - 0.75$ | $V_{REF} + 0.75$ | 25                 | 1.25      | $V_{REF}$          |
| SSTL3_I                      | 1.5           | $V_{REF} - 0.75$ | $V_{REF} + 0.75$ | 50                 | 1.5       | $V_{REF}$          |
| SSTL3_II                     | 1.5           | $V_{REF} - 0.75$ | $V_{REF} + 0.75$ | 25                 | 1.5       | $V_{REF}$          |

Table 27: Test Methods for Timing Measurement at I/Os (Cont'd)

| Signal Standard<br>(IOSTANDARD) | Inputs        |                   |                   | Outputs            |           | Inputs and<br>Outputs |
|---------------------------------|---------------|-------------------|-------------------|--------------------|-----------|-----------------------|
|                                 | $V_{REF}$ (V) | $V_L$ (V)         | $V_H$ (V)         | $R_T$ ( $\Omega$ ) | $V_T$ (V) | $V_M$ (V)             |
| <b>Differential</b>             |               |                   |                   |                    |           |                       |
| LVDS_25                         | -             | $V_{ICM} - 0.125$ | $V_{ICM} + 0.125$ | 50                 | 1.2       | $V_{ICM}$             |
| LVDS_33                         | -             | $V_{ICM} - 0.125$ | $V_{ICM} + 0.125$ | 50                 | 1.2       | $V_{ICM}$             |
| BLVDS_25                        | -             | $V_{ICM} - 0.125$ | $V_{ICM} + 0.125$ | 1M                 | 0         | $V_{ICM}$             |
| MINI_LVDS_25                    | -             | $V_{ICM} - 0.125$ | $V_{ICM} + 0.125$ | 50                 | 1.2       | $V_{ICM}$             |
| MINI_LVDS_33                    | -             | $V_{ICM} - 0.125$ | $V_{ICM} + 0.125$ | 50                 | 1.2       | $V_{ICM}$             |
| LVPECL_25                       | -             | $V_{ICM} - 0.3$   | $V_{ICM} + 0.3$   | N/A                | N/A       | $V_{ICM}$             |
| LVPECL_33                       | -             | $V_{ICM} - 0.3$   | $V_{ICM} + 0.3$   | N/A                | N/A       | $V_{ICM}$             |
| RSDS_25                         | -             | $V_{ICM} - 0.1$   | $V_{ICM} + 0.1$   | 50                 | 1.2       | $V_{ICM}$             |
| RSDS_33                         | -             | $V_{ICM} - 0.1$   | $V_{ICM} + 0.1$   | 50                 | 1.2       | $V_{ICM}$             |
| TMDS_33                         | -             | $V_{ICM} - 0.1$   | $V_{ICM} + 0.1$   | 50                 | 3.3       | $V_{ICM}$             |
| PPDS_25                         | -             | $V_{ICM} - 0.1$   | $V_{ICM} + 0.1$   | 50                 | 0.8       | $V_{ICM}$             |
| PPDS_33                         | -             | $V_{ICM} - 0.1$   | $V_{ICM} + 0.1$   | 50                 | 0.8       | $V_{ICM}$             |
| DIFF_HSTL_I_18                  | 0.9           | $V_{REF} - 0.5$   | $V_{REF} + 0.5$   | 50                 | 0.9       | $V_{REF}$             |
| DIFF_HSTL_II_18                 | 0.9           | $V_{REF} - 0.5$   | $V_{REF} + 0.5$   | 50                 | 0.9       | $V_{REF}$             |
| DIFF_HSTL_III_18                | 1.1           | $V_{REF} - 0.5$   | $V_{REF} + 0.5$   | 50                 | 1.8       | $V_{REF}$             |
| DIFF_HSTL_I                     | 0.9           | $V_{REF} - 0.5$   | $V_{REF} + 0.5$   | 50                 | 0.9       | $V_{REF}$             |
| DIFF_HSTL_III                   | 0.9           | $V_{REF} - 0.5$   | $V_{REF} + 0.5$   | 50                 | 0.9       | $V_{REF}$             |
| DIFF_SSTL18_I                   | 0.9           | $V_{REF} - 0.5$   | $V_{REF} + 0.5$   | 50                 | 0.9       | $V_{REF}$             |
| DIFF_SSTL18_II                  | 0.9           | $V_{REF} - 0.5$   | $V_{REF} + 0.5$   | 50                 | 0.9       | $V_{REF}$             |
| DIFF_SSTL2_I                    | 1.25          | $V_{REF} - 0.5$   | $V_{REF} + 0.5$   | 50                 | 1.25      | $V_{REF}$             |
| DIFF_SSTL2_II                   | 1.25          | $V_{REF} - 0.5$   | $V_{REF} + 0.5$   | 50                 | 1.25      | $V_{REF}$             |
| DIFF_SSTL3_I                    | 1.5           | $V_{REF} - 0.5$   | $V_{REF} + 0.5$   | 50                 | 1.5       | $V_{REF}$             |
| DIFF_SSTL3_II                   | 1.5           | $V_{REF} - 0.5$   | $V_{REF} + 0.5$   | 50                 | 1.5       | $V_{REF}$             |

**Notes:**

- Descriptions of the relevant symbols are as follows:  
 $V_{REF}$  – The reference voltage for setting the input switching threshold  
 $V_{ICM}$  – The common mode input voltage  
 $V_M$  – Voltage of measurement point on signal transition  
 $V_L$  – Low-level test voltage at Input pin  
 $V_H$  – High-level test voltage at Input pin  
 $R_T$  – Effective termination resistance, which takes on a value of 1 M $\Omega$  when no parallel termination is required  
 $V_T$  – Termination voltage
- The load capacitance ( $C_L$ ) at the Output pin is 0 pF for all signal standards.
- According to the PCI specification.

The capacitive load ( $C_L$ ) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a  $C_L$  value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

### Using IBIS Models to Simulate Load Conditions in Application

IBIS models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model ( $V_{REF}$ ,  $R_{REF}$  and  $V_{MEAS}$ ) correspond directly with the parameters used in Table 27 ( $V_T$ ,  $R_T$ , and  $V_M$ ). Do not confuse  $V_{REF}$  (the termination voltage) from the IBIS

model with  $V_{REF}$  (the input-switching threshold) from the table. A fourth parameter,  $C_{REF}$  is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link:

[www.xilinx.com/support/download/index.htm](http://www.xilinx.com/support/download/index.htm)

Delays for a given application are simulated according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 8. Use parameter values  $V_T$ ,  $R_T$ , and  $V_M$  from Table 27.  $C_{REF}$  is zero.
2. Record the time to  $V_M$ .
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including  $V_{REF}$ ,  $R_{REF}$ ,  $C_{REF}$ , and  $V_{MEAS}$  values) or capacitive value to represent the load.
4. Record the time to  $V_{MEAS}$ .
5. Compare the results of steps 2 and 4. Add (or subtract) the increase (or decrease) in delay to (or from) the appropriate Output standard adjustment (Table 26) to yield the worst-case delay of the PCB trace.

### Simultaneously Switching Output Guidelines

This section provides guidelines for the recommended maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins of a given output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the  $V_{CCO}$  rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 28 and Table 29 provide the essential SSO guidelines. For each device/package combination, Table 28

provides the number of equivalent  $V_{CCO}/GND$  pairs. The equivalent number of pairs is based on characterization and may not match the physical number of pairs. For each output signal standard and drive strength, Table 29 recommends the maximum number of SSOs, switching in the same direction, allowed per  $V_{CCO}/GND$  pair within an I/O bank. The guidelines in Table 29 are categorized by package style, slew rate, and output drive current. Furthermore, the number of SSOs is specified by I/O bank. Generally, the left and right I/O banks (Banks 1 and 3) support higher output drive current.

Multiply the appropriate numbers from Table 28 and Table 29 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines might result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

$$SSO_{MAX}/IO\ Bank = Table\ 28 \times Table\ 29$$

The recommended maximum SSO values assumes that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The SSO values assume that the  $V_{CCAUX}$  is powered at 3.3V. Setting  $V_{CCAUX}$  to 2.5V provides better SSO characteristics.

Table 28: Equivalent  $V_{CCO}/GND$  Pairs per Bank

| Device     | Package Style (Pb-free) |        |
|------------|-------------------------|--------|
|            | CSG484                  | FGG676 |
| XA3SD1800A | 6                       | 9      |
| XA3SD3400A | 6                       | 10     |

Table 29: Recommended Number of Simultaneously Switching Outputs per V<sub>CCO</sub>-GND Pair (V<sub>CCAUX</sub>=3.3V)

| Signal Standard (IOSTANDARD)  |         | Package Type            |                         |    |    |
|-------------------------------|---------|-------------------------|-------------------------|----|----|
|                               |         | CSG484, FGG676          |                         |    |    |
|                               |         | Top, Bottom (Banks 0,2) | Left, Right (Banks 1,3) |    |    |
| <b>Single-Ended Standards</b> |         |                         |                         |    |    |
| LVTTTL                        | Slow    | 2                       | 60                      | 60 |    |
|                               |         | 4                       | 41                      | 41 |    |
|                               |         | 6                       | 29                      | 29 |    |
|                               |         | 8                       | 22                      | 22 |    |
|                               |         | 12                      | 13                      | 13 |    |
|                               |         | 16                      | 11                      | 11 |    |
|                               |         | 24                      | 9                       | 9  |    |
|                               |         | Fast                    | 2                       | 10 | 10 |
|                               | 4       |                         | 6                       | 6  |    |
|                               | 6       |                         | 5                       | 5  |    |
|                               | 8       |                         | 3                       | 3  |    |
|                               | 12      |                         | 3                       | 3  |    |
|                               | 16      |                         | 3                       | 3  |    |
|                               | 24      |                         | 2                       | 2  |    |
|                               | QuietIO |                         | 2                       | 80 | 80 |
|                               |         | 4                       | 48                      | 48 |    |
|                               |         | 6                       | 36                      | 36 |    |
|                               |         | 8                       | 27                      | 27 |    |
|                               |         | 12                      | 16                      | 16 |    |
|                               |         | 16                      | 13                      | 13 |    |
|                               |         | 24                      | 12                      | 12 |    |
|                               |         | LVCMOS33                | Slow                    | 2  | 76 |
|                               | 4       |                         |                         | 46 | 46 |
|                               | 6       |                         |                         | 27 | 27 |
| 8                             | 20      |                         |                         | 20 |    |
| 12                            | 13      |                         |                         | 13 |    |
| 16                            | 10      |                         |                         | 10 |    |
| 24                            | –       |                         |                         | 9  |    |
| Fast                          | 2       |                         | 10                      | 10 |    |
|                               | 4       |                         | 8                       | 8  |    |
|                               | 6       |                         | 5                       | 5  |    |
|                               | 8       |                         | 4                       | 4  |    |
|                               | 12      |                         | 4                       | 4  |    |
|                               | 16      |                         | 2                       | 2  |    |
|                               | 24      |                         | –                       | 2  |    |
| QuietIO                       | 2       |                         | 76                      | 76 |    |
|                               | 4       |                         | 46                      | 46 |    |
|                               | 6       |                         | 32                      | 32 |    |
|                               | 8       |                         | 26                      | 26 |    |
|                               | 12      |                         | 18                      | 18 |    |
|                               | 16      |                         | 14                      | 14 |    |
|                               | 24      |                         | –                       | 10 |    |

 Table 29: Recommended Number of Simultaneously Switching Outputs per V<sub>CCO</sub>-GND Pair (V<sub>CCAUX</sub>=3.3V)

| Signal Standard (IOSTANDARD) |         | Package Type            |                         |    |    |
|------------------------------|---------|-------------------------|-------------------------|----|----|
|                              |         | CSG484, FGG676          |                         |    |    |
|                              |         | Top, Bottom (Banks 0,2) | Left, Right (Banks 1,3) |    |    |
| LVCMOS25                     | Slow    | 2                       | 76                      | 76 |    |
|                              |         | 4                       | 46                      | 46 |    |
|                              |         | 6                       | 33                      | 33 |    |
|                              |         | 8                       | 24                      | 24 |    |
|                              |         | 12                      | 18                      | 18 |    |
|                              |         | 16                      | –                       | 11 |    |
|                              |         | 24                      | –                       | 7  |    |
|                              |         | Fast                    | 2                       | 18 | 18 |
|                              | 4       |                         | 14                      | 14 |    |
|                              | 6       |                         | 6                       | 6  |    |
|                              | 8       |                         | 6                       | 6  |    |
|                              | 12      |                         | 3                       | 3  |    |
|                              | 16      |                         | –                       | 3  |    |
|                              | 24      |                         | –                       | 2  |    |
|                              | QuietIO |                         | 2                       | 76 | 76 |
|                              |         | 4                       | 60                      | 60 |    |
|                              |         | 6                       | 48                      | 48 |    |
|                              |         | 8                       | 36                      | 36 |    |
|                              |         | 12                      | 36                      | 36 |    |
|                              |         | 16                      | –                       | 36 |    |
|                              |         | 24                      | –                       | 8  |    |
|                              |         | LVCMOS18                | Slow                    | 2  | 64 |
|                              | 4       |                         |                         | 34 | 34 |
|                              | 6       |                         |                         | 22 | 22 |
| 8                            | 18      |                         |                         | 18 |    |
| 12                           | –       |                         |                         | 13 |    |
| 16                           | –       |                         |                         | 10 |    |
| Fast                         | 2       |                         | 18                      | 18 |    |
|                              | 4       |                         | 9                       | 9  |    |
|                              | 6       |                         | 7                       | 7  |    |
|                              | 8       |                         | 4                       | 4  |    |
|                              | 12      |                         | –                       | 4  |    |
|                              | 16      |                         | –                       | 3  |    |
| QuietIO                      | 2       |                         | 64                      | 64 |    |
|                              | 4       |                         | 64                      | 64 |    |
|                              | 6       |                         | 48                      | 48 |    |
|                              | 8       |                         | 36                      | 36 |    |
|                              | 12      |                         | –                       | 36 |    |
|                              | 16      |                         | –                       | 24 |    |

**Table 29: Recommended Number of Simultaneously Switching Outputs per V<sub>CCO</sub>-GND Pair (V<sub>CCAUX</sub>=3.3V)**

| Signal Standard (IOSTANDARD) |          |      | Package Type               |                            |
|------------------------------|----------|------|----------------------------|----------------------------|
|                              |          |      | CSG484, FGG676             |                            |
|                              |          |      | Top, Bottom<br>(Banks 0,2) | Left, Right<br>(Banks 1,3) |
| LVCMOS15                     | Slow     | 2    | 55                         | 55                         |
|                              |          | 4    | 31                         | 31                         |
|                              |          | 6    | 18                         | 18                         |
|                              |          | 8    | –                          | 15                         |
|                              |          | 12   | –                          | 10                         |
|                              | Fast     | 2    | 25                         | 25                         |
|                              |          | 4    | 10                         | 10                         |
|                              |          | 6    | 6                          | 6                          |
|                              |          | 8    | –                          | 4                          |
|                              |          | 12   | –                          | 3                          |
|                              | QuietIO  | 2    | 70                         | 70                         |
|                              |          | 4    | 40                         | 40                         |
|                              |          | 6    | 31                         | 31                         |
|                              |          | 8    | –                          | 31                         |
|                              |          | 12   | –                          | 20                         |
|                              | LVCMOS12 | Slow | 2                          | 40                         |
| 4                            |          |      | –                          | 25                         |
| 6                            |          |      | –                          | 18                         |
| Fast                         |          | 2    | 31                         | 31                         |
|                              |          | 4    | –                          | 13                         |
|                              |          | 6    | –                          | 9                          |
| QuietIO                      |          | 2    | 55                         | 55                         |
|                              |          | 4    | –                          | 36                         |
|                              |          | 6    | –                          | 36                         |
|                              |          |      |                            |                            |
| PCI33_3                      |          |      | 16                         | 16                         |
| HSTL_I                       |          |      | –                          | 20                         |
| HSTL_III                     |          |      | –                          | 8                          |
| HSTL_I_18                    |          |      | 17                         | 17                         |
| HSTL_II_18                   |          |      | –                          | 5                          |
| HSTL_III_18                  |          |      | 10                         | 8                          |
| SSTL18_I                     |          |      | 7                          | 15                         |
| SSTL18_II                    |          |      | –                          | 9                          |
| SSTL2_I                      |          |      | 18                         | 18                         |
| SSTL2_II                     |          |      | –                          | 9                          |
| SSTL3_I                      |          |      | 8                          | 10                         |
| SSTL3_II                     |          |      | 6                          | 7                          |

**Table 29: Recommended Number of Simultaneously Switching Outputs per V<sub>CCO</sub>-GND Pair (V<sub>CCAUX</sub>=3.3V)**

| Signal Standard (IOSTANDARD)                                    |  | Package Type               |                            |
|---|--|----------------------------|----------------------------|
|   |  | CSG484, FGG676             |                            |
|   |  | Top, Bottom<br>(Banks 0,2) | Left, Right<br>(Banks 1,3) |
| <b>Differential Standards (Number of I/O Pairs or Channels)</b> |  |                            |                            |
| LVDS_25   |  | 22                         | –                          |
| LVDS_33   |  | 27                         | –                          |
| BLVDS_25  |  | 4                          | 4                          |
| MINI_LVDS_25  |  | 22                         | –                          |
| MINI_LVDS_33  |  | 27                         | –                          |
| LVPECL_25   |  | Inputs Only                |                            |
| LVPECL_33   |  | Inputs Only                |                            |
| RSDS_25   |  | 22                         | –                          |
| RSDS_33   |  | 27                         | –                          |
| TMDS_33   |  | 27                         | –                          |
| PPDS_25   |  | 22                         | –                          |
| PPDS_33   |  | 27                         | –                          |
| DIFF_HSTL_I_18  |  | 8                          | 8                          |
| DIFF_HSTL_II_18   |  | –                          | 2                          |
| DIFF_HSTL_III_18  |  | 5                          | 4                          |
| DIFF_HSTL_I   |  | –                          | 10                         |
| DIFF_HSTL_III   |  | –                          | 4                          |
| DIFF_SSTL18_I   |  | 3                          | 7                          |
| DIFF_SSTL18_II  |  | –                          | 1                          |
| DIFF_SSTL2_I  |  | 9                          | 9                          |
| DIFF_SSTL2_II   |  | –                          | 4                          |
| DIFF_SSTL3_I  |  | 4                          | 5                          |
| DIFF_SSTL3_II   |  | 3                          | 3                          |

**Notes:**

- Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in top or bottom banks (I/O banks 0 and 2). Refer to [UG331](#), *Spartan-3 Generation FPGA User Guide* for additional information.
- The numbers in this table are recommendations that assume sound board layout practice. This table assumes the following parasitic factors: combined PCB trace and land inductance per V<sub>CCO</sub> and GND pin of 1.0 nH, receiver capacitive load of 15 pF. Test limits are the V<sub>IL</sub>/V<sub>IH</sub> voltage limits for the respective I/O standard.
- If more than one signal standard is assigned to the I/Os of a given bank, refer to [XAPP689](#), *Managing Ground Bounce in Large FPGAs* for information on how to perform weighted average SSO calculations.

## Configurable Logic Block Timing

Table 30: CLB (SLICEM) Timing

| Symbol                       | Description   | Speed Grade |      | Units |
|------------------------------|---|-------------|------|-------|
|                              |   | -4          |      |       |
|                              |   | Min         | Max  |       |
| <b>Clock-to-Output Times</b> |   |             |      |       |
| $T_{CKO}$                    | When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output | –           | 0.68 | ns    |
| <b>Setup Times</b>           |   |             |      |       |
| $T_{AS}$                     | Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB                                    | 0.36        | –    | ns    |
| $T_{DICK}$                   | Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB                                  | 1.88        | –    | ns    |
| <b>Hold Times</b>            |   |             |      |       |
| $T_{AH}$                     | Time from the active transition at the CLK input to the point where data is last held at the F or G input                               | 0.00        | –    | ns    |
| $T_{CKDI}$                   | Time from the active transition at the CLK input to the point where data is last held at the BX or BY input                             | 0.00        | –    | ns    |
| <b>Clock Timing</b>          |   |             |      |       |
| $T_{CH}$                     | The High pulse width of the CLB's CLK signal  | 0.75        | –    | ns    |
| $T_{CL}$                     | The Low pulse width of the CLK signal   | 0.75        | –    | ns    |
| $F_{TOG}$                    | Toggle frequency (for export control)   | 0           | 667  | MHz   |
| <b>Propagation Times</b>     |   |             |      |       |
| $T_{ILO}$                    | The time it takes for data to travel from the CLB's F (G) input to the X (Y) output   | –           | 0.71 | ns    |
| <b>Set/Reset Pulse Width</b> |   |             |      |       |
| $T_{RPW\_CLB}$               | The minimum allowable pulse width, High or Low, to the CLB's SR input   | 1.61        | –    | ns    |

**Notes:**

- The numbers in this table are based on the operating conditions set forth in [Table 8](#).



Table 31: CLB Distributed RAM Switching Characteristics

| Symbol                       | Description   | Speed Grade |      | Units |
|------------------------------|---|-------------|------|-------|
|                              |   | -4          |      |       |
|                              |   | Min         | Max  |       |
| <b>Clock-to-Output Times</b> |   |             |      |       |
| $T_{SHCKO}$                  | Time from the active edge at the CLK input to data appearing on the distributed RAM output  | -           | 1.72 | ns    |
| <b>Setup Times</b>           |   |             |      |       |
| $T_{DS}$                     | Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM                     | -0.02       | -    | ns    |
| $T_{AS}$                     | Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM                         | 0.36        | -    | ns    |
| $T_{WS}$                     | Setup time of the write enable input before the active transition at the CLK input of the distributed RAM                         | 0.59        | -    | ns    |
| <b>Hold Times</b>            |   |             |      |       |
| $T_{DH}$                     | Hold time of the BX and BY data inputs after the active transition at the CLK input of the distributed RAM                        | 0.13        | -    | ns    |
| $T_{AH}, T_{WH}$             | Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM | 0.01        | -    | ns    |
| <b>Clock Pulse Width</b>     |   |             |      |       |
| $T_{WPH}, T_{WPL}$           | Minimum High or Low pulse width at CLK input  | 1.01        | -    | ns    |

Table 32: CLB Shift Register Switching Characteristics

| Symbol                       | Description  | Speed Grade |      | Units |
|------------------------------|--|-------------|------|-------|
|                              |  | -4          |      |       |
|                              |  | Min         | Max  |       |
| <b>Clock-to-Output Times</b> |  |             |      |       |
| $T_{REG}$                    | Time from the active edge at the CLK input to data appearing on the shift register output                    | -           | 4.82 | ns    |
| <b>Setup Times</b>           |  |             |      |       |
| $T_{SRLDS}$                  | Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register | 0.18        | -    | ns    |
| <b>Hold Times</b>            |  |             |      |       |
| $T_{SRLDH}$                  | Hold time of the BX or BY data input after the active transition at the CLK input of the shift register      | 0.16        | -    | ns    |
| <b>Clock Pulse Width</b>     |  |             |      |       |
| $T_{WPH}, T_{WPL}$           | Minimum High or Low pulse width at CLK input   | 1.01        | -    | ns    |

## Clock Buffer/Multiplexer Switching Characteristics

Table 33: Clock Distribution Switching Characteristics

| Description  | Symbol     | Minimum | Maximum | Units |
|--|------------|---------|---------|-------|
| Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay  | $T_{GIO}$  | -       | 0.23    | ns    |
| Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs.<br>Same as BUFGCE enable CE-input | $T_{GSI}$  | -       | 0.63    | ns    |
| Frequency of signals distributed on global buffers (all sides)   | $F_{BUFG}$ | 0       | 334     | MHz   |

### Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 8](#).

## Block RAM Timing

Table 34: Block RAM Timing

| Symbol                       | Description   | Speed Grade |      | Units |
|------------------------------|---|-------------|------|-------|
|                              |   | -4          |      |       |
|                              |   | Min         | Max  |       |
| <b>Clock-to-Output Times</b> |   |             |      |       |
| $T_{RCKO\_DOA\_NC}$          | When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output | -           | 2.80 | ns    |
| $T_{RCKO\_DOA}$              | Clock CLK to DOUT output (with output register)   | -           | 1.45 | ns    |
| <b>Setup Times</b>           |   |             |      |       |
| $T_{RCKK\_ADDR}$             | Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM                           | 0.46        | -    | ns    |
| $T_{RDCK\_DIB}$              | Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM                    | 0.33        | -    | ns    |
| $T_{RCKK\_ENB}$              | Setup time for the EN input before the active transition at the CLK input of the block RAM                              | 0.60        | -    | ns    |
| $T_{RCKK\_WEB}$              | Setup time for the WE input before the active transition at the CLK input of the block RAM                              | 0.75        | -    | ns    |
| $T_{RCKK\_REGCE}$            | Setup time for the CE input before the active transition at the CLK input of the block RAM                              | 0.40        | -    | ns    |
| $T_{RCKK\_RST}$              | Setup time for the RST input before the active transition at the CLK input of the block RAM                             | 0.25        | -    | ns    |
| <b>Hold Times</b>            |   |             |      |       |
| $T_{RCKC\_ADDR}$             | Hold time on the ADDR inputs after the active transition at the CLK input   | 0.10        | -    | ns    |
| $T_{RDCK\_DIB}$              | Hold time on the DIN inputs after the active transition at the CLK input  | 0.10        | -    | ns    |
| $T_{RCKC\_ENB}$              | Hold time on the EN input after the active transition at the CLK input  | 0.10        | -    | ns    |
| $T_{RCKC\_WEB}$              | Hold time on the WE input after the active transition at the CLK input  | 0.10        | -    | ns    |
| $T_{RCKC\_REGCE}$            | Hold time on the CE input after the active transition at the CLK input  | 0.10        | -    | ns    |
| $T_{RCKC\_RST}$              | Hold time on the RST input after the active transition at the CLK input   | 0.10        | -    | ns    |
| <b>Clock Timing</b>          |   |             |      |       |
| $T_{BPWH}$                   | High pulse width of the CLK signal  | 1.79        | -    | ns    |
| $T_{BPWL}$                   | Low pulse width of the CLK signal   | 1.79        | -    | ns    |
| <b>Clock Frequency</b>       |   |             |      |       |
| $F_{BRAM}$                   | Block RAM clock frequency   | 0           | 280  | MHz   |

### Notes:

- The numbers in this table are based on the operating conditions set forth in [Table 8](#).

## DSP48A Timing

To reference the DSP48A block diagram, see the *XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide* ([UG431](#)).

Table 35: Setup Times for the DSP48A

| Symbol   | Description                         | Pre-adder | Multiplier | Post-adder | Speed Grade | Units |
|--|-------------------------------------|-----------|------------|------------|-------------|-------|
|  |                                     |           |            |            | -4          |       |
|  |                                     |           |            |            | Min         |       |
| <b>Setup Times of Data/Control Pins to the Input Register Clock</b>  |                                     |           |            |            |             |       |
| $T_{\text{DSPDCK\_AA}}$  | A input to A register CLK           | -         | -          | -          | 0.04        | ns    |
| $T_{\text{DSPDCK\_DB}}$  | D input to B register CLK           | Yes       | -          | -          | 1.88        | ns    |
| $T_{\text{DSPDCK\_CC}}$  | C input to C register CLK           | -         | -          | -          | 0.05        | ns    |
| $T_{\text{DSPDCK\_DD}}$  | D input to D register CLK           | -         | -          | -          | 0.04        | ns    |
| $T_{\text{DSPDCK\_OPB}}$   | OPMODE input to B register CLK      | Yes       | -          | -          | 0.42        | ns    |
| $T_{\text{DSPDCK\_OPOP}}$  | OPMODE input to OPMODE register CLK | -         | -          | -          | 0.06        | ns    |
| <b>Setup Times of Data Pins to the Pipeline Register Clock</b>       |                                     |           |            |            |             |       |
| $T_{\text{DSPDCK\_AM}}$  | A input to M register CLK           | -         | Yes        | -          | 3.79        | ns    |
| $T_{\text{DSPDCK\_BM}}$  | B input to M register CLK           | Yes       | Yes        | -          | 4.97        | ns    |
|  |                                     | No        | Yes        | -          | 3.79        | ns    |
| $T_{\text{DSPDCK\_DM}}$  | D input to M register CLK           | Yes       | Yes        | -          | 5.06        | ns    |
| $T_{\text{DSPDCK\_OPM}}$   | OPMODE to M register CLK            | Yes       | Yes        | -          | 5.42        | ns    |
| <b>Setup Times of Data/Control Pins to the Output Register Clock</b> |                                     |           |            |            |             |       |
| $T_{\text{DSPDCK\_AP}}$  | A input to P register CLK           | -         | Yes        | Yes        | 5.49        | ns    |
| $T_{\text{DSPDCK\_BP}}$  | B input to P register CLK           | Yes       | Yes        | Yes        | 6.74        | ns    |
|  |                                     | No        | Yes        | Yes        | 5.48        | ns    |
| $T_{\text{DSPDCK\_DP}}$  | D input to P register CLK           | Yes       | Yes        | Yes        | 6.83        | ns    |
| $T_{\text{DSPDCK\_CP}}$  | C input to P register CLK           | -         | -          | Yes        | 2.18        | ns    |
| $T_{\text{DSPDCK\_OPP}}$   | OPMODE input to P register CLK      | Yes       | Yes        | Yes        | 7.18        | ns    |

### Notes:

- “Yes” means that the component is in the path. “No” means that the component is being bypassed. “-” means that no path exists, so it is not applicable.
- The numbers in this table are based on the operating conditions set forth in [Table 8](#).

Table 36: Clock to Out, Propagation Delays, and Maximum Frequency for the DSP48A

| Symbol  | Description              | Pre-adder | Multiplier | Post-adder | Speed Grade |     | Units |
|---|--------------------------|-----------|------------|------------|-------------|-----|-------|
|   |                          |           |            |            | -4          |     |       |
|   |                          |           |            |            | Max         |     |       |
| <b>Clock to Out from Output Register Clock to Output Pin</b>    |                          |           |            |            |             |     |       |
| $T_{\text{DSPCKO\_PP}}$   | CLK (PREG) to P output   | -         | -          | -          | 1.44        | ns  |       |
| <b>Clock to Out from Pipeline Register Clock to Output Pins</b> |                          |           |            |            |             |     |       |
| $T_{\text{DSPCKO\_PM}}$   | CLK (MREG) to P output   | -         | Yes        | Yes        | 3.63        | ns  |       |
|   |                          | -         | Yes        | No         | 2.23        | ns  |       |
| <b>Clock to Out from Input Register Clock to Output Pins</b>    |                          |           |            |            |             |     |       |
| $T_{\text{DSPCKO\_PA}}$   | CLK (AREG) to P output   | -         | Yes        | Yes        | 7.27        | ns  |       |
| $T_{\text{DSPCKO\_PB}}$   | CLK (BREG) to P output   | Yes       | Yes        | Yes        | 8.56        | ns  |       |
| $T_{\text{DSPCKO\_PC}}$   | CLK (CREG) to P output   | -         | -          | Yes        | 3.87        | ns  |       |
| $T_{\text{DSPCKO\_PD}}$   | CLK (DREG) to P output   | Yes       | Yes        | Yes        | 8.42        | ns  |       |
| <b>Combinatorial Delays from Input Pins to Output Pins</b>      |                          |           |            |            |             |     |       |
| $T_{\text{DSPDO\_AP}}$<br>$T_{\text{DSPDO\_BP}}$                | A or B input to P output | -         | No         | Yes        | 3.19        | ns  |       |
|   |                          | -         | Yes        | No         | 5.28        | ns  |       |
|   |                          | -         | Yes        | Yes        | 6.49        | ns  |       |
| $T_{\text{DSPDO\_BP}}$  | B input to P output      | Yes       | No         | No         | 4.01        | ns  |       |
|   |                          | Yes       | Yes        | No         | 6.65        | ns  |       |
|   |                          | Yes       | Yes        | Yes        | 7.74        | ns  |       |
| $T_{\text{DSPDO\_CP}}$  | C input to P output      | -         | -          | Yes        | 3.17        | ns  |       |
| $T_{\text{DSPDO\_DP}}$  | D input to P output      | Yes       | Yes        | Yes        | 7.82        | ns  |       |
| $T_{\text{DSPDO\_OPP}}$   | OPMODE input to P output | Yes       | Yes        | Yes        | 8.18        | ns  |       |
| <b>Maximum Frequency</b>  |                          |           |            |            |             |     |       |
| $F_{\text{MAX}}$  | All registers used       | Yes       | Yes        | Yes        | 250         | MHz |       |

**Notes:**

1. To reference the DSP48A block diagram, see [UG431](#), *XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide*.
2. “Yes” means that the component is in the path. “No” means that the component is being bypassed. “-” means that no path exists, so it is not applicable.
3. The numbers in this table are based on the operating conditions set forth in [Table 8](#).

## Digital Clock Manager Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 37 and Table 38) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 39 through Table 42) supersede any corresponding ones in the DLL tables. DLL specifications that do not

change with the addition of DFS or PS functions are presented in Table 37 and Table 38.

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

### Delay-Locked Loop

Table 37: Recommended Operating Conditions for the DLL

| Symbol   |   | Description   | Speed Grade                     |                    | Units |    |
|--|---|---|---------------------------------|--------------------|-------|----|
|  |   |   | -4                              |                    |       |    |
|  |   |   | Min                             | Max                |       |    |
| <b>Input Frequency Ranges</b>  |   |   |                                 |                    |       |    |
| $F_{\text{CLKIN}}$   | CLKIN_FREQ_DLL  | Frequency of the CLKIN clock input                    | 5 <sup>(2)</sup>                | 250 <sup>(3)</sup> | MHz   |    |
| <b>Input Pulse Requirements</b>  |   |   |                                 |                    |       |    |
| CLKIN_PULSE  |   | CLKIN pulse width as a percentage of the CLKIN period | $F_{\text{CLKIN}} \leq 150$ MHz | 40%                | 60%   | -  |
|  |   |   | $F_{\text{CLKIN}} > 150$ MHz    | 45%                | 55%   | -  |
| <b>Input Clock Jitter Tolerance and Delay Path Variation<sup>(4)</sup></b> |   |   |                                 |                    |       |    |
| CLKIN_CYC_JITT_DLL_LF  | Cycle-to-cycle jitter at the CLKIN input  |   | $F_{\text{CLKIN}} \leq 150$ MHz | -                  | ±300  | ps |
| CLKIN_CYC_JITT_DLL_HF  |   |   | $F_{\text{CLKIN}} > 150$ MHz    | -                  | ±150  | ps |
| CLKIN_PER_JITT_DLL   | Period jitter at the CLKIN input  |   |                                 | -                  | ±1    | ns |
| CLKFB_DELAY_VAR_EXT  | Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input |   |                                 | -                  | ±1    | ns |

#### Notes:

- DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
- The DFS, when operating independently of the DLL, supports lower  $F_{\text{CLKIN}}$  frequencies. See Table 39.
- To support double the maximum effective  $F_{\text{CLKIN}}$  limit, set the CLKIN\_DIVIDE\_BY\_2 attribute to TRUE. This attribute divides the incoming clock period by two as it enters the DCM. The CLK2X output reproduces the clock frequency provided on the CLKIN input.
- CLKIN input jitter beyond these limits might cause the DCM to lose lock.
- The DCM specifications are guaranteed when both adjacent DCMs are locked.

Table 38: Switching Characteristics for the DLL

| Symbol                                       | Description  | Device  | Speed Grade                  |                               | Units                       |    |
|--|--|---|------------------------------|-------------------------------|-----------------------------|----|
|  |  |   | -4                           |                               |                             |    |
|  |  |   | Min                          | Max                           |                             |    |
| <b>Output Frequency Ranges</b>               |  |   |                              |                               |                             |    |
| CLKOUT_FREQ_CLK0                             | Frequency for the CLK0 and CLK180 outputs  | All   | 5                            | 250                           | MHz                         |    |
| CLKOUT_FREQ_CLK90                            | Frequency for the CLK90 and CLK270 outputs   |   | 5                            | 200                           | MHz                         |    |
| CLKOUT_FREQ_2X                               | Frequency for the CLK2X and CLK2X180 outputs   |   | 10                           | 334                           | MHz                         |    |
| CLKOUT_FREQ_DV                               | Frequency for the CLKDV output   |   | 0.3125                       | 166                           | MHz                         |    |
| <b>Output Clock Jitter<sup>(2,3,4)</sup></b> |  |   |                              |                               |                             |    |
| CLKOUT_PER_JITT_0                            | Period jitter at the CLK0 output   | All   | -                            | ±100                          | ps                          |    |
| CLKOUT_PER_JITT_90                           | Period jitter at the CLK90 output  |   | -                            | ±150                          | ps                          |    |
| CLKOUT_PER_JITT_180                          | Period jitter at the CLK180 output   |   | -                            | ±150                          | ps                          |    |
| CLKOUT_PER_JITT_270                          | Period jitter at the CLK270 output   |   | -                            | ±150                          | ps                          |    |
| CLKOUT_PER_JITT_2X                           | Period jitter at the CLK2X and CLK2X180 outputs  |   | -                            | ±[0.5% of CLKIN period + 100] | ps                          |    |
| CLKOUT_PER_JITT_DV1                          | Period jitter at the CLKDV output when performing integer division   |   | -                            | ±150                          | ps                          |    |
| CLKOUT_PER_JITT_DV2                          | Period jitter at the CLKDV output when performing non-integer division   |   | -                            | ±[0.5% of CLKIN period + 100] | ps                          |    |
| <b>Duty Cycle<sup>(4)</sup></b>              |  |   |                              |                               |                             |    |
| CLKOUT_DUTY_CYCLE_DLL                        | Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion                                     | All   | -                            | ±[1% of CLKIN period + 350]   | ps                          |    |
| <b>Phase Alignment<sup>(4)</sup></b>         |  |   |                              |                               |                             |    |
| CLKIN_CLKFB_PHASE                            | Phase offset between the CLKIN and CLKFB inputs  | All   | -                            | ±150                          | ps                          |    |
| CLKOUT_PHASE_DLL                             | Phase offset between DLL outputs   |   | CLK0 to CLK2X (not CLK2X180) | -                             | ±[1% of CLKIN period + 100] | ps |
|  |  |   | All others                   | -                             | ±[1% of CLKIN period + 150] | ps |
| <b>Lock Time</b>                             |  |   |                              |                               |                             |    |
| LOCK_DLL <sup>(3)</sup>                      | When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase | $5 \text{ MHz} \leq F_{\text{CLKIN}} \leq 15 \text{ MHz}$ | All                          | -                             | 5                           | ms |
|  |  | $F_{\text{CLKIN}} > 15 \text{ MHz}$                       |                              | -                             | 600                         | µs |
| <b>Delay Lines</b>                           |  |   |                              |                               |                             |    |
| DCM_DELAY_STEP <sup>(5)</sup>                | Finest delay resolution, averaged over all steps   | All   | 15                           | 35                            | ps                          |    |

**Notes:**

- The numbers in this table are based on the operating conditions set forth in [Table 8](#) and [Table 37](#).
- Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
- For optimal jitter tolerance and faster lock time, use the CLKIN\_PERIOD attribute.
- Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, the data sheet specifies a maximum jitter of "±[1% of CLKIN period + 150]". Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250 ps, averaged over all steps.
- The typical delay step size is 23 ps.

## Digital Frequency Synthesizer

**Table 39: Recommended Operating Conditions for the DFS**

| Symbol  | Description   | Speed Grade                   |     | Units     |     |
|---|---|-------------------------------|-----|-----------|-----|
|   |   | -4                            |     |           |     |
|   |   | Min                           | Max |           |     |
| <b>Input Frequency Ranges<sup>(2)</sup></b>       |   |                               |     |           |     |
| $F_{CLKIN}$                                       | CLKIN_FREQ_FX   | Frequency for the CLKIN input | 0.2 | 333       | MHz |
| <b>Input Clock Jitter Tolerance<sup>(3)</sup></b> |   |                               |     |           |     |
| CLKIN_CYC_JITT_FX_LF                              | Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency | $F_{CLKFX} \leq 150$ MHz      | -   | $\pm 300$ | ps  |
| CLKIN_CYC_JITT_FX_HF                              |   | $F_{CLKFX} > 150$ MHz         | -   | $\pm 150$ | ps  |
| CLKIN_PER_JITT_FX                                 | Period jitter at the CLKIN input  |                               | -   | $\pm 1$   | ns  |

**Notes:**

- DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
- If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN\_FREQ\_DLL specifications in [Table 37](#).
- CLKIN input jitter beyond these limits may cause the DCM to lose lock.
- The DCM specifications are guaranteed when both adjacent DCMs are locked.

**Table 40: Switching Characteristics for the DFS**

| Symbol                                     | Description   | Device | Speed Grade  |                                  | Units                            |
|--|---|--------|--|----------------------------------|----------------------------------|
|  |   |        | -4   |                                  |                                  |
|  |   |        | Min  | Max                              |                                  |
| <b>Output Frequency Ranges</b>             |   |        |  |                                  |                                  |
| CLKOUT_FREQ_FX <sup>(2)</sup>              | Frequency for the CLKFX and CLKFX180 outputs  | All    | 5  | 311                              | MHz                              |
| <b>Output Clock Jitter<sup>(3,4)</sup></b> |   |        |  |                                  |                                  |
| CLKOUT_PER_JITT_FX                         | Period jitter at the CLKFX and CLKFX180 outputs.  | All    | <b>Typ</b>   |                                  | <b>Max</b>                       |
|  |   |        | Use the Spartan-3A FPGA Jitter Calculator:<br><a href="http://www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip">www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip</a> |                                  |                                  |
|  |   |        | CLKIN $\leq 20$ MHz  | $\pm[1\%$ of CLKFX period + 100] | $\pm[1\%$ of CLKFX period + 200] |
|  | CLKIN $> 20$ MHz  |        |  |                                  | ps                               |
| <b>Duty Cycle<sup>(5,6)</sup></b>          |   |        |  |                                  |                                  |
| CLKOUT_DUTY_CYCLE_FX                       | Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion   | All    | -  | $\pm[1\%$ of CLKFX period + 350] | ps                               |
| <b>Phase Alignment<sup>(6)</sup></b>       |   |        |  |                                  |                                  |
| CLKOUT_PHASE_FX                            | Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used  | All    | -  | $\pm 200$                        | ps                               |
| CLKOUT_PHASE_FX180                         | Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used   | All    | -  | $\pm[1\%$ of CLKFX period + 200] | ps                               |
| <b>Lock Time</b>                           |   |        |  |                                  |                                  |
| LOCK_FX <sup>(2,3)</sup>                   | The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time. | All    | $5 \text{ MHz} \leq F_{CLKIN} \leq 15 \text{ MHz}$   | 5                                | ms                               |
|  |   |        | $F_{CLKIN} > 15 \text{ MHz}$   | -                                | 450                              |

**Notes:**

- The numbers in this table are based on the operating conditions set forth in [Table 8](#) and [Table 39](#).
- DFS performance requires the additional logic automatically added by ISE 9.1i and later software revisions.
- For optimal jitter tolerance and faster lock time, use the CLKIN\_PERIOD attribute.
- Maximum output jitter is characterized within a reasonable noise environment (40 SSOs and 25% CLB switching) on an FPGA. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
- The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
- Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, the data sheet specifies a maximum CLKFX jitter of " $\pm[1\%$  of CLKFX period + 200]". Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is  $\pm[100 \text{ ps} + 200 \text{ ps}] = \pm 300 \text{ ps}$ .



## Phase Shifter

Table 41: Recommended Operating Conditions for the PS in Variable Phase Mode

| Symbol                            | Description   | Speed Grade |     | Units |
|-----------------------------------|---|-------------|-----|-------|
|                                   |   | -4          |     |       |
|                                   |   | Min         | Max |       |
| <b>Operating Frequency Ranges</b> |   |             |     |       |
| PSCLK_FREQ ( $F_{PSCLK}$ )        | Frequency for the PSCLK input                         | 1           | 167 | MHz   |
| <b>Input Pulse Requirements</b>   |   |             |     |       |
| PSCLK_PULSE                       | PSCLK pulse width as a percentage of the PSCLK period | 40%         | 60% | -     |

Table 42: Switching Characteristics for the PS in Variable Phase Mode

| Symbol                      | Description  | Phase Shift Amount  | Units  |
|-----------------------------|--|---|--|
| <b>Phase Shifting Range</b> |  |   |  |
| MAX_STEPS <sup>(2)</sup>    | Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the clock effective clock period. | CLKIN < 60 MHz  | $\pm[\text{INTEGER}(10 \cdot (T_{CLKIN} - 3 \text{ ns}))]$ |
|                             |  | CLKIN $\geq$ 60 MHz   | $\pm[\text{INTEGER}(15 \cdot (T_{CLKIN} - 3 \text{ ns}))]$ |
| FINE_SHIFT_RANGE_MIN        | Minimum guaranteed delay for variable phase shifting   | $\pm[\text{MAX\_STEPS} \cdot \text{DCM\_DELAY\_STEP\_MIN}]$ | ns   |
| FINE_SHIFT_RANGE_MAX        | Maximum guaranteed delay for variable phase shifting   | $\pm[\text{MAX\_STEPS} \cdot \text{DCM\_DELAY\_STEP\_MAX}]$ | ns   |

**Notes:**

- The numbers in this table are based on the operating conditions set forth in [Table 8](#) and [Table 41](#).
- The maximum variable phase shift range, MAX\_STEPS, is only valid when the DCM is has no initial fixed phase shifting, that is, the PHASE\_SHIFT attribute is set to 0.
- The DCM\_DELAY\_STEP values are provided at the bottom of [Table 38](#).

## Miscellaneous DCM Timing

Table 43: Miscellaneous DCM Timing

| Symbol         | Description                           | Min | Max | Units        |
|----------------|---------------------------------------|-----|-----|--------------|
| DCM_RST_PW_MIN | Minimum duration of a RST pulse width | 3   | -   | CLKIN cycles |

## DNA Port Timing

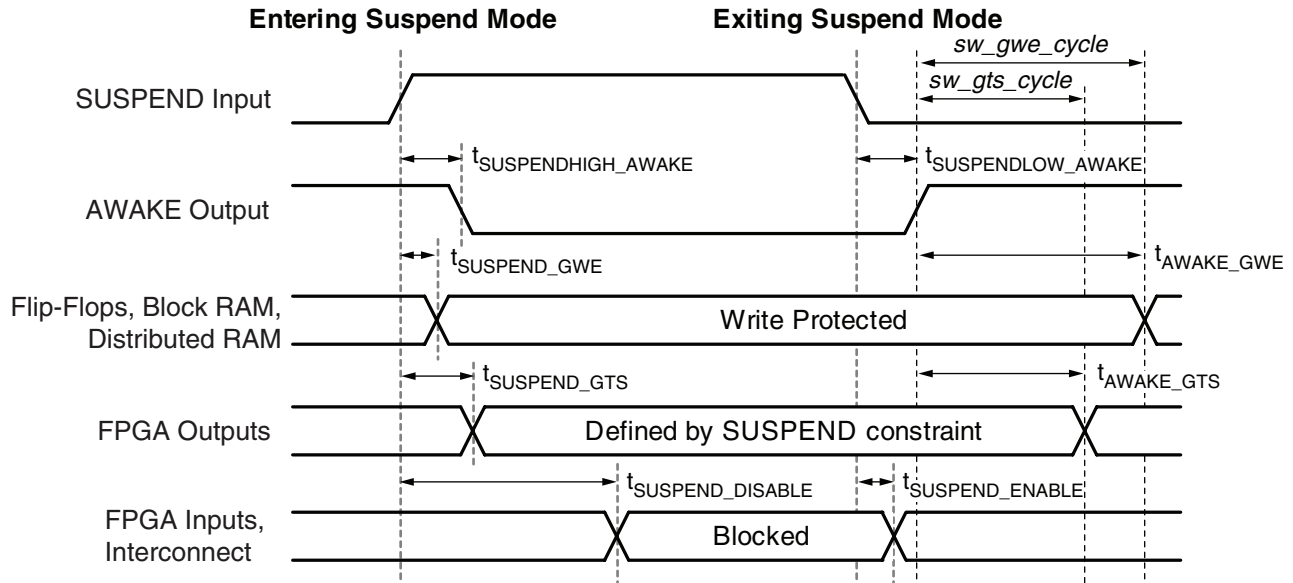
Table 44: DNA\_PORT Interface Timing

| Symbol        | Description  | Min | Max    | Units |
|---------------|--|-----|--------|-------|
| $T_{DNASSU}$  | Setup time on SHIFT before the rising edge of CLK      | 1.0 | –      | ns    |
| $T_{DNASH}$   | Hold time on SHIFT after the rising edge of CLK        | 0.5 | –      | ns    |
| $T_{DNADSU}$  | Setup time on DIN before the rising edge of CLK        | 1.0 | –      | ns    |
| $T_{DNADH}$   | Hold time on DIN after the rising edge of CLK          | 0.5 | –      | ns    |
| $T_{DNARSU}$  | Setup time on READ before the rising edge of CLK       | 5.0 | 10,000 | ns    |
| $T_{DNARH}$   | Hold time on READ after the rising edge of CLK         | 0.0 | –      | ns    |
| $T_{DNADCKO}$ | Clock-to-output delay on DOUT after rising edge of CLK | 0.5 | 1.5    | ns    |
| $T_{DNACLKF}$ | CLK frequency  | 0.0 | 100    | MHz   |
| $T_{DNACLKL}$ | CLK High time  | 1.0 | •      | ns    |
| $T_{DNACLKH}$ | CLK Low time   | 1.0 | •      | ns    |

### Notes:

1. The minimum READ pulse width is 5 ns, and the maximum READ pulse width is 10  $\mu$ s.

## Suspend Mode Timing



DS705\_09\_061908

Figure 9: Suspend Mode Timing

Table 45: Suspend Mode Timing Parameters

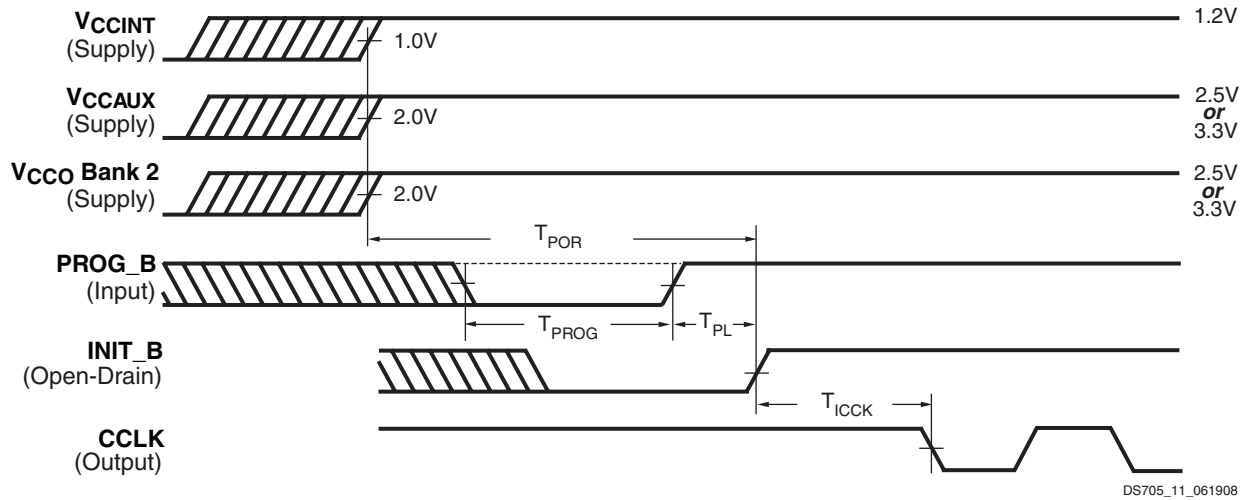
| Symbol                       | Description  | Min  | Typ        | Max  | Units |
|------------------------------|--|------|------------|------|-------|
| <b>Entering Suspend Mode</b> |  |      |            |      |       |
| $T_{SUSPENDHIGH\_AWAKE}$     | Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter ( <i>suspend_filter:No</i> )   | –    | 7          | –    | ns    |
| $T_{SUSPENDFILTER}$          | Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled ( <i>suspend_filter:Yes</i> )  | +160 | +300       | +600 | ns    |
| $T_{SUSPEND\_GWE}$           | Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior  | –    | 10         | –    | ns    |
| $T_{SUSPEND\_GTS}$           | Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements  | –    | <5         | –    | ns    |
| $T_{SUSPEND\_DISABLE}$       | Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled  | –    | 340        | –    | ns    |
| <b>Exiting Suspend Mode</b>  |  |      |            |      |       |
| $T_{SUSPENDLOW\_AWAKE}$      | Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM lock time.   | –    | 4 to 108   | –    | μs    |
| $T_{SUSPEND\_ENABLE}$        | Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled   | –    | 3.7 to 109 | –    | μs    |
| $T_{AWAKE\_GWE1}$            | Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using <i>sw_clk:InternalClock</i> and <i>sw_gwe_cycle:1</i> .       | –    | 67         | –    | ns    |
| $T_{AWAKE\_GWE512}$          | Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using <i>sw_clk:InternalClock</i> and <i>sw_gwe_cycle:512</i> .     | –    | 14         | –    | μs    |
| $T_{AWAKE\_GTS1}$            | Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using <i>sw_clk:InternalClock</i> and <i>sw_gts_cycle:1</i> .   | –    | 57         | –    | ns    |
| $T_{AWAKE\_GTS512}$          | Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using <i>sw_clk:InternalClock</i> and <i>sw_gts_cycle:512</i> . | –    | 14         | –    | μs    |

**Notes:**

1. These parameters based on characterization.
2. For information on using the Suspend feature, see [XAPP480](#), *Using Suspend Mode in Spartan-3 Generation FPGAs*.

## Configuration and JTAG Timing

### General Configuration Power-On/Reconfigure Timing



**Notes:**

1. The  $V_{CCINT}$ ,  $V_{CCAUX}$ , and  $V_{CCO}$  supplies can be applied in any order.
2. The Low-going pulse on  $PROG\_B$  is optional after power-on.
3. The rising edge of  $INIT\_B$  samples the voltage levels applied to the mode pins (M0 - M2).

Figure 10: Waveforms for Power-On and the Beginning of Configuration

Table 46: Power-On Timing and the Beginning of Configuration

| Symbol           | Description  | Device | Min | Max | Units   |
|------------------|--|--------|-----|-----|---------|
| $T_{POR}^{(2)}$  | The time from the application of $V_{CCINT}$ , $V_{CCAUX}$ , and $V_{CCO}$ Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the $INIT\_B$ pin | All    | -   | 18  | ms      |
| $T_{PROG}$       | The width of the low-going pulse on the $PROG\_B$ pin  | All    | 0.5 | -   | $\mu$ s |
| $T_{PL}^{(2)}$   | The time from the rising edge of the $PROG\_B$ pin to the rising transition on the $INIT\_B$ pin   | All    | -   | 2   | ms      |
| $T_{INIT}$       | Minimum Low pulse width on $INIT\_B$ output  | All    | 300 | -   | ns      |
| $T_{ICCK}^{(3)}$ | The time from the rising edge of the $INIT\_B$ pin to the generation of the configuration clock signal at the $CCLK$ output pin  | All    | 0.5 | 4   | $\mu$ s |

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 8. This means power must be applied to all  $V_{CCINT}$ ,  $V_{CCO}$ , and  $V_{CCAUX}$  lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the SPI and BPI modes.
4. For details on configuration, see [UG332, Spartan-3 Generation Configuration User Guide](#).

## Configuration Clock (CCLK) Characteristics

Table 47: CCLK Output Period by *ConfigRate* Option Setting

| Symbol        | Description                                    | <i>ConfigRate</i> Setting | Temperature Range   | Minimum | Maximum | Units |
|---------------|--|---------------------------|---------------------|---------|---------|-------|
| $T_{CCLK1}$   | CCLK clock period by <i>ConfigRate</i> setting | 1<br>(power-on value)     | I-Grade/<br>Q-Grade | 1,180   | 2,500   | ns    |
| $T_{CCLK3}$   |  | 3                         | I-Grade/<br>Q-Grade | 390     | 833     | ns    |
| $T_{CCLK6}$   |  | 6                         | I-Grade/<br>Q-Grade | 195     | 417     | ns    |
| $T_{CCLK7}$   |  | 7                         | I-Grade/<br>Q-Grade | 168     | 357     | ns    |
| $T_{CCLK8}$   |  | 8                         | I-Grade/<br>Q-Grade | 147     | 313     | ns    |
| $T_{CCLK10}$  |  | 10                        | I-Grade/<br>Q-Grade | 116     | 250     | ns    |
| $T_{CCLK12}$  |  | 12                        | I-Grade/<br>Q-Grade | 97      | 208     | ns    |
| $T_{CCLK13}$  |  | 13                        | I-Grade/<br>Q-Grade | 88      | 192     | ns    |
| $T_{CCLK17}$  |  | 17                        | I-Grade/<br>Q-Grade | 68      | 147     | ns    |
| $T_{CCLK22}$  |  | 22                        | I-Grade/<br>Q-Grade | 51      | 114     | ns    |
| $T_{CCLK25}$  |  | 25                        | I-Grade/<br>Q-Grade | 45      | 100     | ns    |
| $T_{CCLK27}$  |  | 27                        | I-Grade/<br>Q-Grade | 42      | 93      | ns    |
| $T_{CCLK33}$  |  | 33                        | I-Grade/<br>Q-Grade | 34      | 76      | ns    |
| $T_{CCLK44}$  |  | 44                        | I-Grade/<br>Q-Grade | 25      | 57      | ns    |
| $T_{CCLK50}$  |  | 50                        | I-Grade/<br>Q-Grade | 21      | 50      | ns    |
| $T_{CCLK100}$ | 100  | I-Grade/<br>Q-Grade       | 10.6                | 25      | ns      |       |

### Notes:

1. Set the *ConfigRate* option value when generating a configuration bitstream.

Table 48: CCLK Output Frequency by ConfigRate Option Setting

| Symbol               | Description  | ConfigRate Setting    | Temperature Range   | Minimum | Maximum | Units |
|----------------------|--|-----------------------|---------------------|---------|---------|-------|
| F <sub>CCLK1</sub>   | Equivalent CCLK clock frequency by <b>ConfigRate</b> setting | 1<br>(power-on value) | I-Grade/<br>Q-Grade | 0.400   | 0.847   | MHz   |
| F <sub>CCLK3</sub>   |  | 3                     | I-Grade/<br>Q-Grade | 1.20    | 2.57    | MHz   |
| F <sub>CCLK6</sub>   |  | 6                     | I-Grade/<br>Q-Grade | 2.40    | 5.13    | MHz   |
| F <sub>CCLK7</sub>   |  | 7                     | I-Grade/<br>Q-Grade | 2.80    | 5.96    | MHz   |
| F <sub>CCLK8</sub>   |  | 8                     | I-Grade/<br>Q-Grade | 3.20    | 6.81    | MHz   |
| F <sub>CCLK10</sub>  |  | 10                    | I-Grade/<br>Q-Grade | 4.00    | 8.63    | MHz   |
| F <sub>CCLK12</sub>  |  | 12                    | I-Grade/<br>Q-Grade | 4.80    | 10.31   | MHz   |
| F <sub>CCLK13</sub>  |  | 13                    | I-Grade/<br>Q-Grade | 5.20    | 11.37   | MHz   |
| F <sub>CCLK17</sub>  |  | 17                    | I-Grade/<br>Q-Grade | 6.80    | 14.61   | MHz   |
| F <sub>CCLK22</sub>  |  | 22                    | I-Grade/<br>Q-Grade | 8.80    | 19.61   | MHz   |
| F <sub>CCLK25</sub>  |  | 25                    | I-Grade/<br>Q-Grade | 10.00   | 22.23   | MHz   |
| F <sub>CCLK27</sub>  |  | 27                    | I-Grade/<br>Q-Grade | 10.80   | 23.81   | MHz   |
| F <sub>CCLK33</sub>  |  | 33                    | I-Grade/<br>Q-Grade | 13.20   | 29.23   | MHz   |
| F <sub>CCLK44</sub>  |  | 44                    | I-Grade/<br>Q-Grade | 17.60   | 40.00   | MHz   |
| F <sub>CCLK50</sub>  |  | 50                    | I-Grade/<br>Q-Grade | 20.00   | 47.66   | MHz   |
| F <sub>CCLK100</sub> | 100  | I-Grade/<br>Q-Grade   | 40.00               | 94.34   | MHz     |       |

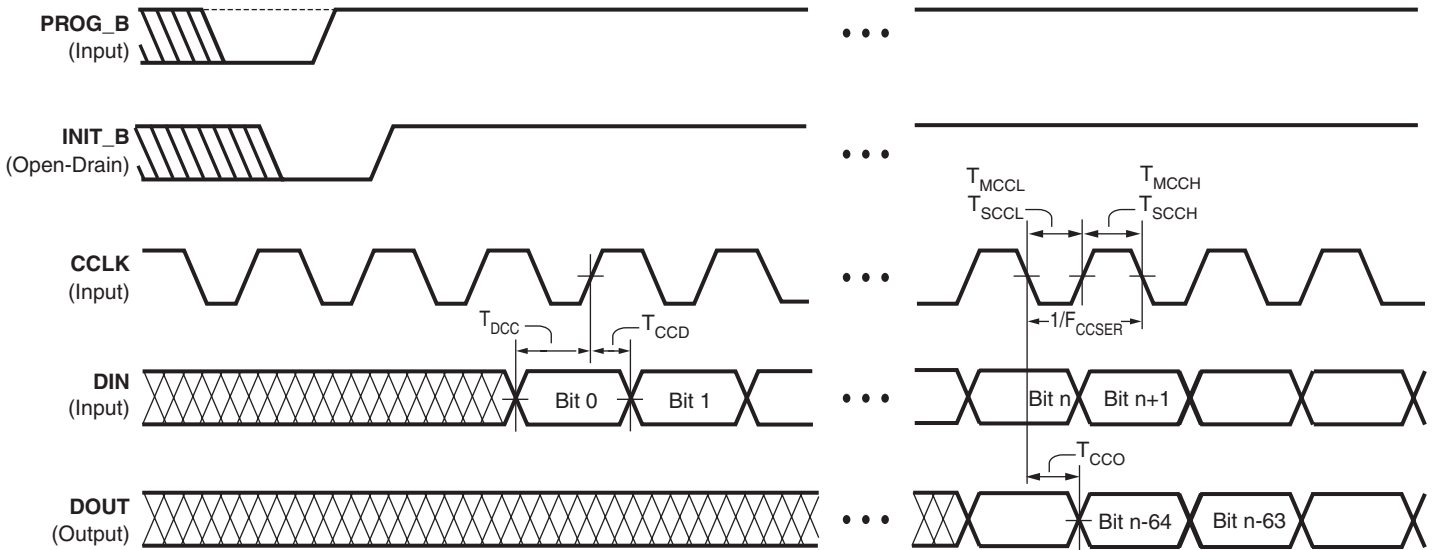
Table 49: CCLK Output Minimum Low and High Time

| Symbol                                   | Description                          |                     | ConfigRate Setting |     |      |      |      |      |      |      |      |      |      |      |      |      |      |     | Units |
|--|--------------------------------------|---------------------|--------------------|-----|------|------|------|------|------|------|------|------|------|------|------|------|------|-----|-------|
|  |                                      |                     | 1                  | 3   | 6    | 7    | 8    | 10   | 12   | 13   | 17   | 22   | 25   | 27   | 33   | 44   | 50   | 100 |       |
| T <sub>MCCL</sub> ,<br>T <sub>MCCH</sub> | CCLK<br>Minimum Low<br>and High Time | I-Grade/<br>Q-Grade | 560                | 185 | 92.6 | 79.8 | 69.8 | 55.0 | 46.0 | 41.8 | 32.3 | 24.2 | 21.4 | 20.0 | 16.2 | 11.9 | 10.0 | 5.0 | ns    |

Table 50: CCLK Input Low and High Time

| Symbol                                   | Description            | Min | Max | Units |
|--|------------------------|-----|-----|-------|
| T <sub>SCCL</sub> ,<br>T <sub>SCCH</sub> | CCLK Low and High time | 5   | ∞   | ns    |

Slave Serial Mode Timing



DS705\_12\_062308

Figure 11: Waveforms for Slave Serial Configuration

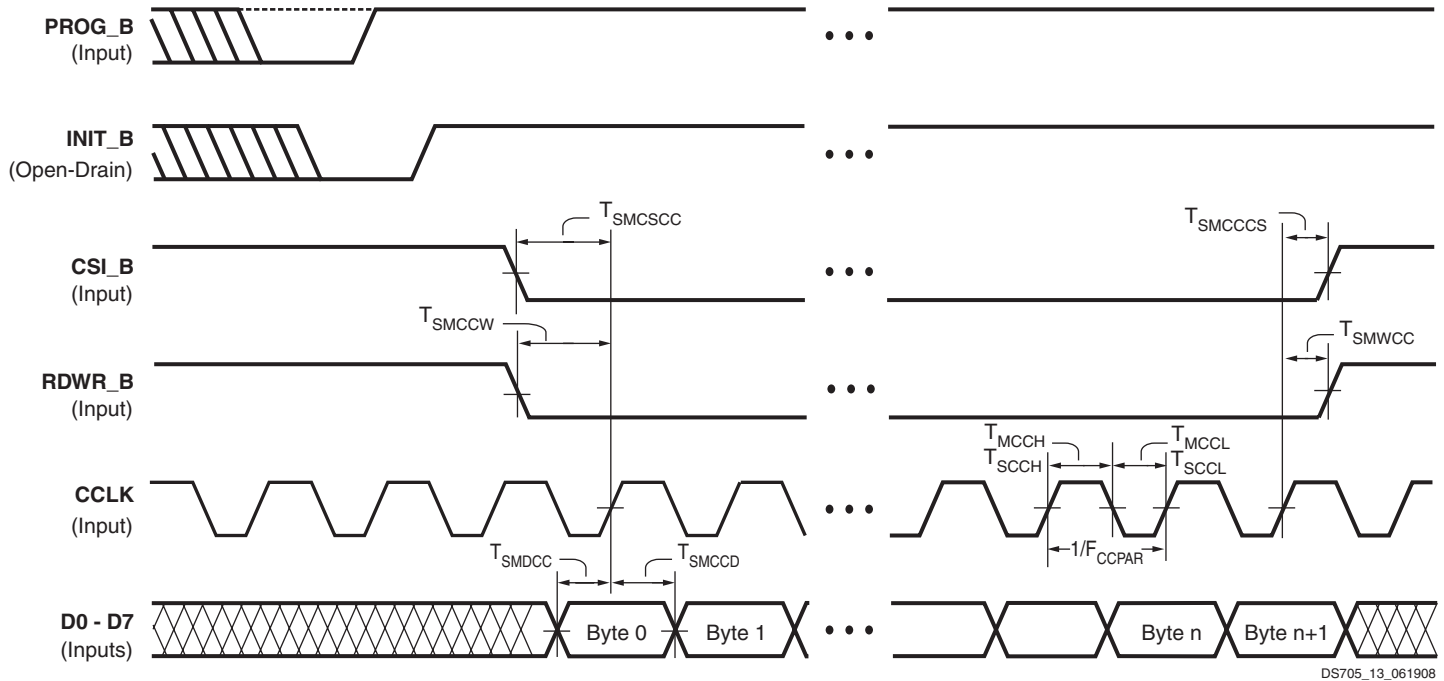
Table 51: Timing for the Slave Serial Configuration Modes

| Symbol                       | Description  | Min                        | Max | Units |     |
|------------------------------|--|----------------------------|-----|-------|-----|
| <b>Clock-to-Output Times</b> |  |                            |     |       |     |
| $T_{CCO}$                    | The time from the falling transition on the CCLK pin to data appearing at the DOUT pin                 | 1.5                        | 10  | ns    |     |
| <b>Setup Times</b>           |  |                            |     |       |     |
| $T_{DCC}$                    | The time from the setup of data at the DIN pin to the rising transition at the CCLK pin                | 7                          | -   | ns    |     |
| <b>Hold Times</b>            |  |                            |     |       |     |
| $T_{CCD}$                    | The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin | 1.0                        | -   | ns    |     |
| <b>Clock Timing</b>          |  |                            |     |       |     |
| $T_{CCH}$                    | High pulse width at the CCLK input pin   | See Table 50               |     |       |     |
| $T_{CCL}$                    | Low pulse width at the CCLK input pin  | See Table 50               |     |       |     |
| $F_{CCSER}$                  | Frequency of the clock signal at the CCLK input pin  | No bitstream compression   | 0   | 100   | MHz |
|                              |  | With bitstream compression | 0   | 100   | MHz |

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Slave Parallel Mode Timing



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Notes:

1. It is possible to abort configuration by pulling CSI\_B Low in a given CCLK cycle, then switching RDWR\_B Low or High in any subsequent cycle for which CSI\_B remains Low. The RDWR\_B pin asynchronously controls the driver impedance of the D0 - D7 bus. When RDWR\_B switches High, be careful to avoid contention on the D0 - D7 bus.
2. To pause configuration, pause CCLK instead of deasserting CSI\_B. See the section in Chapter 7 called “Non-Continuous SelectMAP Data Loading” in [UG332](#) for more details.

Figure 12: Waveforms for Slave Parallel Configuration

Table 52: Timing for the Slave Parallel Configuration Mode

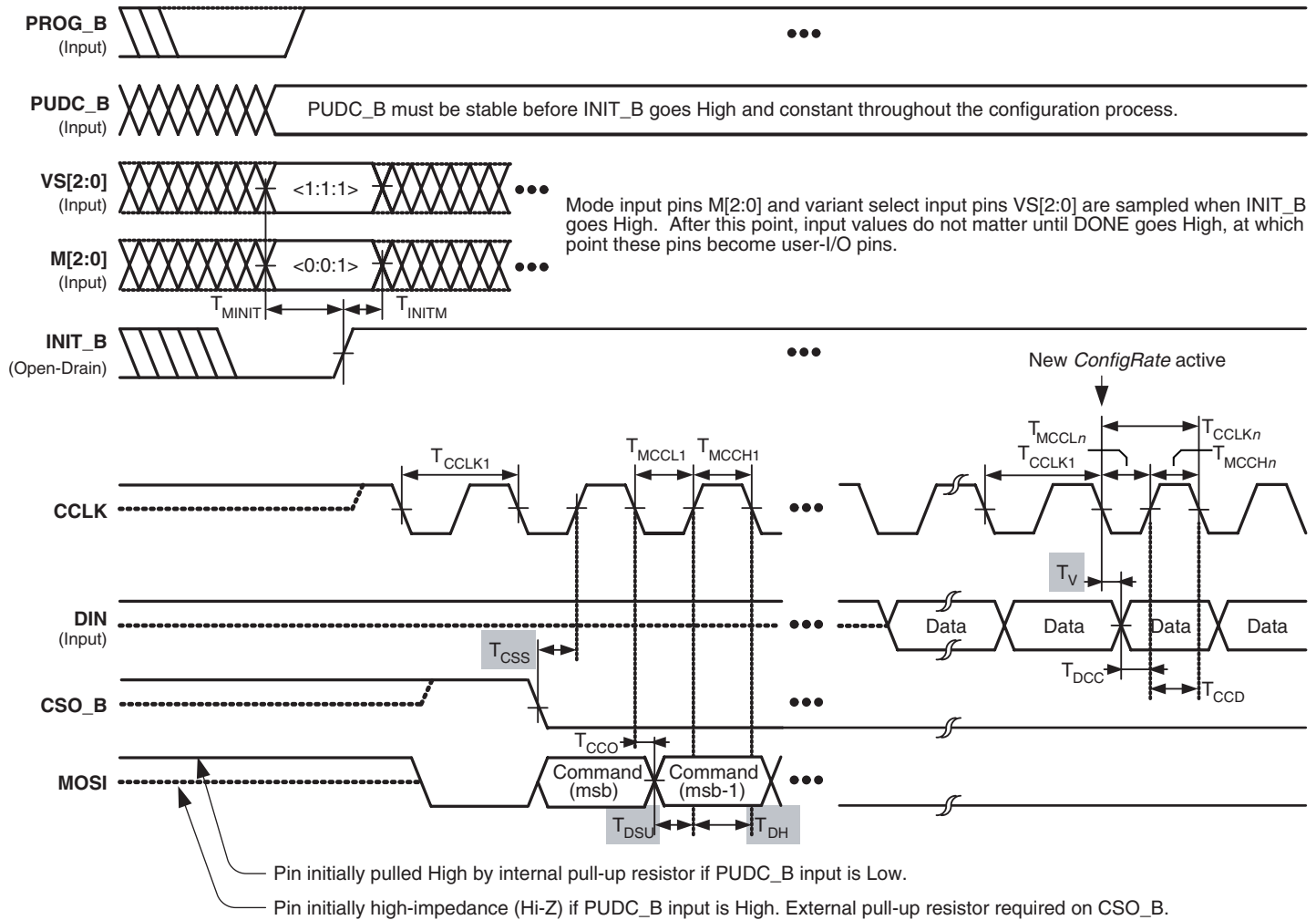
| Symbol              | Description  | Min                        | Max | Units |     |
|---------------------|--|----------------------------|-----|-------|-----|
| <b>Setup Times</b>  |  |                            |     |       |     |
| $T_{SMDCD}^{(2)}$   | The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin                         | 7                          | -   | ns    |     |
| $T_{SMCSCC}$        | Setup time on the CSI_B pin before the rising transition at the CCLK pin   | 7                          | -   | ns    |     |
| $T_{SMCCW}$         | Setup time on the RDWR_B pin before the rising transition at the CCLK pin  | 17                         | -   | ns    |     |
| <b>Hold Times</b>   |  |                            |     |       |     |
| $T_{SMCCD}$         | The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins          | 1                          | -   | ns    |     |
| $T_{SMCCCS}$        | The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin  | 0                          | -   | ns    |     |
| $T_{SMWCC}$         | The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin | 0                          | -   | ns    |     |
| <b>Clock Timing</b> |  |                            |     |       |     |
| $T_{CCH}$           | The High pulse width at the CCLK input pin   | 5                          | -   | ns    |     |
| $T_{CCL}$           | The Low pulse width at the CCLK input pin  | 5                          | -   | ns    |     |
| $F_{CCPAR}$         | Frequency of the clock signal at the CCLK input pin  | No bitstream compression   | 0   | 80    | MHz |
|                     |  | With bitstream compression | 0   | 80    | MHz |

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 8](#).
2. Some Xilinx documents refer to Parallel modes as “SelectMAP” modes.



### Serial Peripheral Interface Configuration Timing



Shaded values indicate specifications on attached SPI Flash PROM.

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Figure 13: Waveforms for Serial Peripheral Interface Configuration

Table 53: Timing for Serial Peripheral Interface Configuration Mode

| Symbol      | Description   | Minimum | Maximum      | Units |
|-------------|---|---------|--------------|-------|
| $T_{CCLK1}$ | Initial CCLK clock period   |         | See Table 47 |       |
| $T_{CCLKn}$ | CCLK clock period after FPGA loads ConfigRate setting   |         | See Table 47 |       |
| $T_{MINIT}$ | Setup time on VS[2:0] variant-select pins and M[2:0] mode pins before the rising edge of INIT_B | 50      | -            | ns    |
| $T_{INITM}$ | Hold time on VS[2:0] variant-select pins and M[2:0] mode pins after the rising edge of INIT_B   | 0       | -            | ns    |
| $T_{CCO}$   | MOSI output valid delay after CCLK falling edge   |         | See Table 51 |       |
| $T_{DCC}$   | Setup time on DIN data input before CCLK rising edge  |         | See Table 51 |       |
| $T_{CCD}$   | Hold time on DIN data input after CCLK rising edge  | 0       | -            | ns    |

Table 54: Configuration Timing Requirements for Attached SPI Serial Flash

| Symbol         | Description  | Requirement                         | Units |
|----------------|--|-------------------------------------|-------|
| $T_{CCS}$      | SPI serial Flash PROM chip-select time   | $T_{CCS} \leq T_{MCCL1} - T_{CCO}$  | ns    |
| $T_{DSU}$      | SPI serial Flash PROM data input setup time  | $T_{DSU} \leq T_{MCCL1} - T_{CCO}$  | ns    |
| $T_{DH}$       | SPI serial Flash PROM data input hold time   | $T_{DH} \leq T_{MCCH1}$             | ns    |
| $T_V$          | SPI serial Flash PROM data clock-to-output time  | $T_V \leq T_{MCCLn} - T_{DCC}$      | ns    |
| $f_C$ or $f_R$ | Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used) | $f_C \geq \frac{1}{T_{CCLKn(min)}}$ | MHz   |

**Notes:**

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.

### Byte Peripheral Interface Configuration Timing

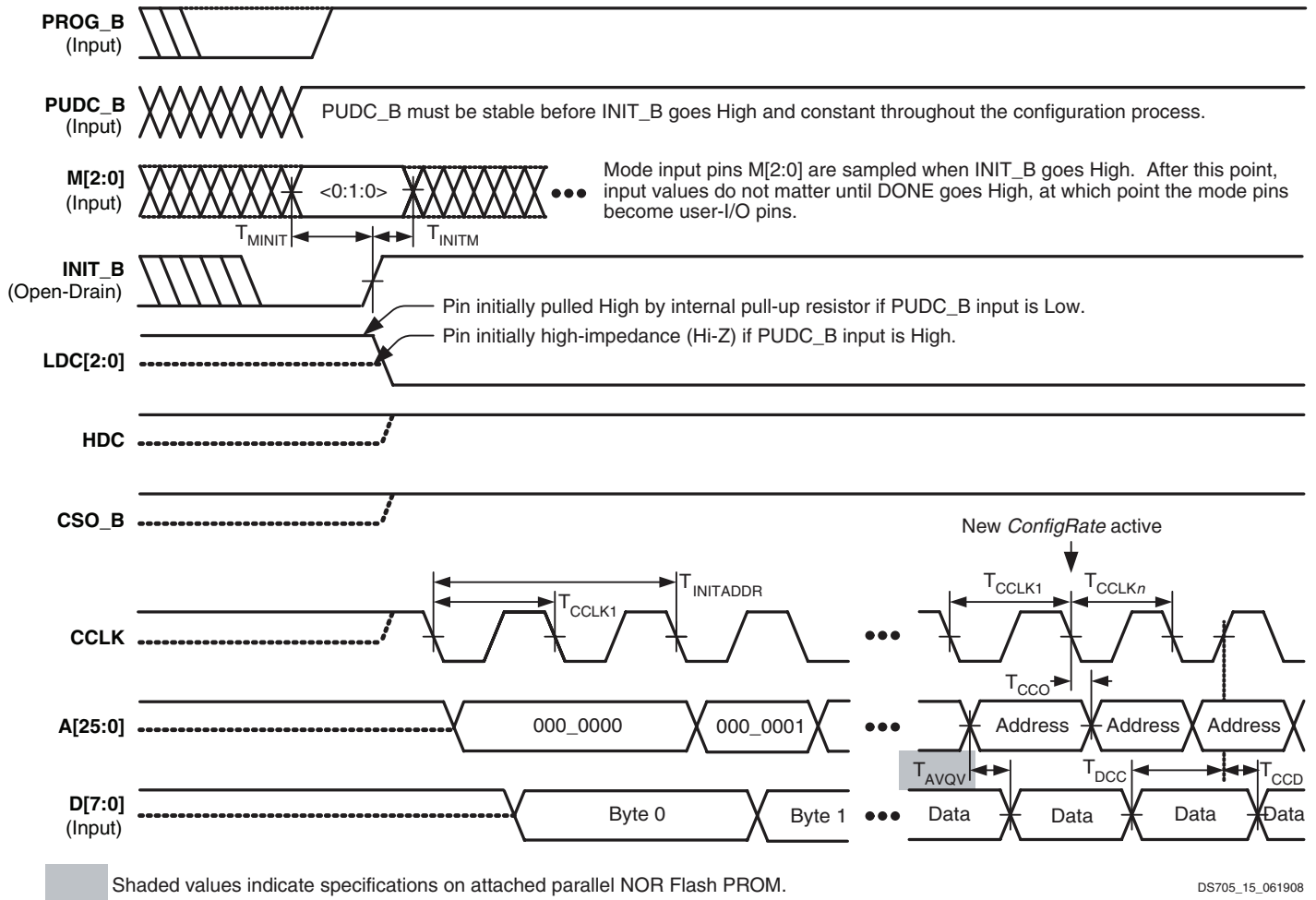


Figure 14: Waveforms for Byte-wide Peripheral Interface Configuration

Table 55: Timing for Byte-wide Peripheral Interface Configuration Mode

| Symbol         | Description  | Minimum                     | Maximum | Units              |
|----------------|--|-----------------------------|---------|--------------------|
| $T_{CCLK1}$    | Initial CCLK clock period  | See Table 47                |         |                    |
| $T_{CCLKn}$    | CCLK clock period after FPGA loads ConfigRate setting                                    | See Table 47                |         |                    |
| $T_{MINIT}$    | Setup time on M[2:0] mode pins before the rising edge of INIT_B                          | 50                          | -       | ns                 |
| $T_{INITM}$    | Hold time on M[2:0] mode pins after the rising edge of INIT_B                            | 0                           | -       | ns                 |
| $T_{INITADDR}$ | Minimum period of initial A[25:0] address cycle; LDC[2:0] and HDC are asserted and valid | 5                           | 5       | $T_{CCLK1}$ cycles |
| $T_{CCO}$      | Address A[25:0] outputs valid after CCLK falling edge                                    | See Table 51                |         |                    |
| $T_{DCC}$      | Setup time on D[7:0] data inputs before CCLK rising edge                                 | See $T_{SMDCC}$ in Table 52 |         |                    |
| $T_{CCD}$      | Hold time on D[7:0] data inputs after CCLK rising edge                                   | 0                           | -       | ns                 |

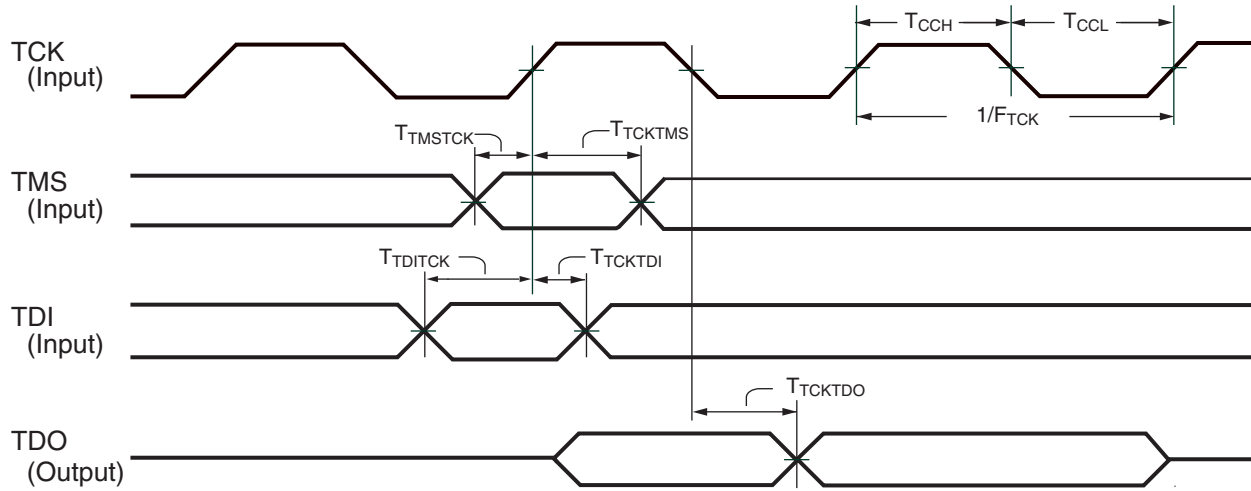
Table 56: Configuration Timing Requirements for Attached Parallel NOR Flash

| Symbol                                 | Description  | Requirement  | Units |
|--|--|--|-------|
| $T_{CE}$<br>( $t_{ELQV}$ )             | Parallel NOR Flash PROM chip-select time                         | $T_{CE} \leq T_{INITADDR}$                                   | ns    |
| $T_{OE}$<br>( $t_{GLQV}$ )             | Parallel NOR Flash PROM output-enable time                       | $T_{OE} \leq T_{INITADDR}$                                   | ns    |
| $T_{ACC}$<br>( $t_{AVQV}$ )            | Parallel NOR Flash PROM read access time                         | $T_{ACC} \leq 50\% T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$ | ns    |
| $T_{BYTE}$<br>( $t_{FLQV}, t_{FHQV}$ ) | For x8/x16 PROMs only: BYTE# to output valid time <sup>(3)</sup> | $T_{BYTE} \leq T_{INITADDR}$                                 | ns    |

**Notes:**

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's PUDC\_B pin is High or Low.

IEEE 1149.1/1553 JTAG Test Access Port Timing



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Figure 15: JTAG Waveforms

Table 57: Timing for the JTAG Test Access Port

| Symbol                       | Description  | Min  | Max  | Units |
|------------------------------|--|--|------|-------|
| <b>Clock-to-Output Times</b> |  |  |      |       |
| $T_{TCKTDO}$                 | The time from the falling transition on the TCK pin to data appearing at the TDO pin                           | 1.0  | 11.0 | ns    |
| <b>Setup Times</b>           |  |  |      |       |
| $T_{TDITCK}$                 | The time from the setup of data at the TDI pin to the rising transition at the TCK pin                         | All functions except those shown below                 |      | ns    |
|                              |  | Boundary-Scan commands (INTEST, EXTEST, SAMPLE)        |      |       |
| $T_{TMSTCK}$                 | The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin                | 7.0  | –    | ns    |
| <b>Hold Times</b>            |  |  |      |       |
| $T_{TCKTDI}$                 | The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin          | All functions except those shown below                 |      | ns    |
|                              |  | Configuration commands (CFG_IN, ISC_PROGRAM)           |      |       |
| $T_{TCKTMS}$                 | The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin | 0  | –    | ns    |
| <b>Clock Timing</b>          |  |  |      |       |
| $T_{CCH}$                    | The High pulse width at the TCK pin  | All functions except ISC_DNA command                   |      | ns    |
| $T_{CCL}$                    | The Low pulse width at the TCK pin   |  |      | ns    |
| $T_{CCHDNA}$                 | The High pulse width at the TCK pin  | During ISC_DNA command                                 |      | ns    |
| $T_{CCLDNA}$                 | The Low pulse width at the TCK pin   |  |      | ns    |
| $F_{TCK}$                    | Frequency of the TCK signal  | BYPASS or HIGHZ instructions                           |      | MHz   |
|                              |  | All operations except for BYPASS or HIGHZ instructions |      |       |

Notes:

- The numbers in this table are based on the operating conditions set forth in Table 8.
- For details on JTAG, see “JTAG Configuration Mode and Boundary-Scan” in Chapter 9 of UG332, Spartan-3 Generation Configuration User Guide.

## Revision History

The following table shows the revision history for this document:

| Date     | Version | Description of Revisions  |
|----------|---------|---|
| 07/10/08 | 1.0     | Initial Xilinx release.   |
| 01/20/09 | 1.1     | <ul style="list-style-type: none"> <li>Updated "Features" and "Key Feature Differences from Commercial XC Devices."</li> <li>Removed MultiBoot description from "Configuration."</li> <li>Updated Note 2 in Figure 10.</li> <li>Updated T<sub>ACC</sub> requirement in Table 56.</li> </ul> |

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