Data Sheet | April 25, 2008 | FN6494.0

VR11.1 Compatible Synchronous Rectified Buck MOSFET Drivers

The ISL6620, ISL6620A is a high frequency MOSFET driver designed to drive upper and lower power N-Channel MOSFETs in a synchronous rectified buck converter topology. The advanced PWM protocol of ISL6620, ISL6620A is specifically designed to work with Intersil VR11.1 controllers and combined with N-Channel MOSFETs, form a complete core-voltage regulator solution for advanced microprocessors. When ISL6620, ISL6620A detects a $\overline{PSI}$ protocol sent by an Intersil VR11.1 controller, it activates Diode Emulation (DE) operation; otherwise, it operates in normal Continuous Conduction Mode (CCM) PWM mode.

The IC is biased by a single low voltage supply (5V), minimizing driving losses in high MOSFET gate capacitance and high switching frequency applications. Each driver is capable of driving a 3nF load with less than 10ns rise/fall time. Bootstrapping of the upper gate driver is implemented via an internal low forward drop diode, reducing implementation cost, complexity, and allowing the use of higher performance, cost effective N-Channel MOSFETs.

To further enhance light load efficiency, ISL6620, ISL6620A enables diode emulation operation during $\overline{PSI}$ mode. This allows Discontinuous Conduction Mode (DCM) by detecting when the inductor current reaches zero and subsequently turning off the low side MOSFET to prevent it from sinking current.

An advanced adaptive shoot-through protection is integrated to prevent both the upper and lower MOSFETs from conducting simultaneously and to minimize dead time. The ISL6620, ISL6620A has a 20kΩ integrated high-side gate-to-source resistor to prevent self turn-on due to high input bus dV/dt.

Features

- Dual MOSFET Drives for Synchronous Rectified Bridge
- Advanced Adaptive Zero Shoot-Through Protection
- 36V Internal Bootstrap Schottky Diode
- Advanced PWM Protocol (Patent Pending) to Support $\overline{PSI}$ Mode, Diode Emulation, Three-State Operation
- Diode Emulation For Enhanced Light Load Efficiency
- Bootstrap Capacitor Overcharging Prevention
- Supports High Switching Frequency
  - 4A Sinking Current Capability
  - Fast Rise/Fall Times and Low Propagation Delays
- VCC Undervoltage Protection
- Enable Input and Power-On Reset
- Expandable Bottom Copper Pad for Enhanced Heat Sinking
- DFN Package:
  - Compliant to JEDEC PUB95 MO-220 DFN - Dual Flat No Leads - Package Outline
  - Near Chip Scale Package Footprint, which Improves PCB Efficiency and has a Thinner Profile
- Pb-Free (RoHS Compliant)

Applications

- High Light Load Efficiency Voltage Regulators
- Core Regulators for Advanced Microprocessors
- High Current DC/DC Converters
- High Frequency and High Efficiency VRM and VRD

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB417 “Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators” for Power Train Design, Layout Guidelines, and Feedback Compensation Design

Ordering Information

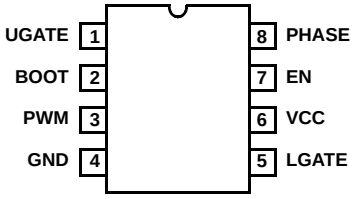
PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6620CBZ*	6620 CBZ	0 to +70	8 Ld SOIC	M8.15
ISL6620CRZ*	620Z	0 to +70	10 Ld 3x3 DFN	L10.3x3
ISL6620IBZ*	6620 IBZ	-40 to +85	8 Ld SOIC	M8.15
ISL6620IRZ*	620I	-40 to +85	10 Ld 3x3 DFN	L10.3x3
ISL6620ACBZ*	6620A CBZ	0 to +70	8 Ld SOIC	M8.15
ISL6620ACRZ*	620A	0 to +70	10 Ld 3x3 DFN	L10.3x3
ISL6620AIBZ*	6620A IBZ	-40 to +85	8 Ld SOIC	M8.15
ISL6620AIRZ*	20AI	-40 to +85	10 Ld 3x3 DFN	L10.3x3

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

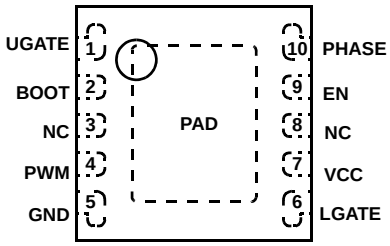
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

ISL6620, ISL6620A
(8 LD SOIC)
TOP VIEW

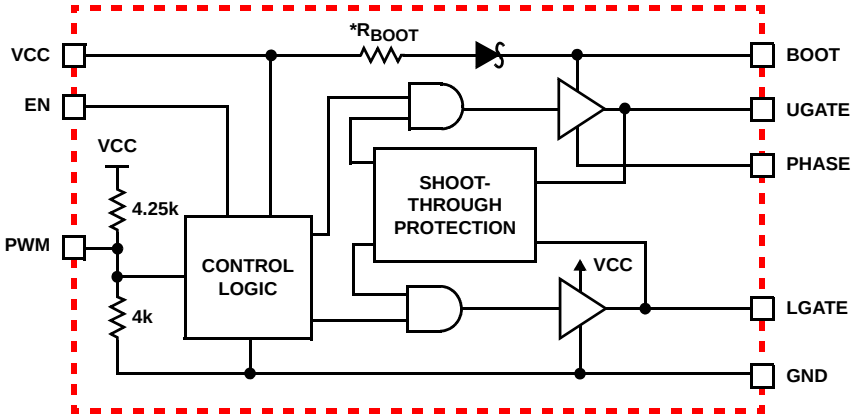


ISL6620, ISL6620A
(10 LD 3x3 DFN)
TOP VIEW



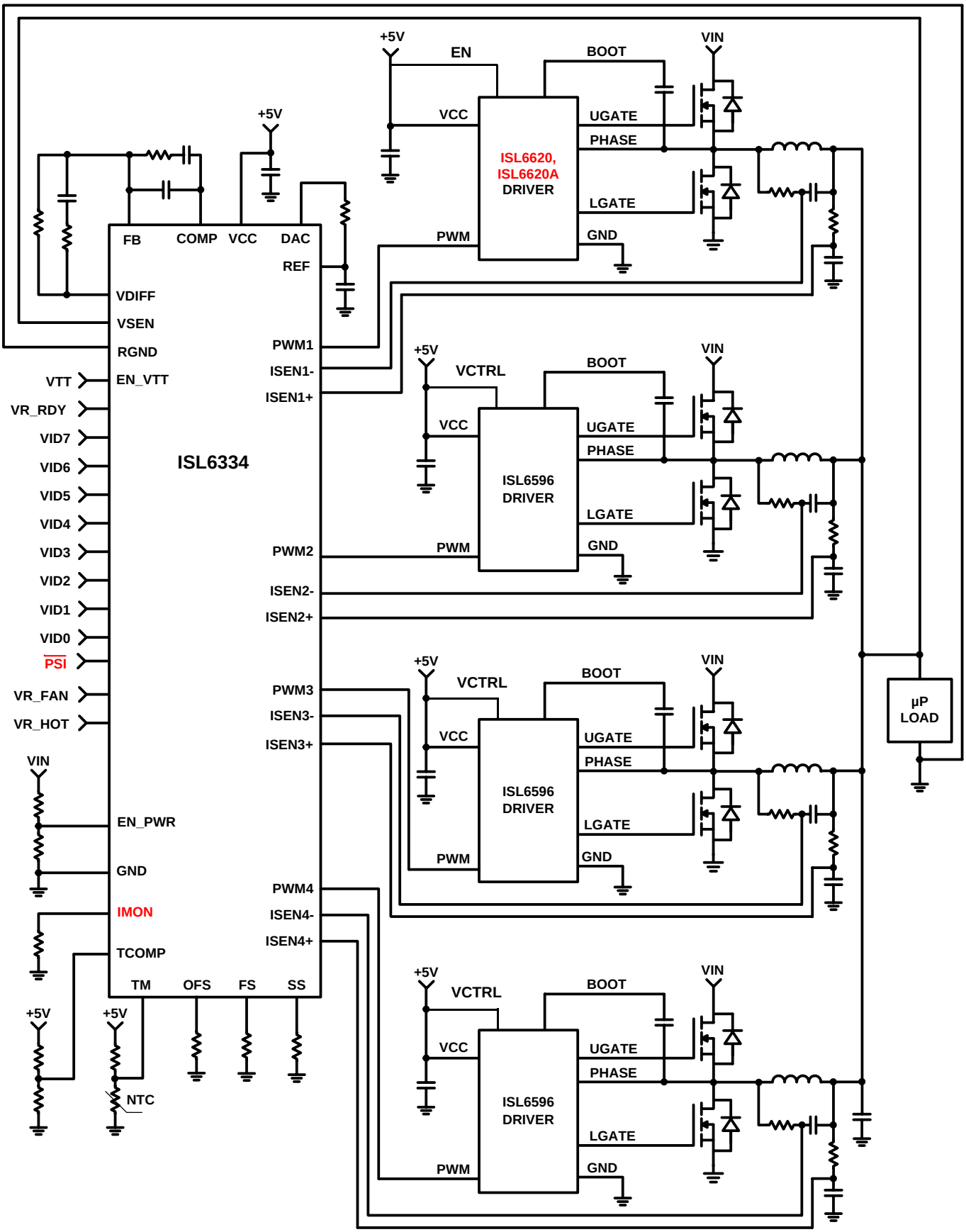
Block Diagrams

ISL6620, ISL6620A



***INTEGRATED 3Ω RESISTOR (R_{BOOT}) AVAILABLE ONLY IN ISL6620A**

Typical Application Circuit



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.3V to 7V
Input Voltage (V_{EN}, V_{PWM}) . . . . . -0.3V to VCC + 0.3V
BOOT Voltage ($V_{BOOT-GND}$) . . . -0.3V to 25V (DC) or 36V (<200ns)
BOOT To PHASE Voltage ($V_{BOOT-PHASE}$) . . . . . -0.3V to 7V (DC)
-0.3V to 9V (<10ns)
PHASE Voltage . . . . . GND - 0.3V to 15V (DC)
GND -8V (<20ns Pulse Width, 10µJ) to 30V (<100ns)
UGATE Voltage . . . . . V_{PHASE} - 0.3V (DC) to V_{BOOT}
V_{PHASE} - 5V (<20ns Pulse Width, 10µJ) to V_{BOOT}
LGATE Voltage . . . . . GND - 0.3V (DC) to VCC + 0.3V
GND - 2.5V (<20ns Pulse Width, 5µJ) to VCC + 0.3V
Ambient Temperature Range . . . . . -40°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	100	N/A
DFN Package (Notes 2, 3)	48	7

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range
ISL6620IBZ, ISL6620IRZ, ISL6620AIBZ, ISL6620AIRZ
. . . . . -40°C to +85°C
ISL6620CBZ, ISL6620CRZ, ISL6620ACBZ, ISL6620ACRZ
. . . . . 0°C to +70°C
Maximum Operating Junction Temperature . . . . . +125°C
Supply Voltage, VCC . . . . . 5V ±10%

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC Supply Current						
No Load Switching Supply Current	IVCC	f_PWM = 300kHz, V_VCC = 5V		1.27		mA
Standby Supply Current	IVCC	PWM 0V to 2.5V transition, EN = High		1.85		mA
		PWM 0V to 2.5V transition, EN = Low		1.15		mA
POWER-ON RESET AND ENABLE						
VCC Rising POR Threshold			3.2	3.8	4.4	V
VCC Falling POR Threshold			3.0	3.4	4.0	V
VCC POR Hysteresis			130	300	530	mV
EN High Threshold			1.40	1.65	1.90	V
EN Low Threshold			1.20	1.35	1.55	V
PWM INPUT (See TIMING DIAGRAM" on page 6)						
Input Current	IPWM	VPWM = 5V		500		µA
		VPWM = 0V		-430		µA
PWM Rising Threshold (Note 4)		VCC = 5V		3.4		V
PWM Falling Threshold (Note 4)		VCC = 5V		1.6		V
Three-State Lower Gate Falling Threshold		VCC = 5V		1.6		V
Three-State Lower Gate Rising Threshold		VCC = 5V		1.1		V
Three-State Upper Gate Rising Threshold		VCC = 5V		3.2		V
Three-state Upper Gate Falling Threshold		VCC = 5V		2.8		V
UGATE Rise Time (Note 4)	t_RU	VCC = 5V, 3nF load, 10% to 90%		8		ns

Electrical Specifications Recommended Operating Conditions; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LGATE Rise Time (Note 4)	t_RL	VCC = 5V, 3nF load, 10% to 90%		8		ns
UGATE Fall Time (Note 4)	t_FU	VCC = 5V, 3nF load, 10% to 90%		8		ns
LGATE Fall Time (Note 4)	t_FL	VCC = 5V, 3nF load, 10% to 90%		4		ns
UGATE Turn-On Propagation Delay (Note 4)	t_PDHU	VCC = 5V, 3nF load, adaptive		40		ns
LGATE Turn-On Propagation Delay (Note 4)	t_PDHL	VCC = 5V, 3nF load, adaptive		23		ns
UGATE Turn-Off Propagation Delay (Note 4)	t_PDLU	VCC = 5V, 3nF load		18		ns
LGATE Turn-Off Propagation Delay (Note 4)	t_PDLL	VCC = 5V, 3nF load		25		ns
Minimum Lgate on time at Diode emulation	t_LG_ON_DM	VCC = 5V	230	330	450	ns
OUTPUT (Note 4)						
Upper Drive Source Current	I_U_Source	VCC = 5V, 3nF load		2		A
Upper Drive Source Impedance	R_U_SOURCE	20mA source current		1		Ω
Upper Drive Sink Current	I_U_SINK	VCC = 5V, 3nF load		2		A
Upper Drive Sink Impedance	R_U_SINK	20mA sink current		1		Ω
Lower Drive Source Current	I_L_SOURCE	VCC = 5V, 3nF load		2		A
Lower Drive Source Impedance	R_L_SOURCE	20mA source current		1		Ω
Lower Drive Sink Current	I_L_SINK	VCC = 5V, 3nF load		4		A
Lower Drive Sink Impedance	R_L_SINK	20mA sink current		0.4		Ω

NOTE:

4. Limits should be considered typical and are not production tested.

Functional Pin Description

PACKAGE PIN #		PIN SYMBOL	FUNCTION
SOIC	DFN		
1	1	UGATE	Upper gate drive output. Connect to gate of high-side power N-Channel MOSFET.
2	2	BOOT	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See “Internal Bootstrap Device” on page 7 for guidance in choosing the capacitor value.
-	3, 8	NC	No connect.
3	4	PWM	The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation. See “Advanced PWM Protocol (Patent Pending)” on page 6 for further details. Connect this pin to the PWM output of the controller.
4	5	GND	Bias and reference ground. All signals are referenced to this node. It is also the power-ground return of the driver.
5	6	LGATE	Lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.
6	7	VCC	Connect this pin to 5V bias supply. This pin supplies power to the upper gate and lower gate drive. Place a high quality low ESR ceramic capacitor from this pin to GND.
7	9	EN	Enable input pin. Connect this pin high to enable driver and low to disable driver.
8	10	PHASE	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET. This pin provides a return path for the upper gate drive.
-	11	PAD	Connect this pad to the power ground plane (GND) via thermally enhanced connection.

Description

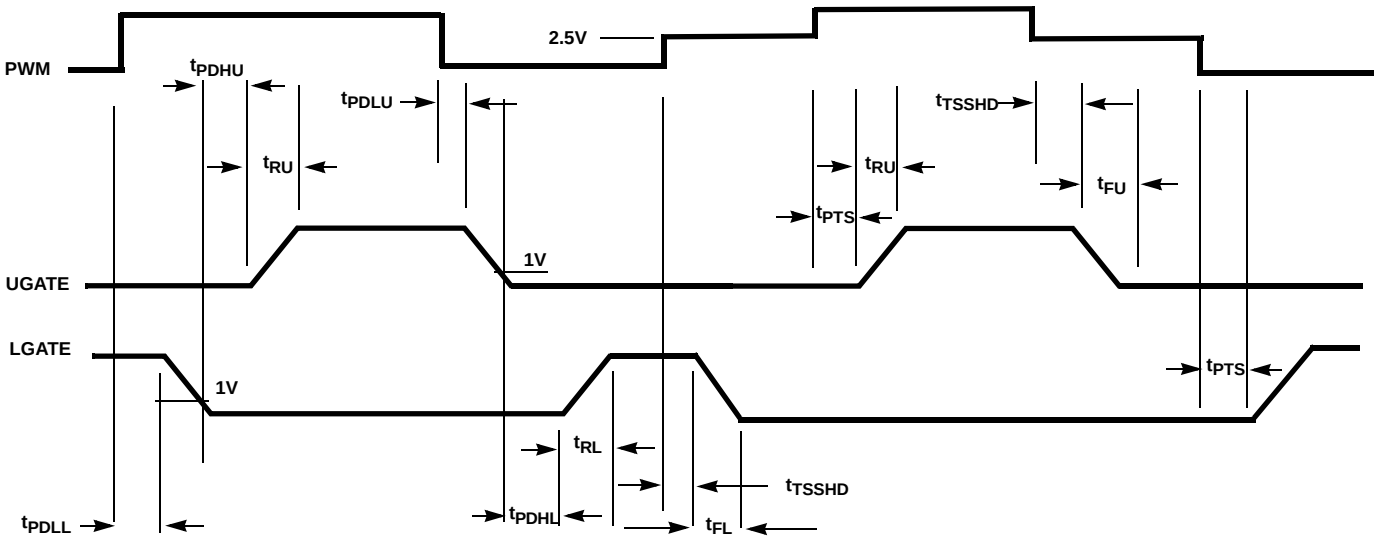


FIGURE 1. TIMING DIAGRAM

Operation and Adaptive Shoot-through Protection

Designed for high speed switching, the ISL6620, ISL6620A MOSFET driver controls both high-side and low-side N-Channel FETs from one externally provided PWM signal.

A rising transition on PWM initiates the turn-off of the lower MOSFET (see Timing Diagram). After a short propagation delay [t_{PDLL}], the lower gate begins to fall. Typical fall times [t_{FL}] are provided in the “Electrical Specifications” table on page 4. Adaptive shoot-through circuitry monitors the LGATE voltage and turns on the upper gate following a short delay time [t_{PDHU}] after the LGATE voltage drops below ~1V. The upper gate drive then begins to rise [t_{RU}] and the upper MOSFET turns on.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [t_{PDLU}] is encountered before the upper gate begins to fall [t_{FU}]. The adaptive shoot-through circuitry monitors the UGATE-PHASE voltage and turns on the lower MOSFET a short delay time [t_{PDHL}], after the upper MOSFET’s gate voltage drops below 1V. The lower gate then rises [t_{RL}], turning on the lower MOSFET. These methods prevent both the lower and upper MOSFETs from conducting simultaneously (shoot-through), while adapting the dead time to the gate charge characteristics of the MOSFETs being used.

This driver is optimized for voltage regulators with large step down ratio. The lower MOSFET is usually sized larger compared to the upper MOSFET because the lower MOSFET conducts for a longer time during a switching period. The lower gate driver is therefore sized much larger to meet this application requirement. The 0.4Ω ON-resistance and 4A sink current capability enable the lower gate driver to absorb the current injected into the lower gate through the drain-to-gate capacitor of the lower MOSFET and help prevent shoot-through caused by the self turn-on of the lower MOSFET due to high dV/dt of the switching node.

Advanced PWM Protocol (Patent Pending)

The advanced PWM protocol of ISL6620, ISL6620A is specifically designed to work with Intersil VR11.1 controllers. When ISL6620, ISL6620A detects a $\overline{\text{PSI}}$ protocol sent by an Intersil VR11.1 controller, it turns on diode emulation operation; otherwise, it remains in normal CCM PWM mode.

The controller communicates the tri-state signal to the driver by transitioning the PWM signal from 0V to 2V. The driver recognizes Diode Emulation mode and after 330ns (typically) evaluates the PHASE voltage to detect negative current, thus turning off LGATE. With no further PWM pulses from the controller, both UGATE and LGATE are low and the output can shut down. This feature helps prevent a negative transient on the output voltage when the output is shut down, eliminating the Schottky diode that is used in some systems for protecting the load from reversed output voltage events. Otherwise, the PWM rising and falling thresholds outlined in the “Electrical Specifications” on page 4 determine when the lower and upper gates are enabled.

Note that the LGATE will not turn off until the diode emulation minimum LGATE ON-time of 350ns is expired for a PWM low to tri-level (2.5V) transition.

Diode Emulation

Diode emulation allows for higher converter efficiency under light-load situations. With diode emulation active, the ISL6620, ISL6620A detects the zero current crossing of the output inductor and turns off LGATE. This prevents the low side MOSFET from sinking current and ensures that discontinuous conduction mode (DCM) is achieved. The LGATE has a minimum ON-time of 350ns in DCM mode.

Power-On Reset (POR) Function

During initial start-up, the VCC voltage rise is monitored. Once the rising VCC voltage exceeds 3.8V (typically), operation of the driver is enabled and the PWM input signal takes control of the gate drives. If VCC drops below the falling threshold of 3.5V (typically), operation of the driver is disabled.

Internal Bootstrap Device

ISL6620, ISL6620A features an internal bootstrap Schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the trailing-edge of the PHASE node. This reduces voltage stress on the BOOT to PHASE pins.

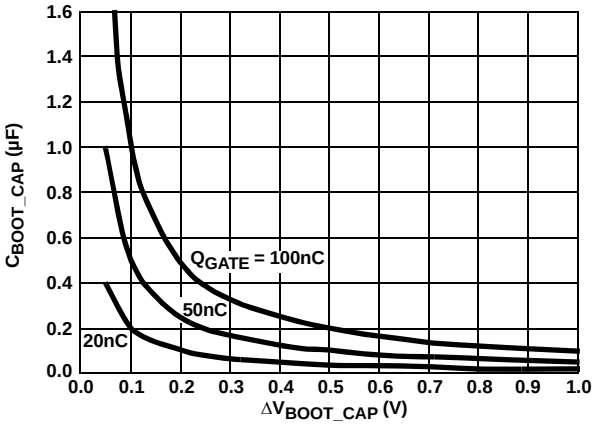


FIGURE 2. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

The bootstrap capacitor must have a maximum voltage rating well above the maximum voltage intended for VCC. Its capacitance value can be estimated using Equation 1:

$$C_{BOOT\_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT\_CAP}} \qquad \text{(EQ. 1)}$$

$$Q_{GATE} = \frac{Q_{G1} \bullet VCC}{V_{GS1}} \bullet N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive. Select results are exemplified in Figure 2.

Power Dissipation

Package power dissipation is mainly a function of the switching frequency (F_{SW}), the output drive impedance, the layout resistance, and the selected MOSFET's internal gate resistance and total gate charge (Q_G). Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level may push the IC beyond the maximum recommended operating junction temperature. The DFN package is more suitable for high frequency applications. See "Layout Considerations" on page 8 for thermal impedance improvement suggestions. The total gate drive power losses due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current can be estimated using Equations 2 and 3, respectively:

$$P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \bullet VCC \qquad \text{(EQ. 2)}$$

$$P_{Qg\_Q1} = \frac{Q_{G1} \bullet UVCC^2}{V_{GS1}} \bullet F_{SW} \bullet N_{Q1}$$

$$P_{Qg\_Q2} = \frac{Q_{G2} \bullet LVCC^2}{V_{GS2}} \bullet F_{SW} \bullet N_{Q2}$$

$$I_{DR} = \left(\frac{Q_{G1} \bullet UVCC \bullet N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \bullet LVCC \bullet N_{Q2}}{V_{GS2}}\right) \bullet F_{SW} + I_Q \qquad \text{(EQ. 3)}$$

where the gate charge (Q_{G1} and Q_{G2}) is defined at a particular gate to source voltage (V_{GS1} and V_{GS2}) in the corresponding MOSFET data sheet; I_Q is the driver's total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are number of upper and lower MOSFETs, respectively; UVCC and LVCC are the drive voltages for both upper and lower FETs, respectively. The I_Q*VCC product is the quiescent power of the driver without a load.

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + I_Q \bullet VCC \qquad \text{(EQ. 4)}$$

$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \bullet \frac{P_{Qg\_Q1}}{2}$$

$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \bullet \frac{P_{Qg\_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

The total gate drive power losses are dissipated among the resistive components along the transition path, as outlined in Equation 4. The drive resistance dissipates a portion of the total gate drive power losses, the rest will be dissipated by the external gate resistors (R_{G1} and R_{G2}) and the internal gate resistors (R_{GI1} and R_{GI2}) of MOSFETs. Figures 3 and 4 show the typical upper and lower gate drives turn-on current paths.

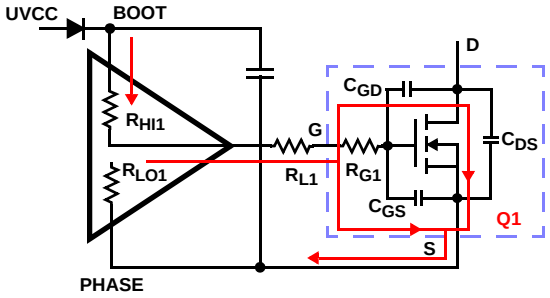


FIGURE 3. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

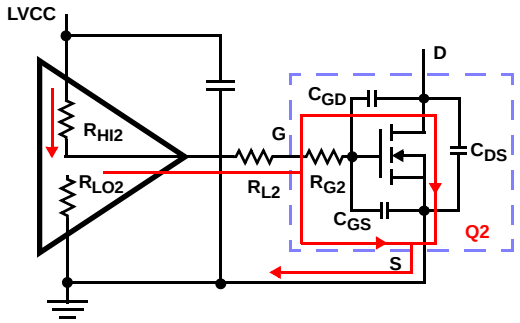


FIGURE 4. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

Application Information

MOSFET and Driver Selection

The parasitic inductances of the PCB and of the power devices' packaging (both upper and lower MOSFETs) can cause serious ringing, exceeding the device's absolute maximum ratings. The negative ringing at the edges of the PHASE node could increase the bootstrap capacitor voltage through the internal bootstrap diode, and in some cases, it may overstress the upper MOSFET driver. Careful layout, proper selection of MOSFETs and packaging, as well as the driver can minimize such unwanted stress.

The selection of D^2-PAK, or D-PAK packaged MOSFETs, is a much better match (for the reasons discussed) for the ISL6620A. Low-profile MOSFETs, such as Direct FETs and multi-source leads devices (SO-8, LFPAK, PowerPAK), have low parasitic lead inductances and can be driven by either ISL6620 or ISL6620A (assuming proper layout design). The ISL6620, missing the 3Ω integrated BOOT resistor, typically yields slightly higher efficiency than the ISL6620A.

Layout Considerations

FA good layout helps reduce the ringing on the switching node (PHASE) and significantly lower the stress applied to the output drives. The following advice is meant to lead to an optimized layout:

- Keep decoupling loops (VCC-GND and BOOT-PHASE) as short as possible.
- Minimize trace inductance, especially on low-impedance lines. All power traces (UGATE, PHASE, LGATE, GND, VCC) should be short and wide, as much as possible.
- Minimize the inductance of the PHASE node. Ideally, the source of the upper and the drain of the lower MOSFET should be as close as thermally allowable.
- Minimize the current loop of the output and input power trains. Short the source connection of the lower MOSFET to ground as close to the transistor pin as feasible. Input capacitors (especially ceramic decoupling) should be placed as close to the drain of upper and source of lower MOSFETs as possible.

In addition, connecting the thermal pad of the DFN package to the power ground through a via, or placing a low noise copper plane underneath the SOIC part is recommended for high switching frequency, high current applications. This is to improve heat dissipation and allow the part to achieve its full thermal potential.

Upper MOSFET Self Turn-on Effects at Start-up

Should the driver have insufficient bias voltage applied, its outputs are floating. If the input bus is energized at a high dV/dt rate while the driver outputs are floating, due to self coupling via the internal C_{GD} of the MOSFET, the gate of the upper MOSFET could momentarily rise up to a level greater than the threshold voltage of the device, potentially turning on the upper switch. Therefore, if such a situation could conceivably be encountered, it is a common practice to place a resistor (R_{UGPH}) across the gate and source of the upper MOSFET to suppress the Miller coupling effect. The value of the resistor depends mainly on the input voltage's rate of rise, the C_{GD}/C_{GS} ratio, as well as the gate-source threshold of the upper MOSFET. A higher dV/dt, a lower C_{DS}/C_{GS} ratio, and a lower gate-source threshold upper FET will require a smaller resistor to diminish the effect of the internal capacitive coupling. For most applications, the integrated 20kΩ resistor is sufficient, not affecting normal performance and efficiency.

The coupling effect can be roughly estimated using Equation 5, which assumes a fixed linear input ramp and neglects the clamping effect of the body diode of the upper drive and the bootstrap capacitor. Other parasitic components, such as lead inductances and PCB capacitances, are also not taken into account. Figure 5 provides a visual reference for this phenomenon and its potential solution.

$$V_{GS\_MILLER} = \frac{dV}{dt} \cdot R \cdot C_{rss}\left(1 - e^{\frac{-V_{DS}}{\frac{dV}{dt} \cdot R \cdot C_{iss}}}\right) \qquad \text{(EQ. 5)}$$

$$R = R_{UGPH} + R_{GI} \qquad C_{rss} = C_{GD} \qquad C_{iss} = C_{GD} + C_{GS}$$

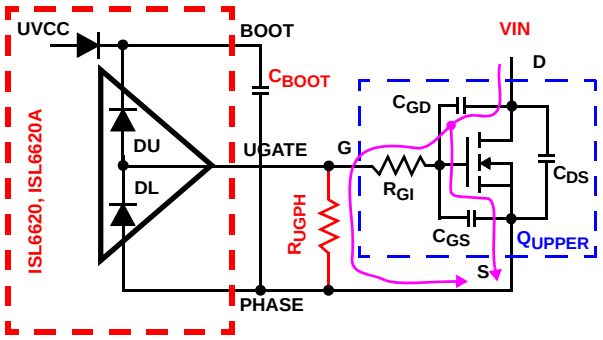
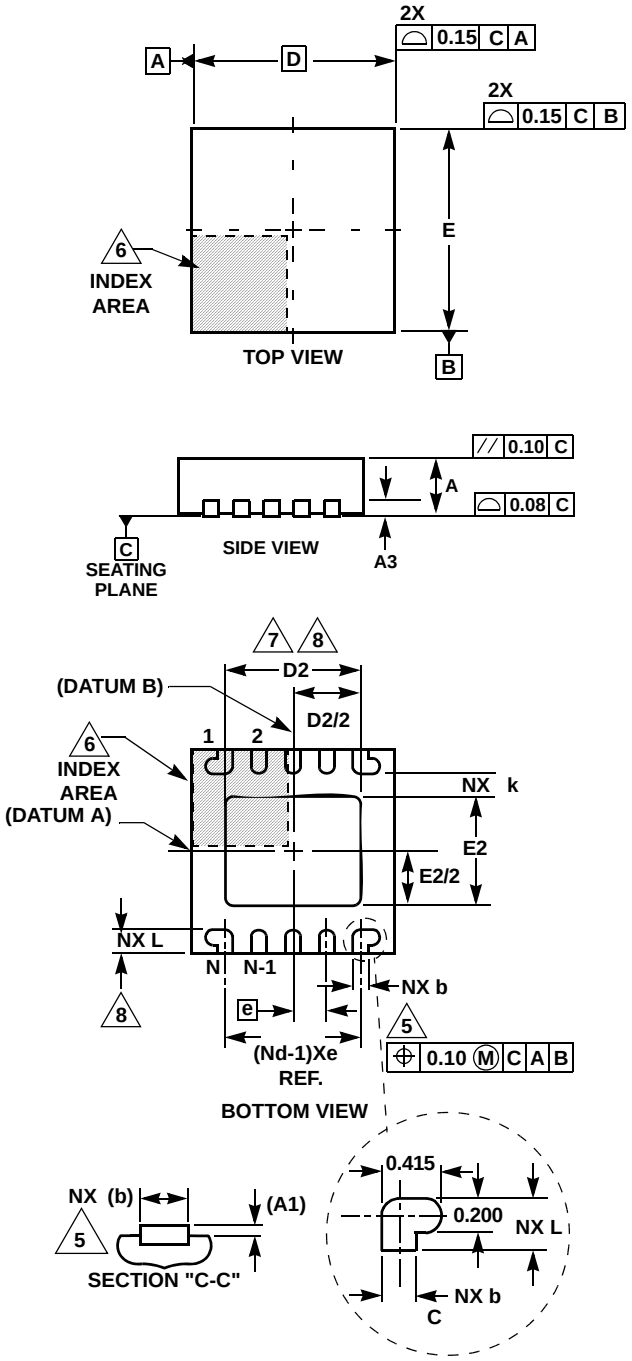


FIGURE 5. GATE TO SOURCE RESISTOR TO REDUCE UPPER MOSFET MILLER COUPLING

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3

10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.23	0.28	5,8
D		3.00 BSC		-
D2	1.95	2.00	2.05	7,8
E		3.00 BSC		-
E2	1.55	1.60	1.65	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.35	0.40	8
N		10		2
Nd		5		3

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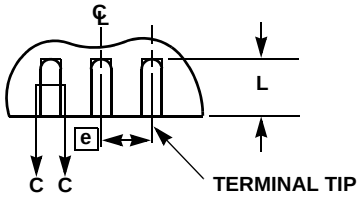
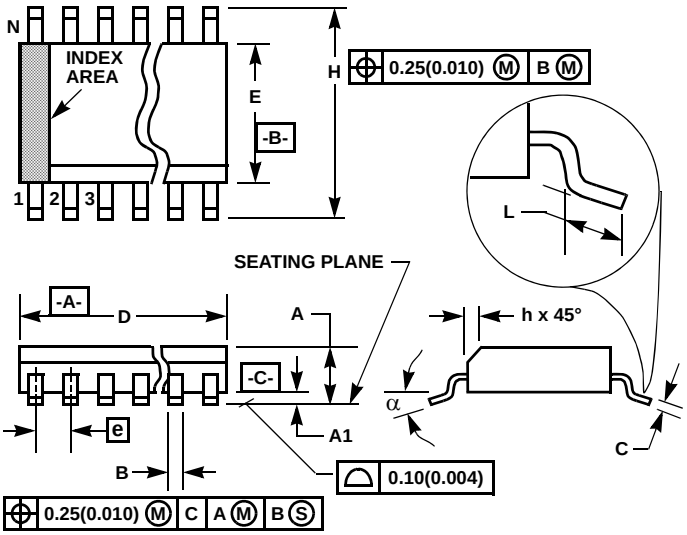
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.



FOR ODD TERMINAL/SIDE

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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