

## D/A Converter Series for Electronic Adjustments

# Standard 8bit 10ch-12ch Type D/A Converters


**BH2223FV, BH2221FV**

No.09052EAT06

**●Description**

BH2223FV and BH2221FV are high performance 8bit R-2R-type D/A converters with 10 and 12 channels outputs, respectively. A built-in RESET function ensures that the output voltage at all channels is Low during power up. And a broad power supply voltage range (2.7V - 5.5V) provides design flexibility.

**●Features**

- 1) Built-in RESET function
- 2) High speed output response characteristics
- 3) 3-line serial interface
- 4) Broad power supply voltage range: 2.7V- 5.5V

**●Applications**

DVCs, DSCs, DVDs, CD-Rs, CD-RWs

**●Lineup**

Parameter	BH2223FV	BH2221FV
Power source voltage range	2.7 to 5.5V	2.7 to 5.5V
Number of channels	10ch	12ch
Current consumption	1.6mA	1.8mA
Differential non linearity error	±1.0LSB	±1.0LSB
Integral non linearity error	±1.5LSB	±1.5LSB
Output current performance	±1.0mA	±1.0mA
Settling time	100µs	100µs
Data transfer frequency	10MHz	10MHz
Input method	CMOS	CMOS
Data latch method	LD method	LD method
Package	SSOP-B16	SSOP-B20

**●Absolute Maximum Ratings (Ta=25°C)**

Parameter	Symbol	Limits	Unit	Remarks
Power source voltage	VCC	-0.3 to 7.0	V	
Terminal voltage	VIN	-0.3 to VCC	V	
Storage temperature range	TSTG	-55 to 125	°C	
Power dissipation	PD	650*1	mW	BH2221FV
		450*2	mW	BH2223FV

\*1 Derated at 6.5mW/°C at Ta>25°C

\*2 Derated at 4.5mW/°C at Ta>25°C

\*3 These products are not robust against radiation

**●Recommended Operating Conditions (Ta=25°C)**

Parameter	Symbol	Limits			Unit	Remarks
		MIN.	TYP.	MAX.		
VCC power source voltage	VCC	2.7	-	5.5	V	-
VDD power source voltage	VDD	2.7	-	VCC	V	-
Terminal input voltage range	VIN	0	-	VCC	V	-
Analog output current	IO	-1.0	0	1.0	mA	-
Action temperature range	TOPR	-20	-	85	°C	-
Serial clock frequency	FSCLK	-	1.0	10.0	MHz	-
Limit load capacity	CL	-	-	0.1	µF	-

●Electrical Characteristics (Unless otherwise specified, VCC=3.0V, VDD=3.0V, RL=OPEN, CL=0pF, Ta=25°C)

Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
<Current consumption>						
VCC system	ICC	-	0.6	1.5	mA	CLK=1MHz, 80H setting
VDD system	IDD	-	1.0	2.0	mA	
<Logic interface>						
L input voltage	VIL	GND	-	0.2VCC	V	
H input voltage	VIH	0.8VCC	-	VCC	V	
Input current	IIN	-10	-	10	μA	
<Buffer amplifier>						
Output zero scale voltage	ZS1	GND	-	0.1	V	00H setting, at no load
	ZS2	GND	-	0.3	V	00H setting, IOH=1.0mA
Output full scale voltage	FS1	VCC-0.1	-	VCC	V	FFH setting, at no load
	FS2	VCC-0.3	-	VCC	V	FFH setting, IOL=1.0mA
<D/A converter precision>						
Differential non linearity error	DNL	-1.0	-	1.0	LSB	Input code 02H to FDH
Integral non linearity error	INL	-1.5	-	1.5	LSB	Input code 02H to FDH
VCC power source voltage rise time	trVCC	100	-	-	μs	VCC=0→2.7V
Power ON reset release voltage	VPOR	-	1.9	-	V	

●Timing Chart (VCC = 3.0V, VDD = 3.0V, RL = OPEN, CL = 0pF, Ta = 25°C, unless otherwise specified.)

Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
CLK L level time	tCLKL	50	-	-	ns	
CLK H level time	tCLKH	50	0	0	ns	
DI setup time	tsDI	20	-	-	ns	
DI hold time	thDI	40	-	-	ns	
LD setup time	tsLD	50	-	-	ns	
LD hold time	thLD	50	-	-	ns	
LD H level time	tLDH	50	-	-	ns	
Output settling time	tOUT	-	-	100	μs	CL=50pF, RL=10kΩ

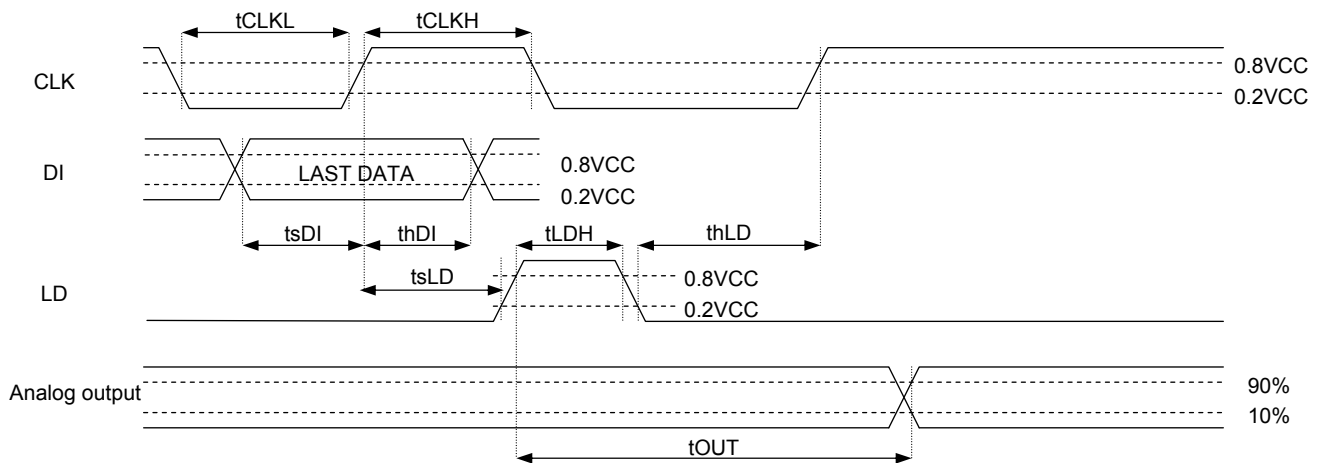


Fig.1

● Pin Description / Block Diagrams

(BH2223FV)

Terminal	Terminal name	Function
1	AO2	Analog output terminal
2	AO3	
3	AO4	
4	AO5	
5	AO6	
6	AO7	
7	AO8	
8	AO9	
9	VCC	Power source terminal
10	AO10	Analog output terminal
11	NC	Not connected yet
12	LD	Serial data load input terminal
13	CLK	Serial clock input terminal
14	DI	Serial data input terminal
15	AO1	Analog output terminal
16	GND	Ground terminal

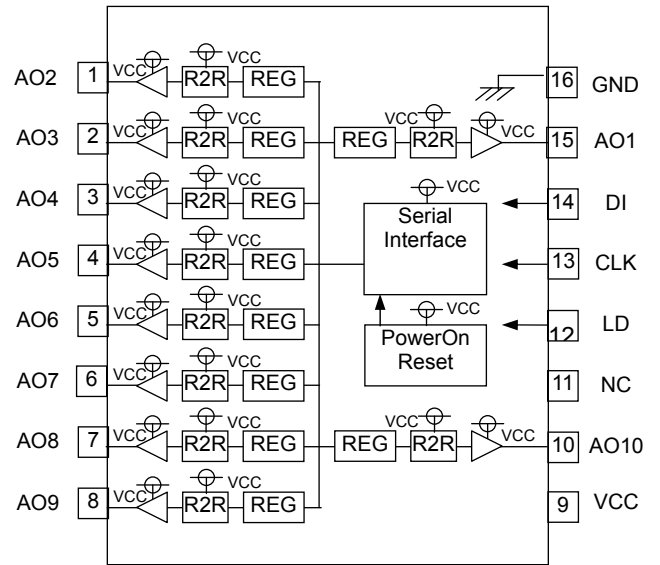


Fig.2

(BH2221FV)

Terminal	Terminal name	Function
1	NC	Not connected yet
2	AO3	Analog output terminal
3	AO4	
4	AO5	
5	AO6	
6	AO7	
7	AO8	
8	AO9	
9	AO10	
10	VDD	D/A converter standard power source terminal
11	VCC	Power source terminal
12	AO11	Analog output terminal
13	AO12	
14	NC	Not connected yet
15	LD	Serial data
16	CLK	Serial clock input terminal
17	DI	Serial data input terminal
18	AO1	Analog output terminal
19	AO2	
20	GND	Ground terminal

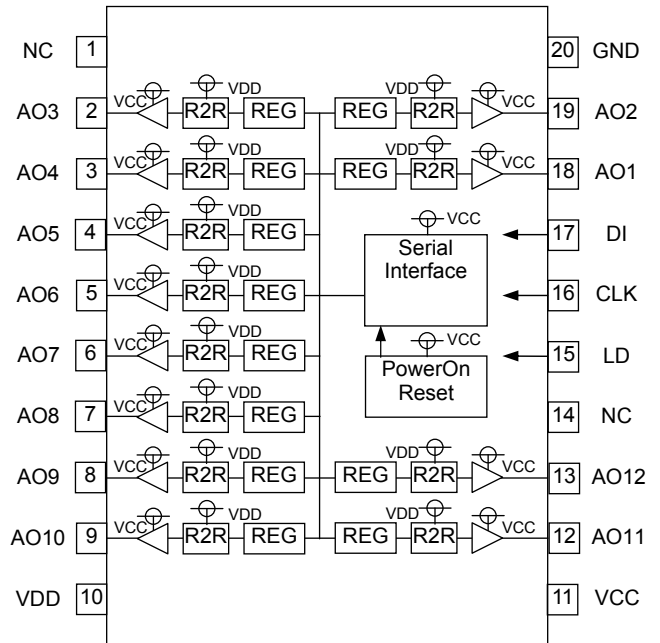


Fig.3

●Equivalent Circuit

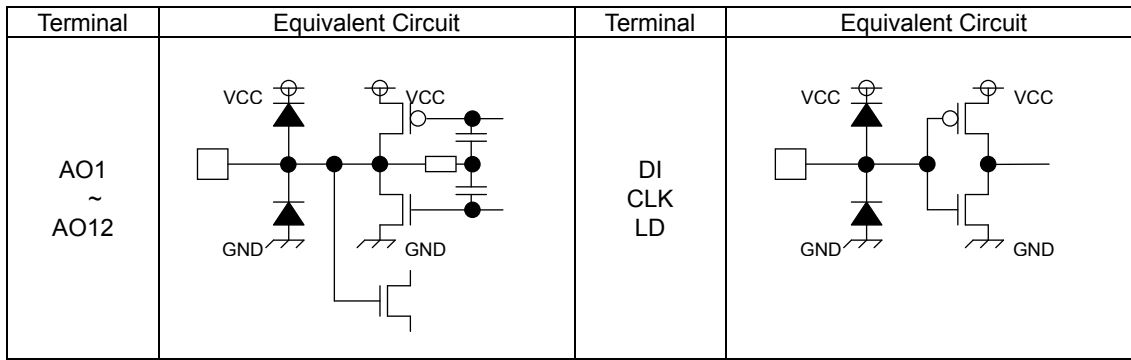


Fig.4 Equivalent Circuit

●Operation Description

Command Transmission

The Control command consists of 3 lines of 12bit serial input data (MSB first).

Data is read at the rising edge of the CLK, and output data is determined in LD High area and held in the LD Low area.

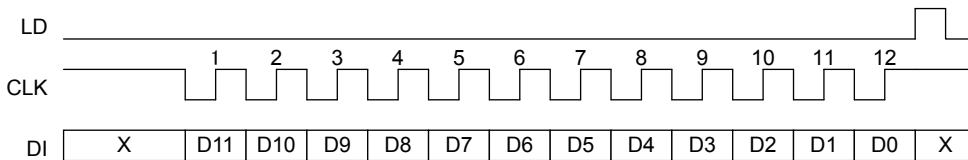


Fig.5

Data Settings

D0	D1	D3	D3	D4	D5	D6	D7	Setting
0	0	0	0	0	0	0	0	GND
1	0	0	0	0	0	0	0	(VCC or VDD-GND)/256x1
0	1	0	0	0	0	0	0	(VCC or VDD-GND)/256x2
1	1	0	0	0	0	0	0	(VCC or VDD-GND)/256x3
0	0	1	0	0	0	0	0	(VCC or VDD-GND)/256x4
~								~
0	1	1	1	1	1	1	1	(VCC or VDD-GND)/256x254
1	1	1	1	1	1	1	1	(VCC or VDD-GND)/256x255

Channel Settings

D8	D9	D10	D11	BH2223FV	BH2221FV
0	0	0	0	Inconsequential	Inconsequential
0	0	0	1	AO1	AO1
0	0	1	0	AO2	AO2
0	0	1	1	AO3	AO3
0	1	0	0	AO4	AO4
0	1	0	1	AO5	AO5
0	1	1	0	AO6	AO6
0	1	1	1	AO7	AO7
1	0	0	0	AO8	AO8
1	0	0	1	AO9	AO9
1	0	1	0	AO10	AO10
1	0	1	1	Inconsequential	AO11
1	1	0	0	Inconsequential	AO12
1	1	0	1	Inconsequential	Inconsequential
1	1	1	0	Inconsequential	Inconsequential
1	1	1	1	Inconsequential	Inconsequential

●Electrical Characteristics Curves

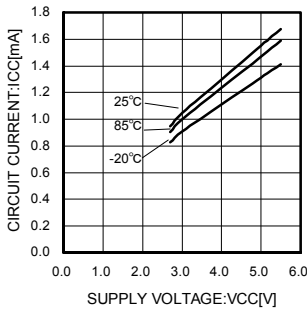


Fig.6 VCC system current consumption

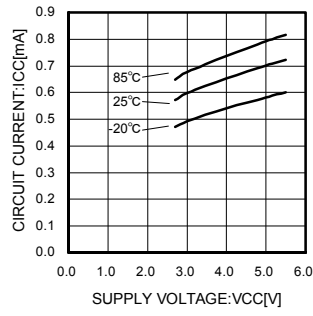


Fig.7 VDD system current consumption

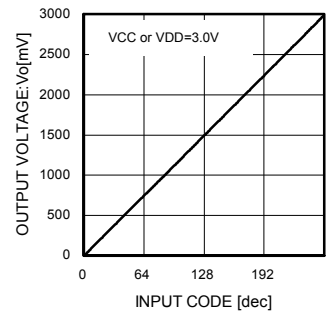


Fig.8 Output voltage characteristic

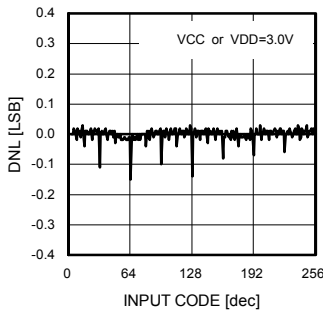


Fig.9 Differential non linearity error

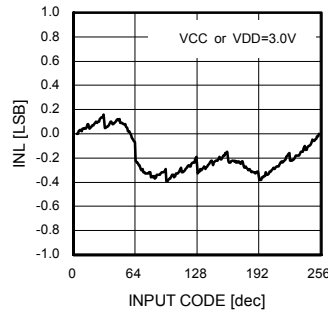


Fig.10 Integral non linearity error

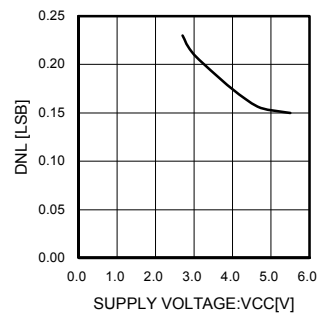


Fig.11 Power source voltage to differential non linearity error

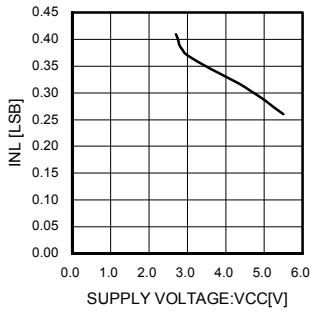


Fig.12 Power source voltage to integral non linearity error

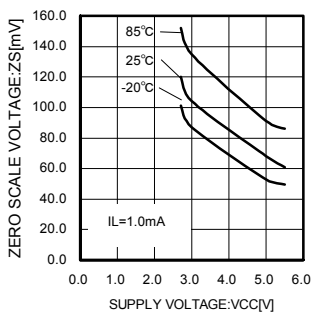


Fig.13 Output zero scale voltage

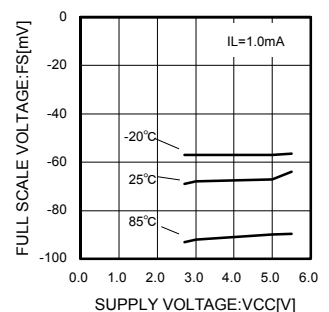


Fig.14 Output full scale voltage

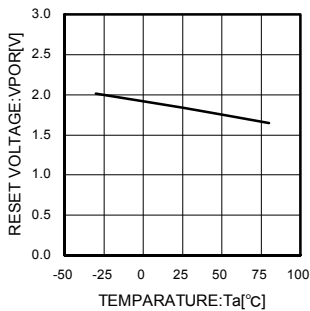


Fig.15 Reset release voltage

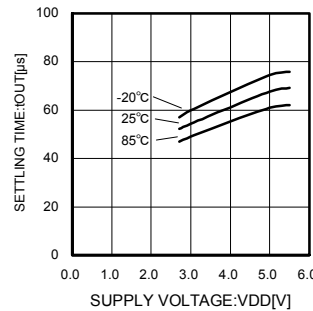


Fig.16 Settling time

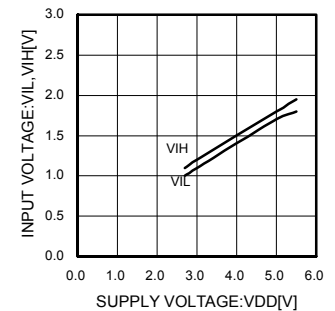


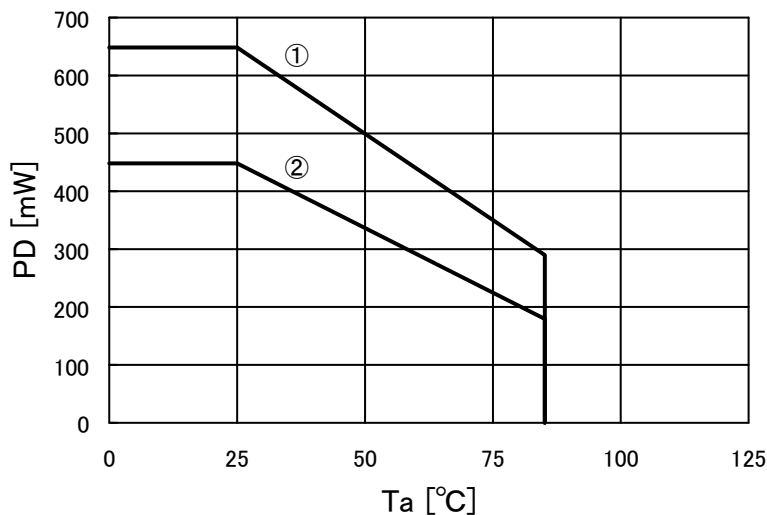
Fig.17 Input voltage

### ● Operation Notes

- (1) Numbers and data in entries are representative design values and are not guaranteed values of the items.
- (2) Although we are confident in recommending the sample application circuits, carefully check their characteristics further when using them. When modifying externally attached component constants before use, determine them so that they have sufficient margins by taking into account variations in externally attached components and the Rohm LSI, not only for static characteristics but also including transient characteristics.
- (3) Absolute maximum ratings  
Operating or testing the device over the maximum specifications may damage the part itself as well as peripheral components. Therefore, please ensure that the specifications are not exceeded.
- (4) GND potential  
Ensure that the GND terminal is at the lowest potential under all operating conditions.
- (5) Thermal design  
Use a thermal design that allows for a sufficient margin regarding power dissipation (Pd) under actual operating conditions.]
- (6) Terminal shorts and mis-mounting  
Incorrect orientation or misalignment of the IC when mounting to the PCB may damage part. Short-circuits caused by the introduction of foreign matter between the output terminals or across the output and power supply or GND may also result in destruction.
- (7) Operation in a strong magnetic field  
Operation in a strong electromagnetic field may cause malfunction.
- (8) Power source voltage  
Set the power source voltage so that  $VCC \geq VDD$ .
- (9) Reset Function  
The power on reset circuit, which initializes internal settings, may malfunction during abrupt power ons. Therefore, set the time constant so as to satisfy the power source rise time.

### ● Thermal Derating Curve

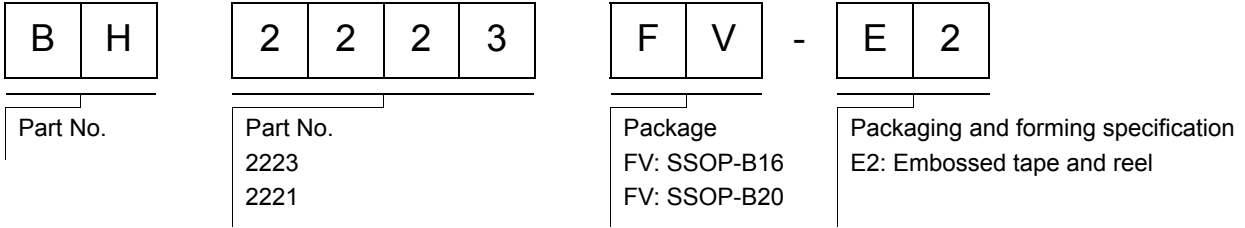
- ① SSOP-B20(BH2221FV)
- ② SSOP-B16(BH2223FV)



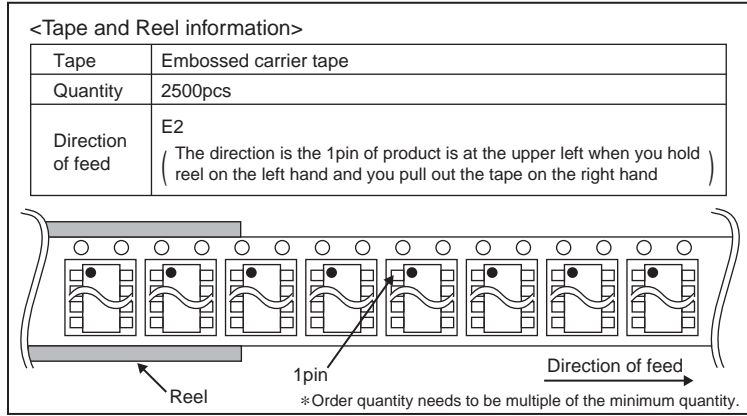
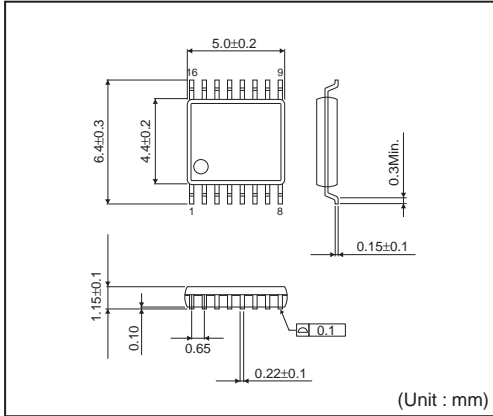
Mounted on a 70x70x1.6mm FR4 glass epoxy board (copper foil area 3% or below)

Fig.18

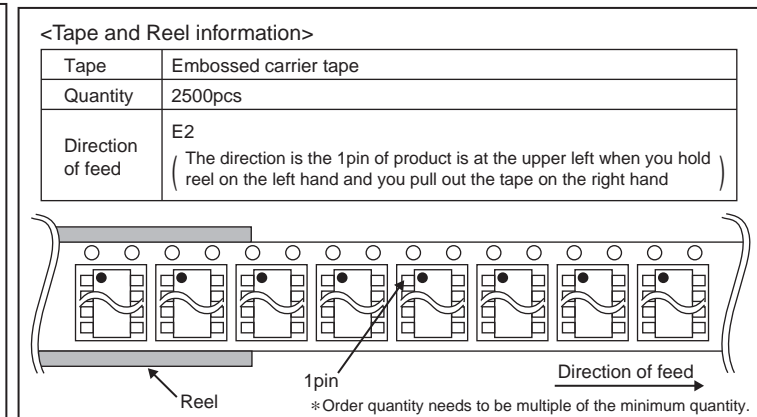
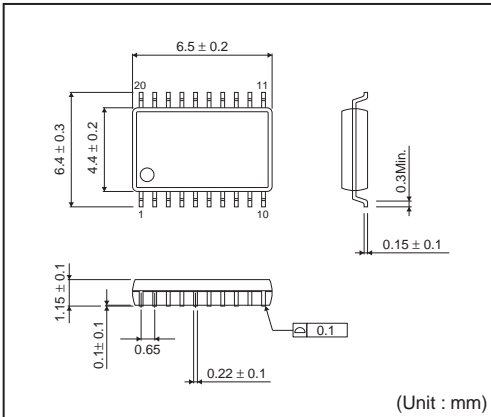
●Ordering part number



**SSOP-B16**



**SSOP-B20**



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