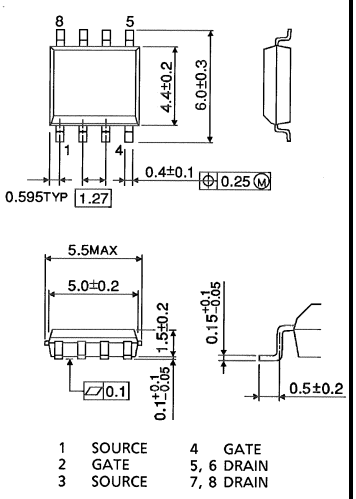
TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U−MOSII)

TPC8305

Lithium Ion Battery Applications
Portable Equipment Applications
Notebook PC Applications

- Small footprint due to small and thin package
- Low drain−source ON resistance : $R_{DS\ (ON)}$ = 24 mΩ (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 12 S (typp.)
- Low leakage current : I_{DSS} = −10 μA (max) (V_{DS} = −20 V)
- Enhancement mode : V_{th} = −0.5~ −1.2 V (V_{DS} = −10 V, I_D = −1mA)

Unit: mm



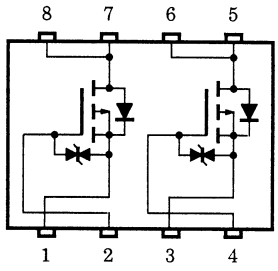
JEDEC	—
JEITA	—
TOSHIBA	2-6J1E

Weight: 0.08 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	−20	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	−20	V
Gate-source voltage		V_{GSS}	±12	V
Drain curren	DC (Note 1)	I_D	−5	A
	Pulse	I_{DP}	−20	
Drain power dissipation (t = 10s) (Note 2a)	Single-device operation (Note 3a)	$P_{D\ (1)}$	1.5	W
	Single-device value at dual operation (Note 3b)	$P_{D(2)}$	1.0	
Drain power dissipation (t = 10s) (Note 2b)	Single-device operation (Note 3a)	$P_{D\ (1)}$	0.75	W
	Single-device value at dual operation (Note 3b)	$P_{D\ (2)}$	0.45	
Single pulse avalanche energy (Note 4)		E_{AS}	32.5	mJ
Avalanche current (Note 1)		I_{AR}	−5	A
Repetitive avalanche energy Single-device value at operation (Note 2a, Note 3b, Note 5)		E_{AR}	0.10	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Circuit Configuration



Note: (Note 1), (Note 2a), (Note 2b), (Note 3a), (Note 3b), (Note 4) and (Note 5): See the next page.

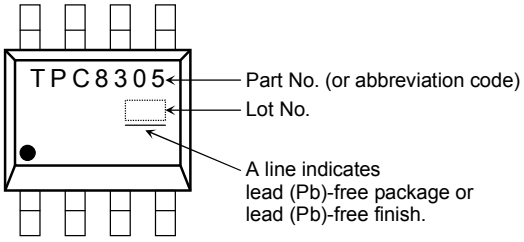
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Please handle with caution.

Thermal Characteristics

Characteristics		Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10s) (Note 2a)	Single-device operation (Note 3a)	$R_{th\ (ch\text{-}a)\ (1)}$	83.3	°C/W
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch\text{-}a)\ (2)}$	125	
Thermal resistance, channel to ambient (t = 10s) (Note 2b)	Single-device operation (Note 3a)	$R_{th\ (ch\text{-}a)\ (1)}$	167	
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch\text{-}a)\ (2)}$	278	

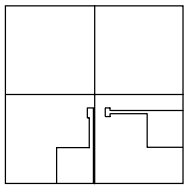
Marking (Note 6)



Note 1: Ensure that the channel temperature does not exceed 150°C.

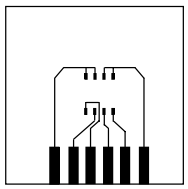
Note 2:

a) Device mounted on a glass-epoxy board (a)



(a)

b) Device mounted on a glass-epoxy board (b)



(b)

Note 3:

a) The power dissipation and thermal resistance values are shown for a single device (During single-device operation, power is only applied to one device.)

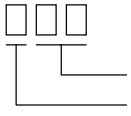
b) The power dissipation and thermal resistance values are shown for a single device (During dual operation, power is evenly applied to both devices.)

Note 4: V_{DD} = −16 V, T_{ch} = 25°C (initial), L = 1.0 mH, R_G = 25 Ω, I_{AR} = −5 A

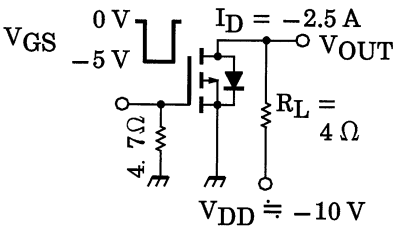
Note 5: Repetitive rating: pulse width limited by maximum channel temperature

Note 6: ● on lower left of the marking indicates Pin 1.

※ Weekly code: (Three digits)

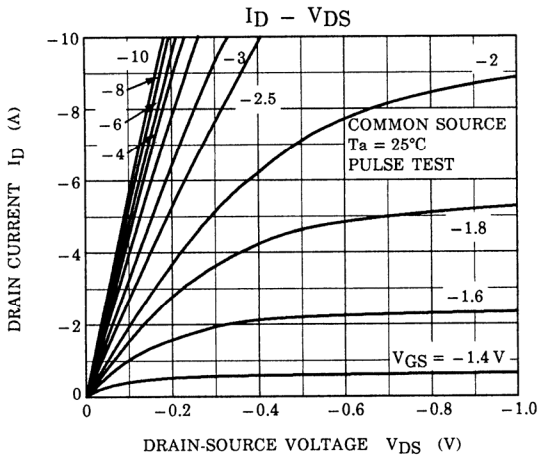


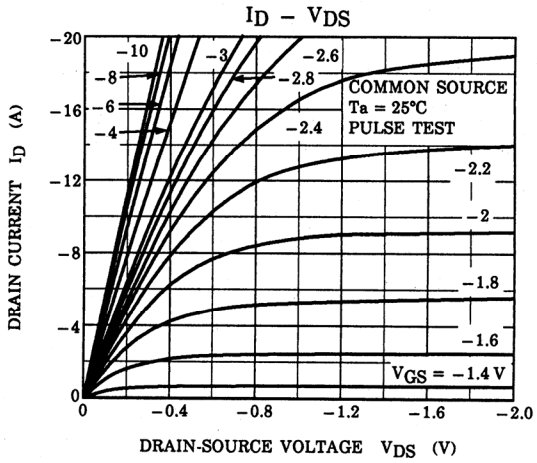
Electrical Characteristics (Ta = 25°C)

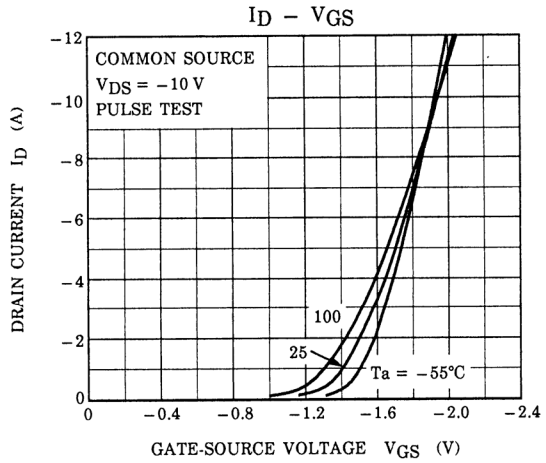
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut−off current		I_{DSS}	V_{DS} = −20 V, V_{GS} = 0 V	—	—	−10	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−20	—	—	V
			I_D = −10 mA, V_{GS} = 12 V	−8	—	—	
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −200 μA	−0.5	—	−1.2	V
Drain−source ON resistance		$R_{DS\ (ON)}$	V_{GS} = −2.0 V, I_D = −2.5 A	—	56	80	mΩ
		$R_{DS\ (ON)}$	V_{GS} = −2.5 V, I_D = −2.5 A	—	38	50	mΩ
		$R_{DS\ (ON)}$	V_{GS} = −4.5 V, I_D = −2.5 A	—	24	30	mΩ
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D = −2.5 A	6	12	—	S
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	2030	—	pF
Reverse transfer capacitance		C_{rss}		—	400	—	
Output capacitance		C_{oss}		—	580	—	
Switching time	Rise time	t_r		—	25	—	ns
	Turn−ON time	t_{on}		—	35	—	
	Fall time	t_f		—	95	—	
	Turn−OFF time	t_{off}		—	200	—	
Total gate charge (gate−source plus gate−drain)		Q_g	V_{DD} ≈ −16 V, V_{GS} = −5 V, I_D = −5 A	—	24	—	nC
Gate−source charge		Q_{gs}		—	17	—	
Gate−drain (“miller”) charge		Q_{gd}		—	7	—	

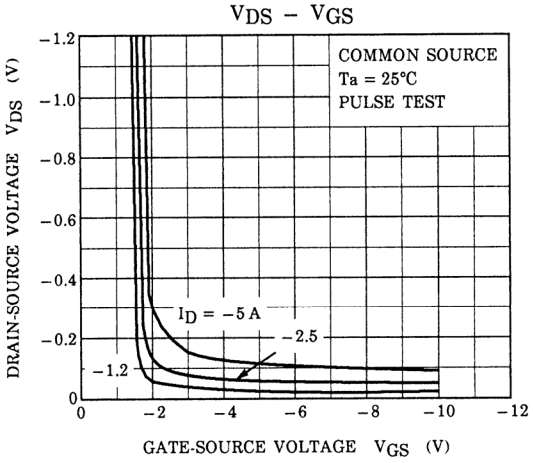
Source−Drain Ratings and Characteristics (Ta = 25°C)

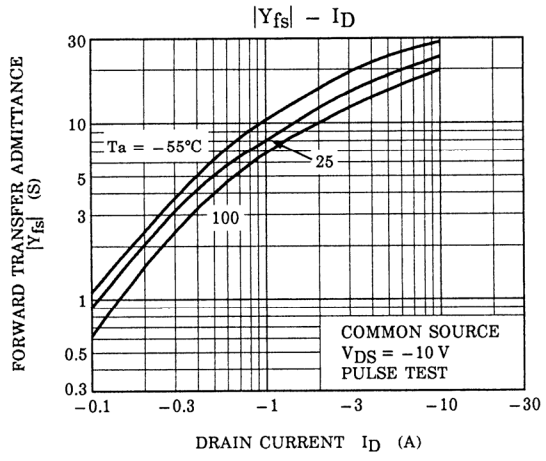
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	−20	A
Forward voltage (diode)		V_{DSF}	I_{DR} = −5 A, V_{GS} = 0 V	—	—	1.2	V

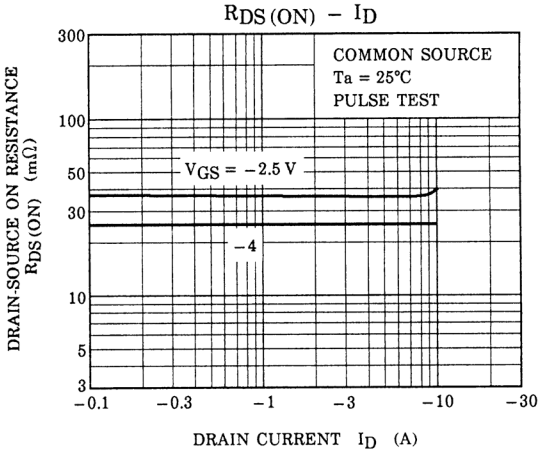

I_D – V_{DS}
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)
COMMON SOURCE
Ta = 25°C
PULSE TEST
−10
−8
−6
−4
−3
−2.5
−2
−1.8
−1.6
V_{GS} = −1.4 V
0
−0.2
−0.4
−0.6
−0.8
−1.0


I_D – V_{DS}
DRAIN CURRENT I_D (A)
DRAIN-SOURCE VOLTAGE V_{DS} (V)
COMMON SOURCE
Ta = 25°C
PULSE TEST
−10
−8
−6
−4
−3
−2.8
−2.6
−2.4
−2.2
−2
−1.8
−1.6
V_{GS} = −1.4 V
0
−0.4
−0.8
−1.2
−1.6
−2.0

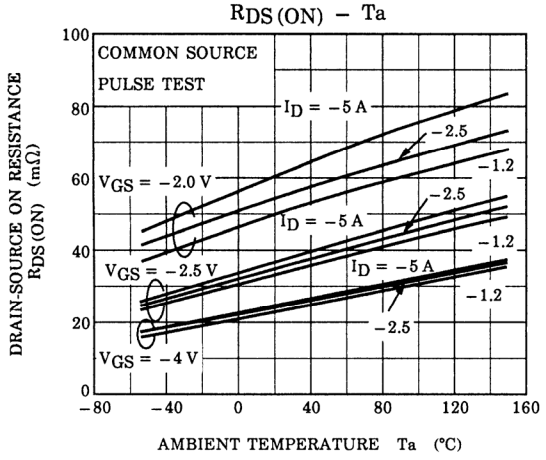

I_D – V_{GS}
DRAIN CURRENT I_D (A)
GATE-SOURCE VOLTAGE V_{GS} (V)
COMMON SOURCE
V_{DS} = −10 V
PULSE TEST
100
25
Ta = −55°C
0
−0.4
−0.8
−1.2
−1.6
−2.0
−2.4


V_{DS} – V_{GS}
DRAIN-SOURCE VOLTAGE V_{DS} (V)
GATE-SOURCE VOLTAGE V_{GS} (V)
COMMON SOURCE
Ta = 25°C
PULSE TEST
I_D = −5 A
−2.5
−1.2
0
−2
−4
−6
−8
−10
−12

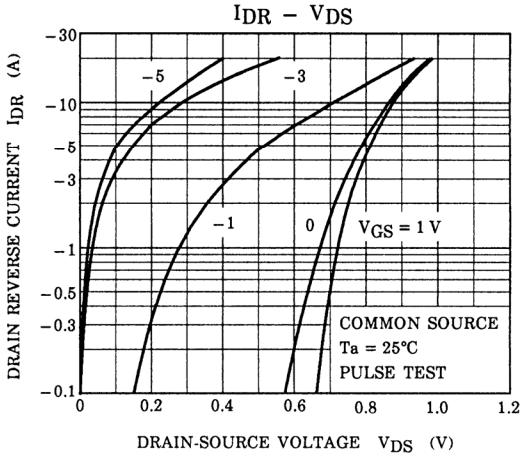

$|Y_{fs}|$ – I_D
FORWARD TRANSFER ADMITTANCE $|Y_{fs}|$ (S)
DRAIN CURRENT I_D (A)
Ta = −55°C
25
100
COMMON SOURCE
V_{DS} = −10 V
PULSE TEST
30
10
5
3
1
0.5
0.3
−0.1
−0.3
−1
−3
−10
−30


$R_{DS\,(ON)}$ – I_D
DRAIN-SOURCE ON RESISTANCE $R_{DS(ON)}$ (mΩ)
DRAIN CURRENT I_D (A)
COMMON SOURCE
Ta = 25°C
PULSE TEST
V_{GS} = −2.5 V
−4
300
100
50
30
10
5
3
−0.1
−0.3
−1
−3
−10
−30

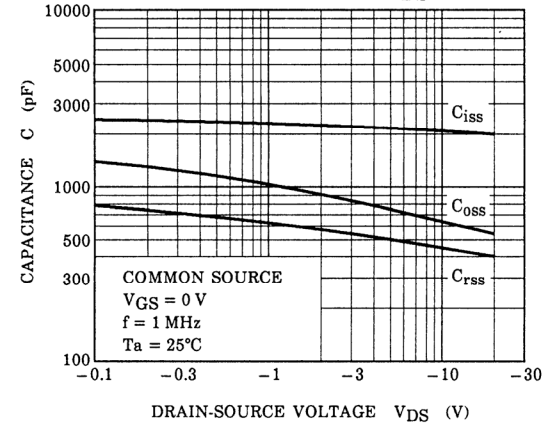
$R_{DS\,(ON)}$ – Ta



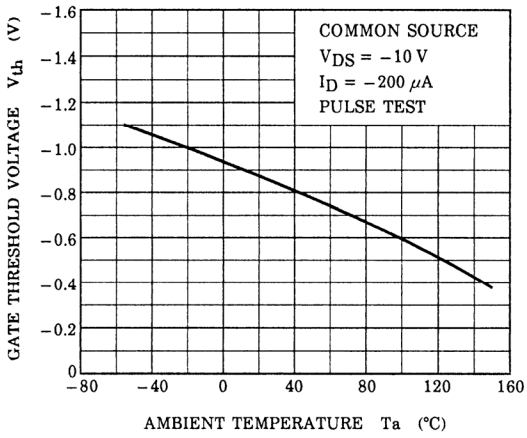
I_{DR} – V_{DS}



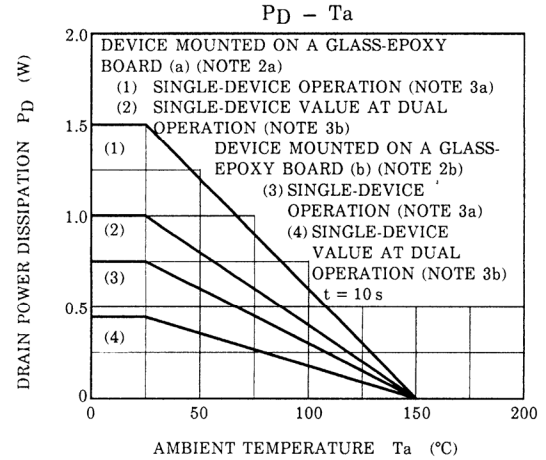
CAPACITANCE – V_{DS}



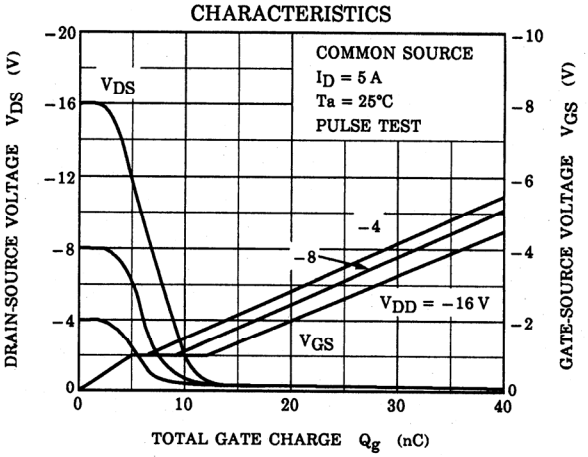
V_{th} – Ta



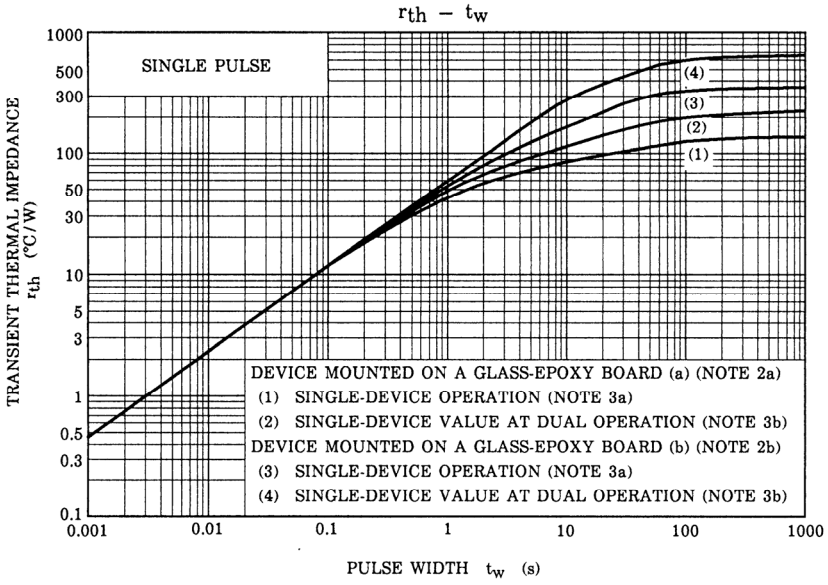
P_D – Ta



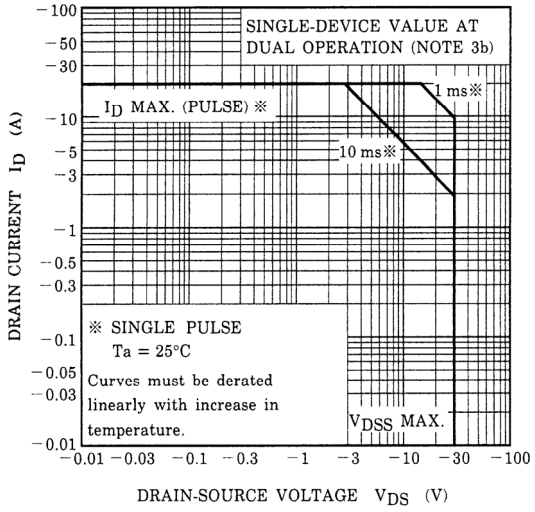
DYNAMIC INPUT / OUTPUT CHARACTERISTICS



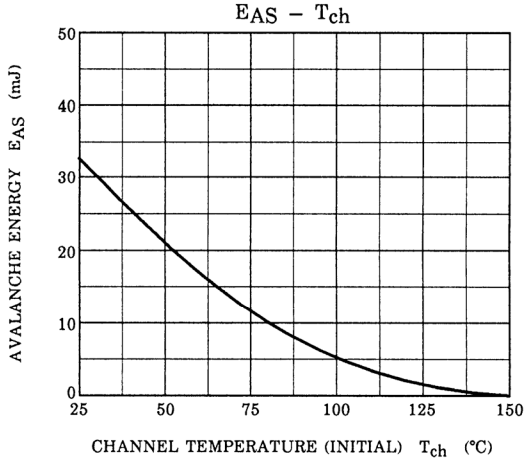
$r_{th} - t_w$

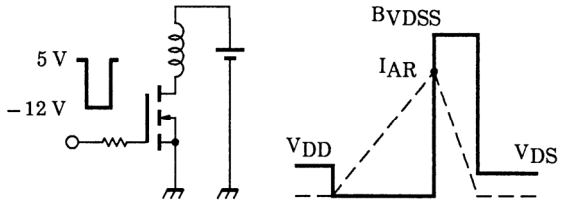


SAFE OPERATING AREA



$E_{AS} - T_{ch}$





TEST CIRCUIT WAVE FORM

T_{ch} = 25°C (Initial)
Peak I_{AR} = −5 A, R_G = 25 Ω
V_{DD} = −16 V, L = 1.0 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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