RTD2523/2513
Flat Panel Display Controller

Confidential

Revision 0.18

March 19, 2004

Revision History

Rev.	Description	Date
0.18	l Pin-Description modification of TCON function in TTL output interface l Explanation for register DV_Total	March 2004

1. Features

General
- Embedded dual DDC support DDC1, DDC2B, DDC/CI
- Zoom scaling up and down
- Embedded Pattern Generator
- No external memory required.
- Require only one crystal to generate all timing
- Embedded reset control output
- Embedded crystal output to MICROP
- 3 channels 8 bits PWM output, and selectable PWM clock frequency.

Analog RGB Input Interface
- Integrated 8-bit triple-channel 140MHz ADC/PLL
- Support up to 140MHz (SXGA@ 75Hz)
- Embedded programmable Schmitt trigger of HSYNC
- Support Sync On Green (SOG) and de-composite sync modes
- On-chip high-performance PLLs
- 32 phase APLL

Digital Input Interface
- Support 8-bit video (ITU 656) format input
- Built-in YUV to RGB color space converter & de-interlace

DVI Compliant Digital Input Interface
- Single link on-chip TMDS receiver
- Operation up to 165Mhz
- Direct connect to DVI compliant TMDS transmitter

Auto Detection /Auto Calibration
- Input format detection
- Compatibility with standard VESA mode and support user-defined mode
- Smart engine for Phase and Image position calibration

Scaling
- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement

Color Processor
- Digital brightness and contrast adjustments
- sRGB compliance
- Gamma correction
- Dithering logic for 18-bit panel color depth enhancement

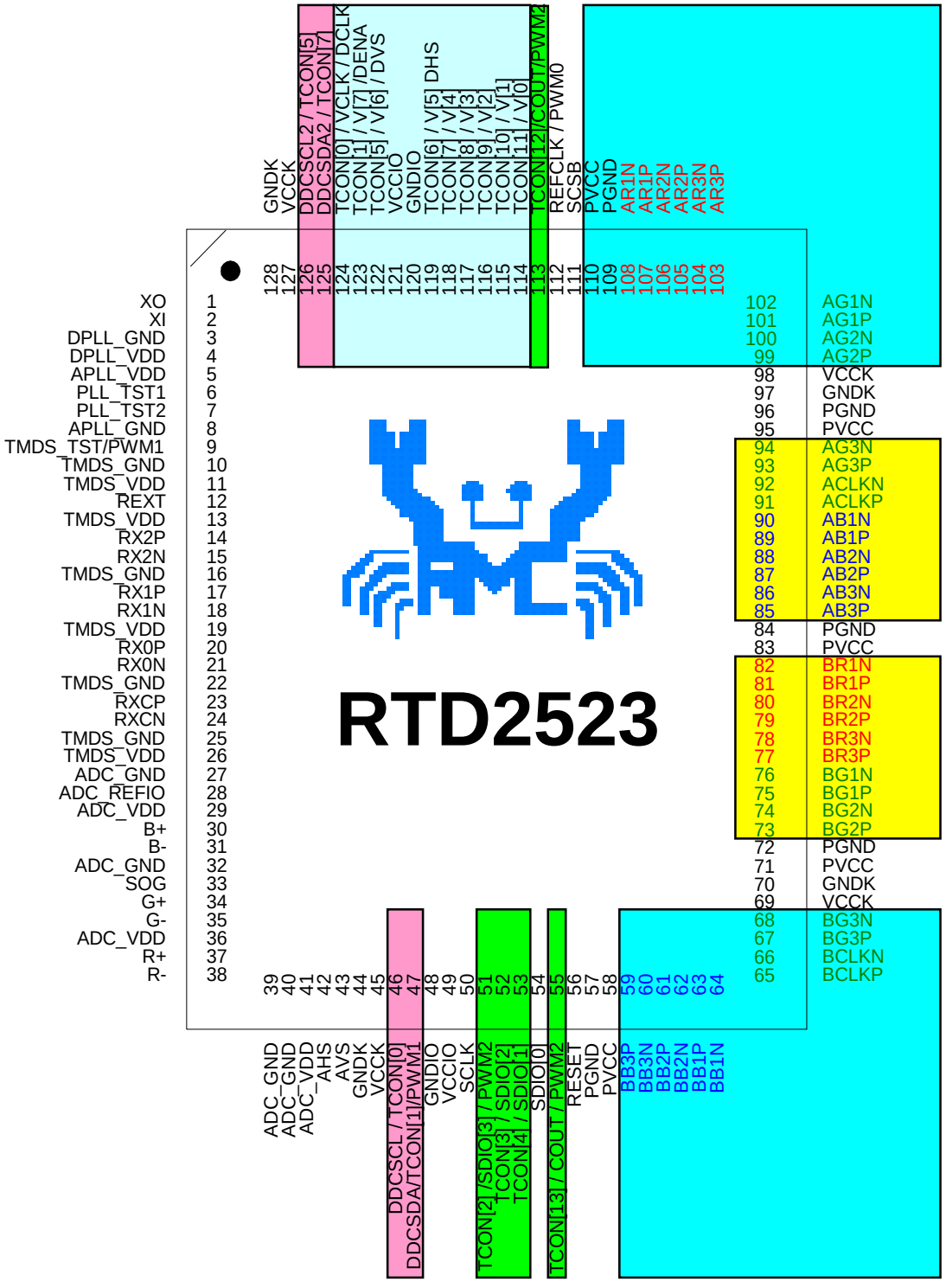
Output Interface
- Built-in display timing generator and fully programmable
- (RTD2523) 1 and 2-pixel/clock panel support and up to 140MHz
- (RTD2513) 1 and 2-pixel/clock panel support and up to 95MHz
- Scaler internal LSB/MSB swap, odd/even swap and red/blue group swap.
- Programmable TCON function support
- RSDS (Reduced Swing Differential Signaling) data bus type 1~3.
- Dual/Single LVDS interface output
- Reduced EMI and power saving feature
- Integrated Spread-Spectrum DCLK PLL.

Host Interface
- Support MCU serial bus interface
- Support MCU parallel bus interface

Embedded OSD
- Embedded 11.25K SRAM dynamically stores OSD command and fonts
- Support multi-color RAM font, 1, 2 and 4-bit per pixel
- 16 color palette with 24bit true color selection
- Maximum 8 window with alpha-blending/ gradient/dynamic fade-in/fade-out, bordering/ shadow/3D window type
- Every window can place anywhere on the screen
- Rotary 90,180,270 degree
- Independent row shadowing/bordering
- Programmable blinking effects for each character
- OSD-made internal pattern generator for factory mode
- Support 12x18~4x18 proportional font

Power & Technology
- 2.5V/3.3V power supplier
- 0.25um CMOS process; 128-pin QFP package.

2. RTD2523/2513 Pin-Out Diagram



:LVDS+RSDS+TTLO
:RSDS+TTLO
:TTLO (TCON)
:TTLIO (TCON / VIDEO)
:TTLIO (DDC / TCON)

Figure 1 Pin-Out Diagram (6-bit Dual RSDS)

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

n ADC: 15 pins

Name	I/O	Pin No	Description	Note
ADC_GND	AG	27	ADC ground	
ADC_REFIO	AP	28	ADC band-gap voltage de-coupling	1.20V
ADC_VDD	AP	29	Analog power	(3.3V)
BLUE+	AI	30	Analog input from BLUE channel	
BLUE-	AI	31	Analog input ground from BLUE channel	
ADC_GND	AG	32	ADC ground	
SOG/ADC_TEST	AIO	33	SOG in/ADC test pin	
GREEN+	AI	34	Analog input from GREEN channel	
GREEN-	AI	35	Analog input ground from GREEN channel	
ADCB_VDD	AP	36	Analog power	(3.3V)
RED+	AI	37	Analog input from RED channel	
RED-	AI	38	Analog input ground from RED channel	
ADC_GND	AG	39	Analog ground	
ADC_GND	AG	40	Analog ground	
ADC_VDD	AP	41	Analog power	(3.3V)
AHS	AI	42	Analog HS input	**(10)**, (4), (5)
AVS	AI	43	Analog VS input	(2), (4), (5)

n PLL: 8 pins

Name	I/O	Pin No	Description	Note
XO	AI	1	Reference clock output	
XI	AO	2	Reference clock input	
DPLL_GND	AG	3	Ground for digital PLL	
DPLL_VDD	AP	4	Power for digital PLL	(3.3V)
APLL_VDD	AP	5	Power for multi-phase PLL	(3.3V)
PLL_TEST1	AIO	6	Test Pin 1 / IRQ#	3.3V tolerance
PLL_TEST2	AIO	7	Test Pin 2/Power-on-latch for crystal out Frequency	
APLL_GND	AG	8	Ground for multi-phase PLL	

n Control Interface: 7 pins

Name	I/O	Pin No	Description	Note
SDIO [0]	IO	54	Serial control I/F data in / Parallel port data [0]	(2), (3), / 2mA
SDIO [1] / TCON [4] / BBLU [0]	IO	53	Parallel port data [1] / TCON [4] / TTL BBLU [0]	(1), (2), (3), / 2mA
SDIO [2] / TCON [3] / BBLU [1]	IO	52	Parallel port data [2] / TCON [3] / TTL BBLU [1]	(1), (2), (3), / 2mA
SDIO [3] / PWM2 / TCON [2]	IO	51	Parallel port data [1] / TCON [4] / PWM2	(1), (2), (3), / 2mA
SCLK	I	50	Serial control I/F clock	(2), (3), (5)
SCSB	I	111	Serial control I/F chip select	(2), (3), (5)
RESET	O	56	RESET output for Micron	(2), (5), (6) / 2mA

n Display & TCON/VIDEO-8 Port: 54 pins

:LVDS+RSDS+TTLO :RSDS+TTLO :RSDS+TTLIO :TTLO :TTLIO

Pin NO.	6-bits Dual RSDS	6 bits Single RSDS	8/6 bits Dual/Single LVDS	8 bits Dual/Single TTL	6 bits Dual TTL	6 bits Single TTL	Note
51	S[3] / TCON[2] / PWM2	S[3] / TCON[2] / PWM2	S[3] / TCON[2] / PWM2	S[3] / TCON[2] / PWM2	S[3] / TCON[2] / PWM2	S[3] / TCON[2] / PWM2	(1), (2), (3)/ 2mA
52	S[2] / TCON[3]	S[2] / TCON[3]	S[2] / TCON[3]	S[2] /BBLU[1] / TCON[3]	S[2] / TCON[3]	S[2] / TCON[3]	(1), (2), (3)/ 2mA
53	S[1] / TCON[4]	S[1] / TCON[4]	S[1] / TCON[4]	S[1]/ BBLU[0] / TCON[4]	S[1] / TCON[4]	S[1] / TCON[4]	(1), (2), (3)/ 2mA
55	PWM2 / COUT / TCON[13]	PWM2 / COUT / TCON[13]	PWM2 / COUT / TCON[13]	PWM2 / COUT / TCON[13]	PWM2 / COUT / TCON[13]	PWM2 / COUT / TCON[13]	(1), (2), (3)/ 2mA
59	BB3P	BB3P	NC	BBLU [7]	BBLU [7]	BBLU [7]	
60	BB3N	BB3N	NC	BBLU [6]	BBLU [6]	BBLU [6]	
61	BB2P	BB2P	NC	BBLU [5]	BBLU [5]	BBLU [5]	
62	BB2N	BB2N	NC	BBLU [4]	BBLU [4]	BBLU [4]	
63	BB1P	BB1P	NC	BBLU [3]/T0	BBLU [3]	BBLU [3]	
64	BB1N	BB1N	NC	BBLU [2] / T1	BBLU [2]	BBLU [2]	
65	BCLKP	BCLKP	NC	BGRN [1] / T2	TCON [6]	TCON [6]	
66	BCLKN	BCLKN	NC	BGRN [0] / T3	TCON [5]	TCON [5]	
67	BG3P	BG3P	NC	BGRN[7]	BGRN [7]	BGRN [7]	
68	BG3N	BG3N	NC	BGRN[6]	BGRN [6]	BGRN [6]	
73	BG2P	BG2P	TODP	BGRN [5] / T4	BGRN [5]	BGRN [5]	
74	BG2N	BG2N	TODN	BGRN [4] / T5	BGRN [4]	BGRN [4]	
75	BG1P	BG1P	TOCLKP	BGRN [3] / T6	BGRN [3]	BGRN [3]	
76	BG1N	BG1N	TOCLKN	BGRN [2] / T7	BGRN [2]	BGRN [2]	
77	BR3P	BR3P	TOCP	BRED [7] / T8	BRED [7]	BRED [7]	
78	BR3N	BR3N	TOCN	BRED [6] / T9	BRED [6]	BRED [6]	
79	BR2P	BR2P	TOBP	BRED [5] / T10	BRED [5]	BRED [5]	
80	BR2N	BR2N	TOBP	BRED [4] / T11	BRED [4]	BRED [4]	
81	BR1P	BR1P	TOAP	BRED [3] / T12	BRED [3]	BRED [3]	
82	BR1N	BR1N	TOAP	BRED [2] / T13	BRED [2]	BRED [2]	
85	AB3P	NC	TEDP	ABLU [7] / T14	ABLU [7]	ABLU [7]	
86	AB3N	NC	TEDN	ABLU [6] / T15	ABLU [6]	ABLU [6]	

87	AB2P	NC	TECLKP	ABLU [5] / T16	ABLU [5]	ABLU [5]	
88	AB2N	NC	TECLKN	ABLU [4] / T17	ABLU [4]	ABLU [4]	
89	AB1P	NC	TECP	ABLU [3] / T18	ABLU [3]	ABLU [3]	
90	AB1N	NC	TECN	ABLU [2] / T19	ABLU [2]	ABLU [2]	
91	ACLKP	NC	TEBP	ABLU [1] / T20	TCON [1]	TCON [1]	
92	ACLKN	NC	TEBN	ABLU [0] / T21	TCON [0]	TCON [0]	
93	AG3P	NC	TEAP	AGRN [7] / T22	AGRN [7]	AGRN [7]	
94	AG3N	NC	TEAN	AGRN [6] / T23	AGRN [6]	AGRN [6]	
99	AG2P	TCON [11]	NC	AGRN [5] / T24	AGRN [5]	AGRN [5]	
100	AG2N	TCON [10]	NC	AGRN [4] / T25	AGRN [4]	AGRN [4]	
101	AG1P	TCON [9]	NC	AGRN [3] / T26	AGRN [3]	AGRN [3]	
102	AG1N	TCON [8]	NC	AGRN [2] / T27	AGRN [2]	AGRN [2]	
103	AR3P	TCON [7]	NC	ARED [7] / T28	ARED [7]	ARED [7]	
104	AR3N	TCON [6]	NC	ARED [6] / T29	ARED [6]	ARED [6]	
105	AR2P	TCON [5]	NC	ARED [5] / TH	ARED [5]	ARED [5]	
106	AR2N	TCON [1]	NC	ARED [4] / TV	ARED [4]	ARED [4]	
107	AR1P	TCON [0]	NC	ARED [3] / TE	ARED [3]	ARED [3]	
108	AR1N	NC	NC	ARED [2] / TK	ARED [2]	ARED [2]	
113	PWM2 / COUT / TCON[12]	PWM2 / COUT / TCON[12]	PWM2 / COUT / TCON[12]	ARED [1]	COUT	PWM2 / COUT / TCON[12]	(9)
114	TCON [11] /V[0]	V [0]	V [0]	ARED [0]		TCON [11]	(1), (7), (8)
115	TCON [10] /V[1]	V [1]	V [1]	BRED [1]		TCON [10]	(1), (7), (8)
116	TCON [9] / V[2]	V [2]	V [2]	BRED [0]		TCON [9]	(1), (7), (8)
117	TCON [8] / V[3]	V [3]	V [3]	AGRN [1]		TCON [8]	(1), (7), (8)
118	TCON [7] / V[4]	V [4]	V [4]	AGRN [0]		TCON [7]	(1), (7), (8)
119	TCON [6] / V[5]	V [5]	V [5]	DHS	DHS	DHS	(1), (7), (8)
122	TCON [5] / V[6]	V [6]	V [6]	DVS	DVS	DVS	(1), (7), (8)
123	TCON [1] / V[7]	V [7]	V [7]	DENA	DENA	DENA	(1), (7), (8)
124	TCON [0] / VCLK	VCLK	VCLK	DCLK	DCLK	DCLK	(1), (7), (8)

* Single RSDS, even/odd swap, data(59~82) output to pin85~108, TCON(99~108) output to pin59~68.
* In 6-bit dual TTL output mode, Video8 cannot output TCON7~TCON11; while video8 can output TCON in 6-bit single TTL mode.

n TMDS: 18 pins

Name	I/O	Pin No	Description	Note
TMDS_TST/ PWM1	AIO	9	TMDS_TEST Pin / PWM1 / Power-on-latch for serial / parallel port	
TMDS_GND	G	10		
TMDS_VDD	P	11		(3.3V)
EXT_RES	A	12	Impedance Match Reference.	
TMDS_VDD	P	13		(3.3V)
RX2P	I	14	Differential Data Input	
RX2N	I	15	Differential Data Input	
TMDS_GND	G	16		
RX1P	I	17	Differential Data Input	
RX1N	I	18	Differential Data Input	
TMDS_VDD	P	19		(3.3V)
RX0P	I	20	Differential Data Input	
RX0N	I	21	Differential Data Input	
TMDS_GND	G	22		
RXCP	I	23	Differential Data Input	
RXCN	I	24	Differential Data Input	
TMDS_GND	G	25		
TMDS_VDD	P	26		(3.3V)

n PWM Interface: (PWM1, PWM2 can be selected from 1 of 3 possible pins.)

Name	I/O	Pin No	Description	Note
PWM2 / TCON [2] / S [3]	O	51	PWM2 / TCON [2] / SDIO [3]	(1), (2), (3), (5), (8),
PWM2 / TCON [13] / COUT	O	55	PWM2 / TCON [13] / Crystal out	(2), (8), (9)
PWM2 / TCON [12] / COUT	O	113	PWM2 / TCON [12] / Crystal out	(2), (8), (9) 6bit dual TTL cannot support
PWM1 / TMDS_TST	AIO	9	PWM1/ TMDS_TEST Pin / Power-on-latch for serial / parallel port	(2), (7), (8)
PWM1 / DDCSDA / TCON [1] / BBLU [0]	IO	47	PWM1 / DDC serial control I/F data input / output / TCON [4]	(1), (2), (3), (5), (8),
PWM1 / DDCSDA2 / TCON [7]	IO	125	PWM1 / DDC serial control I/F data input / output / TCON [7]	(1), (2), (3), (5), (8),
PWM0 / REFCLK	IO	112	PWM0 / (In / out) test pin for DCLK / Video8 even-odd signal	(2), (9)

n DDC Channel: 4 pins

Name	I/O	Pin No	Description	Note
DDCSCL / TCON [0] / BBLU [1]	I	46	DDC serial control I/F clock / TCON [0] / TTL BBLU [1]	(2), (3), (5)
DDCSDA / TCON [1] / PWM1 / BBLU [0]	IO	47	DDC serial control I/F data input / output / TCON [1] / PWM1 / TTL BBLU [0]	(1), (2), (3), (5), (6), (8)/ 8mA /no slew
DDCSCL2 / TCON [5]	I	126	DDC serial control I/F clock / TCON [5]	(2), (3), (5)
DDCSDA2 / TCON [7] /PWM1	IO	125	DDC serial control I/F data input / output / TCON [7] / PWM1	(1), (2), (3), (5), (6), (8)/ 8mA /no slew

n Power & Ground: 22 pins

Name	I/O	Pin No	Description
3.3V Power	P	49,121	VCCIO: 2
3.3V Ground	G	48,120	GNDIO: 2
3.3V Power	P	58,71,83,95,110	PVCC: 5
3.3V Ground	G	57,72,84,96,109	PGND: 5
2.5V Power	P	45,69,98,127	VCCK: 4
2.5V Ground	G	44,70,97,128	GNDK: 4

Note: (1) TTL compatible CMOS Input (Vt=1.7V); VCC=3.3V;
(2) 5V tolerance pad;
(3) Internal 75K Ohms pull high resistor.
(4) Internal 75K Ohms pull low resistor.
(5) Schmitt trigger CMOS Input (Vt=1.4-~2.2V);
(6) Open-Drain, Output Drive low & Pull-high.
(7) Bi-directional input/output
(8) Programmable driving current (2~10mA)
(9) TTL output 5V & 3.3V
(10) 4V tolerance pad

3. General Description

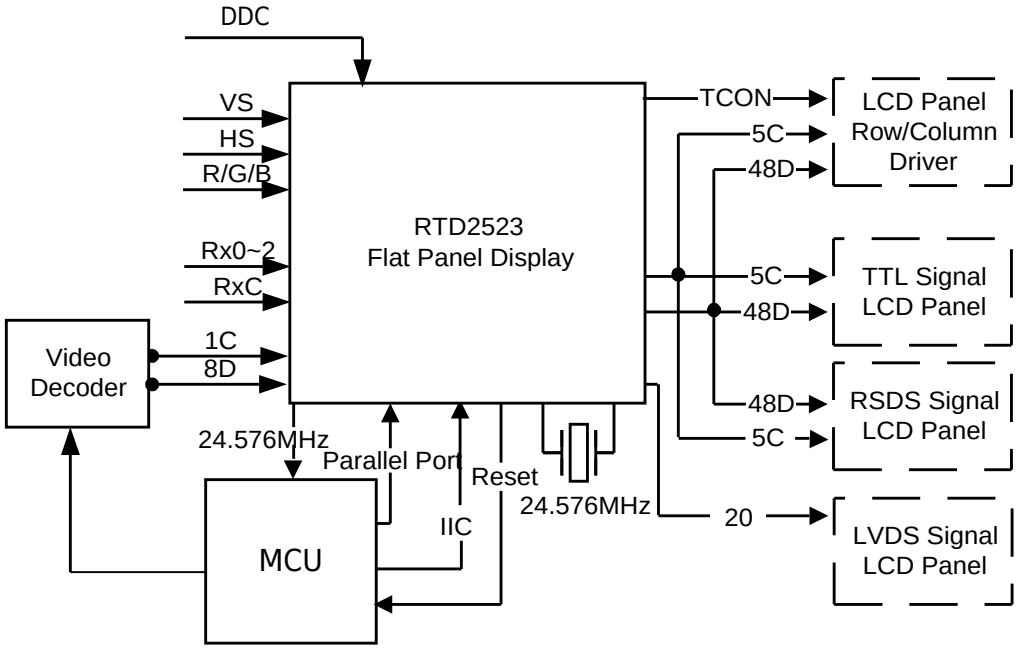


Figure 2 Application System Block Diagram

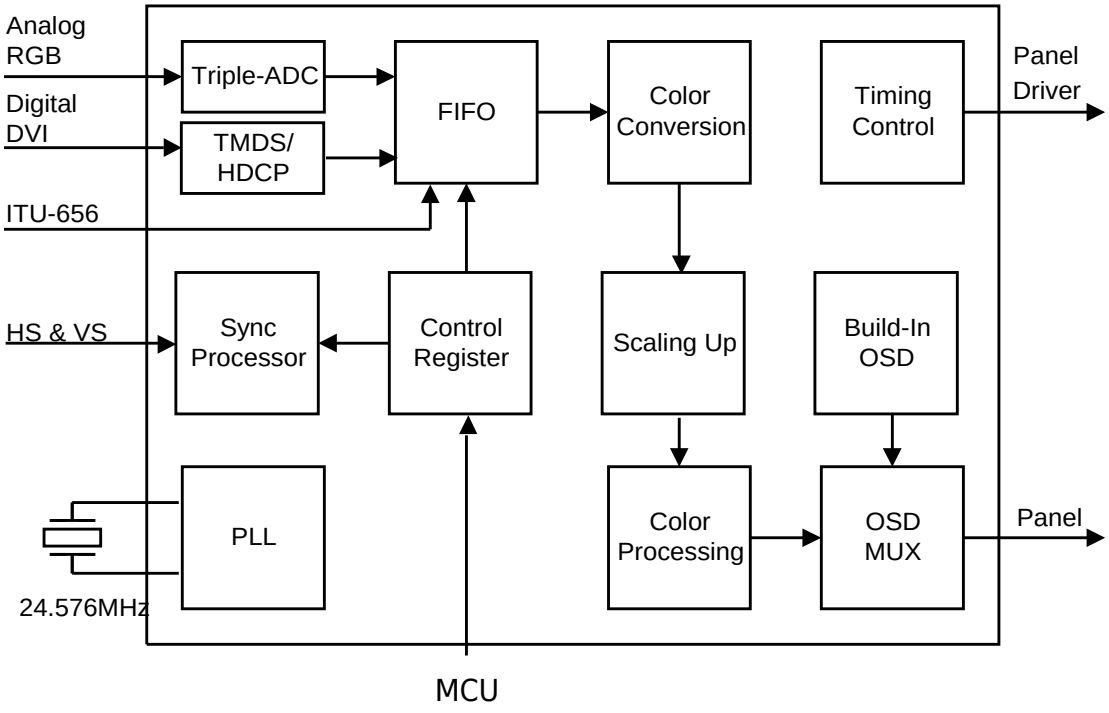


Figure 3 Chip Functional Block Diagram

4. Functional Description

4.1 Input

Digital Input (ITU 656)

RTD is designed to connect the interface of digital signal from video decoder. Input data is latched within a capture window defined in registers. The timing scheme designed for input devices are showed in the following diagram.

There are not H sync、V sync signals provided by the video decoder with ITU BT.656, these synchronal signals have to be generated by decoding the EAV & SAV timing reference signals.

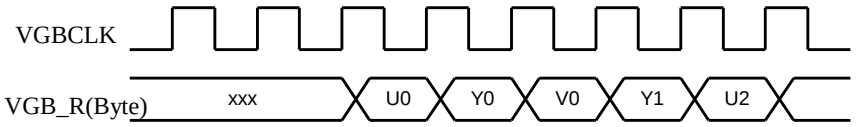


Figure 4 Input YUV 4:2:2(8-bits) Timing

Only 254 of possible 256 8-bit words may be used to express a signal value, 0 and 255 are reserved for data identification purposes. Video 8 data stream is as below:

Blanking period			Timing reference code				720 pixels YUV 422 DATA								Timing reference code				Blanking period		
…	80	10	FF	00	00	SAV	Cb0	Y0	Cr0	Y1	Cb2	Y2	…	Cr718	Y719	FF	00	00	EAV	80	10	…

Cbn: U(B-Y) colour difference component
Yn : luminance component
Crn: V(R-Y) colour difference component

SAV/EAV format

Bit 7	Bit 6(F)	Bit 5(V)	Bit 4(H)	Bit 3(P3)	Bit 2(P2)	Bit 1(P1)	Bit 0(P0)
1	Field bit 1st field F=0 2nd field F=1	Vertical blanking bit V=1 Active video V=0	H=0 in SAV H=1 in EAV	Protection bits			

Hardware can recognize the occurrence of EAV & SAV by detecting the 0xff , 0x00 , 0x00 data sequence, and then generate the Hsync、Vsync、Field signals internally by decoding the fourth word of the timing reference signal(EAV、SAV). F & V change state synchronously with the EAV(End of active video) reference code at the beginning of the digital line.

Bits P0, P1, P2, P3, have states dependent on the states of the bits F, V and H as shown below. At the receiver this permits one-bit errors to be corrected and two-bits errors to be detected.

Protection bits

F	V	H	P_3	P_2	P_1	P_0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

Error correction

A = P1 xor F xor V
B = P2 xor F xor H
C = P3 xor V xor H
D = F xor V xor H xor P3 xor P2 xor P1 xor P0

F' = F xor (D · A · B · C#)
V' = V xor (D · A · B# · C)
H' = H xor (D · A# · B · C)

SAV/EAV one-bit error occurs when D · (A + B + C)
SAV/EAV two-bit error occurs when D# · (A + B + C)

Analog Input
RTD integrates three ADC's (analog-to-digital converters), one for each color (red, green, and blue). The sync-processor can deal with Separate-Sync, Composite-Sync, and Sync-On-Green. And the PLL can generate very low jitter clock from HS to sample the analog signal to digital data. Input data is latched within a capture window defined in registers refer to VS and HS leading edge.

TMDS Input
RTD integrates high-speed single link receiver. It can operate up to 165Mhz.

Input Capture Window
Inside RTD, there are four registers IPH_ACT_STA, IPH_ACT_WID, IPV_ACT_STA & IPV_ACT_LEN to define input capture window for the selected input video on either A or B input port while programmed analog input mode. The horizontal sync (IHS) & vertical sync (IVS) signals are used from the selected port to determine the capture window region.

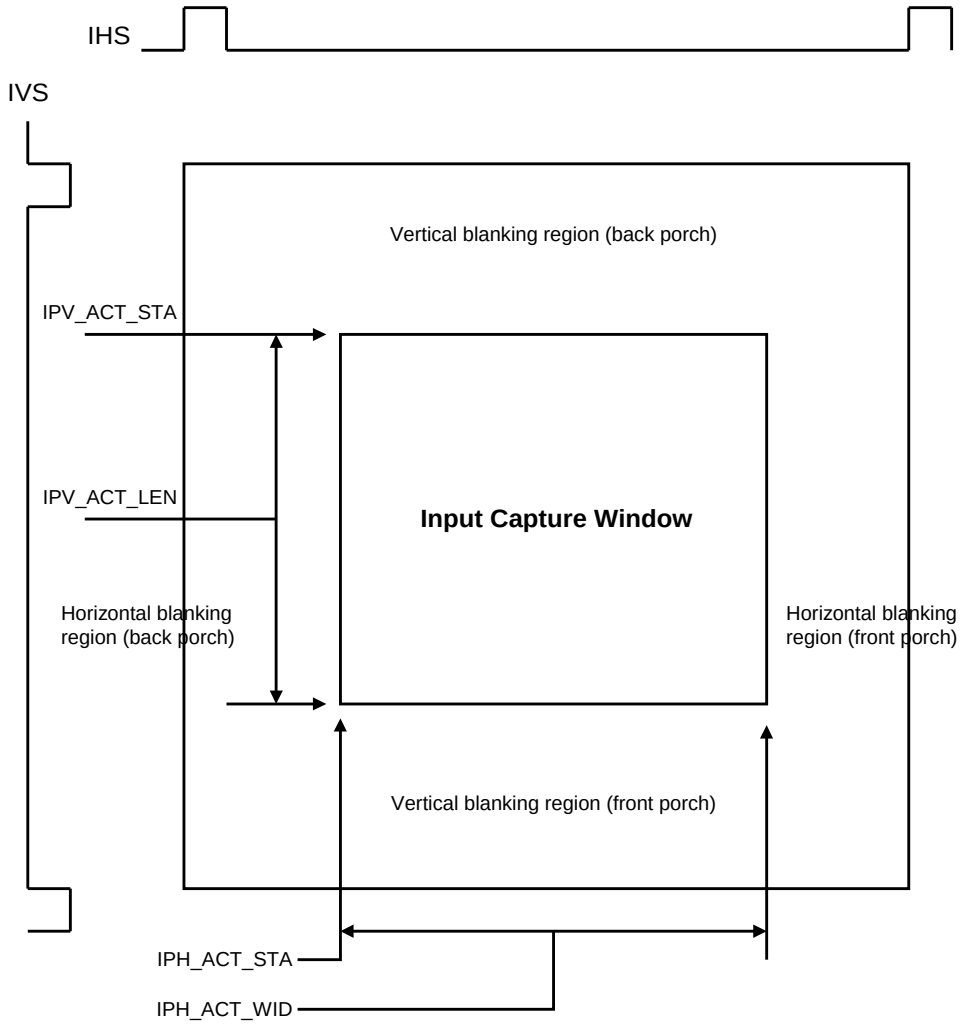


Figure 5 Input Capture Window

4.2 Output Timing

Display Output Timing

The display output port sends single/double pixel data transfer and synchronized display timing to an external device. The display port also support display panel with 6-bit per color, turn on the dithering function to enhance color depth.

In single pixel output mode, single pixel data (24-bit RGB) is transferred to display port A on each active edge of DCLK, the rate of DCLK is also equal to display pixel clock. The sync & enable signals are also sent to display port on each active edge of DCLK.
Seeing figure13 as below

In double pixel output mode, double pixel data (48-bit RGB) is transferred to display port A & B on each active edge of DCLK and the rate of DCLK is equal to half display pixel clock at this moment. The sync & enable signals are also sent to display port on each active edge of DCLK. Seeing figure14 as below.

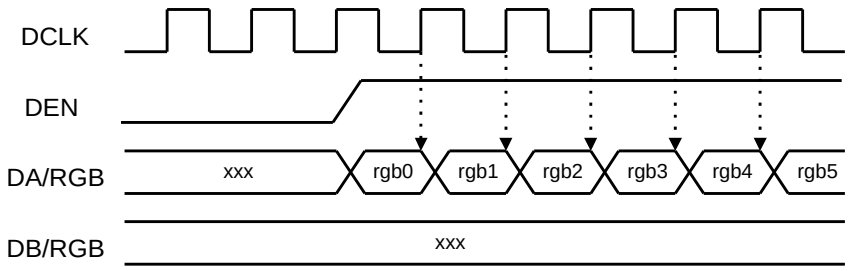


Figure 6 Single Pixel Mode Display Data Timing

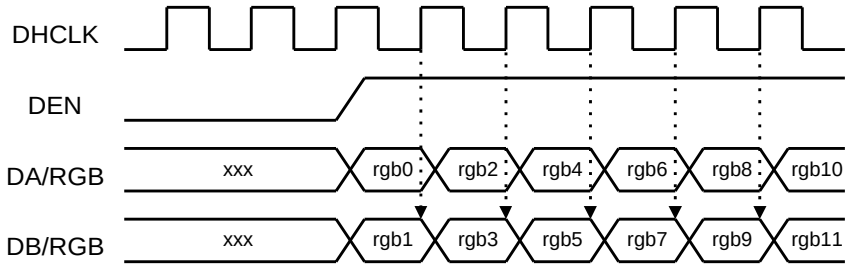


Figure 7 Double Pixel Mode Display Data Timing

Display Active Window

These registers to define the display active window are showed us below in application with frame buffer. In the case of without frame buffer that means frame sync mode, the definitions of these registers are quiet different from the description below. There are two frame sync modes applied to RTD chip for various applications. Refer to the register description for detailed.

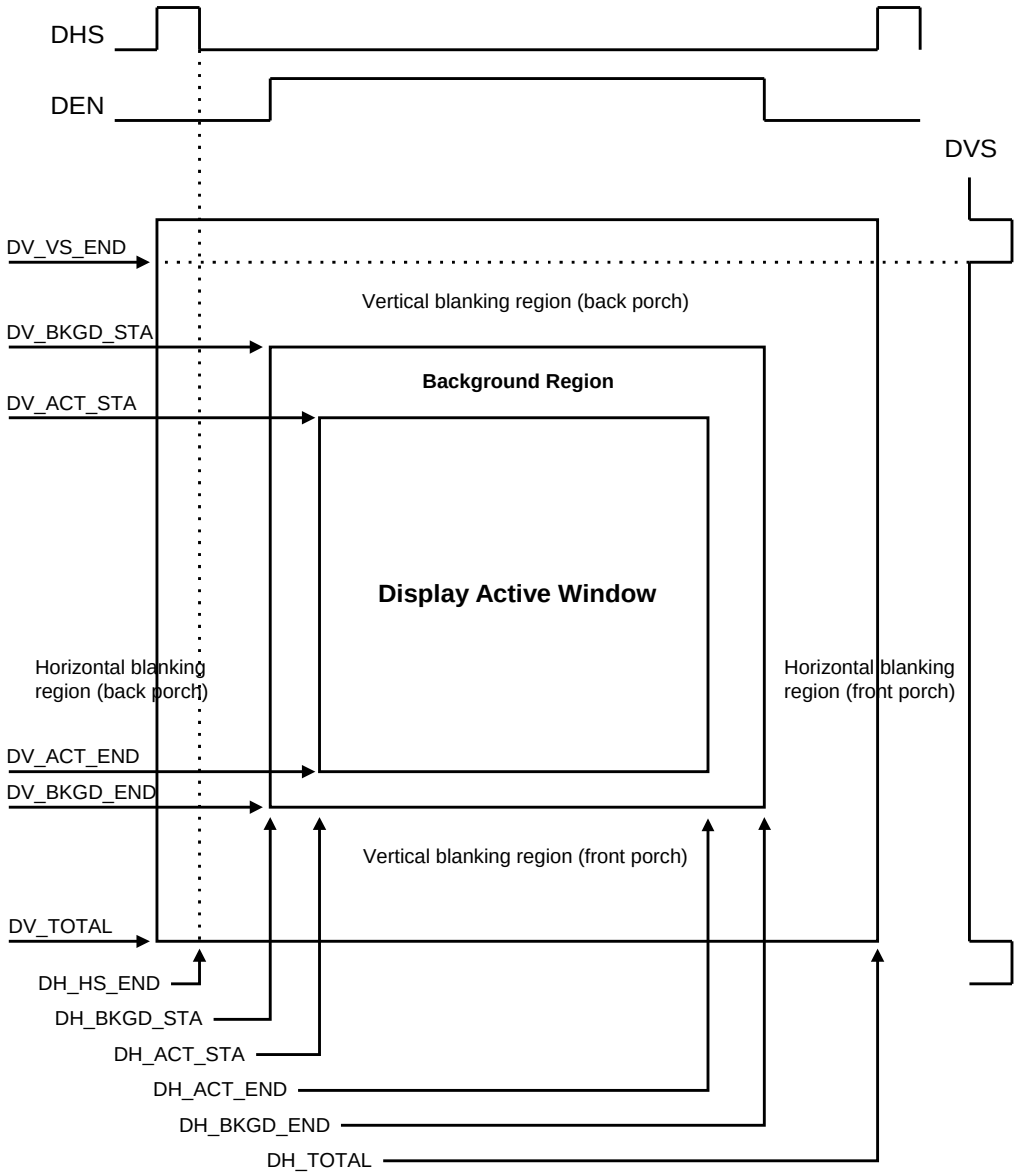


Figure 8 Display Active Window Diagram

4.3 Color Processing

Digital color R & G & B independent channel contrast & brightness controls are built in RTD. The contrast control is performed a multiply value from 0/128, 1/128, 2/128… to 255/128 for each R/G/B channel. The brightness control is used to set an offset value from –128 to +127 also for each R/G/B channel.

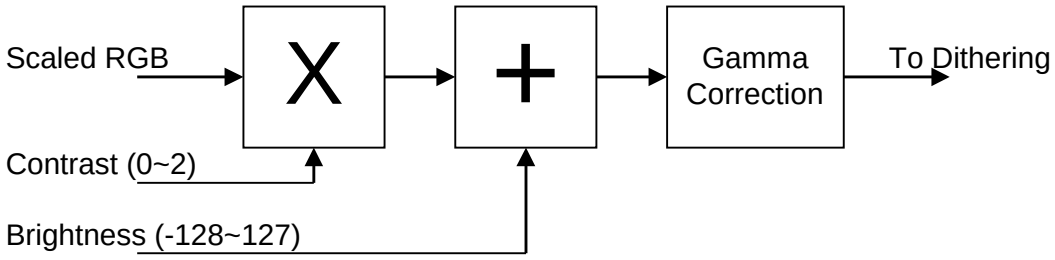


Figure 9 Brightness, Contrast & Gamma Correction block diagram

4.4 OSD & Color LUT

Build-In OSD

The detailed function-description of build-in OSD, please refer to the application note for RTD embedded OSD.

Color LUT & Overlay Port

The following diagram presents the data flow among the gamma correction, dithering, overlay MUX, OSD LUT and output format conversion blocks.

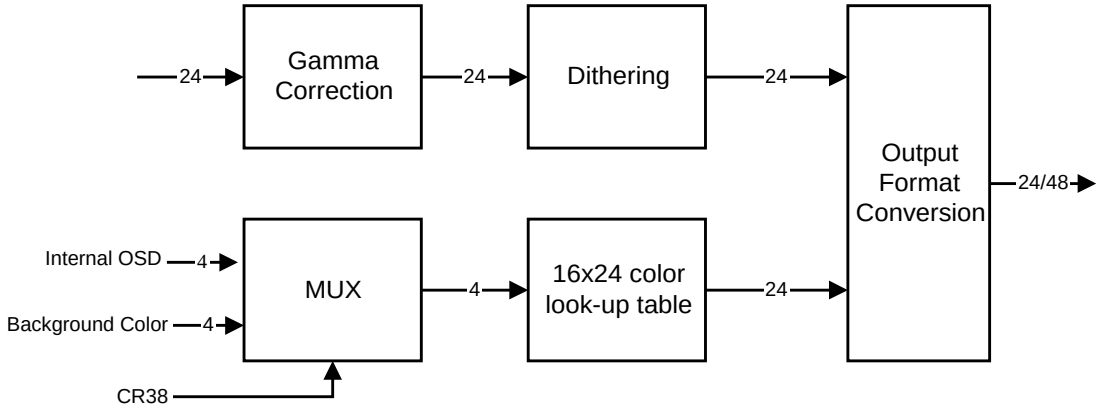


Figure 10 OSD color look-up table data path diagram

4.5 Auto-Adjustment

There are two main independent auto-adjustment functions supported by RTD, including auto-position & auto-tracking. The operation procedure is as following;

Auto-Position

1. Define the RGB color noise margin (7B,7C,7D): When the value of color channel R or G or B is greater than these noise margins, a valid pixel is found.
2. Define the threshold-pixel for vertical boundary search (7C[1:0]).
3. Define the boundary window of searching (75 ~ 7A) for horizontal boundary search.
4. Start auto-function (7F[0]) .
5. The result can be read from register (80 ~ 87).

Auto-Tracking

1. Setting the control-registers (7F) for the function (auto-phase, auto-balance) according to the Control-Table.
2. Define the Diff-Threshold (7E).
3. Define the boundary window of searching (75 ~ 7A) for tracking window.
4. Start auto-function (7F[0]) .
5. The result can be read from register (88 ~ 8B).

4.6 PLL System

Inside the RTD, there are three PLL systems for display clock and ADC sample clock.

DCLK PLL

PLL provides a wide range of user-programmable frequency synthesis options, and the formula as following; The frequency before VCO_Divide must be 50MHz~450MHz.

DCLK = Fin * DPM / DPN / VCO_Divide,

Meanwhile, Fin = 24.576MHz, the DPLL_M[7:0] & DPLL_N[5:0] are the 8-bit M & 6-bit N value of DCLK. DPM=DPLL_M[7:0]+2, DPN=DPLL_N[5:0]+2.

Of course, you can force this clock from external oscillators through pins REFCLK for your own applications.

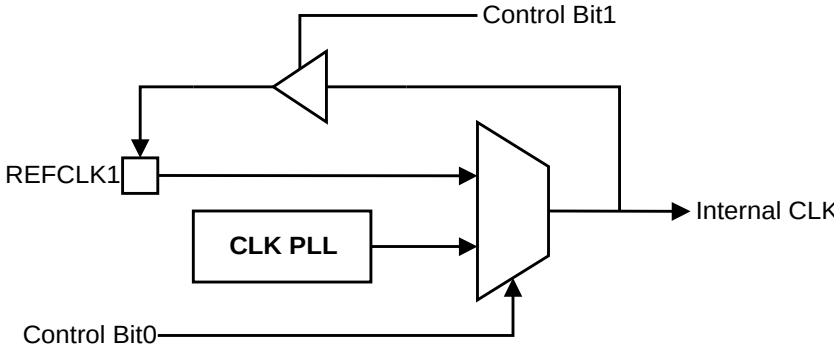


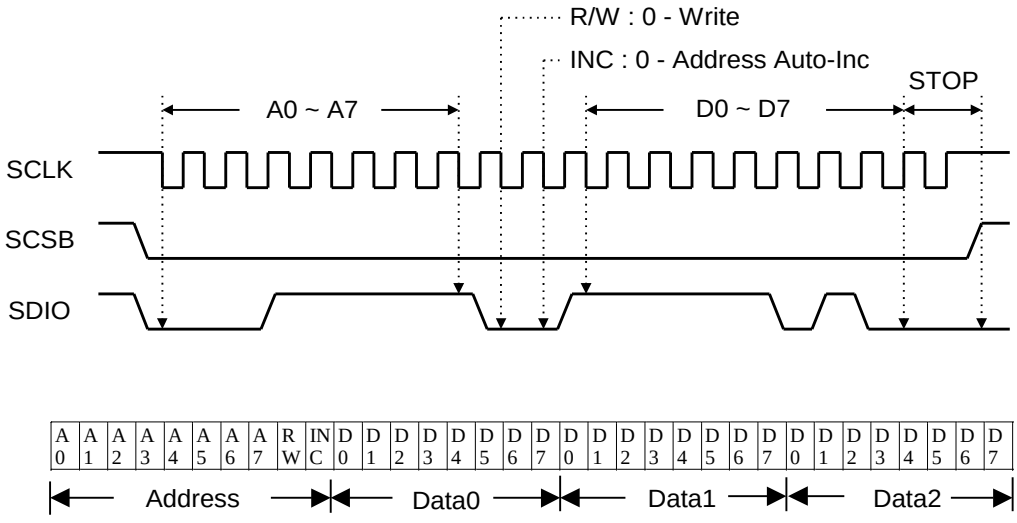
Figure 11 PLL System Control Diagram

Spread-Spectrum function is also build in DCLK to reduce EMI while using TCON. You can control the SSP_I, SSP_W, and FMDIV to fine-tune the EMI.

4.7 Host Interface

Serial Port:

Any transaction should start from asserted the SCS# and stop after de-asserted the SCS#. Within this period, any data are driving by clock rising edge and latched by clock falling edge. The detailed timing diagrams are as following;



Address: A0~A7

R/W: Read/Write Mode for Data Phase, 0 -- Write, 1 -- Read

INC: Address Auto-Increasing Mode, 0 -- enable auto-increasing, 1 -- disable

Figure 12 Serial Port Write Timing & Data Format

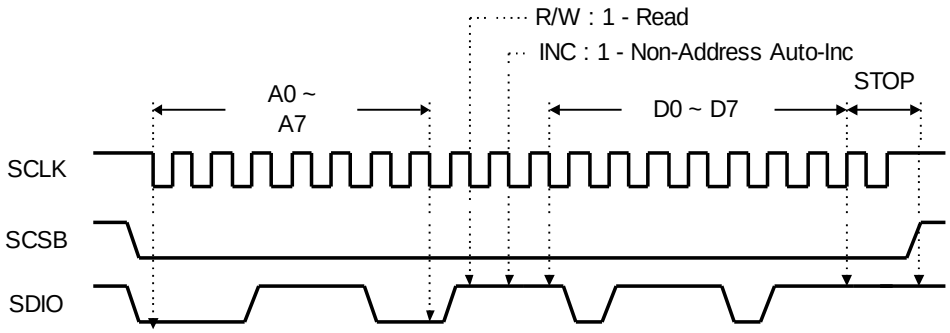


Figure 13 Serial Port Read Timing

Parallel Port:

After RESET end, the status of pin 9 (TMDS_TST) can be sensed to determine the interface mode: **high à parallel port, low à serial port.**

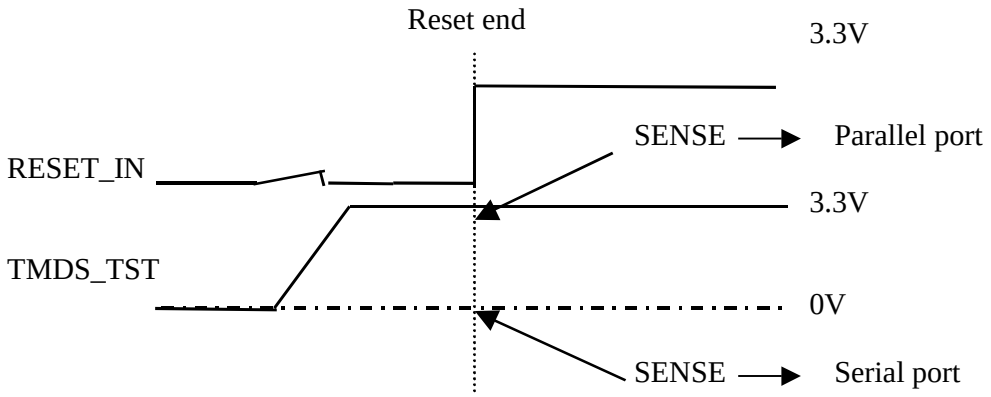
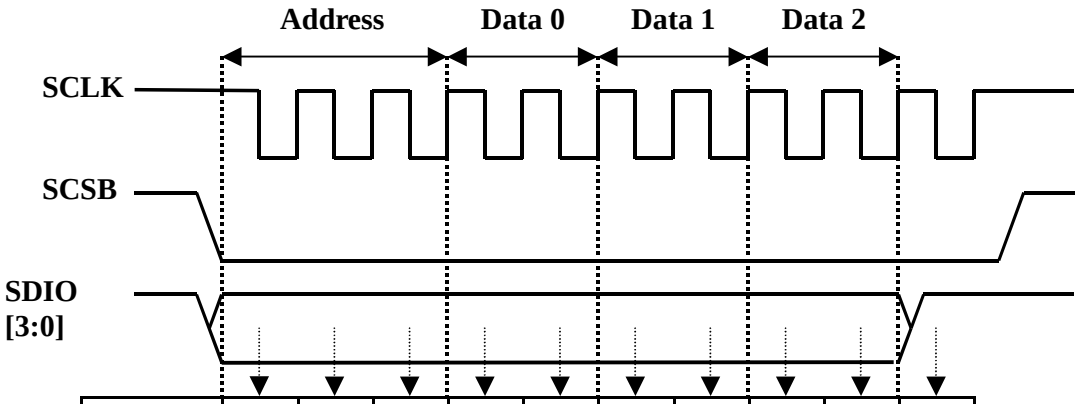


Figure 15 Serial Port / Parallel Port Select

The 4-bit parallel port works just like our serial port. The biggest difference is that the address part needs 3 clocks but data 2. All the other definitions like "R/W", "INC" and "STOP" are the same with the serial port. The detailed timing diagrams are as following;



SDIO [0]	A [0]	A [4]	R/W	D0 [0]	D0 [4]	D1 [0]	D1 [4]	D2 [0]	D2 [4]	1
SDIO [1]	A [1]	A [5]	INC	D0 [1]	D0 [5]	D1 [1]	D1 [5]	D2 [1]	D2 [5]	1
SDIO [2]	A [2]	A [6]	X	D0 [2]	D0 [6]	D1 [2]	D1 [6]	D2 [2]	D2 [6]	1
SDIO [3]	A [3]	A [7]	X	D0 [3]	D0 [7]	D1 [3]	D1 [7]	D2 [3]	D2 [7]	1

Figure 16 Parallel Port Timing

4.8 Reset Output

We have the RESET_OUT function, and also reserve the RESET_IN function. By the bounding of internal pins we can select three kinds of reset function. First of all is only reset-out, we can output the reset signal to microns, and the micron can reset the RTD by firmware. The second choice is only reset-in, the RTD can be reset by input signal or also firmware. The last is RTD output reset and also reset itself. Noticed that the reset output is positive polarity, the reset in is negative polarity. Besides, the reset output is open-drain pin.

The reset function operating voltage is determined by ADC_VDD voltage. The negative threshold voltage is 1.8V at power-on status, but it can be programmed by registers to be 1.8V, 2.0V, 2.2V and 2.4V after power on. The registers are 0xEB [7:6]

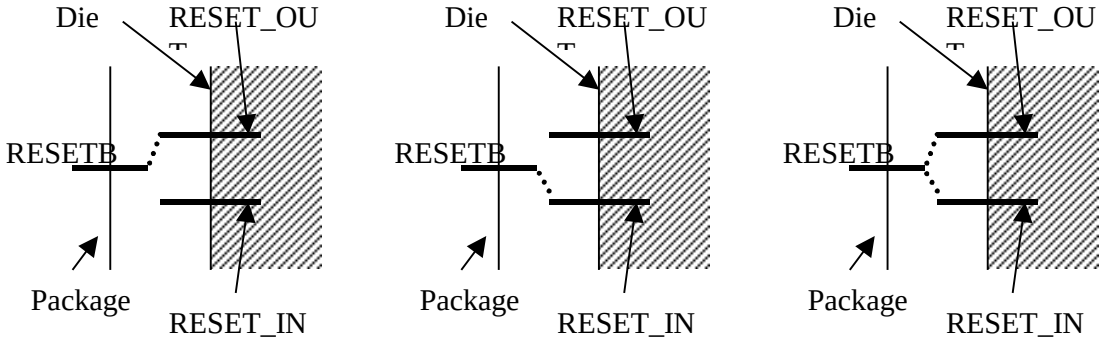


Figure 17 Three kinds of RESET function

For the reset-out function, the characteristics are below:

Parameter	Symbol	Min.	Typ.	Max.	Unit
Detection Voltage	$-V_{det}$	1.8	2.4		V
Release Voltage	$+V_{det}$		2.6		V
Delay Time	td	50			ms

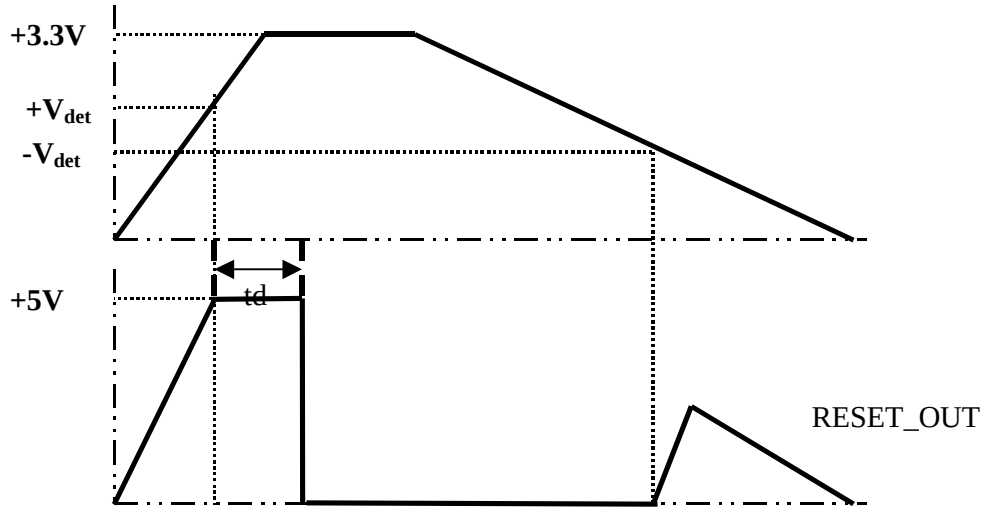


Figure 18 The RESET_OUT Timing Diagram

4.9 The Programmable Schmitt Trigger of HSYNC

To get better waveform of the input HSYNC, we have a programmable Schmitt Trigger circuit. For different HSYNC amplitude and polarity, we can select different setting of the threshold voltage. The $\mathbf{V_t^+}$ and the $\mathbf{V_t^-}$ can be selected by register 0xED.

We can select the old mode or the new mode. When using the new mode we can directly determine the positive threshold voltage (1.4V, 1.6V… 2.6V), and we can choose the distance from the $\mathbf{V_t^+}$ to determine the $\mathbf{V_t^-}$ (0.6V, 0.8V, 1.0V, 1.2V). We also can finely tune the voltage by minus 0.1V. For application, we can select different threshold voltage by the polarity of the HSYNC. The control register is 0xED.

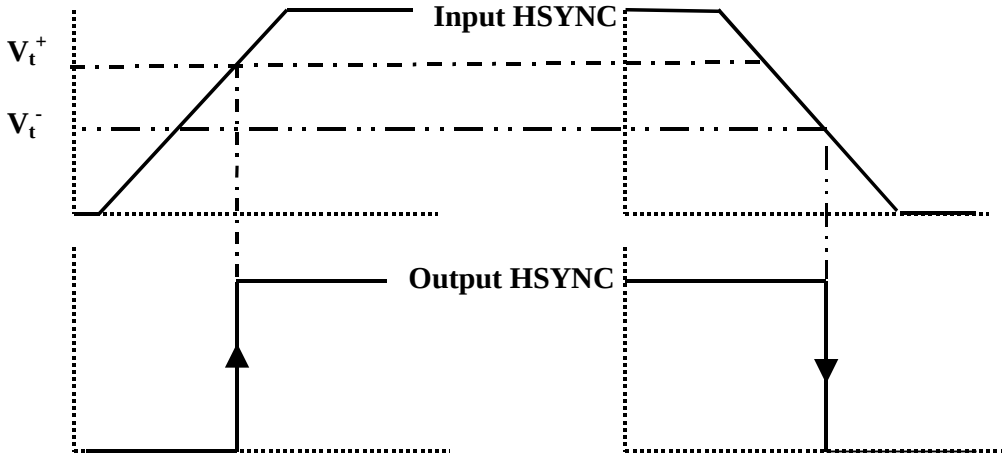


Figure 18 The Schmitt Trigger Behavior Diagram

4.10 Crystal Frequency Output

RTD can output crystal frequency or half crystal frequency to external MCU to save a crystal device. After power on, RTD latch the state of PLL_TEST2 pin to determine which frequency to output, and the result shows in TCON register address 0x00[0]. 0 is for half of crystal frequency and 1 is for crystal frequency. When power on, crystal frequency output to TCON12 and TCON13. Hence, crystal-in pin of external MCU can connect to TCON12 or TCON13. Firmware can turn off the signal output of other pin, and the control register is in TCON register 0x00[1] and 0x00[2].

4.11 Pin Out Configuration

RTD supports TTL, LVDS and RSDS output interface. After power on, display port is high impedance. Firmware can set its control register in TCON address 0x03[7:6] to select output interface. Refer to Pin Out Diagram for output pin definition.

RSDS interface

For dual RSDS output interface, set 2'b11 to "Display Port Configuration" in TCON 0x03[7:6], 1'b1 to "Display 18 bit RGB Mode Enable" in 0x20[4], and 1'b1 to "Display Output Double-Width Pixel Enable" in 0x20[2].

"Display Even/Odd Data Swap" in 0x21[7] can swap even pixel and odd pixel output to RSDS A Port and RSDS B Port. "Display Red/Blue Data Swap" in 0x21[6] can swap red-channel data and blue-channel data. "Display MSB/LSB Data Swap" in 0x21[5] can swap bit order between "bit7, 6, 5, 4, 3, 2" and "bit2, 3, 4, 5, 6, 7". "RSDS Green / Clock Pair Swap" in TCON 0x03[5] can swap three green pair and clock pair order between "G1, G2, G3, CLOCK" and "CLOCK, G1, G2, G3". "RSDS High/Low Bit Swap (data)" in TCON 0x03[1] can swap bit order in one data pair. "RSDS Differential pair PN swap (data)" in TCON 0x03[0] can swap differential positive and negative pin.

TCON signal shares pin with parallel access port, PWM, crystal frequency output, video port and DDC channel.

For single RSDS output interface, set 2'b11 to "Display Port Configuration" in TCON 0x03[7:6], 1'b1 to "Display 18 bit RGB Mode Enable" in 0x20[4], and 1'b0 to "Display Output Double-Width Pixel Enable" in 0x20[2].

"Display Red/Blue Data Swap" in 0x21[6] can swap red-channel data and blue-channel data. "Display MSB/LSB Data Swap" in 0x21[5] can swap bit order between "bit7, 6, 5, 4, 3, 2" and "bit2, 3, 4, 5, 6, 7". "RSDS Green / Clock Pair Swap" in TCON 0x03[5] can swap three green pair and clock pair order between "G1, G2, G3, CLOCK" and "CLOCK, G1, G2, G3". "RSDS High/Low Bit Swap (data)" in TCON 0x03[1] can swap bit order in one data pair. "RSDS Differential pair PN swap (data)" in TCON 0x03[0] can swap differential positive and negative pin.

TCON11, 10, 9, 8, 7, 6, 5, 1, 0 use dedicated pin and output to pin 99~107. Video input port also has dedicated pin.

LVDS interface

For single/dual LVDS output interface, set 2'b10 to "Display Port Configuration" in TCON 0x03[7:6]. "Display 18 bit RGB Mode Enable" in 0x20[4] determines 6bits or 8bits data output per channel. "Display Output Double-Width Pixel Enable" in 0x20[2] determines one pixel or two pixels output per display clock. "Display Even/Odd Data Swap" in 0x21[7] swap Even port and Odd port data when output double-width pixel enable, and determine output to Even port or Odd port in output single-width pixel mode.

"Display Red/Blue Data Swap" in 0x21[6] can swap red-channel data and blue-channel data. Set "Bit-Mapping Table Select" in 0xC2[0] 0 for 8bit LVDS output interface and 1 for 6bit LVDS output interface.

TTL interface

For 8bit TTL output interface, set 2'b10 to "Display Port Configuration" in TCON 0x03[7:6], 1'b0 to "Display 18 bit RGB Mode Enable" in 0x20[4]. "Display Output Double-Width Pixel Enable" in 0x20[2] determines one pixel or two pixels output per display clock. "Display Even/Odd Data Swap" in 0x21[7] swaps A port and B port data when output double-width pixel enable, and determine output to A port or B port in output single-width pixel mode. "Display Red/Blue Data Swap" in 0x21[6] can swap red-channel data and blue-channel data. "Display MSB/LSB Data Swap" in 0x21[5] can swap bit order between "bit7, 6, 5, 4, 3, 2, 1, 0" and "bit0, 1, 2, 3, 4, 5, 6, 7".

"TTL Display B port Blue [1:0] Location" in TCON register 0x04[4] select where B port

Blue[1:0] output to. If Blue[1:0] output to pin 52&53, RTD must work on serial port access mode. If Blue[1:0] output to pin 46&47, ADC_DDC must be disabled.

For 6bit TTL output interface, LSB 2bit of TTL 8bit output is not necessary, and it is used as TCON signal.

TCON

Due to the limitation of pin count, TCON shares pins with other signals. Refer to "Display & TCON / Video-8 Port" in the pin definition for TCON configuration. The configuration is in TCON Control Register.

4.12 Display Clock

DPLL

DPLL frequency = F_IN * DPM / DPN * Divider.

F_IN is input crystal frequency. DPM and DPN is in 0xD1[7:0] and 0xD2[3:0]. Divider is in 0xD2[7:6], and it divide PLL frequency by 1, 2, 4 or 8.

According to parameter DPN, you must set LPF Mode in 0xD3[2]. If LPF Mode is 1, the charge pump current, Ich, must be DPM/17.6, while Ich must be DPM/1.67 if LPF Mode is 0. The charge pump current Ich is in 0xD0[0,7:3].

Offset Frequency

The resolution of DPLL frequency from DPM and DPN factor might be not fine enough. Setting DCLK Offset[11:0] can fine tune DPLL close to target frequency.

Employing spread spectrum can fine tune DPLL frequency. "Enable DDS Spread Spectrum Output Enable" in register 0x5A[3] allows DDS to output spread spectrum control signal, and "DPLL Spread Spectrum Enable" in 0xD2[5] allows DPLL to receive control signal. "Offset Frequency Direction Induced by Spread Spectrum" in 0xD2[4] controls the direction of offset frequency. "DCLK Offset[11:0]" in 0x9A and 0x9B[3:0] determines the magnitude of offset frequency. Every step of offset frequency is DCLK*2^(-15).

In interlaced mode, odd field and even field have different period. Setting 0x9B[6] and 0x9B[4] can enable offset frequency function only in even filed or odd field.

Spread Spectrum

Spread spectrum can distribute the radiation energy to a band and reduce EMI. "DCLK Spreading Range" in 0x99[7:4] control spread spectrum range of 0~7.5% (peak-to-peak). "Spread Spectrum FMDIV" in 0x99[3] control spreading frequency 33k or 66kHz.

Fixed the Number of DCLK in a Frame

"Enable the Fixed DVTOTAL & Last Line Length" in 0x5A[4] makes there are fixed DVTOTAL and Last Line Length in every frame. Fixed Last Line Length[10:0] is in 0x59 and

0x5A[2:0], and DVTOTAL[10:0] is in register 0x97 and 0x98[2:0]. Output frame is synchronized with input frame by selecting higher-frequency DCLK and lower-frequency DCLK – N*dF according to the position of Display VS leading edge. N is controlled in register 0x99[1:0] and dF is DCLK*2^(-15).

Registers Description

Reading unimplemented registers will return 0.

Address: 00 ID_REG **Default: 81h**

Bit	Mode	Function
7:0	R	**MSB 4 bits:** 1000 product code **LSB 4 bits:** 0001 rev. code

Address: 01 STATUS (Status Register) **Default: 00h**

Bit	Mode	Function
7	R	**ADC_PLL Non-Lock:** If the ADC_PLL non-lock occurs, this bit is set to “1”.
6	R	**Input VSYNC Error** If the input vertical sync occurs within the programmed active period, this bit is set to “1”.
5	R	**Input HSYNC Error** If the input horizontal sync occurs within the programmed active period, this bit is set to “1”.
4	R	**Input ODD Toggle Occur** If the ODD signal(from SAV/EAV) toggle occurs, this bit is set to “1”.
3	R	**Video-8 Input Vertical Sync Occurs** If the YUV input vertical sync edge occurs, this bit is set to “1”.
2	R	**ADC Input Vertical Sync Occurs** If the RGB input vertical sync edge occurs, this bit is set to “1”.
1	R	**Input Overflow Status** (Frame Sync Mode) If an overflow in the input data capture buffer occurs, this bit is set to “1”.
0	R	**Line Buffer Underflow status** (Frame Sync Mode) If an underflow in the line-buffer occurs, this bit is set to “1”.

Write to clear status.

Address: 02 HOSTCTRL Default: 02h

Bit	Mode	Function
7	R	**Display Support** 0: XGA (RTD2513/2013) 1: SXGA (RTD2523/2023)
6:5	---	**Reserved**
4	R/W	**SOG_Mode** 0: DC-offset, using POLY R 1: DC-offset, using MOS R
3	---	**Reserved**
2	R/W	**Power Down Mode Enable** 0: Normal 1: Enable power down mode
1	R/W	**Power Saving Mode Enable** (except sync processor & serial port): 0: Normal 1: Enable power saving mode
0	R/W	**Reset Whole Chip** (Low pulse at least 8ms): 0: Normal 1: Enable reset

Address: 03 IRQ_CTRL0 (IRQ Control Register 0) Default: 00h

Bit	Mode	Function
7	R/W	**IRQ (ADC_PLL Non-Lock)** 0: Disable the ADC_PLL non-lock error event as an interrupt source 1: Enable the ADC_PLL non-lock error event as an interrupt source
6	R/W	**IRQ (Input VSYNC Error)** 0: Disable the Input VSYNC error event as an interrupt source 1: Enable the Input VSYNC error event as an interrupt source
5	R/W	**IRQ (Input HSYNC Error)** 0: Disable the Input HSYNC error event as an interrupt source 1: Enable the Input HSYNC error event as an interrupt source
4	R/W	**IRQ (Input ODD Toggle Occur)** 0: Disable the Input ODD toggle event as an interrupt source 1: Enable the Input ODD toggle event as an interrupt source
3	R/W	**IRQ (Video-8 Input Vertical Sync Occurs)** 0: Disable the B-port (VGB) Input VSync event as an interrupt source 1: Enable the B-port (VGB) Input VSync event as an interrupt source
2	R/W	**IRQ (ADC Input Vertical Sync Occurs)** 0: Disable the A-port (VGA) Input VSync event as an interrupt source 1: Enable the A-port (VGA) Input VSync event as an interrupt source
1	R/W	**IRQ (Input Overflow Status)** 0: Disable the Input Buffer overflow event as an interrupt source 1: Enable the Input Buffer overflow event as an interrupt source
0	R/W	**IRQ (Line Buffer Underflow status)** 0: Disable the Line Buffer underflow event as an interrupt source 1: Enable the Line Buffer underflow event as an interrupt source

Input Video Capture

a. Capture Format

Address: 04 VGIP_CTRL (Video Graphic Input Control Register) Default: 00h

Bit	Mode	Function
7	R/W	**Vertical Scale-Down Compensation** 0: disable 1: enable
6	R/W	**Horizontal Scale-Down Compensation** 0: disable 1: enable
5	R/W	**Input Test Mode:** 0: Normal 1: Video8 input will go through RGB channel, AVS=>IVS, AHS=>IHS, VCLK=>ICLK
4:2	R/W	**Input Pixel Format** 000: From Embedded ADC 001: Reserved 010: Low Speed Input (<60MHz) from Embedded ADC 011: Video-8 from B port (8bits) 100: From Embedded TMDS 101: Reserved 110: Low Speed Input (<60MHz) from Embedded TMDS 111: Reserved
1	R/W	**Input graphic/video mode** 0: From analog input (input captured by 'Input Capture Window') 1: From digital input (captured start by 'enable signal', but sill stored in 'capture window size')
0	R/W	**Input Video Run Enable** 0: No data is transferred 1: Sampling input pixels

Address: 05 VGIP_SIGINV (Input Control Signal Inverted Register) Default: 00h

Bit	Mode	Function
7	R/W	**IVS Sync with IHS Control** 0: Enable 1: Disable
6	R/W	**Input HS Measured Source Select** 0: A/B/C port HS 1: HS_RAW/SOG
5	R/W	**Input CSYNC (HS_RAW or SOG) Inverted Enable** 0: Disable 1: Enable
4	R/W	**Input Video ODD signal invert enable (from EAV)** 0: Not inverted (ODD = positive polarity) 1: Inverted (ODD = negative polarity)
3	R/W	**Input VS Signal Polarity Inverted** 0: Not inverted (VS = positive polarity) 1: Inverted (VS = negative polarity)
2	R/W	**Input HS Signal Polarity Inverted** 0: Not inverted (HS = positive polarity) 1: Inverted (HS = negative polarity)
1	R/W	**Input ENA Signal Polarity Inverted** 0: Not inverted (input high active) 1: Inverted (while input low active)
0	R/W	**Input Clock Polarity** 0: Rising edge latched 1: Falling edge latched

b. Input Frame Window

Address: 06 IPH_ACT_STAL (Input Horizontal Active Start Low)

Bit	Mode	Function
7:0	R/W	Input Video Horizontal Active Start -- Low Byte [7:0]

Address: 07 IPH_ACT_STAH (Input Horizontal Active Start)

Bit	Mode	Function
2:0	R/W	Input Video Horizontal Active Start -- High Byte [10:8]

The number of pixel clocks from the leading edge of HS to the first pixel of the active line.
IPH_ACT_STA must bigger than 2.

Address: 08 IPH_ACT_WIDL (Input Horizontal Active Width Low)

Bit	Mode	Function
7:0	R/W	Input Video Horizontal Active Width -- Low Byte [7:0]

Address: 09 IPH_ACT_WIDH (Input Horizontal Active Width High)

Bit	Mode	Function
2:0	R/W	Input Video Horizontal Active Width – High Byte [10:8]

This register defines the number of active pixel clocks to be captured.
(Horizontal Active Start + Horizontal Active Width) < 2047
This capture width must be increments of four.

Address: 0A IPV_ACT_STAL (Input Vertical Active Start Low)

Bit	Mode	Function
7:0	R/W	Input Video Vertical Active Start – Low Byte [7:0]

Address: 0B IPV_ACT_STAH (Input Vertical Active Start High)

Bit	Mode	Function
2:0	R/W	Input Video Vertical Active Start – High Byte [10:8]

The number of lines from the leading edge of selected input video VSYNC to the first line of the active window.

Address: 0C IPV_ACT_LENL (Input Vertical Active Lines)

Bit	Mode	Function
7:0	R/W	Input Video Vertical Active Lines – Low Byte [7:0]

Address: 0D IPV_ACT_LENH (Input Vertical Active Lines)

Bit	Mode	Function
2:0	R/W	Input Video Vertical Active Lines – High Byte [10:8]

This register defines the number of active lines to be captured.

Address: 0E IRQ_CTRL1 (IRQ Control Register 1) Default: xxxx_xx00b

Bit	Mode	Function
7	R	This bit set to '1' indicates that the read before display SRAM is not ready
6:2	---	**Reserved.**
1	R/W	**Internal IRQ Enable:** 0: Disable these interrupt. 1: Enable these interrupt. The DDC & Status0 IRQ enable will be logically "ORed" together.
0	---	**Reserved**

Embedded ADC Test Mode

Address: 0F PTNPOS_LO

Bit	Mode	Function
7:0	R/W	**Test Pattern Position Register** [7:0] Assign the test pattern digitized position in pixel.

Address: 10 PTNPOS_HI Default: 00xx_xxxxb

Bit	Mode	Function
7	R/W	**TEST (Enable Test Function)** 0: Disable 1: Enable, and clear to 0 after latch completed
6	R/W	**ADC Test Output Enable** 0: Disable 1: ADC test data output to ADCOUT [7:0] & ADC_CLK output to BCLK
5:3	R/W	**Select Color Output To ADC_Test [7:0]** 00x: B color 01x: G color 10x: R color 110: Signals (IVS, Coast, IHS, HS_out, IENA , SOG_in, Clamp, IFD_ODD) (MSB—LSB) 111: Signals (IVS, Coast, IHS, HS_out, Phase Error , SOG_in, FAV4, MSB2 signal) (MSB—LSB)
2:0	R/W	**Test Pattern Position Register**[10:8] Assign the test pattern digitized position in pixel.

Use PTNPOS to assign the pixel position after HSYNC leading edge that input signal digitized. Each time the PTNPOS is written, the digitized results will be loaded into PTNRD, PTNGD and PTNBD. For test issue, make the input signal a fixed pattern before PTNPOS is written. Then the same digitized output will be got.

Address: 11 PTNRD

Bit	Mode	Function
7:0	R	Red Channel Test Pattern Digitized Result.

The test pattern digitized result after HSYNC leading edge about PTNPOS pixel.

Address: 12 PTNGD

Bit	Mode	Function
7:0	R	Green Channel Test Pattern Digitized Result.

Address: 13 PTNBD

Bit	Mode	Function
7:0	R	Blue Channel Test Pattern Digitized Result.

Address: 14 INTERNAL FIELD DETECTION Default: 00h

Bit	Mode	Function
7:5	----	**Reserved**
4	R/W	**Video mode compensation:** 0: disable 1: enable
3	R/W	**Internal ODD-signal inverse for FS_Delay_Fine_Tuning** 0: No invert 1: Invert
2	R/W	**ODD to Control FS_Delay_Fine_Tuning** 0: Disable 1: Enable (FS_Delay_Fine_Tuning must set enable)
1	R/W	**Internal ODD-signal inverse for video-compensation** 0: No invert 1: invert
0	R/W	**Internal ODD signal selection** 0: ODD signal (from EAV) 1: Internal Field Detection ODD signal (Also support under DVI input)

Scaling Up Function

Address: 15 SCALE_CTRL (Scale Control Register) Default: 00h

Bit	Mode	Function
7:6	R/W	**Fine Tune Delay of coefficient SRAM Access**
5:4	R/W	**Vertical Filter Effect:** 00: Filter 1 01: Filter 2 10: Filter 3 11: Filter 4
3:2	R/W	**Horizontal Filter Effect:** 00: Filter 1 01: Filter 2 10: Filter 3 11: Filter 4
1	R/W	**Enable the Vertical Filter Function:** 0: By pass the vertical filter function block 1: Enable the vertical filter function block
0	R/W	**Enable the Horizontal Filter Function:** 0: By pass the horizontal filter function block 1: Enable the horizontal filter function block

Address: 16 HOR_SCA_M (Horizontal Scale Factor Medium)

Bit	Mode	Function
7:0	R/W	Bit [11:4] of horizontal scale factor

Address: 17 HOR_SCA_H (Horizontal Scale Factor High)

Bit	Mode	Function
7:0	R/W	Bit [19:12] of horizontal scale factor

This horizontal scale factor includes a 20-bit fraction part to present a horizontal scaled up size over the stream input. For example, for 800-pixel original picture scaled up to 1024-pixel, the factor should be filled in as follows:
(800/1024) x 2^20 = 0.78125 x 2^20 = 819200 = C8000h = C8h, 00h, 0h.

Address: 18 VER_SCA_M (Vertical Scale Factor Low)

Bit	Mode	Function
7:0	R/W	Bit [11:4] of vertical scale factor

Address: 19 VER_SCA_H (Vertical Scale Factor High)

Bit	Mode	Function
7:0	R/W	Bit [19:12] of vertical scale factor

This vertical scale factor includes a 20-bit fraction part to present a vertical scaled up size over the stream input. For example, for 600-line original picture scaled up to 768-line, the factor should be filled in as follows:
(600/768) x 2^20 = 0.78125 x 2^20 = 819200 = C8000h = C8h, 00h, 0h.

Address: 1A HV_SCA_L (Horizontal/Vertical Scale Factor Low) Default: xx00xx00b

Bit	Mode	Function
7:6	R/W	Bit [3:2] of horizontal scale factor
5:4	R/W	Scale Up Horzontial Latch Delay Fine Tune
3:2	R/W	Bit [3:2] of vertical scale factor
1:0	R/W	Scale Up Vertical Latch Delay Fine Tune

Address: 1B FILTER_CTRL0 (Filter Control Register 1) Default: C4h

Bit	Mode	Function
7:2	R/W	**Horizontal filter coefficient initial value**; default: 110001
1	R/W	**Enable user defined vertical filter coefficient table** 0: disable 1: enable
0	R/W	**Enable user defined horizontal filter coefficient table** 0: disable 1: enable

Address: 1C FILTER_CTRL1 (Filter Control Register 2) Default: C4h

Bit	Mode	Function
7:2	R/W	**Vertical filter coefficient initial value**; default: 110001
1	R/W	**Select User Defined Filter Coefficient Table for Access Channel** 0: Horizontal 1: Vertical
0	R/W	**Enable Filter Coefficient Access** 0: disable 1: enable the access channels

Address: 1D FILTER_PORT (User Defined Filter Access Port)

Bit	Mode	Function
7:0	W	Access port for user defined filter coefficient table

When enable filter coefficient accessing, the first write byte is stored into the LSB(bit[7:0]) of coefficient #1 and the second byte is into MSB (bit[8:11]). Therefore, the valid write sequence for this table is c0-LSB, c0-MSB, c1-LSB, c1-MSB, c2-LSB, c2-MSB … c63-LSB & c63-MSB, totally 64 * 2 cycles. Since the 128 taps is symmetric, we need to fill the 64-coefficient sequence into table only.

Address: 1E FS_DELAY_FINE_TUNING (Frame Sync Delay Fine Tuning) Default: 00h

Bit	Mode	Function
7:0	R/W	Frame Sync Mode Delay Fine Tune, “00” to disable

In Frame Sync Mode #1, this register [7:0] represents output VS delay fine-tuning. For example, it delays the number of (this register[7:0] * 16 + 16) input clocks.

Address: 1F STATUS1 (Status1 Register)

Bit	Mode	Function
7	R	**Line Buffer Overflow Status** 1: Line Buffer overflow has occurred since the last status read
6	R	**Line Buffer Underflow Status** 1: Line Buffer underflow has occurred since the last status read
5	R	**OENA Stop Event Status** 1: If the OENA stop event occurred since the last status read
4	R	**OENA Start Event Status** 1: If the OENA start event occurred since the last status read
3	R	**OVS Start Event Status** 1: If the OVS start event occurred since the last status read
2	R	**IENA Stop Event Status** 1: If the IENA stop event occurred since the last status read
1	R	**IENA Start Event Status** 1: If the IENA start event occurred since the last status read
0	R	**IVS Start Event Status** 1: If the IVS start event occurred since the last status read

Write to clear status.

Display Format

Address: 20 VDIS_CTRL (Video Display Control Register) Default: 00h

Bit	Mode	Function
7	R/W	**DHS Output Format Select (only available in Frame Sync #1)** 0: The first DHS after DVS is active 1: The first DHS after DVS is inactive
6	R/W	**Display Data Output Inverse Enable** 0: Disable 1: Enable (only when data bus clamp to 0)
5	R/W	**Display Output Force to Background Color** 0: Display output operates normally 1: Zoom Filter output is forced to the color as selected by background color
4	R/W	**Display 18 bit RGB Mode Enable** 0: All individual output pixels are full 24-bit RGB 1: All individual output pixels are rounded to 18-bit RGB
3	R/W	**Frame Sync Mode Enable** 0: Free running mode 1: Frame sync mode
2	R/W	**Display Output Double-Width Pixel Enable** 0: Single width pixels are output to the display with every DCLK cycle 1: Double width pixels are output to the display with every DCLK cycle
1	R/W	**Display Output Run Enable** 0: DHS, DVS, DEN & data bus are clamped to "0" 1: Display output normal operation.
0	R/W	**Display Video Timing Run Enable** 0: Display Timing Generator is halted, Zoom Filter halted 1: Display Timing Generator and Zoom Filter enabled to run normally

Step to disable output: First set CR20_1=0, set CR20_6 & inverse control, then set CR20_0=0 to disable output.

Address: 21 VDIS_SIGINV (Display Control Signal Inverted) Default: 00h

Bit	Mode	Function
7	R/W	**Display Even/Odd Data Swap:** 0: Disable 1: Enable
6	R/W	**Display Red/Blue Data Swap** 0: Disable 1: Enable
5	R/W	**Display MSB/LSB Data Swap** 0: Disable 1: Enable
4	R/W	**Skew Data Output** 0: Non-skew data output 1: Skew data output
3	R/W	**Display Vertical Sync (DVS) Output Invert Enable:** 0: Display Vertical Sync output normal active high logic 1: Display Vertical Sync output inverted logic
2	R/W	**Display Horizontal Sync (DHS) Output Invert Enable:** 0: Display Horizontal Sync output normal active high logic 1: Display Horizontal Sync output inverted logic
1	R/W	**Display Data Enable (DEN) Output Invert Enable:** 0: Display Data Enable output normal active high logic 1: Display Data Enable output inverted logic
0	R/W	**TMDS_TEST 34 Data Output** 0: Disable 1: Enable (only when TTL mode, 24 bit output)

Address: 22 DH_TOTAL (Display Horizontal Total Pixels)

Bit	Mode	Function
7:0	R/W	**Display Horizontal Total Pixel Clocks:** Low Byte[7:0]

Address: 23 DH_TOTAL (Display Horizontal Total Pixels)

Bit	Mode	Function
7:3	R/W	**Frame Sync Mode Fine Tune:** Reference 0x31[4] setting
2:0	R/W	**Display Horizontal Total Pixel Clocks**: High Byte[10:8]

Determines the number of DCLK cycles in each display line minus 2. (DHS leading edge to DHS leading edge)
//**DH_Total (Reg[22],Reg[23], Reg[23]-bit7:3).爲了安全起見, Reg[22] 的値在 Reg[23]寫入後才能寫入** //

Address: 24 DH_HS_END (Display Horizontal Sync End)

Bit	Mode	Function
7:0	R/W	**Display Horizontal Sync End:** Determines the width of DHS pulse in DCLK cycles

Address: 25 DH_BKGD_STA (Display Horizontal Background Start)

Bit	Mode	Function
7:0	R/W	**Display Horizontal Background Start**: Low Byte [7:0]

Address: 26 DH_BKGD_STA (Display Horizontal Background Start)

Bit	Mode	Function
7:3	R	The Width Bit [4:0] of Last Line Before Sync in Frame Sync Mode 1
2:0	R/W	**Display Horizontal Background Start**: High Byte [10:8]

Determines the number of DCLK cycles from leading edge of DHS to first pixel of Background region.

Address: 27 DH_ACT_STA (Display Horizontal Active Start)

Bit	Mode	Function
7:0	R/W	**Display Horizontal Active Region Start**: Low Byte [7:0]

Address: 28 DH_ACT_STA (Display Horizontal Active Start)

Bit	Mode	Function
2:0	R/W	**Display Horizontal Active Region Start**: High Byte [10:8]

Determines the number of DCLK cycles from leading edge of DHS to first pixel of Active region.

Address: 29 DH_ACT_END (Display Horizontal Active End)

Bit	Mode	Function
7:0	R/W	**Display Horizontal Active Width**: Low Byte [7:0]

Address: 2A DH_ACT_END (Display Horizontal Active End)

Bit	Mode	Function
2:0	R/W	**Display Horizontal Active Width**: High Byte [10:8]

Determines the number of DCLK cycles from leading edge of DHS to the pixel of background region.

Address: 2B DH_BKGD_END (Display Horizontal Background End)

Bit	Mode	Function
7:0	R/W	**Display Horizontal Background end**: Low Byte [7:0]

Address: 2C DH_BKGD_END (Display Horizontal Background End)

Bit	Mode	Function
7:3	R	The Width Bit [9:5] of Last Line Before Sync in Frame Sync Mode 1
2:0	R/W	**Display Horizontal Background end**: High Byte [10:8]

Determines the number of DCLK cycles from leading edge of DHS to the start of horizontal blanking. REG_2C[7:3] &REG_26[7:3] indicates the width (counted by two pixel) of last line before VSYNC in frame sync mode 1.

Address: 2D DV_TOTAL (Display Vertical Total Lines)

Bit	Mode	Function
7:0	R/W	**Display Vertical Total:** Low Byte [7:0]

Address: 2E DV_TOTAL (Display Vertical Total Lines)

Bit	Mode	Function
7:3	R/W	**Reserved**
2:0	R/W	**Display Vertical Total**: High Byte [10:8]

In framesync mode, when the line number of Display HS is equal to Display Vertical Total, a status CR3D_7 is set.
In FreeRun mode, Display Vertical Total is assigned in {0x98[2:0], 0x97[7:0]}.

Address: 2F DV_VS_END (Display Vertical Sync End)

Bit	Mode	Function
7:0	R/W	**Display Vertical Sync End:** Determines the duration of DVS pulse in lines

Address: 30 DV_BKGD_STA (Display Vertical Background Start)

Bit	Mode	Function
7:0	R/W	**Display Vertical Background Start:** Low Byte [7:0]

Address: 31 DV_BKGD_STA (Display Vertical Background Start) Default: 00000xxxb

Bit	Mode	Function
7	R/W	Auto switch when the line number of Display HS is equal to Display Vertical Total 0: Disable 1: Enable
6	R/W	Auto switch to (for timing) 0: Disable 1: Free Run
5	R/W	Auto switch to (for data) 0: Disable 1: Background
4	R/W	Fine Tune Delay Mode Select 0: 0/32 -- 2/32 -- 4/32 -- 6 /32 ~~~ 62/32 1: 0/32 -- 4/32 -- 8/32 --12/32 ~~~ 124/32
3	R	Reserved
2:0	R/W	**Display Vertical Background Start:** High Byte [10:8]

Determines the number of lines from leading edge of DVS to first line of background region.

Address: 32 DV_ACT_STA (Display Vertical Active Start)

Bit	Mode	Function
7:0	R/W	**Display Vertical Active Region Start:** Low Byte [7:0]

Address: 33 DV_ACT_STA (Display Vertical Active Start) Default: 000000xxxb

Bit	Mode	Function
~~7~~	~~R/W~~	~~Auto switch when auto fine tune delay function over max. /min. margin.~~ ~~0: Disable~~ ~~1: Enable~~
~~6~~	~~R/W~~	~~IRQ Enable~~ ~~0: Disable auto fine tune delay function over margin occurs as an interrupt source~~ ~~1: Enable auto fine tune delay function over margin occurs as an interrupt source~~
~~5~~	~~R~~	~~Auto fine tune delay function over max. margin status.~~
~~4~~	~~R~~	~~Auto fine tune delay function over min. margin status.~~
3	R/W	DVS sync with x4 clock 0: Disable 1: Enable
2:0	R/W	**Display Vertical Active Region Start:** High Byte [10:8]

~~Write to clear status.~~
Determines the number of lines from leading edge of DVS to first line of active region.

Address: 34 DV_ACT_END (Display Vertical Active End)

Bit	Mode	Function
7:0	R/W	**Display Vertical Active Region End**: Low Byte [7:0]

Address: 35 DV_ACT_END (Display Vertical Active End)

Bit	Mode	Function
7:4	R	**Measure al Length Result**: Low Byte [3:0]
3	R/W	**Reserved**
2:0	R/W	**Display Vertical Active Region End:** High Byte [10:8]

Determines the number of lines from leading edge of DVS to the line of follow background region.

Address: 36 DV_BKGD_END (Display Vertical Background End)

Bit	Mode	Function
7:0	R/W	**Display Vertical Background end:** Low Byte [7:0]

Address: 37 DV_BKGD_END (Display Vertical Background End)

Bit	Mode	Function
2:0	R/W	**Display Vertical Background end:** High Byte [10:8]

Determines the number of lines from leading edge of DVS to the line of start of vertical blanking.

Address: 38 IV_DV_LINES (IVS to DVS Lines)

Bit	Mode	Function
7:0	R/W	**IVS to DVS Lines:** (Only for FrameSync Mode) The number of input HS from input VS to output VS.

YUV-to-RGB Control

Address: 39 YUV2RGB (YUV to RGB Control Register) Default: 00h

Bit	Mode	Function
7	R/W	SRGB Enable
6	R/W	**YUV-to-RGB Conversion Mode Selection:** 0: YUV422 1: YUV444
5	R/W	**Enable YUV to RGB Conversion:** 0: Disable YVB-to-RGB conversion 1: Enable YUV-to-RGB conversion
4	R/W	SRGB SRAM Control
3:2	R/W	SRGB Coefficient Write Enable 00: Disable 01: R port 10: G port 11: B port
1:0	R/W	U/VROM data latch clock fine tune 01=>10=>00=>11(from fastest to slowest) 00: defalut, each stage=>~0.25ns

Address: 3A DIS_TIMING (Display Clock Fine Tuning Register) Default: 00h

Bit	Mode	Function
7	R/W	**YUV-to-RGB Color Space Conversion Test Mode:** 0: Normal 1: Direct output conversion result to display port
6	R/W	**Internal OSD Port Latch Clock Delay** 0: normal 1: 1ns delay
5	R/W	**Force Display Timing Generator Enable:** 0: wait for input VS trigger 1: force enable
4	---	Reserved
3	R/W	**Display Output Clock Coarse Tuning Control:** 0: Disable 1: 8ns delay
2:0	R/W	**Display Output Clock Fine Tuning Control:** 000: DCLK rising edge correspondents with output display data 001: 1ns delay 010: 2ns delay 011: 3ns delay 100: 4ns delay 101: 5ns delay 110: 6ns delay 111: 7ns delay

Address: 3B DIS_TIMING (Display Clock Fine Tuning Register) Default: 00h

Bit	Mode	Function
7	---	**Reserved**
6	R/W	**PLL_TEST1 input crystal clock (reference to table2. test-pin pair setting)** 0: Disable 1: Enable
5:4	R/W	**DPLL Output Select** 00: Select the internal PLL clock source as DPLL output (PWM0 output to REFCLK) 01: Select the external REFCLK clock source as DPLL output 10: Select the internal PLL clock source as DPLL & REFCLK output 11: Select the internal PLL clock source as DPLL output (Video odd/even from EAV output to

		REFCLK)
3	R/W	**DCLK Polarity Inverted** 0: Non-Inverted 1: Inverted
2	R/W	**DCLK Output Enable** 0: Disable 1: Enable
1	R/W	**DCLK (on REFCLK pin) Polarity Inverted** 0: Non-Inverted 1: Inverted
0	R/W	**DCLK (on REFCLK pin) Enable** 0: Disable 1: Enable

Address: 3C PE_CTRL **Default: 00h**

Bit	Mode	Function
7	R/W	**DDS Tracking Edge** 0: HS positive edge 1: HS negative edge
6	R/W	**PE Measure Enable** 0: Disable 1: Enable PE Measurement, clear after finish.
~~5~~	~~R/W~~	~~**FCROM Static Pull-High Control**~~ ~~0: Disable~~ ~~1: Enable~~
4:0	R	**PE Value**

Address: 3D Status **Default: 00h**

Bit	Mode	Function
7	R	The line number of Display HS is equal to Display Vertical Total, this bit is set to “1”. Write to clear status.
6	W	**PE Max. Measure Clear** 0: clear after finish 1: write ‘1’ to clear PE Max. Value
5	R/W	**PE Max. Measure Enable** 0: Disable 1: Enable PE Max. Measurement
4:0	R	**PE Max Value**

Address: 3E DUTY_FINE_TUNE

Bit	Mode	Function
7:4	R/W	**Internal Display Clock (IDCLK) Duty Fine-tune:** (3F_bit1 to enable) 1111 (min fine-tune) à 1110 à 1100 à 1000 à 0000 (max fine-tune)
3:0	R/W	**Color Processing Clock (CPCLK) Duty Fine-tune:** (3F_bit2 to enable) 1111 (min fine-tune) à 1110 à 1100 à 1000 à 0000 (max fine-tune)

Address: 3F DUTY_FINE_TUNE_CTRL Default:00h

Bit	Mode	Function
7	R/W	**RSDS data latch Inverted** 0: Non-Inverted 1: Inverted
6:4	R/W	**RSDS data latch Delay** 000: 0ns delay 001: 0.5ns delay 010: 1ns delay 011: 1.5ns delay 100: 2ns delay 101: 2.5ns delay 110: 3ns delay 111: 3.5ns delay
3	R/W	**Internal Display Clock (IDCLK) Delay Enable:** 0: Disable. 1: Enable IDCLK delay.
2	R/W	**Color Processing Clock (CPCLK) Duty Fine-tune Enable:** 0: Disable. 1: Enable CPCLK duty fine-tune (setting in 3E_bit3:0)
1	R/W	**Internal Display Clock (IDCLK) Duty Fine-tune Enable:** 0: Disable. 1: Enable IDCLK duty fine-tuner (setting in 3E_bit7:4)
0	R/W	**Internal Display Clock (IDCLK) Invert.** 0: Disable 1: IDCLK invert enable.

FIFO Display Window

Address: 40 DRWL_BSU (Display Read Pixel Low Byte Before Scaling-Up)

Bit	Mode	Function
7:0	R/W	**Display window read width before scaling up:** Low Byte [7:0]

Address: 41 DRWH_BSU (Display Read Pixel High Byte Before Scaling-Up)

Bit	Mode	Function
2:0	R/W	**Display window read width before scaling up:** High Byte [10:8]

Address: 42 DRLL_BSU (Display Read Length Low Byte Before Scaling-Up)

Bit	Mode	Function
7:0	R/W	**Display window read length before scaling up:** Low Byte [7:0]

Address: 43 DRLH_BSU (Display Read Length High Byte Before Scaling-Up)

Bit	Mode	Function
2:0	R/W	**Display window read length before scaling up:** High Byte [10:8]

Address: 44 sRGB

Bit	Mode	Function
7:0	W	When R-port coefficient: RG0, RB0, RG1, RB1, …RG31, RB31, When G-port coefficient: GR0, GB0, GR1, GB1, …GR31, GB31, When B-port coefficient: BR0, BG0, BR1, BG1, …BR31, BG31 total 64 bytes (2's complement : -128~127)

Address: 45 sRGB R-Offset

Bit	Mode	Function
5:0	R/W	(2's complement : -32~31)

Address: 46 sRGB G-Offset

Bit	Mode	Function
5:0	R/W	(2's complement : -32~31)

Address: 47 sRGB B-Offset

Bit	Mode	Function
5:0	R/W	(2's complement : -32~31)

R' = Rin[7:0] + R-Offset
G' = Gin[7:0] + G-Offset
B' = Bin[7:0] + B-Offset

Rout = R'[7:0] + GR(G'[7:3]) + BR(B'[7:3])
Gout = RG(R'[7:3]) + G'[7:0] + BG(B'[7:3])
Bout = RB(R'[7:3]) + GB(G'[7:3]) + B'[7:0]

Address: 48 EVENT_STATUS_CONTROL Default: 00h

Bit	Mode	Function
7	R/W	**Enable Vertical Line Compare Function** 0: Disable 1: Enable
6	R/W	**Gating Vertical Line Compare Function to IRQ**
5	R	**Vertical Line Compare Status (for Polling).** Write to clear
4	R/W	**Select Compare Source:** 0: Input Side 1: Display Side
3	--	**Reserved**

2:0	R/W	**Select Vertical Line –Low Byte [2:0]**

Address: 49 EVENT_LOCATION Default: 00h

Bit	Mode	Function
7:0	R/W	**Select Vertical Line --High Byte [11:3]**

SYNC Processor

Address: 4A SYNC_CTRL **Default: 00h**

Bit	Mode	Function
7	R/W	**IRQ Enable** 0: Disable input sync signal edge occurs as an interrupt source 1: Enable input sync signal edge occurs as an interrupt source
6	R	**SOG Edge Occurs** If the SOG edge occurs, this bit is set to "1".
5	R	**ADC Input Horizontal Sync Occurs (HS_RAW)** If the ADC input horizontal sync edge occurs, this bit is set to "1".
4	R	**Video-8 Input Horizontal Sync Occurs** If the Video-8 input horizontal sync edge occurs, this bit is set to "1".
3	R/W	**Reserved to 0** ~~**Measure VSYNC select**~~ ~~0: The VSYNC chosen by 0x4A [1:0]~~ ~~1: The VSYNC from de-composite~~
2	R/W	**Measure VSYNC Timing Delay 2 clock** 0: disable 1: enable
1:0	R/W	**Measure HSYNC/VSYNC Source Select:** 00: RTD300x/RTD20xx original configuration 01: HS_RAW / AVS 10: Video-8 HSYNC / Video-8 VSYNC 11: TMDS HSYNC / TMDS VSYNC

Write to clear status.

Address: 4B SYNC_CTRL (SYNC Control Register) **Default: 00h**

Bit	Mode	Function
7	R/W	**COAST Signal Invert Enable:** 0: not inverted 1: inverted
6	R/W	**COAST Signal Output Enable:** 0: disable; 1: enable;
5	R/W	**HS_OUT Signal Invert Enable:** 0: not inverted 1: inverted
4	R/W	**HS_OUT Signal Output Enable:** 0: disable; 1: enable;
3	R/W	**CLAMP Signal Invert Enable:** 0: not inverted 1: inverted
2	R/W	**CLAMP Signal Output Enable:** 0: Disable; 1: Enable
1	R/W	**Sync-On-Green Enable:** 0: Disable; 1: Enable (set "1" to Sync-Mode-Select at the same time)
0	R/W	**Sync Mode Select:** 0: Separate H & V; 1: Composite Sync from HSYNC or Green

Address: 4C SYNC_POR (H & V SYNC Polarity Measured Result) **Default: 00h**

Bit	Mode	Function

7	R/W	**Safe Mode** 0: Normal 1: Safe Mode Enable, mask 1 of 2 IVS.
6	R/W	**Sync Processor Test Mode** 0: Normal 1: Enable Test Mode; (switch 70ns-ck to the time-out & polarity counters)
5	R/W	**Select HS_OUT Source Signal** 0: Bypass HS_RAW 1: Select De-Composite HS out (In Composite mode)
3	R	**Input VSYNC Polarity Indicator** 0: negative polarity (high period is longer than low one) 1: positive polarity (low period is longer than high one)
2	R	**Input HSYNC Polarity Indicator** 0: negative polarity (high period is longer than low one) 1: positive polarity (low period is longer than high one)
1	R/W	**Start a HS & VS period / H & V resolution & polarity measurement** 0: disable to start a measurement 1: enable to start a measurement, cleared after finished
0	R/W	**HSYNC & VSYNC Measured Mode** 0: HS period counted by crystal clock & VS period counted by HS 1: H resolution counted by input clock & V resolution counted by ENA (Get the correct resolution which is triggered by enable signal, ENA)

Address: 4D MEAS_HS_PER (HSYNC Period Measured Result)

Bit	Mode	Function
7:0	R	**Input HSYNC Period Measurement Result:** Low Byte[7:0]

Address: 4E MEAS_HS_PER (HSYNC Period Measured Result) Default: 8'bx000xxxx

Bit	Mode	Function
7	R	**Input HSYNC Period Measurement Result:** Over-flow bit 1: Over-flow occurred
6	R/W	**ODD invert for ODD-Controlled-IVS_delay.** 0: Disable 1: Invert
5	R/W	**ODD-Controlled-IVS_delay Enable** 0: Disable 1: Enable
4	R/W	**Input HSYNC Synchronize Edge** 0: Input HSYNC is synchronized by the positive edge of the input clock 1: Input HSYNC is synchronized by the negative edge of the input clock
3:0	R	**Input HSYNC Period Measurement Result:** High Byte[11:8]

This result is expressed in terms of crystal clocks. When measured digitally, the result is expressed as the number of input clocks between 2 input HS signals divided by 2.

Address: 4F MEAS_VS_PER (VSYNC Period Measured Result)

Bit	Mode	Function
7:0	R	**Input VSYNC Period Measurement Result:** Low Byte[7:0]

Address: 50 MEAS_VS_PER (VSYNC Period Measured Result)

Bit	Mode	Function
7	R	**Input VSYNC Period Measurement Result:** Over-flow bit 1: Over-flow occurred
6	R	**Internal Field Detection ODD toggle happen**
5:4	R	**The number of input HS between 2 input VS**. LSB bit [1:0]
3	---	Reserved
2:0	R	**Input VSYNC Period Measurement Result:** High Byte[10:8]

This result is expressed in terms of input HS pulses. When measured digitally, the result is expressed as the number of input enable signal within a frame.

Address: 51 MEAS_HS_HI (HSYNC High Period Measured Result)

Bit	Mode	Function
7:0	R	**Input HSYNC Period Measurement Result:** Low Byte[7:0]

Address: 52 MEAS_HS_HI (HSYNC High Period Measured Result) Default: 8'b00xx_xxxx

Bit	Mode	Function
7	R/W	**HS Recovery in Coast** 0: Disable 1: Enable (can turn on when CS or SOG)
6	R/W	**HSYNC Synchronize source** 0: Input HS 1: Feedback HS
3:0	R	**Input HSYNC Period Measurement Result:** High Byte[11:8]

This result is expressed in terms of crystal clocks. When measured digitally, the result is expressed as the number of input clocks inside the input enable signal divided by 2.

Address: 53 MEAS_VS_HI (VSYNC High Period Measured Result)

Bit	Mode	Function
7:0	R	**Input VSYNC Period Measurement Result:** Low Byte[7:0]

Address: 54 MEAS_VS_HI (VSYNC High Period Measured Result) Default: 8'bxxx00xxx

Bit	Mode	Function
7	R	6-iclk-delay HS level latched by VS rising edge

6	R	HS level latched by VS rising edge
5	R	HS level latched by 6-iclk-delay VS rising edge
4	R/W	**Feedback HSYNC Synchronize Edge** 0: Feedback HSYNC is synchronized by the positive edge of the input clock 1: Feedback HSYNC is synchronized by the negative edge of the input clock
3	R/W	**VSYNC Synchronize Edge** 0: latch VS by the positive edge of input HSYNC 1: latch VS by the negative edge of input HSYNC
2:0	R	**Input VSYNC Period Measurement Result:** High Byte[10:8]

This result is expressed in terms of input HS pulses

Clamping Signal Control

Address: 55 CLAMP_START (Clamp Signal Output Start)

Bit	Mode	Function
7:0	R/W	**Start of Output Clamp Signal Pulse:** Determine the number of input double-pixel between the trailing edge of input HSYNC and the start of the output CLAMP signal.

Address: 56 CLAMP_END (Clamp Signal Output End)

Bit	Mode	Function
7:0	R/W	**End of Output Clamp Signal Pulse:** Determine the number of input double-pixel between the trailing edge of input HSYNC and the end of the output CLAMP signal.

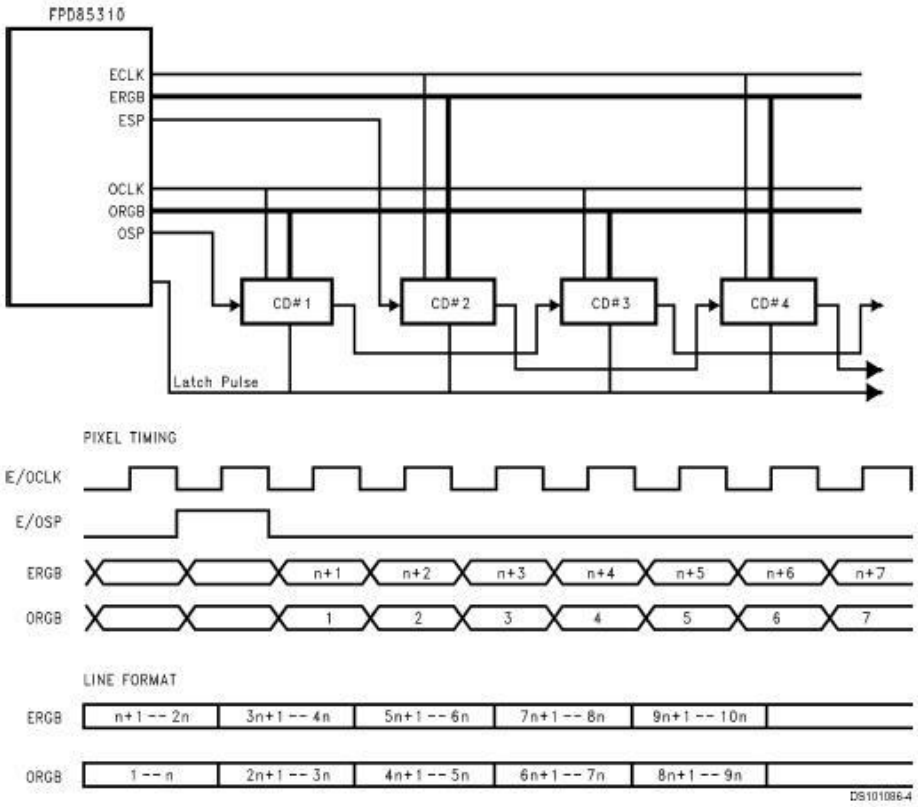
Display Data Bus Control (For RSDS type-3)

Address: 57 Display Data Bus Interleaving Line Buffer Length Low Byte Default: 00h

Bit	Mode	Function
7:0	R/W	**Interleaving Line Buffer Line Bufer:** Low Byte [7:0]

Address: 58 Display Data Bus Interleaving Line Buffer Length High Byte Default: 00h

Bit	Mode	Function
2	R/W	**Display Data Bus Interleaving Enable** 0: Disable 1: Enable
~~1:0~~	~~R/W~~	~~**Interleaving Line Buffer Line Bufer:** High Byte [9:8]~~



Note 7: Programmable CD Size "n" (up to 128)
Note 8: One or both clocks can be used
Note 9: Unused clocks can be turned off
Note 10: E/OCLK polarity is programmable

FIGURE 10. Dual Bus Single Port Column Driver Interface
(Non-skewed outputs)

Fixed Last Line Length

Address: 59 FX_LST_LN_LNGTH_LSB

Bit	Mode	Function
7:0	R/W	**Fixed Last Line Length [7:0]**

Address: 5A FX_LST_LN_LNGTH_MSB **Default: 0000_0xxxb**

Bit	Mode	Function
7	R/W	**New Dithering** 0: Disable 1: Enable
6	R/W	**RSDS_TET_EN** 0: Disable 1: Enable
5	R/W	**SSCG_TST_EN Test Enable** 0: Disable 1: Enable(SDMOUT[3:0] will be pass to V8_DATA[3:0])
4	R/W	**Enable the Fixed DVTOTAL & Last Line Length Function** 0: Disable 1: Enable
3	R/W	**Enable DDS Spread Spectrum Output Function** 0: Disable 1: Enable
2:0	R/W	**Fixed Last Line Length** [10:8]

Anti-Flicker Control

Address: 5B Pixel Threshold Value for Smart Polarity (TH1) Default: 00h

Bit	Mode	Function
7:0	R/W	**2 line Sum of Difference Threshold Value: bit [7:0]**

Address: 5C Line Threshold Value for Smart Polarity (TH2) Default: 0x000000b

Bit	Mode	Function
7	R/W	**Measure Dot Pattern over Threshold (depend on 0x00[1])** 1: run. /* Auto: always measure Manual: start to measure, clear after finish */ 0: stop
6	R	**Dot Pattern Sum of Difference Measure Result** 1: over threshold 0: under threshold
5	R/W	**TCON [7] Polarity one / two Line Toggle Control** 1: Auto /* If sum of difference under threshold, TCON [7] will auto switch to “normal ” output. If sum of difference over threshold, TCON [7] will auto switch to “original setting” output */. 0: Manual
4:0	R/W	**Over Difference Line Threshold Value: bit [4:0]**

動作說明	
0x5C[7] & 0x5C[5]	
‘1’ & ‘1’	**自動 anti-flicker**
‘1’ & ‘0’	**透過 manual 方式,當 0x5C[7]設爲’1’,便會自動執行一個 frame,做完後 0x5C[7] clear 成’0’**
‘0’ & ‘x’	**沒動作**

Color Processor Control

Address: 5D COLOR_CTRL (Color Control Register) Default: 00h

Bit	Mode	Function
7	R/W	**Dithering Frame Modulation Vertical Enable** 0: disable 1: enable
6	R/W	**Dithering Frame Modulation Horizontal Enable** 0: disable 1: enable
5	R/W	**Enable Access Channel for Dithering Table:** 0: disable this channel 1: enable this channel (address should not auto increase)
4	R/W	**Enable Access Channels for Gamma Correction Coefficient:** 0: disable these channels 1: enable these channels (address should not auto increase)
3	R/W	**Enable Dithering Function:** 0: disable the dithering function 1: enable the dithering function
2	R/W	**Enable Look-Up Table for Gamma Correction Coefficient:** 0: disable the look-up table 1: enable the look-up table coefficient
1	R/W	**Enable Contrast Control Coefficient:** 0: disable the coefficient 1: enable the coefficient
0	R/W	**Enable Brightness Control Coefficient:** 0: disable the coefficient

		1: enable the coefficient

Brightness Coefficient:

Address: 5E BRI_R_COE (Brightness Red Coefficient)

Bit	Mode	Function
7:0	W	**Brightness Red Coefficient:** Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 5F BRI_G_COE (Brightness Green Coefficient)

Bit	Mode	Function
7:0	W	**Brightness Green Coefficient: Valid range:** -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 60 BRI_B_COE (Brightness Blue Coefficient)

Bit	Mode	Function
7:0	W	**Brightness Blue Coefficient:** Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Contrast Coefficient:

Address: 61 CTS_R_COE (Contrast Red Coefficient)

Bit	Mode	Function
7:0	W	**Contrast Red Coefficient:** Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 62 CTS_G_COE (Contrast Green Coefficient)

Bit	Mode	Function
7:0	W	**Contrast Green Coefficient:** Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 63 CTS_B_COE (Contrast Blue Coefficient)

Bit	Mode	Function
7:0	W	**Contrast Blue Coefficient:** Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Gamma Correction :

Address: 64 RED_GAMMA_PORT (Red Gamma Table Access Port)

Bit	Mode	Function
7:0	W	**Access port for red gamma correction table**

Address: 65 GRN_GAMMA_PORT (Green Gamma Table Access Port)

Bit	Mode	Function
7:0	W	**Access port for green gamma correction table**

Address: 66 BLU_GAMMA_PORT (Blue Gamma Table Access Port)

Bit	Mode	Function
7:0	W	**Access port for blue gamma correction table**

When enable gamma correction table accessing, total size of coefficient table is 256 bytes for each color respectively. And the input data sequence is c0, c1, c2, … c255.

Dithering Coefficient:

Address: 67 DITHER_PORT (Dithering Table Access Port)

Bit	Mode	Function
7:0	W	**Access port for dithering table**

Old dithering(0x5A[7] = 0): When enable dithering table accessing, total size of coefficient table is 16 * 4 bits for RGB color. And the input data sequence is {c1, c0}, {c3, c2}, … {c15, c14}.

C0	C1	C2	C3
C4	C5	C6	C7
C8	C9	C10	C11
C12	C13	C14	C15

New dithering(0x5A[7] = 1): One dithering sequence table contains 32element, s0, s1, … , s31. Each element has 2bit to index one of 4 dithering table. Input data sequence is {s3,s2,s1,s0}, {s7,s6,s5,s4}, … , {s31,s30,s29,s28}. R + (2R+1) * C choose sequence element, where R is Row Number / 2, and C is Column Number / 2.

4 dithering table, 0,1,2,3, is

C0	C1
C4	C5

C2	C3
C6	C7

C8	C9
C12	C13

C10	C11
C14	C15

Cyclic-Redundant-Check

Address: 68 OP_CRC_CTRL (Output CRC Control Register) Default: FCh

Bit	Mode	Function
7:2	R/W	**SRAM Control //111111 (F, I, A, M, G, C)** F (bit 7): four-line SRAM I (bit 6): input SRAM A (bit 5): OSD attribute SRAM M (bit 4): OSD font map SRAM G (bit 3): Gamma, Dithering table SRAM C (bit 2): filter coefficient SRAM
1	R/W	**Enable Full Line buffer:** 0: Disable 1: Enable
0	R/W	**Output CRC Control:** 0: Stop or finish (Auto-stop after checked a completed display frame) 1: Start

CRC function = X^24 + X^7 + X^2 + X + 1.

Address: 69 OP_CRC_BYTE_0 (Output CRC Checksum Byte 0)

Bit	Mode	Function
7:0	R	Output CRC-24 bit 7~0

Address: 6A OP _CRC_BYTE_1 (Output CRC Checksum Byte 1)

Bit	Mode	Function
7:0	R	Output CRC-24 bit 15~8

Address: 6B OP _CRC_BYTE_2 (Output CRC Checksum Byte 2)

Bit	Mode	Function
7:0	R	Output CRC-24 bit 23~16

Background color control

Address: 6C Background color control

Bit	Mode	Function
7:0	R/W	**Background color RGB 8-bit value**

There are 3 bytes color select of background R, G, B, and the writing and reading is selected by 0x6D[7:6].

Overlay Control

Address: 6D OVL_CTRL (Overlay Display Control Register) Default: 00h

Bit	Mode	Function
7:6	R/W	**Background color select (select the writing and reading byte of 0x6c)** 00: Red 01: Green 10: Blue 11: X
5:3	R/W	**Alpha blending level 00:Disable, 001 ~111: 1/8~ 7/8**
2	---	Reserved
1	R/W	**Overlay Sampling Mode Select:** 0: dual pixels per clock 1: single pixel per clock
0	R/W	**Overlay Port Enable:** 0: Disable 1: Enable

Address: 6E OVL_LUT_ADDR (Overlay LUT Address) Default: 00h

Bit	Mode	Function
7	R/W	**Enable Overlay Color Plate Access:** 0: Disable 1: Enable
6	---	Reserved
5:0	R/W	**Overlay 16x24 Look-Up-Table Write Address [5:0]**

Auto-increment while every accessing “Overlay LUT Access Port”.

Address: 6F OVL_LUT_PORT (Overlay LUT Access Port)

Bit	Mode	Function
7:0	W	**Overlay 16x24 Look-Up-Table access port [7:0]**

Using this port to access overlay color plate which addressing by the above registers.
The writing sequence into LUT is {R0, G0, B0, R1, G1, B1, … R15, G15, and B15} and the address counter will be automatic increment and circular from 0 to 47.

Scale Down Control

Address: 70 SCALE_DOWN_CTRL (Scale Down Control Register) Default: 00h

Bit	Mode	Function
7	R/W	**Video 8 Port Input Latch Bus MSB to LSB Swap Control:** 0: normal 1: Switched Video8 port MSB to LSB sequence into LSB to MSB
6	R/W	Default='0'. When set to '1', vertical scale down is disable in scale down mode
5	R/W	**Internal ENA (I_ENA) Delay Control:** 0: normal; 1: 2ns delay;
4	R/W	**Internal VS (I_VS) Delay Control:** 0: normal; 1: 2ns delay;
3	R/W	**Internal HS (I_HS) Delay Control:** 0: normal; 1: 2ns delay;
2:1	R/W	**Input Clock Delay Control:** 00: Normal 01: 1ns delay 10: 2ns delay 11: 3ns delay
0	R/W	**Scale down function enable:** 0: disable scale down function 1: enable scale down function

Address: 71 H_SCALE_DL (Horizontal scale down factor register)

Bit	Mode	Function
7:0	R/W	**Horizontal Scale Down Factor:** Low Byte [7:0]

Address: 72 H_SCALE_DH (Horizontal scale down factor register)

Bit	Mode	Function
7:0	R/W	**Horizontal Scale Down Factor:** High Byte [15:8]

Registers { H_SCALE_DH, H_SCALE_DL} = (Xi / Xm) x (2^12) truncate. If not truncate, fill minus 1.
Meanwhile, Xi = horizontal input width; Xm = horizontal memory write width

Address: 73 V_SCALE_DL (Vertical scale down factor register)

Bit	Mode	Function
7:0	R/W	**Vertical Scale Down Factor:** Low Byte [7:0]

Address: 74 V_SCALE_DH (Vertical scale down factor register)

Bit	Mode	Function
7:0	R/W	**Vertical Scale Down Factor:** High Byte [15:8]

Registers { V_SCALE_DH, V_SCALE_DL} = (Yi / Ym) x (2^12) truncate. If not truncate, fill minus 1
Meanwhile, Yi = vertical input width; Ym = vertical memory write width

Image Auto Function

Address: 75 H_BOUNDARY_STA_L

Bit	Mode	Function
7:0	R/W	**Horizontal Boundary Start:** Low Byte [7:0]

Address: 76 H_BOUNDARY_END_L

Bit	Mode	Function
7:0	R/W	**Horizontal Boundary End:** Low Byte [7:0]

Address: 77 H_BOUNDARY_HIGH **Default: 8'b0xxx_xxxx**

Bit	Mode	Function
7	R/W	**Field_Select_Enable:** Auto-Function only active when Even or Odd field. 0: Disable 1: Enable
6:4	R/W	**Horizontal Boundary Start:** High Byte [10:8] //11-bit=2048
3:0	R/W	**Horizontal Boundary End:** High Byte [11:8] //12-bit=4096

Address: 78 V_BOUNDARY_STA_L

Bit	Mode	Function
7:0	R/W	**Vertical Boundary Start:** Low Byte [7:0] //(Invalid when Vertical Auto-Boundary)

Address: 79 V_BOUNDARY_END_L

Bit	Mode	Function
7:0	R/W	**Vertical Boundary End:** Low Byte [7:0] //(Invalid when Vertical Auto-Boundary)

Address: 7A V_BOUNDARY_HIGH **Default: 8'b0xxx_xxxx**

Bit	Mode	Function
7	R/W	**Field_Select:** Select Even or Odd field. Active when **Field_Select_Enable**. 0: Active when ODD signal is "0" 1: Active when ODD signal is "1"
6:4	R/W	**Vertical Boundary Start:** High Byte [10:8] //11-bit //(Invalid when Vertical Auto-Boundary)
3:0	R/W	**Vertical Boundary End:** High Byte [11:8] //12-bit //(Invalid when Vertical Auto-Boundary)

Address: 7B RED_NOISE_MARGIN (Red Noise Margin Register) **Default: 8'bxxxxxx00**

Bit	Mode	Function
7:2	R/W	**Red pixel noise margin setting register**
1	R/W	Even or Odd pixel be measured 0: Even 1: Odd
0	R/W	Measure only Even or Odd pixel enable 0: Disable 1: Enable

Address: 7C GRN_NOISE_MARGIN (Green Noise Margin Register) **Default: 8'bxxxxxx00**

Bit	Mode	Function
7:2	R/W	**Green pixel noise margin setting register**
1:0	R/W	**Vertical boundary search:** 00: 1 pixel over threshold; 01: 2 pixel over threshold 10: 4 pixel over threshold; 11: 8 pixel over threshold

Address: 7D BLU_NOISE_MARGIN (Blue Noise Margin Register) **Default: 8'bxxxxxx00**

Bit	Mode	Function
7:2	R/W	**Blue pixel noise margin setting register**
1:0	R/W	**Color Source Select for Detection:** 00: B color 01: G color 10: R color

Address: 7E DIFF_THRESHOLD

Bit	Mode	Function
7:0	R/W	**Difference Threshold**

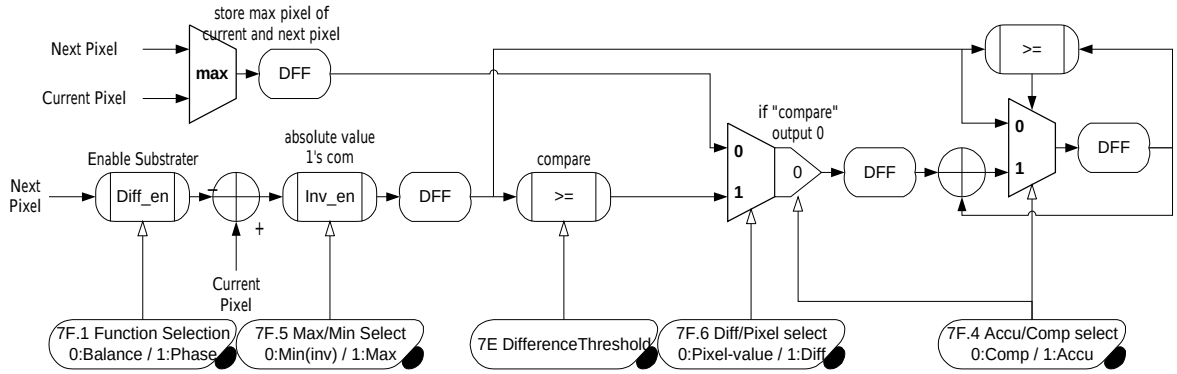


Figure 14 Auto-Tracking Control Block

Address: 7F AUTO_ADJ_CTRL (Auto adjustment control register) Default: 00h

Bit	Mode	Function
7	R/W	**Measure Digital Enable Info when boundary search active** 0: Normal Boundary Search 1: Digital Enable Info Boundary Search. (The vertical & horizontal, start & end information of external digital signal can be obtained from CR80~87).
6	R/W	**Accumulation Type** 0: Type1 1: Type2
5	R/W	**Color Max or Min Measured Select:** 0: MIN color measured (Only when Balance-Mode, result must be complemented) 1: MAX color measured
4	R/W	**Accumulation or Compare Mode** 0: Compare Mode 1: Accumulation Mode
3:2	R/W	Mode Selection (00 is forbidden) 01: Mode1 10: Mode2 11: Mode3
1	R/W	**Function (Phase/Balance) Selection** 0: Auto-Balance 1: Auto-Phase
0	R/W	**Start Auto-Function Tracking Function:** 0: stop or finished 1: start

Control Table/ Function	Sub-Function	7F.6	7F.5	7F.4	7F.3	7F.2	7F.1	7E
Auto-Balance	**Max pixel**	X	1	0	0	X	0	X
	Min pixel	X	0	0	0	X	0	X
Auto-Phase Type1	**Mode1**	0	1	1	0	1	1	Th
	Mode2	0	1	1	1	0	1	Th
	Mode3	0	1	1	1	1	1	Th
Auto-Phase Type2	**Mode1**	1	1	1	0	1	1	Th
	Mode2	1	1	1	1	0	1	Th
	Mode3	1	1	1	1	1	1	Th
Accumulation	**All pixel**	1	1	1	0	1	0	0

Table 1 Auto-Tracking Control Table

Address: 80 VER_START_L (Active region vertical start Register)

Bit	Mode	Function

7:0	R	**Active region vertical start measurement result:** bit[7:0]

Address: 81 VER_START_H (Active region vertical start Register)

Bit	Mode	Function
3:0	R	**Active region vertical start measurement result:** bit[11:8]

Address: 82 VER_END_L (Active region vertical end Register)

Bit	Mode	Function
7:0	R	**Active region vertical end measurement result:** bit[7:0]

Address: 83 VER_END_H (Active region vertical end Register)

Bit	Mode	Function
3:0	R	**Active region vertical end measurement result:** bit[11:8]

Address: 84 HOR_START_L (Active region horizontal start Register)

Bit	Mode	Function
7:0	R	**Active region horizontal start measurement result:** bit[7:0]

Address: 85 HOR_START_H (Active region horizontal start Register)

Bit	Mode	Function
3:0	R	**Active region horizontal start measurement result:** bit[11:8]

Address: 86 HOR_END_L (Active region horizontal end Register)

Bit	Mode	Function
7:0	R	**Active region horizontal end measurement result:** bit[7:0]

Address: 87 HOR_END_H (Active region horizontal end Register)

Bit	Mode	Function
3:0	R	**Active region horizontal end measurement result:** bit[11:8]

Address: 88 AUTO_PHASE_0 (Auto phase result byte0 register)

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[7:0] / The measured value of R or G or B color max or min. (Auto-Balance)

Address: 89 AUTO_PHASE_1 (Auto phase result byte1 register)

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[15:8]

Address: 8A AUTO_PHASE_2 (Auto phase result byte2 register)

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[23:16]

Address: 8B AUTO_PHASE_3 (Auto phase result byte3 register)

Bit	Mode	Function
7:0	R	**Auto phase measurement result:** bit[31:24]

Address: 8C IVS_DELAY (Internal Input-VS Delay Control Register) Default: 00h

Bit	Mode	Function
7:0	R/W	Input VS delay count by Input HS to reset input data

Address: 8D IHS_DELAY (Internal Input-HS Delay Control Register) Default: 00h

Bit	Mode	Function
7:0	R/W	Input HS delay count by Input clock

Address: 8E ODD_CTRL (ODD Source Control Register) Default: 00h

Bit	Mode	Function
7	R	SAV/EAV two-bit error
6	R	SAV/EAV one-bit error
5	R/W	Auto switch when ADC-PLL non-lock 0: Disable 1: Enable
4	R/W	Auto switch when overflow or underflow

		0: Disable 1: Enable
3	R/W	**Decode Video-8 when ADC or TMDS active** 0: Disable 1: Enable
2	R/W	Input Auto Toggle (TEST) Enable: 0: Disable 1: Enable (DCLK feed to ICLK) (Only works in Video8 port single pixel mode, ~~R & B~~ toggle by ICLK rate, ~~but G toggle by ICLK2 rate~~)
1	R/W	**EAV Error Correction Enable in video8** 0: Disable 1: Enable
0	R/W	**8-bit Random Generator** 0: Disable 1: Enable

~~In video8 input format, the bit1 should be the complement of remainder of SAV location clock count/2.~~

Address: 8F FCLK (Scale Down Clcok) Fine Tune Default: 00h

Bit	Mode	Function
7:3	--	Reserved
3	R/W	Select VGIP clock 0: Reference clock 1: DDCSCL
2	R/W	Select source of FCLK 0: original setting (default) 1: select ADC_CLK without combinational logic delay
1:0	R/W	0x8F[1] & 0x8F[0] FCLK fine tune 01: slowest 00: typical 1x: fastest

Embedded OSD

Address: 90 OSD_ADDR_MSB (OSD Address MSB 8-bit)

Bit	Mode	Function
7:0	R/W	OSD MSB 8-bit address

Address: 91 OSD _ADDR_LSB (OSD Address LSB 8-bit)

Bit	Mode	Function
7:0	R/W	OSD LSB 8-bit address

Address: 92 OSD_DATA_PORT (OSD Data Port)

Bit	Mode	Function
7:0	W	Data port for embedded OSD access

Refer to the embedded OSD application note for the detailed.

Address: 93 OSD_TEST **Default: 00h**

Bit	Mode	Function
7:0	R/W	**Testing Pattern**

Address: 94 OSD_SCRAMBLE **Default: 00h**

Bit	Mode	Function
7	R/W	**BIST Start** 0: stop 1: start (auto clear)
6	R/W	**BIST Result** 0: fail 1: success

Embedded Timing Controller

Address: 95 TCON_ADDR _PORT Default: 00h

Bit	Mode	Function
7:0	**R/W**	Address port for embedded TCON access

Address: 96 TCON_DATA _PORT

Bit	Mode	Function
7:0	**R/W**	Data port for embedded TCON access

DCLK Spread Spectrum

Address: 97 FIXED_LAST_LINE_MODE_DVTOTAL_LSB

Bit	Mode	Function
7:0	**R/W**	Fixed Last Line Mode DVTOTAL [7:0]

Address: 98 FIXED_LAST_LINE_MODE_DVTOTAL_MSB

Bit	Mode	Function
2:0	**R/W**	Fixed Last Line Mode DVTOTAL [10:8]

In FreeRun mode, Display Vertical Total is assigned in {0x98[2:0], 0x97[7:0]}.

Address: 99 SPREAD_SPECTRUM Default: 00h

Bit	Mode	Function
7:4	R/W	DCLK Spreading range (0.0~7.5%) 0000: 0.0% 0001: 0.5% 0010: 1.0% 0011: 1.5% 0100: 2.0% 0101: 2.5% 0110: 3.0% 0111: 3.5% 1000: 4.0% 1001: 4.5% 1010: 5.0% 1011: 5.5% 1100: 6.0% 1101: 6.5% 1110: 7.0% 1111: 7.5%
3	R/W	Reserved to 0 ~~Spread Spectrum FMDIV (SSP_FMDIV)//(0)~~ ~~0: 33K~~ ~~1: 66K~~
2	R/W	Reserved
1:0	R/W	Frequency Synthesis Select (F & F-N*dF) 00~11: N=1~4

df = dclk* 2^(-15)

Address: 9A DCLK_FINE_TUNE_OFFSET_ LSB Default: 00h

Bit	Mode	Function
7:0	**R/W**	**DCLK Offset [7:0] in Fixed DVTOTAL & Last Line Length Mode**

Address: 9B DCLK_FINE_TUNE_OFFSET_ MSB Default: 00h

Bit	Mode	Function

7	---	**Reserved**
6	**R/W**	**Only Even / Odd Field Mode Enable** 0: Disable 1: Enable
5	**R/W**	**Spread Spectrum Setting Ready for Writing** (Auto Clear) 0: Not ready 1: Ready to write
4	**R/W**	**Even / Odd Field Select** 0: Even 1: Odd
3:0	**R/W**	**DCLK Offset [11:8] in Fixed DVTOTAL & Last Line Length Mode**

The "Spread Spectrum Setting Ready for Writing" (0x9B [5]) means 4 kinds of registers will be set after this bit is set: 1. Spreading range (0x99 [7:4]) 2. Spreading FMDIV (0x99 [3]) 3. DCLK offset setting (0x9A, 0x9B[3:0]) 4. Frequency synthesis select (0x99 [1:0])

Hardware Enhanced Auto Function

Address: 9E HARDWARE_AUTO_PHASE Default: 00h

Bit	Mode	Function
7	**R**	**HS_ACT_FLAG**
2	**R/W**	**Hardware / Software Auto Phase Switch** 0: Software 1: Hardware
1:0	**R/W**	**Hardware Auto Phase Step** 00: Step =1 01: Step =2 10: Step =4 11: Step =8

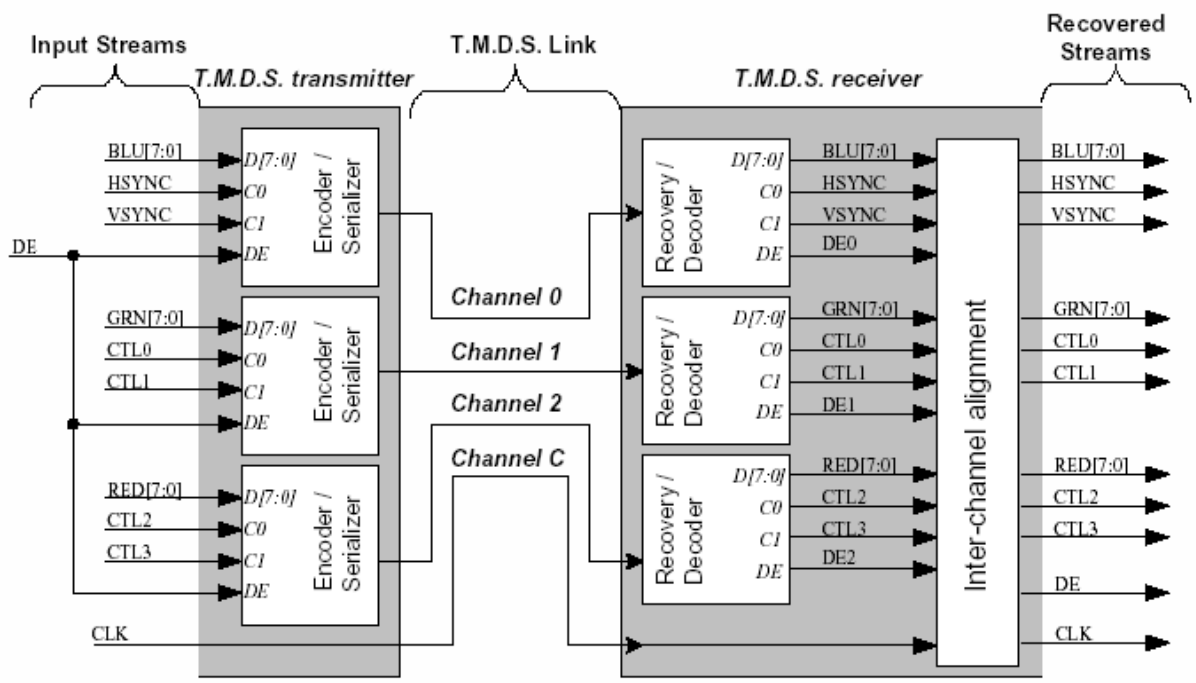
When hardware auto phase enabled, if the 0x7F [0] is set, then the procedure will start. Every frame the 0x89, 0x8A, 0x8B will be updated by auto-increased phase; the phase will be initially 0 and auto-increased by step setting. The Micron have to read 0x89~8B every frame to get the information.

Address: 9F PLLPHASE (Select Phase to A/D) Default: 00h

Bit	Mode	Function
7	R/W	**X control**
6:3	R/W	**16 phases pre-select**
2:1	R/W	**Reserved to 00** ~~**Phase shift**~~ ~~00: Original phase selected by X, Y, and 16-phase pre-select~~ ~~01~11: Add 1~3 phase to the Original phase selected by X, Y, and 16-phase pre-select~~
0	R/W	**Y control**

Phase	[X ^^^^ Y]	Phase	[X ^^^^ Y]	Phase	[X ^^^^ Y]	Phase	[X ^^^^ Y]
0	[1 0000 1]	**32**	[0 1000 1]	**64**	[1 0000 0]	**96**	[0 1000 0]
4	[1 0001 1]	**36**	[0 1001 1]	**68**	[1 0001 0]	**100**	[0 1001 0]
8	[1 0010 1]	**40**	[0 1010 1]	**72**	[1 0010 0]	**104**	[0 1010 0]
12	[1 0011 1]	**44**	[0 1011 1]	**76**	[1 0011 0]	**108**	[0 1011 0]
16	[1 0100 1]	**48**	[0 1100 1]	**80**	[1 0100 0]	**112**	[0 1100 0]
20	[0 0101 1]	**52**	[1 1101 0]	**84**	[1 0101 0]	**116**	[1 1101 1]
24	[0 0110 1]	**56**	[1 1110 0]	**88**	[0 0110 0]	**120**	[1 1110 1]
28	[0 0111 1]	**60**	[1 1111 0]	**92**	[0 0111 0]	**124**	[1 1111 1]

Embedded TMDS



Address A0: Output Port Enable **Default: 6Fh**

Bit	Mode	Function
7	R/W	Power down TMDS whole function High: Normal Run Low: Power Down
6:5	R/W	**TMDS_TEST 34 Data Output Select (30 bit over-sampled data, DEN, HS, VS, CLK)** 00: Blue channel 01: Green channel 10: Red channel 11: Disable
4	R/W	**TMDS_TEST 3 DE Output Select** 0: Disable 1: 3 channel DE output with CLK (HS, VS be replaced by DE1, DE2)
3	R/W	Output control by auto function High: Auto output, Low: Manual.
2:0	R/W	Bit 0: Enable Blue output port. Bit 1: Enable Green output port Bit 2: Enable Red output port

Address A1: Input Port Enable **Default: EFh**

Bit	Mode	Function
7	R/W	Mcufirst High: disable DDC channel and MCU access only Low: enable DDC channel and MCU access only when DDC is not busy
6	R/W	Reserved
5	R/W	1: Original power up sequence, turn on R/G when DE low 128 clocks 0: Turn On R/G channel when DE low 128 clocks and VS rising and falling appears
4	R	Chbok: Detect Blue Channel DE low last 128 dclk High: Active, Low: Non-Active

3	R/W	Input control by auto function High: Auto enable, Low: Manual
2:0	R/W	Bit 0: Enable Blue input port. Bit 1: Enable Green input port Bit 2: Enable Red input port

Address A2: Analog Performance#1 **Default: 8Bh**

Bit	Mode	Function
7	R/W	WDmode: Select Watch Dog mode, Low: Analog, High: Digital.
6:5	R/W	00: Auto 10: Watch Dog Pin='1' x1: Watch Dog Pin='0'
4:3	R/W	sr[1:0]: The resistor of LPF in PLL.
2:0	R/W	si[2:0]: Charge pump current in PLL, Icp=si[2:0]*5u+5u.

Address A3: Analog Performance#2 **Default: 26h**

Bit	Mode	Function
7	R/W	anaWDen: Analog watch dog when ckonctrl =1, control pllckon High: Analog & Digital Low: Digital
6	R/W	ckon_manual: control pllckon when ckon_ctrl =0, Low: off, High: on.
5	R/W	ckonctrl: Low: Manual, High: Auto
4	R/W	z0pow: MCU must pull it up after power stable
3	R/W	down: When down=0, Z0 is auto set 50 ohm.
2:1	R/W	selTST[1:0]: Select the TSTout function of clock port & RD port.
0	R/W	~~ENTST: Enable clock port TSTout pin.~~ ~~0:Analog to TSTPAD (20k ohm to GND)~~ ~~1:Digital to TSTPAD (50 ohm to VDD)~~ ENTST::Enable TMDS test singal 0: Disable 1: Enable

TMDS power down: set A0[7] & A3[4] to 0
TMDS power save: set A0[7] to 0, A3[4] to 1

Address A4: Analog Performance#3 **Default: 35h**

Bit	Mode	Function
7:6		Read as "00"
5:4	R/W	selTST[1:0]: Select the TSTout pin of Z0_control.
3:0	R/W	When down=1, Z0 can be controlled by [3:0]

Address A5: Analog_Test_Output_Selection & Digital WD **Default: 9fh**

Bit	Mode	Function
7:6	R/W	selperd: Choose the freq stable time to turn on pllckon Perd Stable Time 00: 16us 32~48us 01: 64us 128~192us 10:256us 512~768us 11: 1ms 2~3ms
5:3	R/W	~~HZTST: Enable TMDS TSTout pin.~~ ~~0:Enable TSTOUTPAD~~ ~~1:High impedance~~ STSTPAD

		000:TMDS bias to TSTPAD 001:TMDS test singal to TSTPAD 010:D2P (PWM1) singal to TSTPAD 011:P2D (Reserved) singal from TSTPAD (power on latch to select parallel/serial port) 1xx:Force high impedance of TSTPAD
2:0	R/W	selTST[2:0]: Select the TSTout pin to PAD.

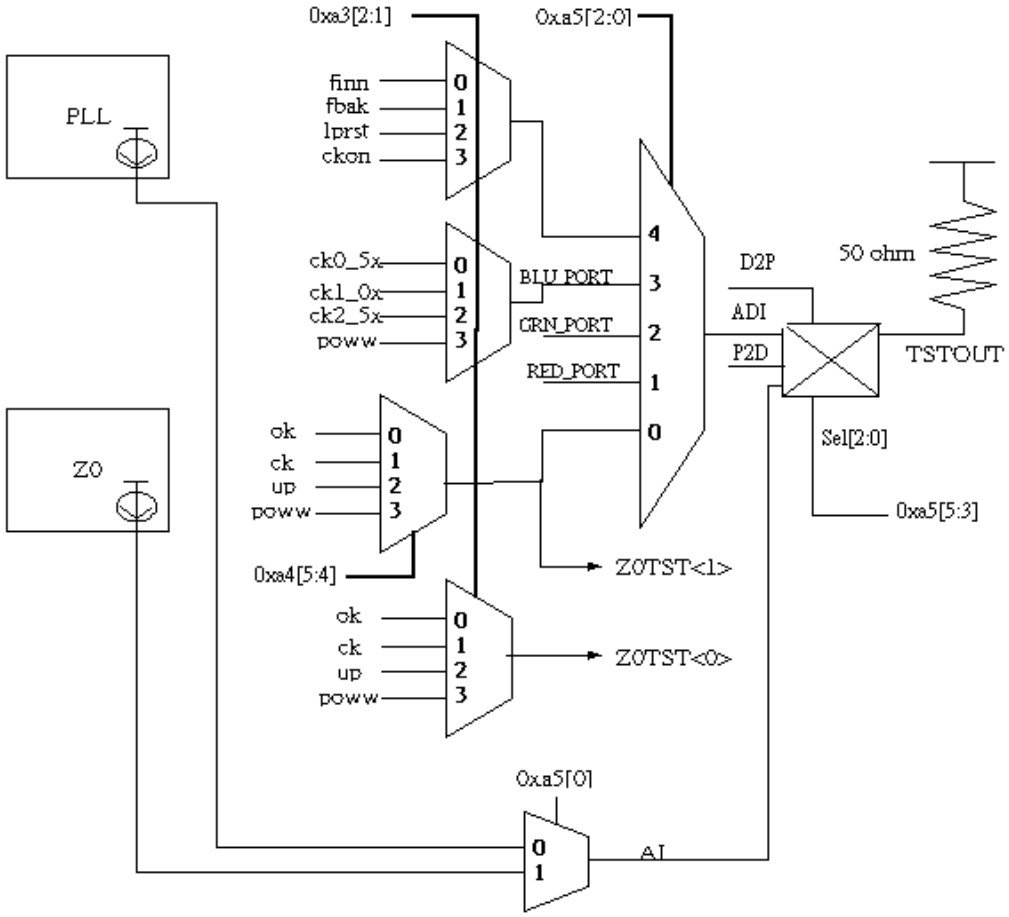


Figure 15 TSTOUT Pin Internal Configuration

Address A6: Control Register **Default: 08h**

Bit	Mode	Function
7	R/W	High: CRC check during the next full frame and clear reg. 0xA7~0xA9. Low: After start CRC
6	R	CRCdone High: When CRC done Low: When set 0xA6[7]
5	R/W	Indicate VSYNC Polarity Mode: High: manual, decided by 0xA6[0] Low: auto, indicate by 0xA6[4]
4	R	Indicate VSYNC Polarity High: Negative Low: Positive
3	R/W	Reserved to 0
2	R/W	Reserved
1	R/W	Always PRE-charge:

		High: Enable, Low: Disable
0	R/W	Reserved

Address A7: CRC Output Byte_0 **Default: XX**

Bit	Mode	Function
7:0	R	CRC output bit 7~0 Cleared when 0x04[2] is set.

Address A8: CRC Output Byte_1 **Default: XX**

Bit	Mode	Function
7:0	R	CRC output bit 15~8

Address A9: CRC Output Byte_2 **Default: XX**

Bit	Mode	Function
7:0	R	CRC output bit 23~16

Address AA: DB Test Mode **Default: 00h**

Bit	Mode	Function
7	R/W	Reserved to 0
6	R	Reserved
5	R/W	TMDS test output enable (only when ADC test output disable) High: TMDS test data output to VIDEO8 PAD Low: Disable
4	R/W	Shwp: show write pointer High: show wp at VIDEO8 [5:0] wp decided by wpsel[1:0] Low: other bits make decision
3	R/W	Shctl: High: bypass CTL3~0 to VIDEO8 [3:0] Low: VIDEO8[3:0]=[0000]
2	R/W	f25tst: After the rising edge first full cycle data and hold system when TI,TO,TCK active, data could be shift out by the order R30bit 0~29,R12bit 0~11,G,B; where 12bit and 30bit data decided by f25sel Z0TST<0>= VIDEO8 [2] Z0TST<1>= VIDEO8 [3] TCK2= AVS, decided by 0xAB[7] TO = VIDEO8 [5], TI = DDCSDA, TCK = DDCSCL,
1	R/W	shauth: High: show authst, authkm, authdone to VIDEO8[2:0] Low: VIDEO8[2:0]={000}
0	R/W	shclk: High: show crystal, fbakdiv5, findiv2, dclk (dclk/2) to VIDEO8[3:0] Low: VIDEO8[3:0]=[0000]

Address AB: DVI_REG_TEST **Default: 00h**

Bit	Mode	Function
7	R/W	tck_mode: High: TCK2 mode Low: Original
6:4	R/W	f25sel: Decision latched data of F2x5FIFOT: check 12bit 30bit 000 [11:0] lat0 29:0 001 [23:12] lat1 29:0 010 [47:36] lat3 59:30 011 [59:48] lat4 59:30 10x [29:24] lat2 29:0 11x [35:30] lat2 59:30

3	R/W	Reserved
2:1	R/W	wpsel: Display selection of write pointer of TMDS, 00: wp=6'h00, 01: wp of blue channel 10: wp of green channel 11: wp of red channel
0	R/W	dclkdiv: Low: out dclk when shwp=0,shck=1 to VIDEO8[0] High: dclk/2

Address AC: Pattern Comparator **Default: 90h**

Bit	Mode	Function
7	R/W	Calibration of FIFO write pointer after Vsync High: Enable calibration, Low: Disable
6	R/W	Calibration write pointer Vsync edge select High: Falling, Low: Rising
5	R/W	Hsync edge select after Vsync calibrate write pointer High: Falling, Low: Rising
4	R/W	Clock delay select after Hsync calibrate write pointer High: Enable delay 5 clock Low: Disable
3	R/W	Calibration of FIFO write pointer and boundary detection after falling DE High: Enable calibration, Low: Disable
2	R/W	pertst: High: start to do pixel error rate test wait for matched pattern Low: stop PERT and clear numerr and perten
1	R/W	pertmode: High: PN code PERT Low: Half clock PERT
0	R	perten: High: matched pattern found PERT(Pixel Error Rate Test) enable Low: clear by pertst reset

Address AD: Pixel Error Rate Low Byte **Default: 00h**

Bit	Mode	Function
7:0	R	Numerr low byte: Total count of pixel error

Address AE: Pixel Error Rate High Byte **Default: 00h**

Bit	Mode	Function
7:0	R	Numerr high byte: Total count of pixel error

Address AF: DVI_CTRL1 **Default: 00h**

Bit	Mode	Function
7	R/W	Reserved
6:4	R	If Red/Green/Blue FIFO overflow or underflow, These will set '1', clear '0' after read.
3	R/W	Reserved
2	R/W	OCLK divide 2: High: Enable Low: Disable
1:0	R/W	Reserved ~~F25CK Delay:~~ ~~00 : 2ns~~ ~~01 : 2.7ns~~ ~~10 : 3.7ns~~ ~~11 : 4.7ns~~ ~~delay clock 1x from analog~~

Address B0: TMDS CTL0~3 Signal Status **Default:30h**

Bit	Mode	Function
7:4	R/W	Reserved
3	R	TMDS internal CTL3 signal status
2	R	TMDS internal CTL2 signal status
1	R	TMDS internal CTL1 signal status
0	R	TMDS internal CTL0 signal status

Address B1: Reserved **Default: 00h**

Bit	Mode	Function
7:0	R/W	Reserved

Address B2: Device Key BIST Pattern

Bit	Mode	Function
7	R/W	Reserved
6:0	W	BIST Pattern Input

Address B3: TMDS_TEST_MODE_1 **Default: 00h**

Bit	Mode	Function
7:6	R/W	Phase select Mode BLUE 00: Original 01: Fix middle 10: Fix back 11: Fix front
5:4	R/W	Phase select Mode GREEN
3:0	R/W	Continuous Change 0000: 1 ~ 1111: 16

Address B4: TMDS_TEST_MODE_2 **Default: 00h**

Bit	Mode	Function
7:6	R/W	Phase select Mode RED
5:4	R/W	Data Picking Select BLUE 0x: Middle 10: Front 11: Back
3:2	R/W	Data Picking Select GREEN
1:0	R/W	Data Picking Select RED

Address B5: Reserved

Address B6: Reserved **Default: 00h**

Bit	Mode	Function
7:0	R/W	Reserved

Address B7: Reserved

Bit	Mode	Function
7:0	R/W	Reserved

Address B8~BF Reserved

DVI DDC Channel

(Refers to the VESA "Display Data Channel Standard" for detailed, DVI channel only support DDC2B)

Address: BC DDC_ENABLE (DDC Channel Enable Register) **Default: 00h**

Bit	Mode	Function
7:5	R/W	DDC Channel Address Least Significant 3 Bits

		(The default DDC channel address MSB 4 Bits is “A”)
4	R	DDC Write Status (for external DDC access only) It is cleared after write.
3	R/W	DDC SRAM Write Enable (for external DDC access only) 0: Disable 1: Enable
2	R/W	DDC Debounce Enable 0: Disable 1: Enable (with crystal / 4)
1	R/W	DDC Channel RAM Size 0: 128 bytes 1: 256 bytes
0	R/W	DDC Channel Enable Bit 0: MCU access Enable 1: DDC channel Enable

Address: BD DDC_INDEX (DDC SRAM R/W Index Register)

Bit	Mode	Function
7:0	R/W	DDC SRAM Read/Write Index Register [7:0]

The DDC channel index register will be auto increased one by one after each read or write cycle.

Address: BE DDC_ACCESS_PORT (DDC Channel ACCESS Port)

Bit	Mode	Function
7:0	R/W	DDC SRAM Read/Write Port

** The DDC function can still work when Power_Down & Power_Save.

** After reset, the register will be set to default value, but the SRAM will keep original data.

Control for LVDS

Address: C0 LVDS_CTRL0 **Default: 00h**

Bit	Mode	Function
7	R/W	**Power down PLL** 0: Power down 1: Normal
6	R/W	**Power down even-port** 0: Power down 1: Normal
5	R/W	**Power down odd-port** 0: Power down 1: Normal
4	R/W	**Enable PLL test signal to PLLTST** 0: Disable 1: Enable
3	R/W	**Select PLLtest-pin** 0: Fbak 1: Fin
2:1	R/W	**Watch Dog Model** 00: Enable Watch Dog 01: Keep PLL VCO = 1V 1x: Disable Watch Dog
0	R	**Watch Dog Control Flag** 0: Disable watch dog 1: Reset PLL and set VCO = 1V

Address: C1 LVDS_CTRL1 **Default: 04h**

Bit	Mode	Function
7	R/W	**TTL_TST_EN** 0: Disable 1: Enable
7:4	---	**Reserved**
3	R/W	**Pin connected with capacitors (2.6pF)** 0: yes 1: no
2:0	R/W	**RSDS / LVDS Output Common Mode (100)**

For **TTL_TST_EN** test mode, we use the video port as input, then we could not test the signal output from video port. In 8 bit TTL mode, if set to 1, these signals will be redirect to other pins, and the test fault coverage will be higher....

Address: C2 LVDS_CTRL2 **Default: 52h**

Bit	Mode	Function
7:6	R/W	SBGL [1:0]: Bandgap Voltage (~1.2V)
5:3	R/W	SIL [2:0]: PLL charge pump current (I=5uA+5uA*code)
2:1	R/W	SRL [1:0]: PLL resistor
0	R/W	BMTS: Bit-Mapping Table Select High: Table 2 Low: Table 1

LVDS	Bit 1	Bit 0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 6	Bit 5
Even A	ER1	ER0	EG0	ER5	ER4	ER3	ER2	ER1	ER0	EG0	ER5
Even B	EG2	EG1	EB1	EB0	EG5	EG4	EG3	EG2	EG1	EB1	EB0
Even C	EB3	EB2	DEN*6	VS*5	HS*5	EB5	EB4	EB3	EB2	DEN*6	VS*5
Even D	ER7	ER6	RSV*7	EB7	EB6	EG7	EG6	ER7	ER6	RSV*7	EB7
Odd A	OR1	OR0	OG0	OR5	OR4	OR3	OR2	OR1	OR0	OG0	OR5

Odd B	OG2	OG1	OB1	OB0	OG5	OG4	OG3	OG2	OG1	OB1	OB0
Odd C	OB3	OB2	DEN*2	VS*1	HS*0	OB5	OB4	OB3	OB2	DEN*2	VS*1
Odd E	OR7	OR6	RSV*3	OB7	OB6	OG7	OG6	OR7	OR6	RSV*3	OB7

TABLE 1 Bit-Mapping 6bit(5~0)+2bit(7~6)

LVDS	Bit 1	Bit 0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 6	Bit 5
Even A	ER3	ER2	EG2	ER7	ER6	ER5	ER4	ER3	ER2	EG2	ER7
Even B	EG4	EG3	EB3	EB2	EG7	EG6	EG5	EG4	EG3	EB3	EB2
Even C	EB5	EB4	DEN*6	VS*5	HS*5	EB7	EB6	EB5	EB4	DEN*6	VS*5
Even D	ER1	ER0	RSV*7	EB1	EB0	EG1	EG0	ER1	ER0	RSV*7	EB1
Odd A	OR3	OR2	OG2	OR7	OR6	OR5	OR4	OR3	OR2	OG2	OR7
Odd B	OG4	OG3	OB3	OB2	OG7	OG6	OG5	OG4	OG3	OB3	OB2
Odd C	OB5	OB4	DEN*2	VS*1	HS*0	OB7	OB6	OB5	OB4	DEN*2	VS*1
Odd E	OR1	OR0	RSV*3	OB1	OB0	OG1	OG0	OR1	OR0	RSV*3	OB1

TABLE 2 Bit-Mapping 6bit(7~2)+2bit(1~0)

Address: C3 LVDS_CTRL3 **Default: 80h**

Bit	Mode	Function
7:6	R/W	E_RSV_s: even port reserve signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [3] 00: PWM_0
5:4	R/W	E_DEN_s: even port data enable signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [2] 00: E_DEN (DENA)
3:2	R/W	E_VS_s: even port VS signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [1] 00: E_VS (DVS)
1:0	R/W	E_HS_s: even port HS signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [0] 00: E_HS (DHS)

Address: C4 LVDS_CTRL4 **Default: 80h**

Bit	Mode	Function
7:6	R/W	O_RSV_s: odd port reserve signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [4] 00: PWM_1
5:4	R/W	O_DEN_s: odd port data enable signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [2] 00: O_DEN (DENA)
3:2	R/W	O_VS_s: odd port VS signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [1]

		00: O_VS (DVS)
1:0	**R/W**	O_HS_s: odd port HS signal select 11: Alawys '1' 10: Alawys '0' 01: TCON [0] 00: O_HS (DHS)

Address: C5 LVDS_CTRL5 **Default: 60h**

Bit	Mode	Function
7:4	**R/W**	**Bias Generator Adjust** (0110)
3	**R/W**	**Bandgap of LVDS/RSDS Power on** 0: Off 1: On
2:0	**R/W**	STSTL [2:0]: select test attribute 000: High Impedance 001: VOCME 010: VBG 011: 60uA (20K ohm to GND) 1xx: TSTPLL (50 ohm to VDD)

Power save & power down: set C0[7:5] to 0, C5[3] to 0

Control for PLL DIV

Address: C8 PLL_DIV_CTRL0 **Default: 00h**

Bit	Mode	Function
7:6	---	Reserved.
5	R/W	DDS Reset Enable 0: Normal function 1: DDS circuit's reset will be asserted, for test only
4	R/W	**Test Mode**: (for production test) 0: Normal 1: Test Mode
3	R/W	**HS output synchronized by** 0: phase 16 1: phase 0
2:1	R/W	**Phase error detect mode** 00: zero mode (FB is aligned to nedegde of Fav) 01: ±1 mode (FB is aligned to posedge of Fav) 1x: direct mode (FB is direct to PFD)
0	R/W	**Clock select for DIV** 0: phase 0 (phase-0 of PLL2) 1: internal CLK (Fav)

Address: C9 I_CODE_L **Default: 61h**

Bit	Mode	Function
7:5	R/W	I_Code [7:5] For old I or New_I mechanism depending on 0xc9[0] & 0xc9[4]
4	R/W	I_Code [4] / I-code control mechanism 0: new linear mode, PE*(2+NEW_I[12])*2^(NEW_P+2) 1: old mode, P-code = P-code_2011 - 1
3:2	R/W	I_Code [3:2] / P-code protection mode 00 => No protection 01 => 1 bit protection 10 => 2 bits protection 11 => 3 bits protection
1	R/W	I_Code [1] / P-code mapping curve 0: choose the new P-code mapping curve 1: choose the old P-code mapping curve
0	R/W	I_Code [0] /I-code multiplication factor 0: choose the new I-code multiplication factor = NEW_I[9:5] (PE)*(2+NEW_I[13])* 2^(NEW_I[9:5]+2) 1: choose the old I-code multiplication factor

Address: CA I_CODE_M **Default: 18h**

Bit	Mode	Function
7:6	R/W	I_Code [15:14]
5	R/W	I_Code [13] / I_code calibrated setting
4	R/W	I_Code [12] / P_code calibrated setting
3	R/W	I_Code [11] / Overwrite 0 to 1 return a new PFD calibrated value.
2	R/W	I_Code [10] / 0: Old PFD 1: New PFD
1:0	R/W	I_Code [9:8] / For old I or New_I mechanism depending on 0xc9[0] & 0xc9[4]

Address: CB P_CODE **Default: 18h**

Bit	Mode	Function
7	---	Reserved

6:5	**R/W**	I_Code[17:16]//00
4:0	**R/W**	P_Code[4:0] //0x18

P_Code=2^N * γ ; *N* is bit number, *N*=32 ; γ is ratio of phase error correction. Default $\gamma=2^{-7}$, *P_Code*=2^{25} ;
P[4:0]=25-1=24=5'h18 ; **P[4:0] can not bigger than 5'h1F-6=5'h19**.
When phase-error is too large, *P_Code* will enlarge to at most 64 times automatically.
I_Code=(α*2^N)/PLLDIV ; *N* is bit number, *N*=32 ; α is ratio of frequency error correction.
Default $\alpha=2^{-9}$, *PLLDIV*=1344, *I_Code*=6241=18'h01861. ***α* must be smaller than *γ***.

Address: CC PLLDIV_HI **Default: 05h**

Bit	Mode	Function
3:0	R/W	PLL Divider Ratio Control. High-Byte [11:8].

Address: CD PLLDIV_LO **Default: 3Fh**

Bit	Mode	Function
7:0	R/W	PLL Divider Ratio Control. Low-Byte [7:0].

This register determines the number of output pixel per horizontal line. PLL derives the sampling clock and data output clock (DCLK) from input HSYNC. ***The real operation Divider Ratio = PLLDIV+1***
The power up default value of PLLDIV is 053Fh(=1343, VESA timing standard, 1024x768 60Hz, Horizontal time).
The setting of PLLDIV must include **sync, back-porch, left border, active, right border, and front-porch** times.
Control-Register CC & CD will filled in when Control-Register CD is written.

Address: CE PFD Calibrated Results

Bit	Mode	Function
5:0	R/W	PFD Calibrated Results

This register determines the number of output pixel per horizontal line. PLL derives the sampling clock and data output

Address: CF Reserved

Phase Lock Loop

Address: D0 **DPLL_CRNT (DPLL Charge Pump Current Register)** **Default: 00010xx0b**

Bit	Mode	Function
7:3	R/W	**Charge Pump Current Idch [4:0]**
2	R	**Watch Dog Status** 0: Normal 1: Abnormal
0	R/W	**Charge Pump Current Idch [5]**

I = 2.5u + D0 [3]*2.5u + D0 [4]*5u + D0 [5]*10u + D0[6]*20u + D0[7]*30u (A)
Ich (Charge pump current) = I * (D0[0] + 1) / 2

Address: D1 **DPLL_M (DPLL M Divider Register)** **Default: 01111101b**

Bit	Mode	Function
7:0	R/W	**DPM value – 2**

Address: D2 **DPLL_N (DPLLN Divider Register)** **Default: 00001010b**

Bit	Mode	Function
7:6	R/W	**DPLL Output Divider** (00 **à** 1, 01 **à** 1/2, 10 **à** 1/4, 11 **à** 1/8) // (01)
5	R/W	**DPLL Spread Spectrum Enable** 0: Disable 1: Enable
4	R/W	**Offset Frequency Direction Induced by Spread Spectrum** 0: Upward 1: Downward
3:0	R/W	**DPN value – 2**

DPLL must be twice DCLK frequency and max DPLL frequency is 320MHz.
Assume **DPLL_M**=0x7D, **DPM**=0x7D+2=127; **DPLL_N**=0x0A, **DPN**=0x0A+2=12; **Divider**=1/4, **F_IN** = 24.576MHz.
F_DPLL = **F_IN** x **DPM** / **DPN** x **Divider** = 24.576 x 127 / 12 / 4 = 65.024MHz.
If **LPF_Mode** = 1, suppose **DPM**=110, **DPN** = 12, **Ich** = Idch[000100] = 6.25uA, **DPLL**=225MHz, then **DPM / Ich =17.6**. Please keep the ratio as **constant**.
If **LPF_Mode** = 0, suppose **DPM**=46, **DPN** = 5, **Ich** = Idch [101010] =27.5uA, **DPLL**=226MHz, then **DPM / Ich = 1.67.** Please keep the ratio as **constant**.

Address: D3 **DPLL_FILTER (Loop Filter Control Register)** **Default: xx10_1111b**

Bit	Mode	Function
7	R/W	**DPLL Output Enable** 0: Enable 1: Disable
6:3	R/W	**Reserved**
2	R/W	**LPF Mode** 0: DPN <= 5 1: DPN <= 16
1:0	R/W	**Loop Filter Resistance Control** 00: 16K (LPF Mode = 0), 46K (LPF Mode = 1) 01: 18K (LPF Mode = 0), 53K (LPF Mode = 1) 10: 20K (LPF Mode = 0), 60K (LPF Mode = 1) 11: 22K (LPF Mode = 0), 67K (LPF Mode = 1)

Address: D4 **DPLL_SSP (Spread Spectrum Control Register)** **Default: 0000011xb**

Bit	Mode	Function
7:6	R/W	**Watch Dog State Setting** 00: WD active 01: WD take over 1x: WD sleep
5:4	R/W	**Watch Dog Voltage Setting**

		00: 0.8V 01: 1.3V 10: 1.8V 11: 2.3V
3	R/W	**Reserved**
2	R/W	**Test-Pin 2 Input/Output Switch** 0: Output 1: Input
1	R/W	**Test-Pin 1 Input/Output Switch** 0: Input 1: Output
0	R/W	**Reserved**

Address: D6 PLL1_CTRL (PLL1 Control Register) **Default: 0001xx10b**

Bit	Mode	Function
7:4	R/W	**Charge Pump Current** (5uA ~ 80uA)//(0001)
3	R	**PLL1 Status** 0: Normal 1: Abnormal
2	----	Reserved
1	R/W	**MSB Clock Stop**//(1) 0: Stop (for Test) 1: Normal Run
0	R/W	**PLL1 Power Down**//(0) 0: Power Down 1: Normal Run

Address: D7 PLL1_M (M Parameter Register) **Default: (0Bh)**

Bit	Mode	Function
7:0	R/W	**P1M** value – 2

Address: D8 PLL1_N (N Parameter Register) **Default: 03h**

Bit	Mode	Function
5:0	R/W	**P1N** value – 2

Assume **PLL1_M**=0x0B, **P1M**=0x0B+2=13; **PLL1_N**=0x03, **P1N**=0x03+2=5; **F_IN** = 24.576MHz.
F_PLL1 = **F_IN** x **P1M** / **P1N** = 24.576 x 13 / 5 = 63.8976MHz
If the target frequency is **F_ADC**, the constraint of **F_PLL1** is ***(15/16)*F_ADC < F_PLL1 < F_ADC***

Address: D9 PLL1_FILTER (Loop Filter Control Register) **Default: 6Fh**

Bit	Mode	Function
7:6	R/W	**BandGap Voltage Select** (Default = 01).
5:3	R/W	**Loop Filter Resistance Control** (1Kohm ~ 8Kohm). 6Kohm is preferred.(101)
2:0	R/W	**Loop Filter Capacitance Control** (20pF ~ 160pF). 160pF is preferred.(111)

Test-Pin	In/Out	Pair select DA[3:1]	Signal	Description
Tp1	0(In)	xxx	lin1	lin1 is sent to ADC by setting (Reference to 0xDD[7:6])
	1(Out)	000	Poweronchk2	Power-on-reset signal (external)
	1(Out)	001	LOCK1	PLL1's clock detector (0 is normal)
	1(Out)	010	cko	PLL's ADC output clock
	1(Out)	011	fav3v	fav signal (from DDS)
	1(Out)	100	ckk2bb	PLL2's VCO output clock
	1(Out)	101	vopp8	PLL1's VCO output clock
	1(Out)	110	BVS	Video8 VS from EAV
	1(Out)	111	IRQ	Low active
x	x	xxx		Crystal signal input (3B[6]=1)

Test-Pin	In/Out	Pair select DA[3:1]	Signal	Description
Tp2	1(In)	xxx	Xtal F. Select	Power on latch to determine the Xtal output frequency
	0(Out)	000	poweron chk1	Power-on-reset signal (internal)
	0(Out)	001	GND	DPLL's clock detector (0 is normal)
	0(Out)	010	LOCK2	PLL2's clock detector (0 is normal)
	0(Out)	011	HSFB	(From DDS)
	0(Out)	100	HSFB	(From DDS)
	0(Out)	101	GND	PLL's GND
	0(Out)	110	BHS	Video8 HS from SAV/EAV
	0(Out)	111	GND	PLL's GND

Table 2 Test-Pin Pair Setting

Address: DA PLL2_CTRL (PLL2 Control Register) Default: 10h

Bit	Mode	Function
7:4	R/W	**Charge Pump Current** (5uA ~ 80uA)//(0001)
3:1	R/W	**Select 1 pair of 8 pairs signal to testpin** (default = 000).
0	R/W	**PLL2 Power Down** //(0) 0: Power Down (default) 1: Normal Run

Address: DB PLL2_M (M Parameter Register) Default: 0Ah

Bit	Mode	Function
7:0	R/W	**P2M** value – 2

Address: DC PLL2_N (N Parameter Register) Default: 04h

Bit	Mode	Function
7	R	**PLL2 Status** 0: Normal 1: Abnormal
5:0	R/W	**P2N** value – 2

Assume **PLL2_M**=0x0A, **P2M**=0x0A+2=12; **PLL2_N**=0x04, **P2N**=0x04+2=6; **F_IN** =65 MHz .
F_PLL2 = F_IN x P2M x 2 / P2N /2 = 65 x 12 x 2 / 6 / 2 = 130 MHz
the constraint of **F_PLL2** is that ***P2N =(int)(F_IN / 10)***

Address: DD PLL2_FILTER (Loop Filter Control Register) Default: EFh

Bit	Mode	Function
7:6	R/W	**Select CLK to A/D from** 00: internal PLL (PLL2 phase-select output) 01: inverse internal PLL (PLL2 phase-select output) 10: test-pad clock (PLL_TEST1 input) 11: internal x2 PLL (PLL2 phase-select output) (Reference to 0xEA[2])
5:3	R/W	**Loop Filter Resistance Control** (1Kohm ~ 8Kohm). 6Kohm is preferred.(101)
2:0	R/W	**Loop Filter Capacitance Control** (20pF ~ 160pF). 160pF is preferred.(111)

Address: DF Reserved Default: 1000_0xx0b

Bit	Mode	Function
7:0	R/W	**Reversed**

Embedded ADC

Address: E0 REDGAIN

Bit	Mode	Function
7:0	R/W	RED Channel Gain Adjust

Address: E1 GRNGAIN

Bit	Mode	Function

7:0	R/W	Green Channel Gain Adjust

Address: E2 BLUGAIN

Bit	Mode	Function
7:0	R/W	Blue Channel Gain Adjust

Adjust the full-scale input range that corresponds to the maximum digital 8-bit binary output. Setting REDGAIN to 0 corresponds to an input full-scale range of 0.5V, and 255 adjust the input full-scale range to 1.0 V. That means the GAIN setting will change the LSB resolution. Increasing the gain results in larger input range, and less contrast effect is visible.

Address: E3 REDOFST

Bit	Mode	Function
7:0	R/W	**Red Channel Clamp Offset** FFh : clamp Vin+128*(Vfs/256) in back porch period as code 00h. 80h : clamp Vin in back porch period as code 00h. 00h : clamp Vin-128*(Vfs/256) in back porch as code 00h.

Address: E4 GRNOFST

Bit	Mode	Function
7:0	R/W	**Green Channel Clamp Offset** FFh : clamp Vin+128*(Vfs/256) in back porch period as code 00h. 80h : clamp Vin in back porch period as code 00h. 00h : clamp Vin-128*(Vfs/256) in back porch as code 00h.

Address: E5 BLUOFST

Bit	Mode	Function
7:0	R/W	**Blue Channel Clamp Offset** FFh : clamp Vin+128*(Vfs/256) in back porch period as code 00h. 80h : clamp Vin in back porch period as code 00h. 00h : clamp Vin-128*(Vfs/256) in back porch as code 00h.

Vfs: Input full-scale voltage ***depends on REDGAIN setting*****, Vin**: Input channel signal, **Vbp**: Vin in back porch period
This register is used to adjust the input clamp level. One LSB offset (=Vfs/256) equals one LSB change in ADC output. Increasing the offset setting results in less brightness. Be careful that input full-scale voltage depends on GAIN setting, so the LSB offset step will be increased when increasing the GAIN setting.

Address: E6 ADC_CTRL **Default: 80h**

Bit	Mode	Function
7:3	R/W	**SOG Reference Control** //(10000)
2	R/W	**ADC R-Channel Power Down** (SOG Circuit always enable) //(0) 0: ADC Power Down 1: Normal
1	R/W	**ADC G-Channel Power Down** (SOG Circuit always enable) //(0) 0: ADC Power Down 1: Normal
0	R/W	**ADC B-Channel Power Down** (SOG Circuit always enable) //(0) 0: ADC Power Down 1: Normal

Address: E7 ADC_REG_CUR_L **Default: 69h**

Bit	Mode	Function
7:6	R/W	ADC master bias current option: vicm, vocm buffer op bias 00 45u 01 60u 10 75u 11 90u
5:4	R/W	ADC master bias voltage option: vicm voltage 00 0.98V 01 1.08V 10 1.20V 11 1.32V

3:2	R/W	ADC master bias voltage option: vocm voltage 00 1.44V 01 1.56V 10 1.68V 11 1.80V
1:0	R/W	ADC master bias current option: ADC op bias 00 45u 01 60u 10 75u 11 90u

Address: E8 ADC_REG_CUR_H Default: 15h

Bit	Mode	Function
7:6	R/W	**ADC_REG_CLK**: Adjust digital clock (ADC_PIXEL_OUT) and analog clock (CKOAD) delay
5:4	R/W	**ADC_REG_CLK**: fine tune GREEN channel phase, hidden.<1:0>, adjust sampling phase in SHA
3:2	R/W	**ADC_REG_CLK**: adjust non-overlapped time in clock generator
1	R/W	**ADC_MODE_DUTY**: 0: 1F (Using normal pixel rate from APLL) 1: 2F (Using double pixel rate from APLL)
0	R/W	**ADC_REG_CUR:** ADC master bias option, hidden. 0: 1.12387V 1: 1.19873V

We have 8 level ADC fine tune phase of RGB, the first is 400ps, and the 2nd to 7th are each 150ps.

Address: E9 ADC_REG_TEST Default: 10h

Bit	Mode	Function
7:5	R/W	**ADC_REG_TEST** //(000) ADC select mux output to ADC_TEST pin in test mode, hidden. 000 Enable clamping buffer 001 Disable clamping buffer 010 test, Voffset connected to SOGIN 011 test, Vicm connected to SOGIN 100 test, Vrb connected to SOGIN 101 test, Vocm connected to SOGIN 110 test, Vrt connected to SOGIN 111 test, Vmid connected to SOGIN
4:3	R/W	**ADC REG_BND** //(10) 00: 75MHz 01: 150MHz 10: 300MHz 11: 500MHz
2	R/W	**ADC Output (Only when CR[EA]-Bit4=0)** 0: Dual output 1: Single output (Even / Odd selected by CR[EA]-bit7:5)
1:0	R/W	**ADC_REG_OUT** //(000) ADC select divider ratio in test mode, hidden. 00 divided by 1 01 divided by 2 10 divided by 3 11 divided by 4

Address: EA ADC_REG_CLK Default: 05h

Bit	Mode	Function
7	R/W	**ADC red channel select:** 0: even 1: odd
6	R/W	**ADC green channel select:**

		0: even 1: odd
5	R/W	**ADC blue channel select:** 0: even 1: odd
4	R/W	**ADC MODE** 0: dual channel 1: single channel
3:2	R/W	**ADC_REG_CLK_R25**: fine tune RED channel phase, hidden.<1:0>, adjust sampling phase in SHA
1:0	R/W	**ADC_REG_CLK_B25**: fine tune BLUE channel phase, hidden.<1:0>, adjust sampling phase in SHA

Address: EB ADC Frame Modulation Default: 00h

Bit	Mode	Function
7:6	R/W	**Power –on-reset Negative Threshold Voltage** 00: 1.8V 01: 2.0V 10: 2.2V 11: 2.4V
5	R/W	**ADC_REG_CLK_R25**: fine tune RED channel phase, hidden.<2>, adjust sampling phase in SHA
4	R/W	**ADC_REG_CLK_G25**: fine tune GREEN channel phase, hidden.<2>, adjust sampling phase in SHA
3	R/W	**ADC_REG_CLK_B25**: fine tune BLUE channel phase, hidden.<2>, adjust sampling phase in SHA
2	R/W	0 frame modulation off, disable VS 1 frame modulation on, enable VS
1	R/W	0 disable HS 1 enable HS
0	R/W	0 negative input polarity 1 positive input polarity

Address: EC ADC Differential Mode Default: 08h

Bit	Mode	Function
7	R/W	**ADC Dual Input Selection** 0: Channel 0 1: Channel 1
6	R/W	**ADC Differential Input Selection** 0: Single-ended 1: Differential
5:3	R/W	**ADC Clamp Voltage Option**
2	R/W	**ADC Red Channel Clamp Selection** 0: To ground 1: To mid-scale
1	R/W	**ADC Green Channel Clamp Selection** 0: To ground 1: To mid-scale
0	R/W	**ADC Blue Channel Clamp Selection** 0: To ground 1: To mid-scale

Note: 0xEC[7] must be 0.

Address: ED HS Schmitt Trigger Control Default: 00h

Bit	Mode	Function
7	R/W	**HS Power Down (only for Schmitt trigger new mode 0xED[5] =1)** 0: Power down 1: Normal

6	R/W	**Polarity Select** 0: Negative HSYNC (high level) 1: Positive HSYNC (low level)
5	R/W	**Schmitt Trigger Mode** 0: Old mode 1: New mode
4	R/W	**Threshold Voltage Fine Tune (only for Schmitt trigger new mode 0xED[5] =1)** **0: 0V** **1: -0.1V**
3:2	R/W	**Positive Threshold Voltage**
1:0	R/W	**Negative Threshold Voltage**

We have 3 mode of the HSYNC Schmitt trigger.

1. Old mode 1: original HSYNC Schmitt trigger.

The 0xED [6:5] **à** 00, The V_t^+ = 1.5V, V_t^- = 1.0V

2. Old mode 2: The easy HSYNC Schmitt trigger.

The 0xED [6:5] **à** 10

0xED [1:0]	V_t^+	V_t^-
01	2.0V	1.5V
11	1.5V	1.0V

3. New mode: Fully programmable Schmitt trigger.

The following table will determine the Schmitt Trigger positive and negative voltage:

0xED [6] = 1		0xED [6] = 0	
0xED [3:2]	0xED [1:0]	0xED [3:2]	0xED [1:0]
00: V_t^+ = 1.4V	00: V_t^- = V_t^+ - 1.2V	00: V_t^+ = 2.0V	00: V_t^- = V_t^+ - 1.2V
01: V_t^+ = 1.6V	01: V_t^- = V_t^+ - 1.0V	01: V_t^+ = 2.2V	01: V_t^- = V_t^+ - 1.0V
10: V_t^+ = 1.8V	10: V_t^- = V_t^+ - 0.8V	10: V_t^+ = 2.4V	10: V_t^- = V_t^+ - 0.8V
11: V_t^+ = 2.0V	11: V_t^- = V_t^+ - 0.6V	11: V_t^+ = 2.6V	11: V_t^- = V_t^+ - 0.6V

After we get the threshold voltage by the table, we still can fine tune it:

Final Positive Threshold Voltage = V_t^+ - 0.1* 0xED[4]

Final Negative Threshold Voltage = V_t^- - 0.1* 0xED[4]

DDC Special Function Access

The following DDC special function registers are only valid when EXT# =0.

Address: F0 DDC_SET_SLAVE **Default: 6E**

Bit	Mode	Function
7:1	R/W	**DDC Slave Address** to decode
0	R/W	**Channel Select** 0: from ADC 1: from DVI

Address: F1 DDC_SUB_IN

Bit	Mode	Function
7:0	R	**DDC Sub-Address Received**

Address: F2 DDC_DATA_IN

Bit	Mode	Function
7:0	R	**DDC Data Received**

Address: F3 DDC_DATA_OUT

Bit	Mode	Function
7:0	W	**DDC Data Output**

Address: F4 DDC_STATUS

Bit	Mode	Function
7:5	----	Reserved
4	R	If **DDC_STOP** signal occurs, this bit is set to "1"
3	R	If **DDC_DATA_OUT** loaded to serial-out-byte, this bit is set to "1"
2	R	If **DDC_DATA_IN** latched, this bit is set to "1"
1	R	If **DDC_SUB** latched, this bit is set to "1"
0	R	If **DDC_SLAVE** latched, this bit is set to "1"

Write to clear status.

Address: F5 DDC_IRQ_CTRL **Default: 00h**

Bit	Mode	Function
7:5	---	**Reserved**
4	R/W	0: Disable the **DDC_STOP** signal as an interrupt source 1: Enable the **DDC_STOP** signal as an interrupt source
3	R/W	0: Disable the **DDC_DATA_OUT** loaded to serial-out-byte as an interrupt source 1: Enable the **DDC_DATA_OUT** loaded to serial-out-byte as an interrupt source
2	R/W	0: Disable the **DDC_DATA_IN** latched as an interrupt source 1: Enable the **DDC_DATA_IN** latched as an interrupt source
1	R/W	0: Disable the **DDC_SUB** latched as an interrupt source 1: Enable the **DDC_SUB** latched as an interrupt source
0	R/W	0: Disable the **DDC_SLAVE** latched as an interrupt source 1: Enable the **DDC_SLAVE** latched as an interrupt source

DDC Channel

(Refers to the VESA "Display Data Channel Standard" for detailed)

Address: FC DDC_ENABLE (DDC Channel Enable Register) Default: 00h

Bit	Mode	Function
7:5	R/W	**DDC Channel Address Least Significant 3 Bits** (The default DDC channel address MSB 4 Bits is "A")
4	R/W	**DDC Write Status (for external DDC access only)** It is cleared after write.
3	R/W	**DDC SRAM Write Enable (for external DDC access only)** 0: Disable 1: Enable
2	R/W	**DDC Debounce Enable** 0: Disable 1: Enable (with crystal/4)
1	R/W	**DDC Channel RAM Size** 0: 128 bytes 1: 256 bytes
0	R/W	**DDC Channel Enable Bit** 0: MCU access Enable 1: DDC channel Enable

Address: FD DDC_INDEX (DDC SRAM R/W Index Register)

Bit	Mode	Function
7:0	R/W	DDC SRAM Read/Write Index Register [7:0]

The DDC channel index register will be auto increased one by one after each read or write cycle.

Address: FE DDC_ACCESS_PORT (DDC Channel ACCESS Port)

Bit	Mode	Function
7:0	R/W	DDC SRAM Read/Write Port

** The DDC function can still work when Power_Down & Power_Save.

** After reset, the register will be set to default value, but the SRAM will keep original data.

Address: FF TMDS Hsync & Vsync Error Correction Default: 00h

Bit	Mode	Function
2	R/W	**ADC Digital Filter** 0: Disable 1: Enable
1:0	R/W	**TMDS Enhancement** 00: orignal output 01: one pixel debouncing 10: one + eight pixels debouncing 11: one+ eight pixels debouncing & masking

Timing Controller

RTD Register Description for Embedded Timing Controller:

Address: 95 TCON_ADDR _PORT Default: 00h

Bit	Mode	Function
7:0	**R/W**	Address port for embedded TCON access

Address: 96 TCON_DATA _PORT

Bit	Mode	Function
7:0	**R/W**	Data port for embedded TCON access

Register Description

Timing Controller Programmable Registers:

Address: 00 TC_CTRL1 (Timing Controller control register1) Default: 0000_011xb

Bit	Mode	Function
7	R/W	**Enable Timing Controller Function (Global)** 0: Disable 1: Enable
6	R/W	**TCON [12] / PWM2 Select** 0: TCON [12] or crystal output (reference to TCON 0x00[2]) 1: PWM2
5	R/W	**TCON [n] Toggle Function Reset** 0: Not reset 1: reset by DVS
4	R/W	**TCON [2] Output Function Select (only for serial port access)** 0: Original TCON 1: PWM2
3	R/W	**Inactive Period Data Controlled by internal TCON [13]** 0: DEN 1: TCON [13]
2	R/W	**TCON [12] Set to Crystal Output (only for TCON 0x00[6] = 0)** 0: Disable 1: Enable
1	R/W	**TCON [13] Set to Crystal Output (only for TCON 0x04[2] = 0)** 0: Disable 1: Enable
0	R	**Power-On latch PLL Test Pin 2 for crystal frequency** 0: x 1/2 1: x 1

After switch display timing or clock, 0x00[5] first must be 1 to reset TCON state.

Address: 01 TC_CTRL2 (Timing Controller control register2) Default: 00h

Bit	Mode	Function
7	R/W	**DCLK Slew-Rate Control** 0: fast 1: slow
6:4	R/W	**DCLK Drive Control** (ACLKP/ACLKN/BCLKP/BCLKN) 000: Lowest Drive (2mA) ~ 111: Highest Drive (16mA) for TTL 000~111: (C2)*2 + (C1)*1 + (C1)*0.5 + 2.5 mA for RSDS
3	R/W	**OCLK Slew-Rate Control (pin112)** 0: fast 1: slow
2:0	R/W	**OCLK Drive Current Control (pin112)** 000: Lowest Drive (2mA) ~ 111: Highest Drive (16mA) for TTL

Address: 02 PURE_TTL_PIN_DRV Default: 00h

Bit	Mode	Function
7	R/W	**Display Data Port Slew-Rate Control** 0: fast 1: slow
6:4	R/W	**Display Data Port Drive Current Control** 000: Lowest Drive (2mA) ~ 111: Highest Drive (16mA)
3	R/W	**TCON Slew-Rate Control** 0: fast 1: slow
2:0	R/W	**TCON Drive Current Control** 000: Lowest Drive (2mA) ~ 111: Highest Drive (16mA)

Address: 03 RSDS Performance Fine Tune Default: 40h

Bit	Mode	Function
7:6	R/W	**Display Port Configuration:** 00: TTL 01: HZ 10: LVDS 11: RSDS
5	R/W	**RSDS Green / Clock Pair Swap**
4:2	R/W	**Display Data Port Drive Current Control (for LVDS pin)** 000~111: (C2)*4 + (C1)*4 + (C0)*2 mA for TTL (C2~C0 is bit 6~4)
1	R/W	**RSDS High/Low Bit Swap (data)**
0	R/W	**RSDS Differential pair PN swap (data)**

//Example:**
AU 17" RSDS panel pin order:
B0B1B2G0G1G2CLKR0R1R2

QDI 17" RSDS panel pin order:
B2B1B0G2G1G0CLKR2R1R0
CMO 17" RSDS panel pin order:
B2B1B0CLKG2G1G0R2R1R0
現在 RTD 有 even/odd swap,red/blue swap,8 bit MSB/LSB swap,6 bit MSB/LSB swap, RSDS high/low bit swap, RSDS P/N swap,加上有 **green/clk swap** 模式,則
-if 6Bit MSB/LSB swap,then
G0G1G2CLK -> G2G1G0CLK
-if green/clock swap, then
G0G1G2CLK -> CLKG0G1G2
-if 6Bit MSB/LSB swap first, then green/clk swap
G0G1G2CLK -> G2G1G0CLK-> CLKG2G1G0
**//

Address: 04 DDC _PARA_VIDEO8_TCON_PWM_SHARING Default: F8h

Bit	Mode	Function
7	**R/W**	**TMDS_DDC Enable** 0: Disable 1: Enable
6	**R/W**	**ADC_DDC Enable** 0: Disable 1: Enable
5	---	**Reserved**
4	**R/W**	**TTL Display B port Blue [1:0] Location (only for TTL 8bit mode)** 0: From pin 52, 53 (must be serial port) 1: From pin 46, 47 (TCON 0x04[6] = 0)
3	**R/W**	**VIDEO-8 port Input / Output Enable** 0: Output 1: Input

2	**R/W**	**TCON [13] / PWM2 Select** 0: TCON [13] or crystal output (reference to TCON 0x00[1]) 1: PWM2
1	**R/W**	**TCON [7] / PWM1 Select (only for TCON 0x04[7] = 0)** 0: TCON [7] 1: PWM1
0	**R/W**	**TCON [1] / PWM1 Select Bit 0 (only for TCON 0x04[6] = 0 && TCON 0x04[4] = 0)** 0: TCON [1] 1: PWM1

Address: 05 RSDS_PIN_DRV (pin 59~108) **Default: 00h**

Bit	Mode	Function
7	R/W	**Display Data Port Slew-Rate Control (for LVDS pin)** 0: fast 1: slow
6:4	R/W	**Display Data Port Drive Current Control (for LVDS pin)** 000~111: (C2)*4 + (C1)*4 + (C0)*2 mA for TTL (C2~C0 is bit 6~4) 000~111: (C2)*2 + (C1)*1 + (C1)*0.5 + 2.5 mA for RSDS & LVDS (C2~C0 is bit6~4)
3	R/W	**TCON Slew-Rate Control (for LVDS pin)** 0: fast 1: slow
2:0	R/W	**TCON Drive Current Control (for LVDS pin)** 000~111: (C2)*4 + (C1)*4 + (C0)*2 mA for TTL (C2~C0 is bit 2~0)

Address: 06~07 Reserved for future

Address: 08 TCON [0]_VS_LSB (TCON [0] Vertical Start LSB Register)

Bit	Mode	Function
7:0	W	Line number [7:0] at which TCON control generation begins

Address: 09 TCON [0]_VS_MSB (TCON [0] Vertical Start/End MSB Register)

Bit	Mode	Function
7		Reserved
6:4	W	Line number [10:8] at which TCON control generation ends
3		Reserved
2:0	W	Line number [10:8] at which TCON control generation begins

Address: 0A TCON [0]_VE_LSB (TCON [0] Vertical End LSB Register)

Bit	Mode	Function
7:0	W	Line number [7:0] at which TCON control generation ends

Address: 0B TCON [0]_HS_LSB (TCON [0] Horizontal Start LSB Register)

Bit	Mode	Function
7:0	W	Pixel count [7:0] at which TCON goes active

Address: 0C TCON [0]_HS_MSB (TCON [0] Horizontal Start/End MSB Register)

Bit	Mode	Function
7		Reserved
6:4	W	Pixel count [10:8] at which TCON goes inactive
3		Reserved
2:0	W	Pixel count [10:8] at which TCON goes active

Notes: To be triggered on rising edge of the DCLK

Address: 0D TCON [0]_HE_LSB (TCON [0] Horizontal End LSB Register)

Bit	Mode	Function
7:0	W	Pixel count [7:0] at which TCON goes inactive

Notes: If the register number is large than display format, the horizontal component is always on.

Address: 0E TCON [0]_CTRL (TCON [0] Control Register) Default: 00h

Bit	Mode	Function
7	R/W	**TCON [n] Enable** (Local) 0: Disable (TCON [n] output clamp to '0') 1: Enable
6	R/W	**Polarity Control** 0: Normal output 1: Inverted output
5	----	Reserved
4	----	Reserved
3	R/W	**Toggle Circuit Enable/Disable** 0: Normal TCON output 1: Toggle Circuit enable
2:0	R/W	**TCON [13:10] & TCON [7:4] (TCON Combination Select)** /*TCON [13] has inactive data controller function. TCON [13]~[10] has dot masking function TCON [7] has flicking reduce function. */ 000: Normal TCON output 001: Select TCON [n] "AND" with TCON [n-1] 010: Select TCON [n] "OR" with TCON [n-1] 011: Select TCON [n] "XOR" with TCON [n-1] 100: Select TCON [n-1] rising edge as toggle trigger signal (when toggle enable) 101: Select TCON [n-1] rising edge as toggle trigger signal, then "AND" (when toggle enable) 110: Select TCON [n-1] rising edge as toggle trigger signal, then "OR" (when toggle enable) 111: Select TCON [n] and TCON [n-1] on alternating frames. --- **TCON [9:8] (TCON Combination Select)** 000: Normal TCON output 001: Select TCON [n] "AND" with TCON [n-1] 010: Select TCON [n] "OR" with TCON [n-1] 011: Select TCON [n] "XOR" with TCON [n-1] 100: Select TCON [n-1] rising edge as toggle trigger signal (when toggle enable) 101: Select TCON [n-1] rising edge as toggle trigger signal, then "AND" (when toggle enable) 110: Select TCON [n-1] rising edge as toggle trigger signal, then "OR" (when toggle enable) 111: Select TCON [n] and TCON [n-1] reference ODD signal as alternating frames. --- **TCON [3] (TCON Combination Select)** 000: Normal TCON output 001: Select TCON [3] "AND" with TCON [2] 010: Select TCON [3] "OR" with TCON [2] 011: Select TCON [3] "XOR" with TCON [2] 100: Select TCON [2] rising edge as toggle trigger signal (when toggle enable) 101: Select TCON [2] rising edge as toggle trigger signal, then "AND" (when toggle enable) 110: Select TCON [2] rising edge as toggle trigger signal, then "OR" (when toggle enable) 111: Select reset(ODD=0) or set(ODD=1) TCON [3] by DVS, when toggle function enable --- **TCON [2] (Clock Toggle Function**)//toggle function is inactive 00x: Normal TCON output 010: Select DCLK/2 when TCON [2] is "0" 011: Select DCLK/2 when TCON [2] is "1" 100: Select DCLK/4 when TCON [2] is "0" 101: Select DCLK/4 when TCON [2] is "1" 110: Select DCLK/8 when TCON [2] is "0" 111: Select DCLK/8 when TCON [2] is "1" --- **TCON [1]** xx0: Normal TCON output xx1: Reverse-Control Signal output

		---------- **TCON [0]** 00x: Normal TCON output 010: EVEN “REV” 18/24-bit function (“REV0” on TCON [0]) ODD “REV” 18/24-bit function (“REV1” on TCON [1]) 011: ALL “REV” 36/48-bit function (“REV” on TCON [0], can also on TCON [1]) 100: EVEN data Output Inversion Controlled by TCON [0] is “0” ODD data Output Inversion Controlled by TCON [1] is “0” 101: EVEN data Output Inversion Controlled by TCON [1] is “1” ODD data Output Inversion Controlled by TCON [1] is “1”

Address: 5F/67/6F/77 TC_DOT_MASKING_CTRL Default: 00h

Bit	Mode	Function
7:3	R/W	**Reserved**
2	R/W	**Red Dot Masking Enable** 0: Disable 1: Enable
1	R/W	**Green Dot Masking Enable** 0: Disable 1: Enable
0	R/W	**Blue Dot Masking Enable** 0: Disable 1: Enable

TCON [0] ~ TCON [13] Control Registers Address Map

Address	Data(# bits)	Default
0A,09,08	TCON [0]_VS_REG (11)	
0D,0C,0B	TCON [0]_HS_REG (11)	
0E	TCON [0]_CTRL_REG	00
0F	Reserved	
12,11,10	TCON [1]_VS_REG (11)	
15,14,13	TCON [1]_HS_REG (11)	
16	TCON [1]_CTRL_REG	00
17	Reserved	
1A,19,18	TCON [2]_VS_REG (11)	
1D,1C,1B	TCON [2]_HS_REG (11)	
1E	TCON [2]_CTRL_REG	00
1F	Reserved	
22,21,20	TCON [3]_VS_REG (11)	
25,24,23	TCON [3]_HS_REG (11)	
26	TCON [3]_CTRL_REG	00
27	Reserved	
2A,29,28	TCON [4]_VS_REG (11)	
2D,2C,2B	TCON [4]_HS_REG (11)	
2E	TCON [4]_CTRL_REG	00
2F	Reserved	
32,31,30	TCON [5]_VS_REG (11)	
35,34,33	TCON [5]_HS_REG (11)	
36	TCON [5]_CTRL_REG	00
37	Reserved	
3A,39,38	TCON [6]_VS_REG (11)	
3D,3C,3B	TCON [6]_HS_REG (11)	
3E	TCON [6]_CTRL_REG	00
3F	Reserved	
42,41,40	TCON [7]_VS_REG (11)	
45,44,43	TCON [7]_HS_REG (11)	
46	TCON [7]_CTRL_REG	00
47	Reserved	
4A,49,48	TCON [8]_VS_REG (11)	
4D,4C,4B	TCON [8]_HS_REG (11)	
4E	TCON [8]_CTRL_REG	00
4F	Reserved	
52,51,50	TCON [9]_VS_REG (11)	
55,54,53	TCON [9]_HS_REG (11)	
56	TCON [9]_CTRL_REG	00
57	Reserved	
5A,59,58	TCON [10]_VS_REG (11)	

5D,5C,5B	TCON [10]_HS_REG (11)	
5E	TCON [10]_CTRL_REG	00
5F	TCON [10]_CTRL_REG	
62,61,60	TCON [11]_VS_REG (11)	
65,64,63	TCON [11]_HS_REG (11)	
66	TCON [11]_CTRL_REG	00
67	TCON [11]_CTRL_REG	00
6A,69,68	TCON [12]_VS_REG (11)	
6D,6C,6B	TCON [12]_HS_REG (11)	
6E	TCON [12]_CTRL_REG	00
6F	TCON [12]_CTRL_REG	00
72,71,70	TCON [13]_VS_REG (11)	
75,74,73	TCON [13]_HS_REG (11)	
76	TCON [13]_CTRL_REG	00
77	TCON [13]_CTRL_REG	00

Embedded OSD

Register Access and address

Addressing and Accessing Register

ADDRESS	BIT							
	7	6	5	4	3	2	1	0
High Byte	A15	A14	A13	A12	A11	A10	A9	A8
Low Byte	A7	A6	A5	A4	A3	A2	A1	A0

Figure 16. Addressing and Accessing Registers

Date	BIT							
Byte 0	D7	D6	D5	D4	D3	D2	D1	D0
Byte 1	D7	D6	D5	D4	D3	D2	D1	D0
Byte 2	D7	D6	D5	D4	D3	D2	D1	D0

Figure 2. Data Registers

All kind of registers can be controlled and accessed by these 2 bytes, and each address contains 3-byte data, details are described as follows:

Write mode: **[A15:A14] select which byte to write**

-00: Byte 0 -01:Byte 1 -10: Byte 2 –11: All

****All data are sorted by these three Bytes (Byte0~Byte2)***

[A13] Auto Load (After write 6 byte to buffer, load data wait VSync porch)

[A12] Address indicator

-0: Window and frame control ~~and ***hardware cursor***~~ registers.

-1: Font Select and font map SRAM

[A11:A0] Address mapping

- Font Select and font map SRAM address: 000~EFF **3.75k*3byte**

-Frame control register address: 000~0xx **(Latch)**

-Window control register address: 100~1xx **(Latch)**

~~-Hardware cursor(36x36 pixel) RAM: 200~26b **(SRAM)**~~

**** Selection of SRAM address or Latch address selection is determined by A12!***

Example. Bit [15:14]=00

-All data followed are written to byte0 and address increases.

Byte0 **à** *Byte0* **à** *Byte0… (Address will auto increase)*

Bit [15:14] =01

-All data followed are written to byte1 and address increases.

Byte1 **à** *Byte1* **à** *Byte1… (Address will auto increase)*

Bit [15:14] =11

- Address will be increased after each 3-byte data written.

Byte0 **à** *Byte1* **à** *Byte2* **à** *Byte0* **à** *Byte1* **à** *Byte2… (Address will auto increase)*

Window control registers

- Windows all support shadow/border/3D button
- Window0, 5, 6, 7 support gradient functions.
- Window 4, 5, 6, 7 start/end resolution are 1line(pixel), Window 0, 1, 2, 3 start/end resolution are 4line(pixel),
- All window start and end position include the ***special effect (border/shadow/3D button)*** been assigned
- Font comes after windows by 10 pixels, so you should compensate 10 pixels on windows to meet font position

Window 0 Shadow/Border/Gradient
Address: 100h

Byte 0

Bit	Mode	Function
7:6	--	Reserved
5:3	W	Window 0 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 0 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 0 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 0 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level

2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 0 start position
Address: 101h

Byte 0

Bit	Mode	Function
7:2	W	Window 0 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 0 vertical start [2:0] line
4:0	W	Window 0 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 0 vertical start [10:3] line

Start position must be increments of four.

Window 0 end position
Address: 102h

Byte 0

Bit	Mode	Function
7:2	W	Window 0 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 0 vertical end [2:0] line
4:0	W	Window 0 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 0 vertical end [10:3] line

- End position must be increments of four.

Window 0 control
Address: 103h

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7	--	Reserved
6:4	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient

		010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
3:0	W	Window 0 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7	W	Reserved
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 0 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 0 Enable 0: Disable 1: Enable

Window 1 Shadow/Border/Gradient
Address: 104h

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 1 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 1 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 1 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 1 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 1 start position
Address: 105h

Byte 0

Bit	Mode	Function
7:2	W	Window 1 horizontal start [5:0]
3:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 1 vertical start [2:0] line
4:0	W	Window 1 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 1 vertical start [10:3] line

Start position must be increments of four.

Window 1 end position
Address: 106h

Byte 0

Bit	Mode	Function
7:2	W	Window 1 horizontal end [5:0]
2:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 1 vertical end [2:0] line
4:0	W	Window 1 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 1 vertical end [10:3] line

End position must be increments of four.

Window 1 control
Address: 107h

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7:4	--	Reserved
3:0	W	Window 1 color index in 16-color LUT

Byte 2

default: 00h

Bit	Mode	Function
7:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 1 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 1 Enable 0: Disable 1: Enable

Window 2 Shadow/Border/Gradient
Address: 108h

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 2 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 2 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 2 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 2 border color index in 16-color LUT

		For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 2 start position
Address: 109h

Byte 0

Bit	Mode	Function
7:2	W	Window 2 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 2 vertical start [2:0] line
4:0	W	Window 2 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 2 vertical start [10:3] line

Start position must be increments of four.

Window 2 end position
Address: 10Ah

Byte 0

Bit	Mode	Function
7:2	W	Window 2 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 2 vertical end [2:0] line
4:0	W	Window 2 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 2 vertical end [10:3] line

End position must be increments of four.

Window 2 control
Address: 10Bh

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function

7:4	--	Reserved
3:0	W	Window 2 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 2 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 2 Enable 0: Disable 1: Enable

Window 3 Shadow/Border/Gradient
Address: 10Ch

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 3 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 3 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 3 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 3 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 3 start position
Address: 10Dh

Byte 0

Bit	Mode	Function

7:2	W	Window 3 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 3 vertical start [2:0] line
4:0	W	Window 3 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 3 vertical start [10:3] line

Start position must be increments of four.

Window 3 end position
Address: 10Eh

Byte 0

Bit	Mode	Function
7:2	W	Window 3 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 3 vertical end [2:0] line
4:0	W	Window 3 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 3 vertical end [10:3] line

End position must be increments of four.

Window 3 control
Address: 10Fh

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7:4	--	Reserved
3:0	W	Window 3 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 3 Type 000: Shadow Type 1 001: Shadow Type 2

		010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 3 Enable 0: Disable 1: Enable

Window 4 Shadow/Border/Gradient
Address: 110h

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 4 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4 shadow color index in 16-color LUT For 3D window, it is the left-top/ bottom border color
3:0	W	Window 4 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4 start position
Address: 111h

Byte 0

Bit	Mode	Function
7:2	W	Window 4 horizontal start [5:0]
2:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 4 vertical start [2:0] line
4:0	W	Window 4 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 4 vertical start [10:3] line

Window 4 end position
Address: 112h

Byte 0

Bit	Mode	Function
7:2	W	Window 4 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 4 vertical end [2:0] line
4:0	W	Window 4 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 4 vertical end [10:3] line

Window 4 control
Address: 113h

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7:4	--	Reserved
3:0	W	Window 4 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4 Enable

		0: Disable 1: Enable

Window 5 Shadow/Border/Gradient
Address: 114h

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 5 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 5 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 5 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 5 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 5 start position
Address: 115h

Byte 0

Bit	Mode	Function

7:2	W	Window 5 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 5 vertical start [2:0] line
4:0	W	Window 5 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 5 vertical start [10:3] line

Window 5 end position
Address: 116h

Byte 0

Bit	Mode	Function
7:2	W	Window 5 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 5 vertical end [2:0] line
4:0	W	Window 5 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 5 vertical end [10:3] line

Window 5 control
Address: 117h

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7	--	Reserved
6:4	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
3:0	W	Window 5 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7	W	Reserved
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 5 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 5 Enable 0: Disable 1: Enable

Window 6 Shadow/Border/Gradient
Address: 118h

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 6 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 6 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

PS: This is for non-rotary, rotate 270, rotate 90 and 180.

Byte 1

Bit	Mode	Function
7:4	W	Window 6 shadow color index in 16-color LUT For 3D window, it is the left-top/ bottom border color
3:0	W	Window 6 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease

		1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 6 start position
Address: 119h

Byte 0

Bit	Mode	Function
7:2	W	Window 6 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 6 vertical start [2:0] line
4:0	W	Window 6 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 6 vertical start [10:3] line

Window 6 end position
Address: 11Ah

Byte 0

Bit	Mode	Function
7:2	W	Window 6 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 6 vertical end [2:0] line
4:0	W	Window 6 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 6 vertical end [10:3] line

Window 6 control
Address: 11Bh

Byte 0

Bit	Mode	Function
7:0	--	Reserved

Byte 1

Bit	Mode	Function
7	--	Reserved
6:4	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
3:0	W	Window 6 color index in 16-color LUT

Byte 2 default: 00h

Bit	Mode	Function
7	W	Reserved
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 6 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 6 Enable 0: Disable 1: Enable

Window 7 Shadow/Border/Gradient
Address: 11Ch

Byte 0

Bit	Mode	Function
7:6	W	Reserved
5:3	W	Window 7 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 7 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit[5:3] for 3D button thickness

PS: This is for non-rotary, rotate 270, rotate 90 and 180.

Byte 1

Bit	Mode	Function
7:4	W	Window 7 shadow color index in 16-color LUT For 3D window, it is the left-top/bottom border color
3:0	W	Window 7 border color index in 16-color LUT For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 7 start position
Address: 11Dh

Byte 0

Bit	Mode	Function
7:2	W	Window 7 horizontal start [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 7 vertical start [2:0] line
4:0	W	Window 7 horizontal start [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 7 vertical start [10:3] line

Window 7 end position
Address: 11Eh

Byte 0

Bit	Mode	Function
7:2	W	Window 7 horizontal end [5:0]
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	W	Window 7 vertical end [2:0] line
4:0	W	Window 7 horizontal end [10:6] pixel

Byte 2

Bit	Mode	Function
7:0	W	Window 7 vertical end [10:3] line

Window 7 control
Address: 11Fh

Byte 0

Bit	Mode	Function
7:0	--	Reserved

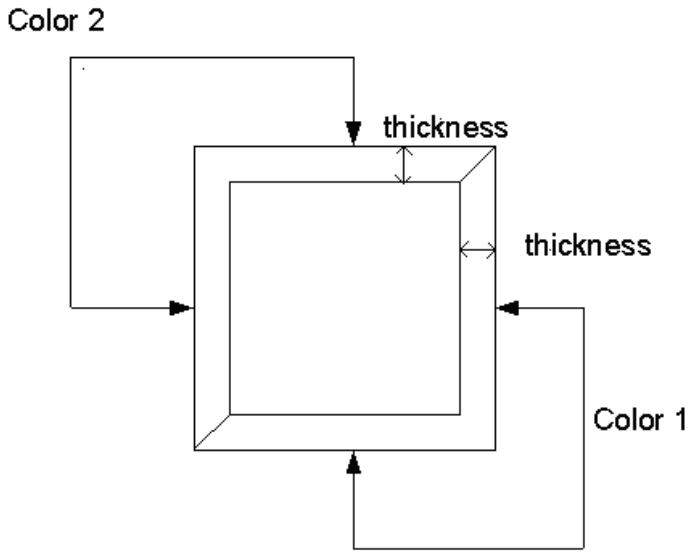
Byte 1

Bit	Mode	Function
7	--	Reserved
6:4	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
3:0	W	Window 7 color index in 16-color LUT

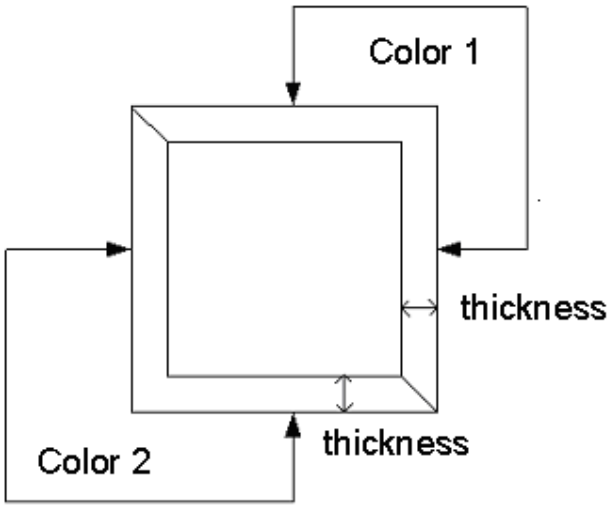
Byte 2 default: 00h

Bit	Mode	Function
7	W	Reserved
6	W	Gradient function

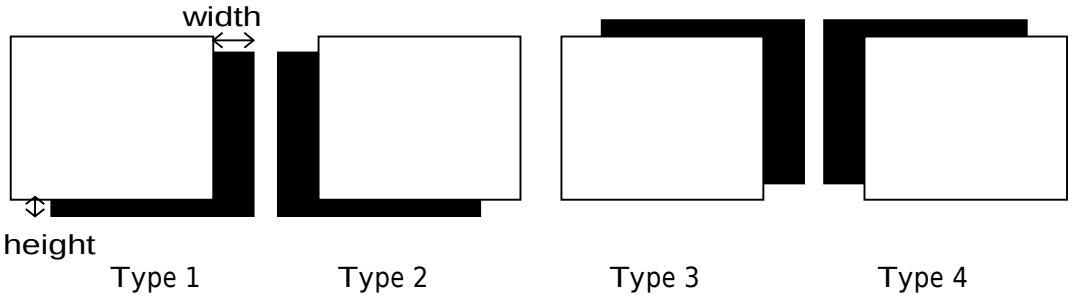
		0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 7 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 7 Enable 0: Disable 1: Enable



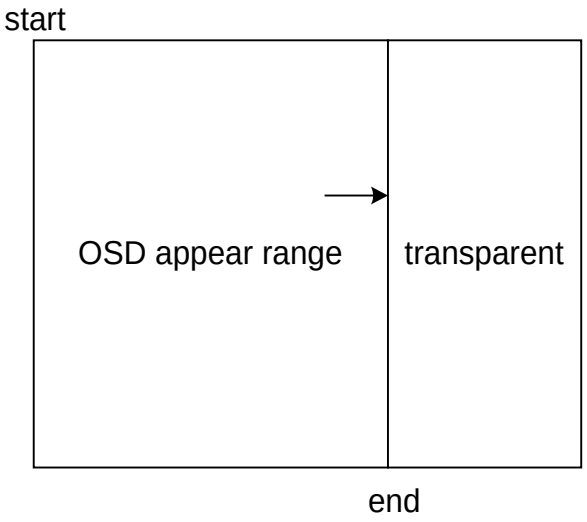
3D Button Type 1



3D Button Type 2



Shadow in all direction



Window mask fade/in out function

Frame control registers

Address: 000h

Byte 0

Bit	Mode	Function
7:0	W	Vertical Delay [8:1] The bits define the vertical starting address. Total 512 step unit: 4 line

Vertical delay minimum should set 1

Byte 1

Bit	Mode	Function
7:0	W	Horizontal Delay [9:2] The bits define the horizontal starting address. Total 1024 step unit:4 pixels

Horizontal delay minimum should set 2

Byte 2

Bit	Mode	Function
7:6	W	Horizontal Delay bit [1:0]
5	W	Vertical Delay [0]
4	W	Global Blinking Enable 0: Disable 1: Enable Note: In order to make blinking function work, add redundant OSD row command to next DVS occurrence.
3:2	W	Display zone, for smaller character width 00: middle 01: left 10: right 11: reserved
1	W	Rotation 0: Normal (data latch 24 bit per 24 bit) 1: Rotation (data latch 18 bit per 24 bit)
0	W	OSD enable 0: OSD circuit is inactivated 1: OSD circuit is activated

When OSD is disabled, Double Width (address 0x002 Byte1[1]) must be disabled to save power.

PWM Duty Width
Address: 001h

Byte 0

Bit	Mode	Function
7:0	W	PWM_0 8bits decides the output duty width and waveform of PWM at PWM channel

Byte 1

Bit	Mode	Function
7:0	W	PWM_1 8bits decides the output duty width and waveform of PWM at PWM channel

Byte 2

Bit	Mode	Function
7:0	W	PWM_2 8bits decides the output duty width and waveform of PWM at PWM channel

PWM _Control
Address: 002h

Byte 0 default: xxxx_xxx0b

Bit	Mode	Function
7	--	Reserved
6	W	Enable Window 7 Mask OSD-Appear-Range Control for Fade In/Out
5	W	Window 7 Mask 0: Mask area appears 1: Mask area transparent
4	W	OSD vertical start input signal source select 0: Select DVS as OSD VSYNC input 1: Select ENA as OSD VSYNC input
3:2	W	00:PWM_CLK/1 01:PWM_CLK/2 10:PWM_CLK/4 11:PWM_CLK/8
1	W	PWM Clock Source From 0:DCLK , 1:Crystal Clock
0	W	Enable PWM output

Byte 1

Bit	Mode	Function
7:4	W	Char shadow/border color
3	W	Blending Enable
2	W	Blending type 0: All blending (including window, character, character background~~, cursor~~) 1: Only window and character background blending
1	W	Double width enable (For all OSD including windows and characters) 0: Normal 1: Double
0	W	Double Height enable (For all OSD including windows and characters) 0: Normal 1: Double

Byte 2

Bit	Mode	Function
7:6	W	Font downloaded swap control 0x: No swap 10: CCW 11: CW
5:0	--	Reserved

Bit	7	6	5	4	3	2	1	0
Firmware	A	B	C	D	E	F	G	H
CW	A	E	B	F	C	G	D	H
CCW	E	A	F	B	G	C	H	D

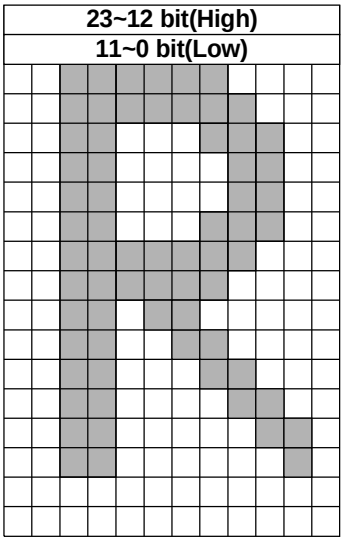


Figure 3 Non-rotated memory alignments

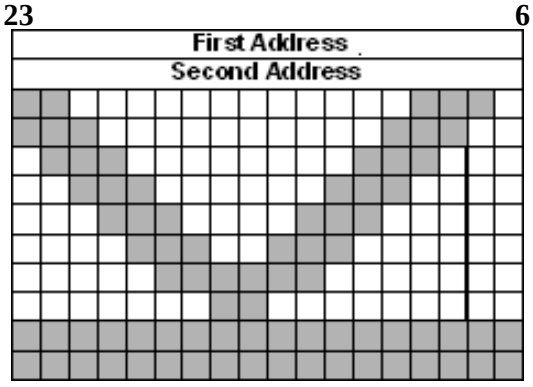


Figure 4 Rotated memory alignments

Base address offset

Address: 003h

Byte 0

Bit	Mode	Function
7:0	W	Font Select Base Address[7:0]

Byte 1

Bit	Mode	Function
7:4	W	Font Select Base Address[11:8]
3:0	W	Font Base Address[3:0]

Byte 2

Bit	Mode	Function
7:0	W	Font Base Address[11:4]

OSD SRAM (Map and font registers)

R0	R1	R2	….			Rn	End				
C01	C02	B03	C04	…		C11	C12	C13	…		
…											
…											
…			Cn1	Cn2	…		1-bit font start		…		
…											
…			2-bit font start				…				
…											
4-bit font start			…								
…											
…											

11.25k bytes SRAM

1. Row Command

R0	R1	R2	R3	R….	Rn	End

Row Command R0~Rn represent the start of new row. Each command contains 3 bytes data which define the length of a row and other attributes. OSD End Command represent the end of OSD. R0 is set in address 0 of SRAM.

2. Character/Blank Command (Font Select)

Character Command is used to select which character font is show. Each command contains three bytes which specify its attribute and 1,2 or 4bit per pixel. Blank Command represents blank pixel to separate the preceding character and following character. Use two or more Blank Command if the character distance exceeds 255 pixel.

The Font Select Base Address in Frame Control Register represents the address of the first character in Row 0, that is, C01 in the above figure. The following character/blank is write in the next address. C11 represents the first character in Row1, C12 represents the second character in Row1, and so on.

The address of the first character Cn1 in Row n = Font Select Base Address + Row 0 font base length + Row 1 font base length + …+Row n-1 font base length.

3. Font

User fonts are stored as bit map data. For normal font, one font has 12x18 pixel, and for rotation font, one has 18x12 pixel. One pixel use 1, 2 or 4 bits.

For 12x18 font,

One 1-bit font requires 9 * 24bit SRAM

One 2-bit font requires 18 * 24bit SRAM

One 4-bit font requires 36 * 24bit SRAM

For 18x12 font,
One 1-bit font requires 12 * 24bit SRAM
One 2-bit font requires 24 * 24bit SRAM
One 4-bit font requires 48 * 24bit SRAM

Font Base Address in Frame Control Register point to the start of 1-bit font.
For normal (12x18) font:
1-bit Font, if CS = 128, Real Address of Font = Font Base Address + 9 * 128
2-bit Font, if CS = 128, Real Address of Font = Font Base Address + 18 * 128
4-bit Font, if CS = 128, Real Address of Font = Font Base Address + 36 * 128
For rotational (18x12) font:
1-bit Font, if CS = 128, Real Address of Font = Font Base Address + 12 * 128
2-bit Font, if CS = 128, Real Address of Font = Font Base Address + 24 * 128
4-bit Font, if CS = 128, Real Address of Font = Font Base Address + 48 * 128
where CS is Character Selector in Character Command.
Note that Row Command, Font Select and Font share the same OSD SRAM.

When we download the font, we have to set the Frame control 002h byte1 [1:0] to set the method of hardware bit swap. If the OSD is Counter-Clock-Wise rotated, we have to set to 0x01 (the 8 bits of every byte of font SRAM downloaded by firmware will be in a sequence of "7 5 3 1 6 4 2 0" (from MSB to LSB) and should be rearranged to "7 6 5 4 3 2 1 0" by hardware). If it is Clock-Wise rotated, we have to set to 0x10 (the 8 bits of every byte of font SRAM downloaded by firmware will be in a sequence of "6 4 2 0 7 5 3 1" (from MSB to LSB) and should be rearranged to "7 6 5 4 3 2 1 0" by hardware). After we finish the downloading or if we don't have to rotate the OSD, we have to set it to 0x00.

Row Command

Byte 0

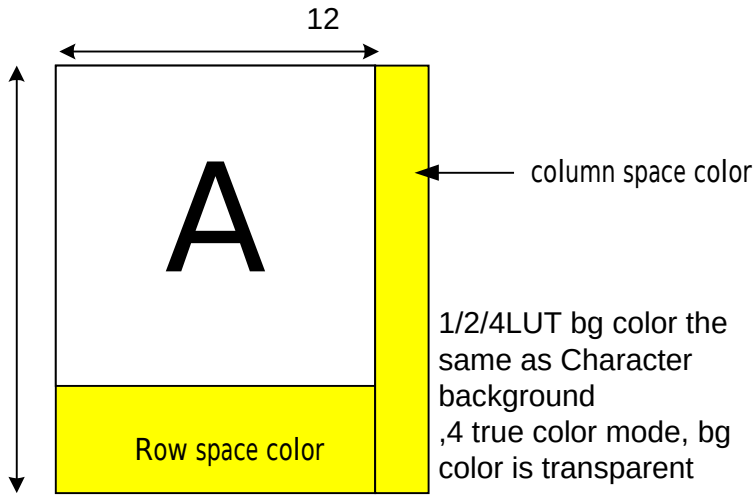
Bit	Mode	Function
7	W	1: Row Start Command 0: OSD End Command Each row must start with row-command, last word of OSD map must be end-command
6:5	W	Reserved
4:2	W	Character border/shadow 000: None 001: Border 100: Shadow (left-top) 101: Shadow (left-bottom) 110: Shadow (right-top) 111: Shadow (right-bottom)
1	W	Double character width 0: x1 1: x2
0	W	Double character height 0: x1 1: x2

Byte 1

Bit	Mode	Function
7:3	W	Row height (1~32)
2:0	W	Column space 0~7 pixel column space When Char is doubled, so is column space.

Notice:
When character height/width is doubled, the row height/column space definition also twice. If the row height is larger than character height, the effect is just like space between rows. If it is smaller than character height, it will drop last several bottom line of character.

When using 1/2/4LUT font, column space and font smaller than row height, the color of column space and row space is the same as font background color, only 4 bit true color font mode, the color is transparent



Byte 2

Bit	Mode	Function	
7:0	W	Row length	unit: font base

Blank Command

Byte 0

Bit	**Mode**	**Function**
7	W	0
6	W	Blinking effect 0: Disable 1: Enable
5:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Blank pixel length

At least 3 pixels, and can't exceed 255 pixels.

Byte 2

Bit	Mode	Function
7:5	W	Reserved
4	W	Reserved
3:0	W	Blank color – select one of 16-color LUT (0 is special for transparent)

Character Command (For 1-bit RAM font)

Byte 0

Bit	Mode	Function
7	W	1
6	W	Character Blinking effect 0: Disable 1: Enable
5:4	W	00 (Font type 00: 1-bit RAM Font 01: 4-bit RAM Font 1x: 2-bit RAM Font)
3:0	W	Character width (only for 1-pixel font, doubled when specifying double-width in Row/Blank command register) **For 12x18 font:** 0100: 4-pixel 0101: 5-pixel 0110: 6-pixel 0111: 7-pixel 1000: 8-pixel 1001: 9-pixel 1010: 10-pixel 1011:11-pixel 1100: 12-pixel **For 18x12 Font (rotated)** 0000: 4-pixel 0001: 5-pixel 0010: 6-pixel 0011: 7-pixel 0100: 8-pixel 0101: 9-pixel 0110: 10-pixel 0111: 11-pixel 1000: 12-pixel 1001:13-pixel 1010:14-pixel 1011:15-pixel 1100: 16-pixel 1101:17-pixel 1110:18-pixel

When using border/shadow/ effect, the width of the 1-bit font should at least 6 pixel.

Byte 1

Bit	Mode	Function
7:0	W	Character Select [7:0]

Byte 2

Bit	Mode	Function
7:4	W	Foreground color Select one of 16-color from color LUT
3:0	W	Background color

		Select one of 16-color from color LUT (0 is special for transparent)

Character command (For 2-bit RAM Font)

Byte 0

Bit	Mode	Function
7	W	1
6	W	Character Blinking effect 0: Disable 1: Enable
5	W	1
4	W	MSB for 16-color LUT
3:1	W	Foreground color 11 Select one of 8 color from color LUT Add Byte0[4] as MSB for 16-color LUT.
0	W	Background color 00 Bit[2] Select one of 8 color from color LUT

Byte 1

Bit	Mode	Function
7:0	W	Character Select [7:0]

Byte 2

Bit	Mode	Function
7:6	W	Background color 00 Bit[1:0] Select one of 8 color from color LUT Add Byte0[4] as MSB for 16-color LUT. While 0 is special for transparent
5:3	W	Foreground color 10 Select one of 8 color from color LUT Add Byte0[4] as MSB for 16-color LUT.
2:0	W	Foreground color 01 Select one of 8 color from color LUT Add Byte0[4] as MSB for 16-color LUT.

Character command (For 4-bit RAM font)

Byte 0

Bit	Mode	Function
7	W	1
6	W	Character Blinking effect 0: Disable 1: Enable
5:4	W	01 (Font type 00: 1-bit RAM Font 01: 4-bit RAM Font 1x: 2-bit RAM Font)
3:0	W	(for Byte1[7] = 0) select one color from 16-color LUT as background (for Byte1[7] = 1) Red color level MSB 4 bits for 8 bits color level (LSB 4 bits are 1111)

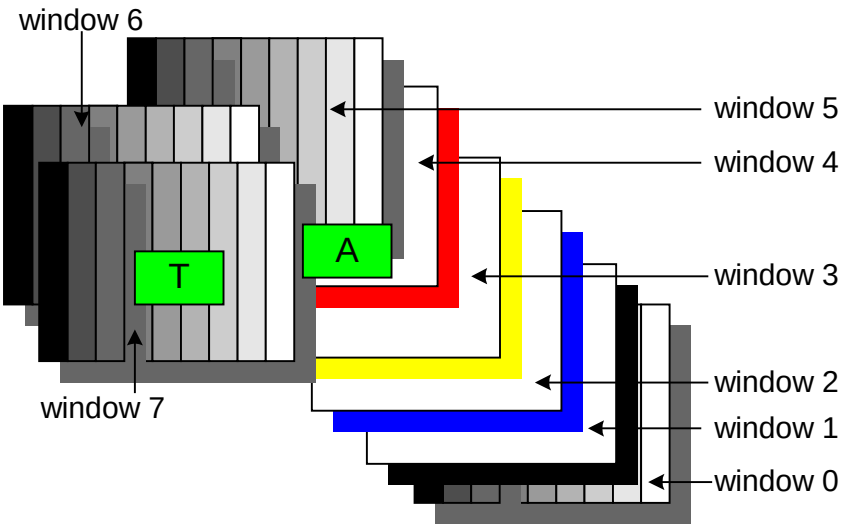
Byte 1

Bit	Mode	Function
7	W	0: 4bit Look Up Table, 0000'b is transparent. 1: 3bit specify R,G,B pattern, color level defined in Byte0[3:0],Byte2. One mask bit defines foreground or background.
6:0	W	Character Select [6:0]

- 當 4-bit look-up table mode時，column space 跟 background 顏色一樣。
- 當爲 4-bit look-up table mode時，當 pixel 爲 0000, byte0[3:0] 爲 0000 時是 transparent.
- 當爲 true color 模式時，pixel 爲 0000 時，定義爲 transparent。

Byte 2

Bit	Mode	Function
7:4	W	(for Byte1[7] = 1) Green color level MSB 4 bits for 8 bits color level (LSB 4 bits are 1111)
3:0	W	(for Byte1[7] = 1) Blue color level MSB 4 bits for 8 bits color level (LSB 4 bits are 1111)

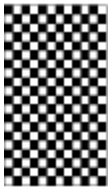


Display Priority

We have four windows with gradient and four windows without gradient, the window priority is as above, character should be always on the top layer of the window.

Pattern gen.
Use OSD to replace display pattern generator.

Chess Board: make a font as below



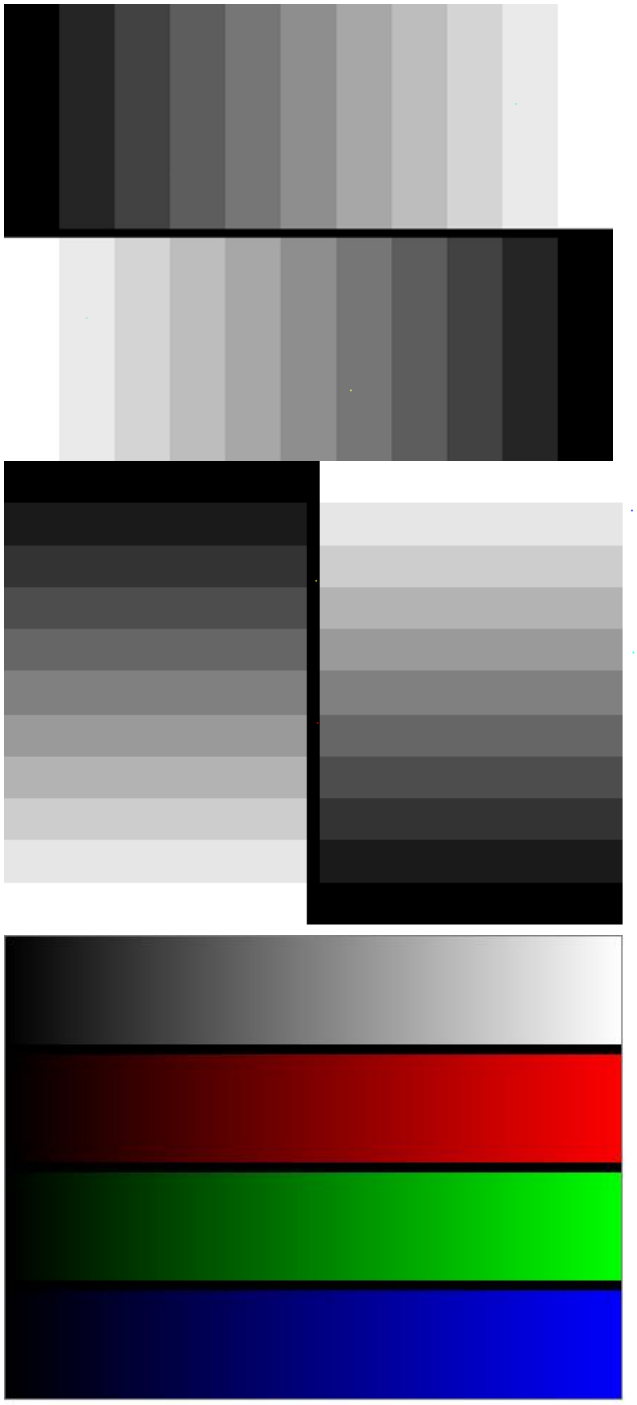
If we want to fill to the full 1280x1024 screen with character, we need 1280*1024 pixels. Required character is:
Using 12*18 font
1280/12 = 106.7 -> 107
1024/18 = 56.9 -> 57
107*57 = 6099 character

The required number of character map is larger than RAM size. We must turn on double width or double height function to reduce the half of character map.

So the basic unit to chessboard is 2x2 pixel. You can use larger chessboard instead of 2x2 pixels unit, such as 4x4 and so on.

Gray level

We can display 256 gray level by gradient window, 8 and 16 gray level by character map. 32 and 64 gray level is not supported.



Electric Specification

DC Characteristics

Table 3 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Voltage on VDD	V_{VDD}	-1		4.6	V
Voltage on Input (5V tolerant)	V_{IN}	-1		5.5	V
Voltage on Output or I/O or NC	V_{IO}	-1		4.6	V
Electrostatic Discharge	V_{ESD}			±2.5	kV
Latch-Up	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	ºC
Storage temperature (plastic)	T_{STG}	-55		125	ºC
Thermal Resistance (Junction to Air)	θ_{JA}			18	ºC/W

Table 4 DC Characteristics/Operating Condition

(0℃<TA<70℃; VDD = 3.3V ± 0.3V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	VDD	3.0	3.3	3.6	V
Supply Current(All function on at 135M)	I_{VDD}		255.2		mA
● digital supply	I_{DVCC}		244		
● DCLK PLL supply	I_{AVCC}		5.2		
● MCLK PLL supply	I_{PVCC}		6		
Supply Current(Power Saving)	I_{VDD}		7.2		mA
● digital supply	I_{DVCC}		5.6		
● DCLK PLL supply	I_{AVCC}		0.6		
● MCLK PLL supply	I_{PVCC}		1		
Output High Voltage	V_{OH}	2.4		VDD	V
Output Low Voltage	V_{OL}	GND		0.5	V
Input High Voltage	V_{IH}	2.0			V
Input Low Voltage	V_{IL}			0.8	V
I/O Pull-up resistance	R_{PU}	100		300	Ω
I/O Pull-down resistance	R_{PD}	50		150	Ω
Input Leakage Current(VI=VCC or GND)	I_{LI}	-10		+10	µA
Output Leakage Current(VO=VCC or GND)	I_{LO}	-20		+20	µA

AC Characteristics

Input Signal

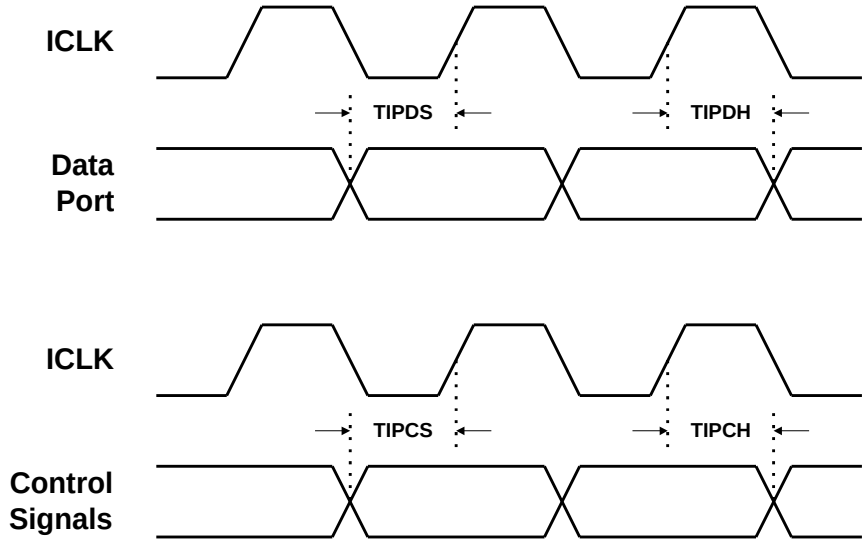


Figure 17 Input Signal Timing

Symbol	Parameter	Min	Max	Unit
TIPCS	Input control signals setup time for ICLK	2		ns
TIPCH	Input control signals hold time for ICLK	1		ns
TIPDS	Input data setup time for ICLK	2		ns
TIPDH	Input data hold time for ICLK	1		ns

Output Signal

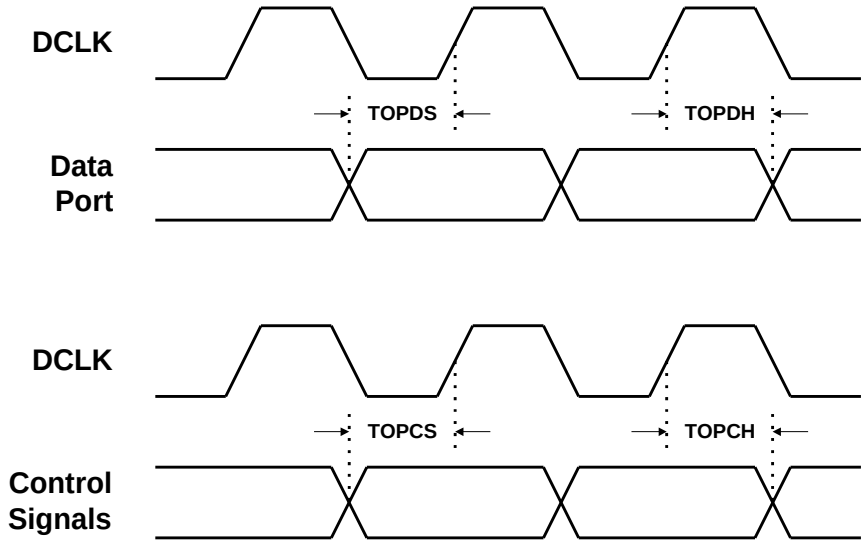


Figure 18 Output Signal Timing

Symbol	Parameter	Min	Max	Unit
TOPCS	Output control signals setup time for	4		ns
TOPCH	Output control signals hold time for	1		ns
TOPDS	Output data setup time for DCLK	4		ns
TOPDH	Output data hold time for DCLK	1		ns

Serial Port Signal

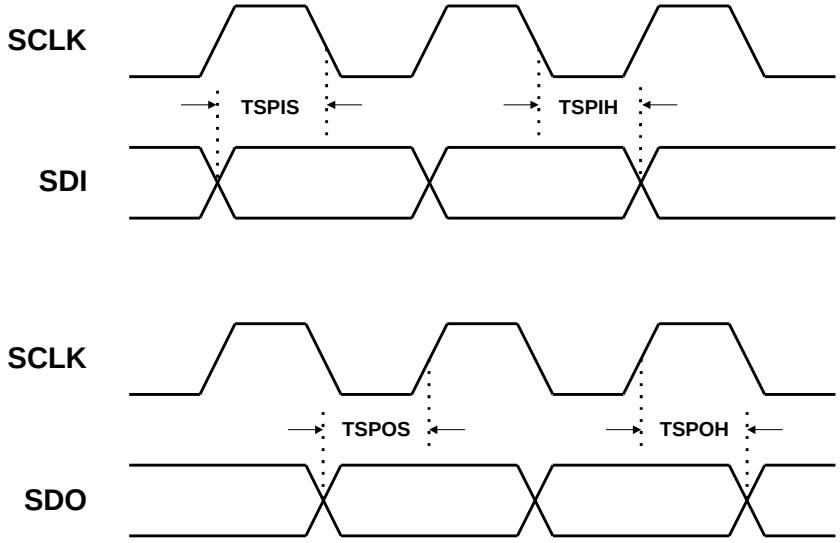
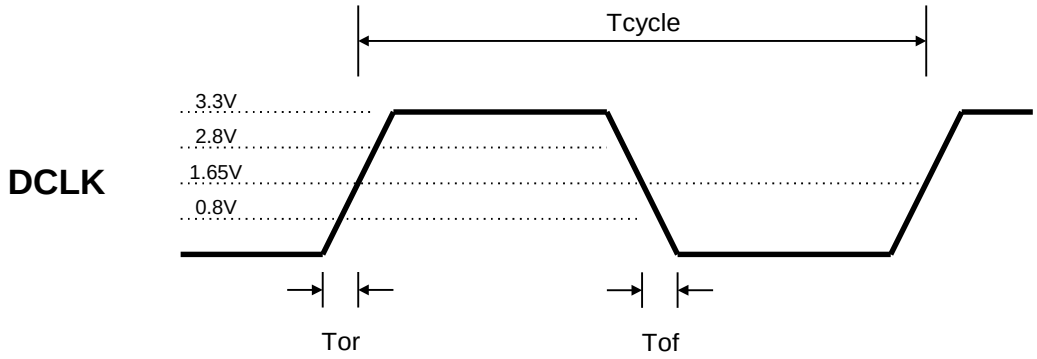


Figure 19 Serial Port Signal Timing

Symbol	Parameter	Min	Max	Unit
TSPIS	Serial port input signal setup time for	2		ns
TSPIH	Serial port input signal hold time for	8		ns
TSPOS	Serial port output signal setup time for	1/3		TCK
TSPOH	Serial port output signal for SCLK	1/2		TCK

1.44.4 PLL

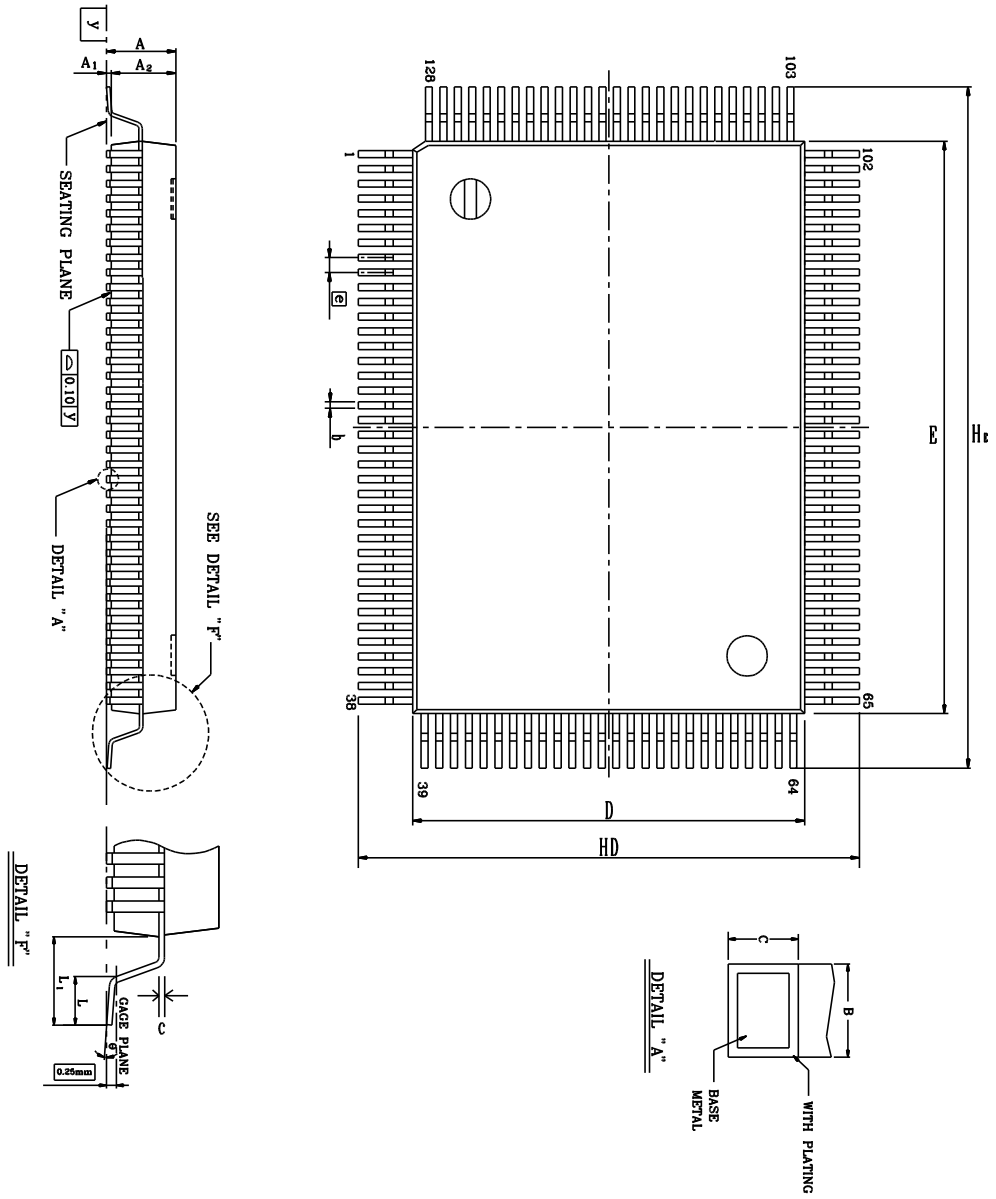


Electrical Characteristics

Characteristics	Symbol	Conditions	Mix	Type	Max	Unit
Output rise time (20pf Load)	Tor	From 0.8V to 2.0V,Vdd=3.3V			2.0	ns
Output fall time (20pf Load)	Tof	From 2.0V to 0.8V,Vdd=3.3V			2.0	ns
Duty cycle (20pf Load, at 1.5V)	Tduty	DCLK	45	50	55	%
Clock Skew (20pf Load, at 1.5V)	Tskw1	DCLK to DCLK			250	ps
Jitter, Absolute (20pf Load)	Tj1	DCLK			300	ps

Mechanical Specification

1.45 128 Pin Package



Note:

Symbol	Dimension in inch			Dimension in mm		
	Min	Type	Max	Min	Type	Max
A	—		0.134	—	—	3.40
A_1	0.004	0.010	0.036	0.10	0.25	0.91
A_2	0.102	0.112	0.122	2.60	2.85	3.10
b	0.005	0.009	0.013	0.12	0.22	0.32
c	0.002	0.006	0.010	0.05	0.15	0.25
D	0.541	0.551	0.561	13.75	14.00	14.25
E	0.778	0.787	0.797	19.75	20.00	20.25
e	0.010	0.020	0.030	0.25	0.5	0.75
H_D	0.665	0.677	0.689	16.90	17.20	17.50
H_E	0.902	0.913	0.925	22.90	23.20	23.50
L	0.027	0.035	0.043	0.68	0.88	1.08
L_1	0.053	0.063	0.073	1.35	1.60	1.85
y	—	—	0.004	—	—	0.10
θ	0°	—	12°	0°	—	12°

1.Dimension D & E do not include interlead flash.
2.Dimension b does not include dambar protrusion/intrusion.
3.Controlling dimension: Millimeter
4.General appearance spec. should be based on final visual inspection spec.

TITLE : 128LD QFP (14x20 mm*2) PACKAGE OUTLINE -CU L/F, FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	530-ASS-P004
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	Q128 - 1
		DATE	MAR. 25.1997
REALTEK SEMI-CONDUCTOR CO., LTD			