



DESCRIPTION

PT6315-S is a Vacuum Fluorescent Display (VFD) Controller driven on a 1/4 to 1/8 duty factor. Eight segment output lines, 4 grid output lines, 4 segment/grid output drive lines, one display memory, control circuit, key scan circuit are all incorporated into a single chip to build a highly reliable peripheral device for a single chip micro computer. Serial data is fed to PT6315-S via a three-line serial interface. It is housed in a 28pins, SOP.

FEATURES

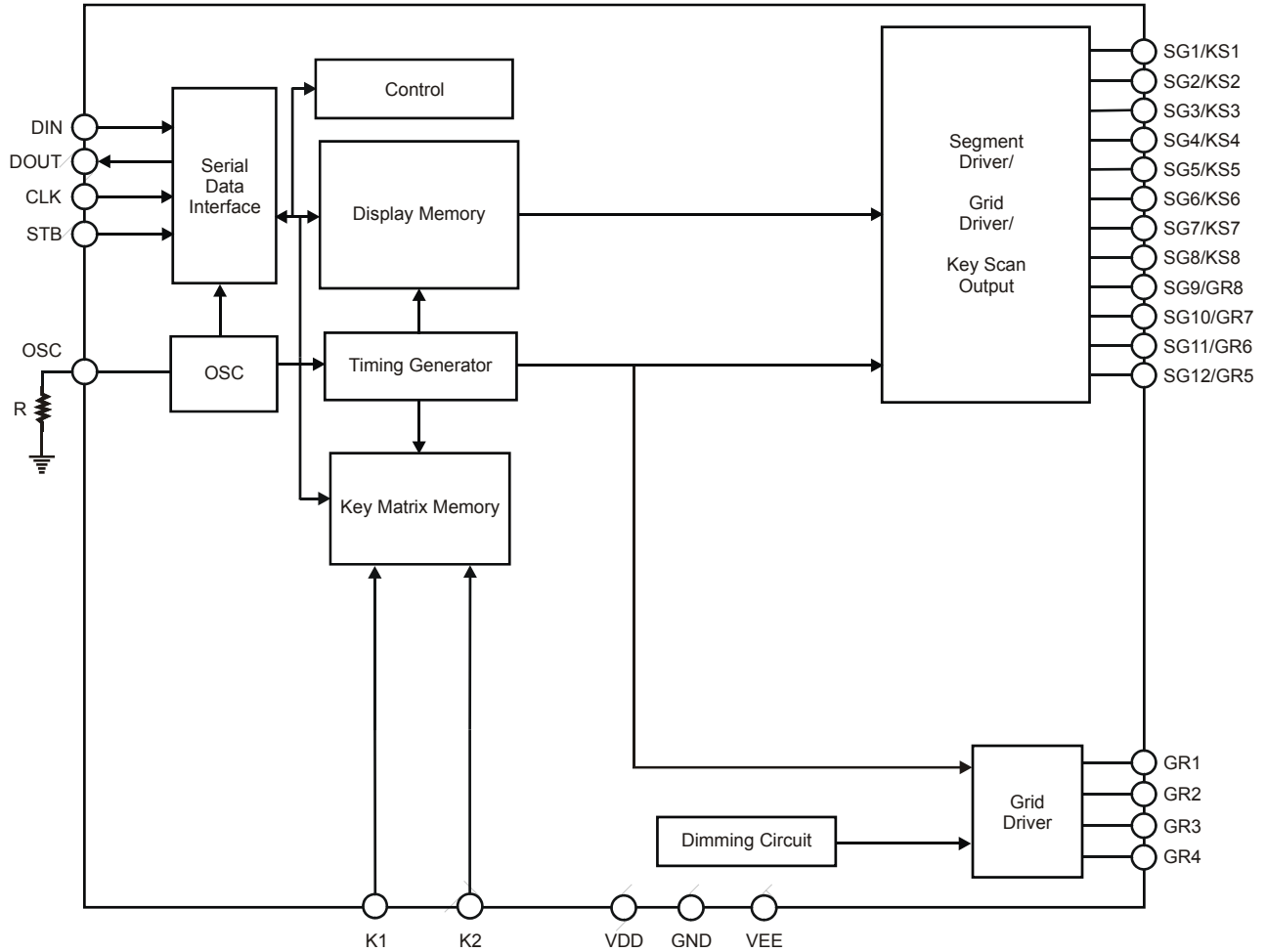
- CMOS Technology
- Low Power Consumption
- Key Scanning (8 x 2 matrix)
- Multiple Display Modes: (8 Segments, 8 Digits to 12 Segments, 4 Digits)
- 8-Step Dimming Circuitry
- Serial Interface for Clock, Data Input, Data Output, Strobe Pins
- No External Resistors Needed for Driver Outputs
- Available in 28pins, SOP

APPLICATION

- Microcomputer Peripheral Devices

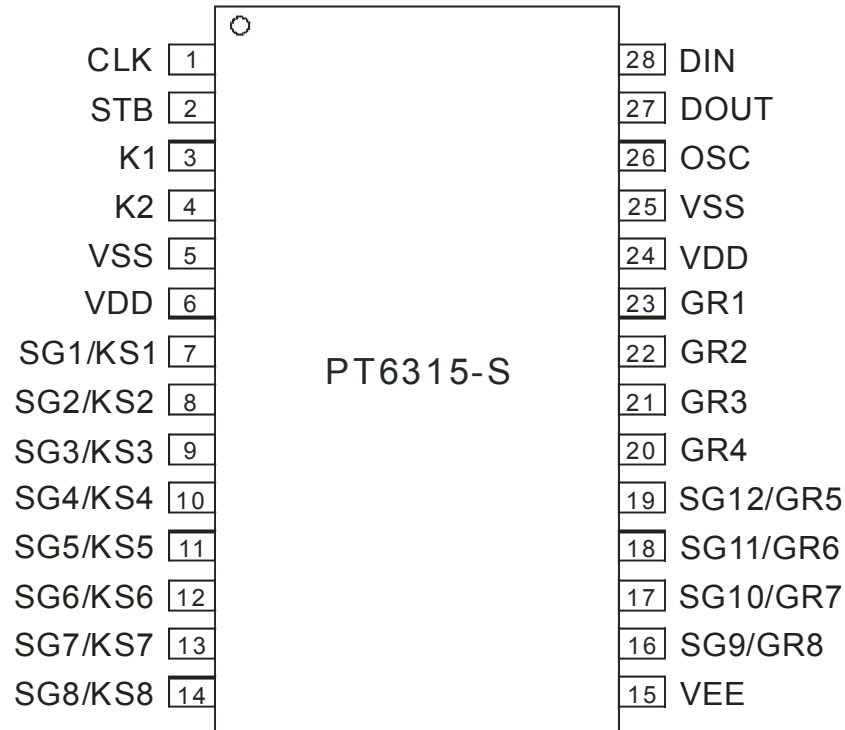


BLOCK DIAGRAM





PIN CONFIGURATION





PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
CLK	I	Clock Input Pin This pin reads serial data at the rising edge and outputs data at the falling edge.	1
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is "HIGH", CLK is ignored.	2
K1 to K2	I	Key Data Input Pins The data sent to these pins are latched at the end of the display cycle.	3, 4
VSS	-	Logic Ground Pin	5, 25
VDD	-	Logic Power Supply	6, 24
SG1/KS1 to SG8/KS8	O	High Voltage Segment Output Pins Also acts as the Key Source	7 to 14
VEE	-	Pull Down Level	15
SG9/GR8 to SG12/GR5	O	High Voltage Segment/Grid Output Pins	16 to 19
GR4 to GR1	O	High Voltage Grid Output Pins	20 to 23
OSC	I	Oscillator Input Pin A resistor is connected to this pin to determine the oscillation frequency.	26
DOUT	O	Data Output Pin (N-Channel, Open Drain) This pin outputs serial data at the falling edge of the shift clock (starting from the lower bit).	27
DIN	I	Data Input Pin This pin inputs serial data at the rising edge of the shift clock (starting from the lower bits).	28



FUNCTION DESCRIPTION

COMMANDS

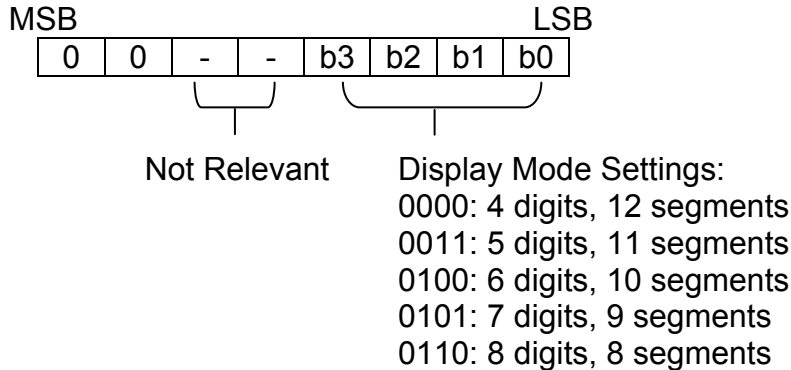
Commands determine the display mode and status of PT6315-S. A command is the first byte (b0 to b7) inputted to PT6315-S via the DIN Pin after STB Pin has changed from “HIGH” to “LOW” State. If for some reason the STB Pin is set to “HIGH” while data or commands are being transmitted, the serial communication is initialized, and the data/commands being transmitted are considered invalid.

COMMAND 1: DISPLAY MODE SETTING COMMANDS

PT6315-S provides 4 display mode settings as shown in the diagram below: As stated earlier a command is the first one byte (b0 to b7) transmitted to PT6315-S via the DIN Pin when STB is “LOW”. However, for these commands, the bits 5 to 6 (b4 to b5) are ignored, bits 7 & 8 (b6 to b7) are given a value of “0”.

The Display Mode Setting Commands determine the number of segments and grids to be used (1/4 to 1/8 duty, 12 to 8 segments). When these commands are executed, the display is forcibly turned off, the key scanning stops. A display “ON” command must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned “ON”, the 8-digit, 8-segment mode is selected.





VFD Driver/Controller IC **PT6315-S**

Display Mode and RAM Address

Data transmitted from an external device to PT6315-S via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of PT6315-S are given below in 8 bits unit.

SG1	SG4	SG5	SG8	SG9	SG12	
00H		01H		02H		DGT1
03H		04H		05H		DGT2
06H		07H		08H		DGT3
09H		0AH		0BH		DGT4
12H		13H		14H		DGT5
15H		16H		17H		DGT6
18H		19H		1AH		DGT7
1BH		1CH		1DH		DGT8

b0							b7
SG1	SG2	SG3	SG4	X	X	X	X

b0							b7
SG5	SG6	SG7	SG8	X	X	X	X

b0							b7
X	X	SG9	SG10	SG11	SG12	X	X

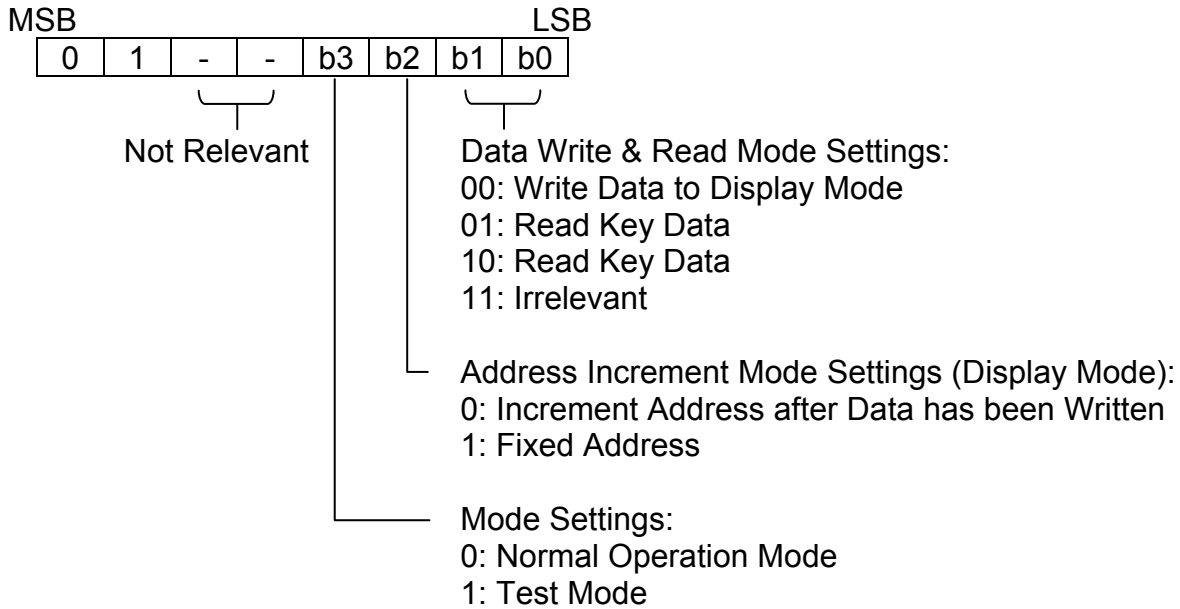
Notes: X=ignore this byte



COMMAND 2: DATA SETTING COMMANDS

The Data Setting Commands executes the Data Write or Data Read Modes for PT6315-S. The Data Setting Command, the bits 5 and 6 (b4, b5) are ignored, bit 7 (b6) is given the value of "1" while bit 8 (b7) is given the value of "0". Please refer to the diagram below.

When power is turned ON, the bit 4 to bit 1 (b3 to b0) are given the value of "0".



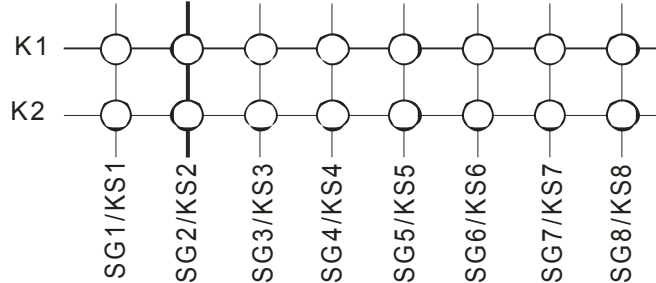


VFD Driver/Controller IC

PT6315-S

PT6315-S Key Matrix & Key Input Data Storage RAM

PT6315-S Key Matrix consists of an 8 x 12 array as shown below:



Each data entered by each key is stored as follows. They are read by a READ Command, starting from the last significant bit. When the most significant bit of the data (SG8, b7) has been read, the least significant bit of the next data (SG0, b1) is read.

K1.....K1	K1.....K2	K1.....K2	K1.....K2	↓ Reading Sequence
SG1/KS1	SG2/KS2	SG3/KS3	SG4/KS4	
*	*	*	*	
SG5/KS5	SG6/KS6	SG7/KS7	SG8/KS8	
b0.....b1	b2.....b3	b4.....b5	b6.....b7	

Note: * = These sections are not relevant but are needed to read the transmission clock.

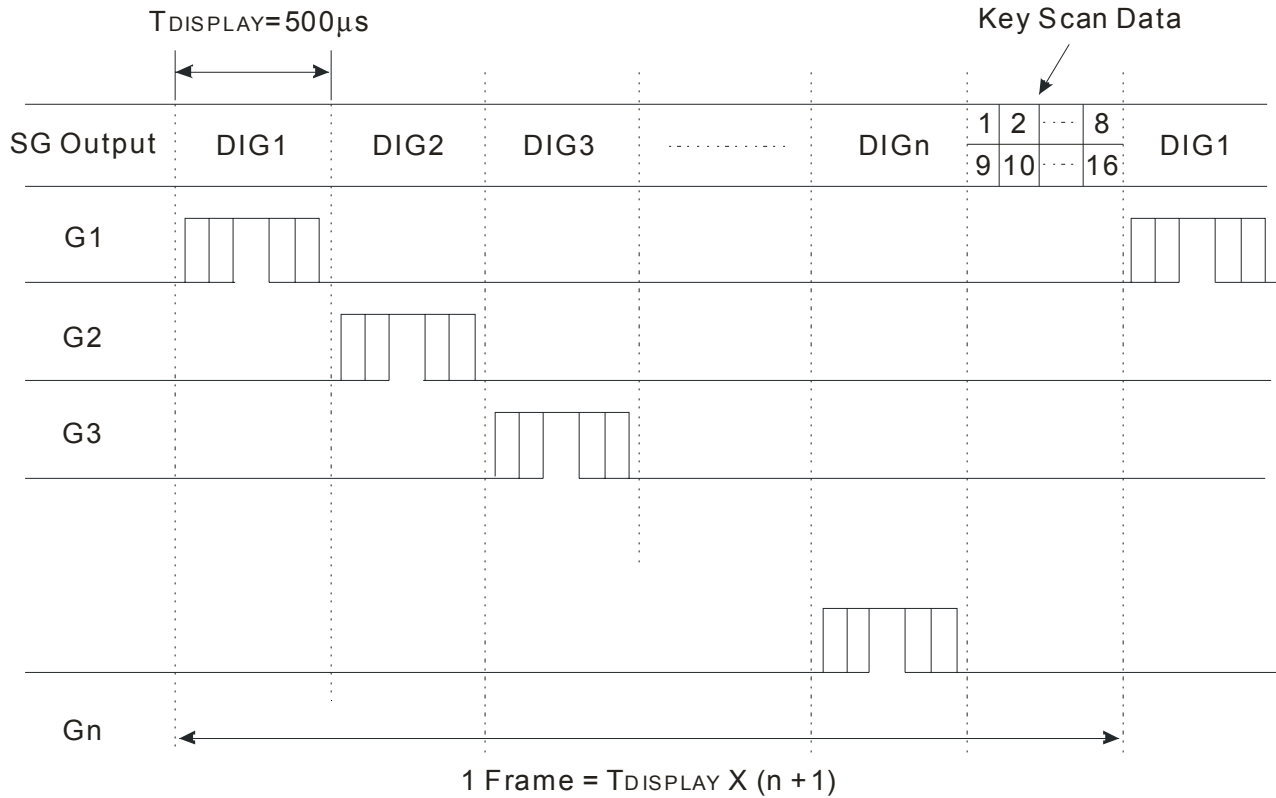


VFD Driver/Controller IC PT6315-S

SCANNING AND DISPLAY TIMING

The Key Scanning and display timing diagram is given below. One cycle of key scanning consists of 2 frames. The data of the 8 x 2 matrix is stored in the RAM.

Internal Operating Frequency (f_{osc}) = 224/T

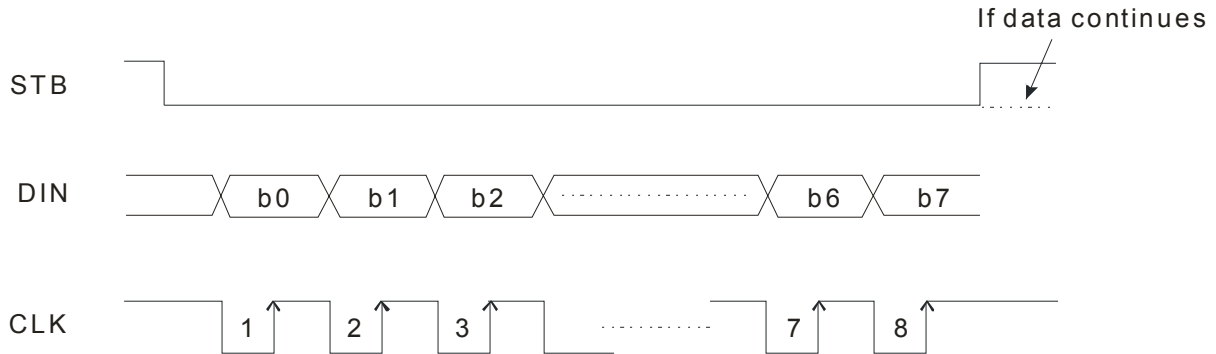




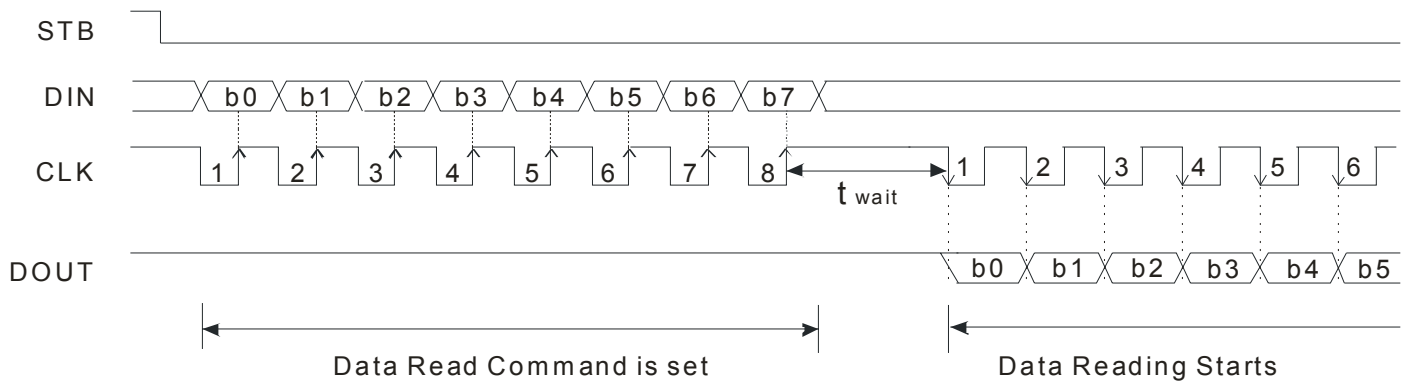
SERIAL COMMUNICATION FORMAT

The following diagram shows the PT6315-S serial communication format. The DOUT Pin is an N-channel, open-drain output pin, therefore, it is highly recommended that an external pull-up resistor (1KΩ to 10KΩ) must be connected to DOUT.

RECEPTION (DATA/COMMAND WRITE)



TRANSMISSION (DATA READ)



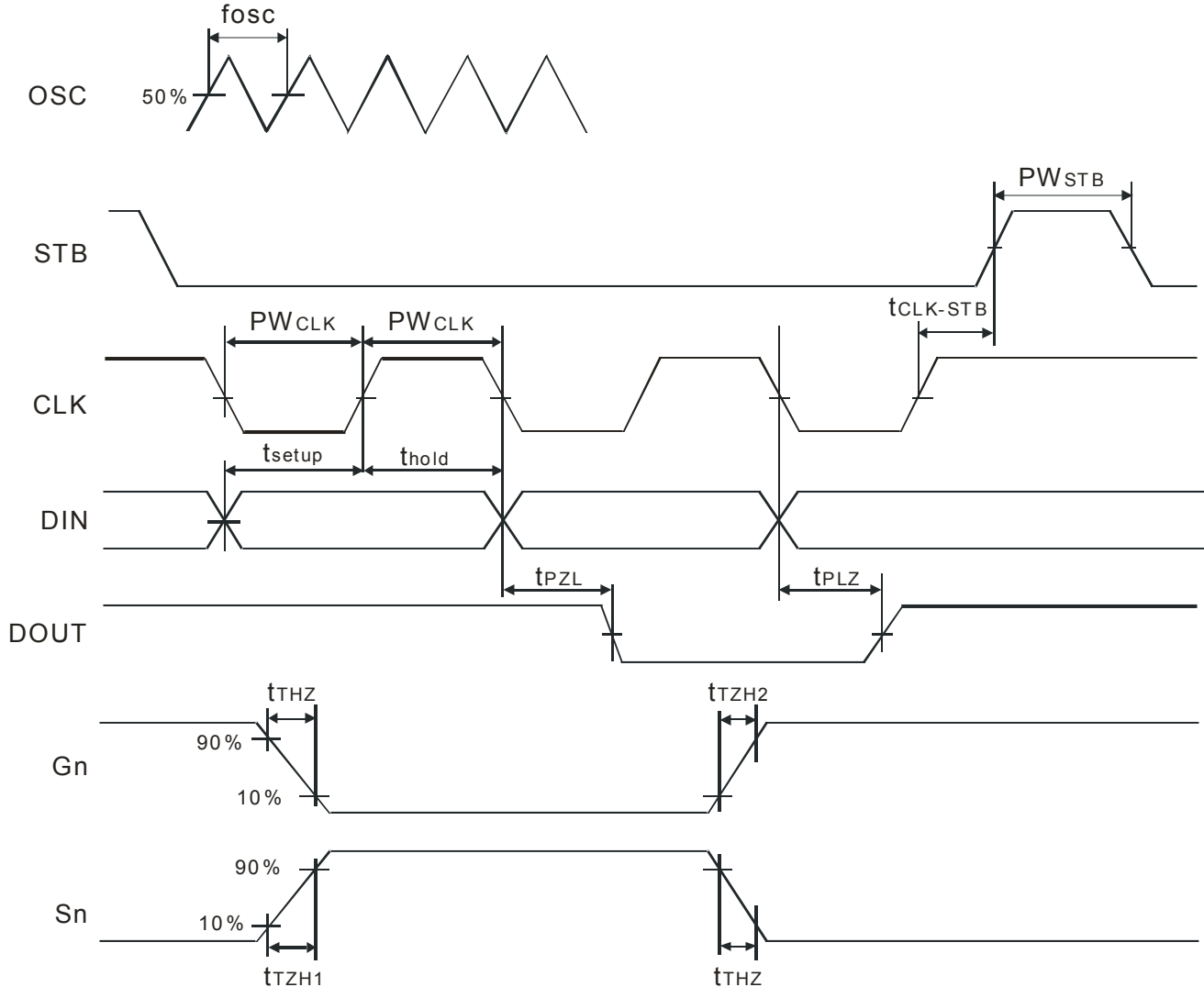
where: t_{wait} (waiting time) $\geq 1\mu s$

It must be noted that when the data is read, the waiting time (t_{wait}) between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data is greater or equal to $1\mu s$.



SWITCHING CHARACTERISTIC WAVEFORM

PT6315-S Switching Characteristics Waveform is given below.



where:

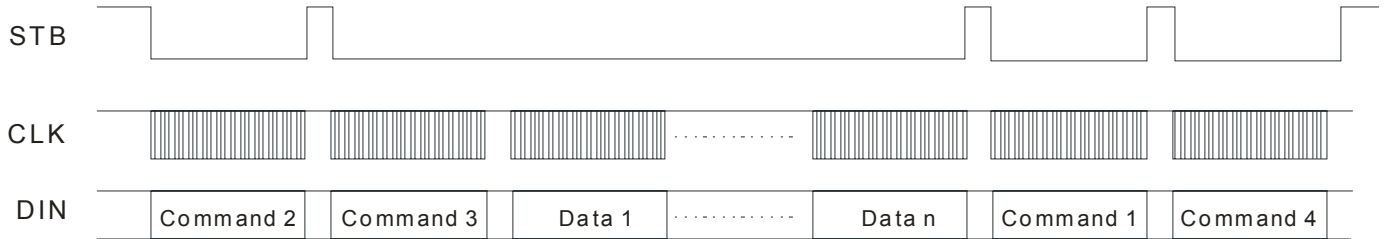
PW_{CLK} (Clock Pulse Width) $\geq 400ns$
 t_{setup} (Data Setup Time) $\geq 100ns$
 $t_{CLK-STB}$ (Clock - Strobe Time) $\geq 1\mu s$
 t_{TZH2} (Grid Rise Time) $\leq 0.5\mu s$ (at VDD=5V)
 t_{TZH2} (Grid Rise Time) $\leq 1.0\mu s$ (at VDD=3.3V)
 t_{TZH1} (Segment Rise Time) $\leq 2.0\mu s$ (at VDD=5V)
 t_{TZH1} (Segment Rise Time) $\leq 3.0\mu s$ (at VDD=3.3V)

PW_{STB} (Strobe Pulse Width) $\geq 1\mu s$
 t_{hold} (Data Hold Time) $\geq 100ns$
 t_{THZ} (Fall Time) $\leq 150\mu s$
 t_{PZL} (Propagation Delay Time) $\leq 100ns$
 t_{PLZ} (Propagation Delay Time) $\leq 400ns$
 f_{osc} = Oscillation Frequency



APPLICATIONS

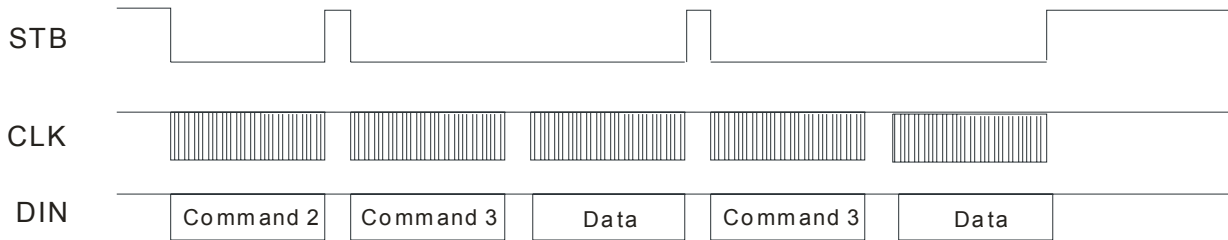
Display memory is updated by incrementing addresses. Please refer to the following diagram.



Where:

- Command 1: Display Mode Setting Command
- Command 2: Data Setting Command
- Command 3: Address Setting Command
- Data 1 to n: Transfer Display Data (24 Bytes max.)
- Command 4: Display Control Command

The following diagram shows the waveforms when updating specific addresses.

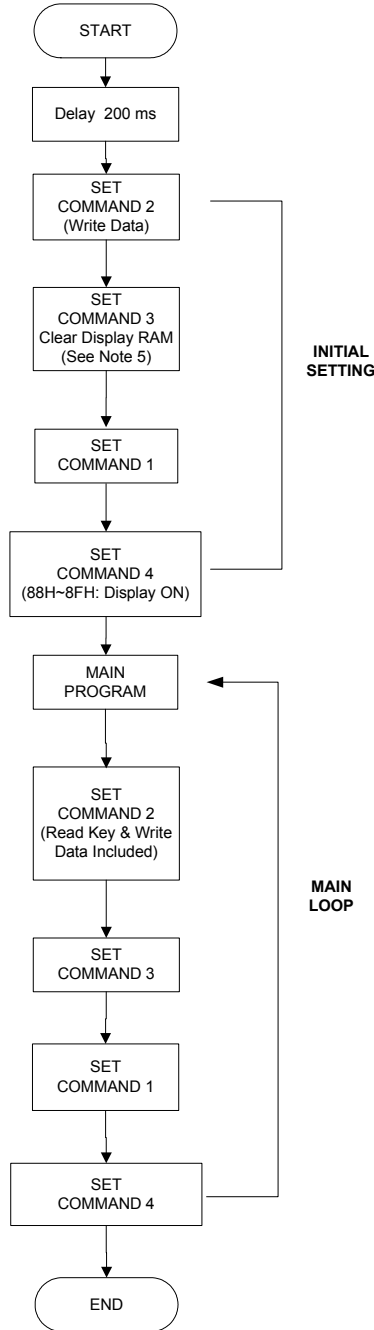


Where:

- Command 2: Data Setting Command
- Command 3: Address Setting Command
- Data: Display Data



RECOMMENDED SOFTWARE FLOWCHART



Notes:

1. Command 1: Display Mode Commands
2. Command 2: Data Setting Commands
3. Command 3: Address Setting Commands
4. Command 4: Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM are not defined; thus, it is strongly suggested that the contents of the Display RAM be cleared during the initial setting.



ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25°C, GND=0V)

Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	VDD	-0.5 to +7	V
Driver Supply Voltage	VEE	VDD +0.5 to VDD -40	V
Logic Input Voltage	VI	-0.5 to VDD +0.5	V
VFD Driver Output Voltage	VO	VEE -0.5 to VDD +0.5	V
VFD Driver Output Current	IOVFD	-40 (Grid) -15 (Segment)	mA
Operating Temperature	Topr	-40 to +85	°C
Storage Temperature	Tstg	-65 to +150	°C

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta=25°C, GND=0V)

Parameter	Symbol	Ratings			Unit
		Min.	Typ.	Max.	
Logic Supply Voltage	VDD	3.0	5	5.5	V
High-Level Input Voltage	VIH	0.7VDD	-	VDD	V
Low-Level Input Voltage	VIL	0	-	0.3VDD	V
Driver Supply Voltage	VEE	VDD -35	-	0	V



ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD=5V, GND=0V, VEE=VDD-35V, Ta=25°C)

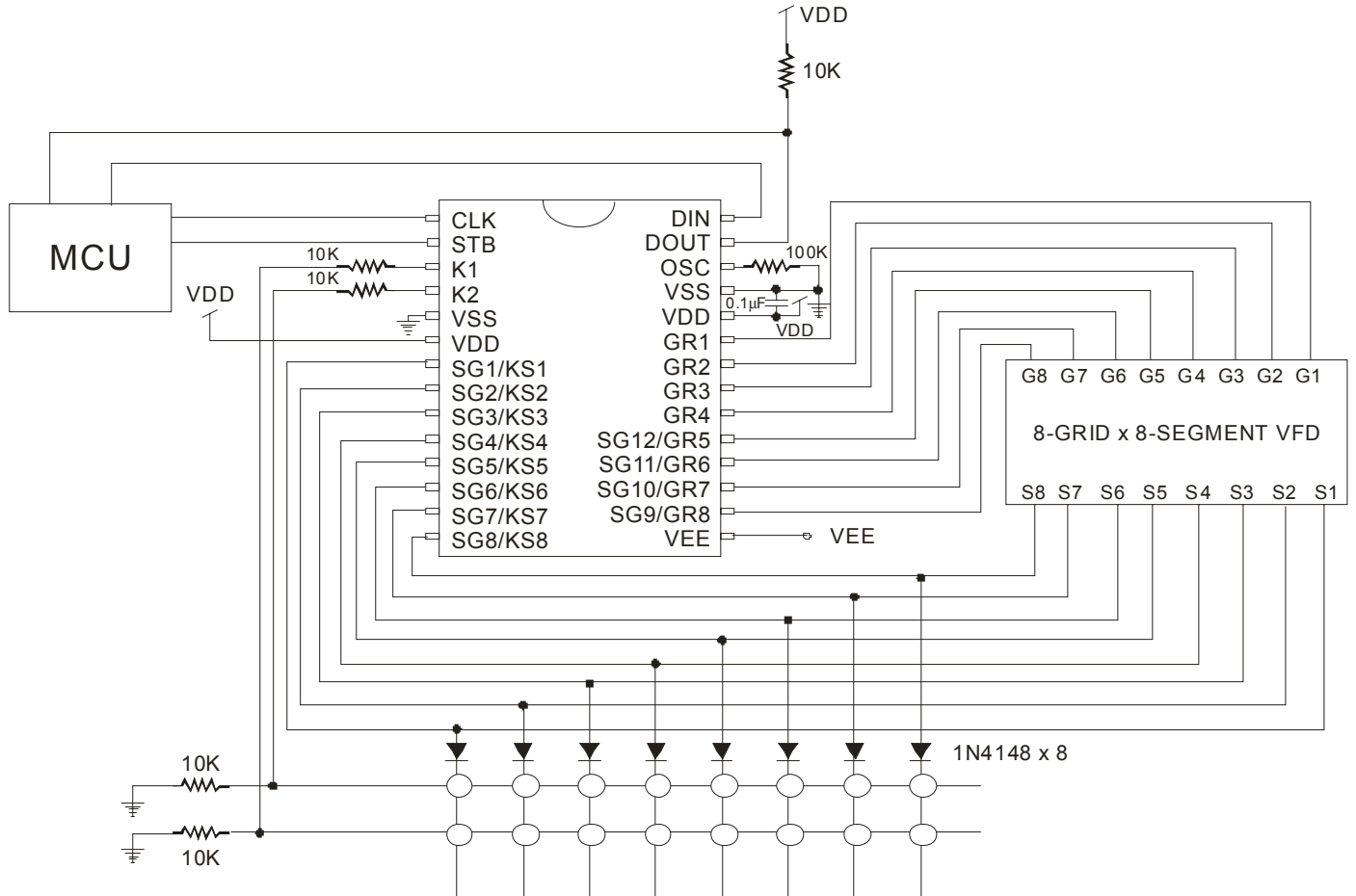
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Low-Level Output Voltage	VOLDOUT	DOUT, IOLDOUT=4mA	-	-	0.4	V
High-Level Output Current	IOHSG	VO=VDD -2V SG1/KS1 to SG8/KS8	-3	-	-	mA
High-Level Output Current	IOHGR	VO=VDD -2V GR1 to GR4, SG9/GR8 to SG12/GR5	-15	-	-	mA
High-Level Input Voltage	VIH	-	0.7VDD	-	-	V
Low-Level Input Voltage	VIL	-	-	-	0.3VDD	V
Oscillation Frequency	fosc	R=100KΩ	350	500	650	KHz
Input Current	II	VI=VDD or VSS	-	-	±1	μA
Dynamic Current Consumption	IDDdyn	Under no load Display OFF	-	-	5	mA

(Unless otherwise stated, VDD=3.3V, GND=0V, VEE=VDD-35V, Ta=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Low-Level Output Voltage	VOLDOUT	DOUT, IOLDOUT=4mA	-	-	0.4	V
High-Level Output Current	IOHSG	VO=VDD -2V SG1/KS1 to SG8/KS8	-1.5	-	-	mA
High-Level Output Current	IOHGR	VO=VDD -2V GR1 to GR4, SG9/GR8 to SG12/GR5	-6	-	-	mA
High-Level Input Voltage	VIH	-	0.7VDD	-	VDD	V
Low-Level Input Voltage	VIL	-	VSS	-	0.3VDD	V
Oscillation Frequency	fosc	R=100KΩ	350	500	650	KHz
Input Current	II	VI=VDD or VSS	-	-	±1	μA
Dynamic Current Consumption	IDDdyn	Under no load Display OFF	-	-	3	mA



APPLICATION CIRCUIT





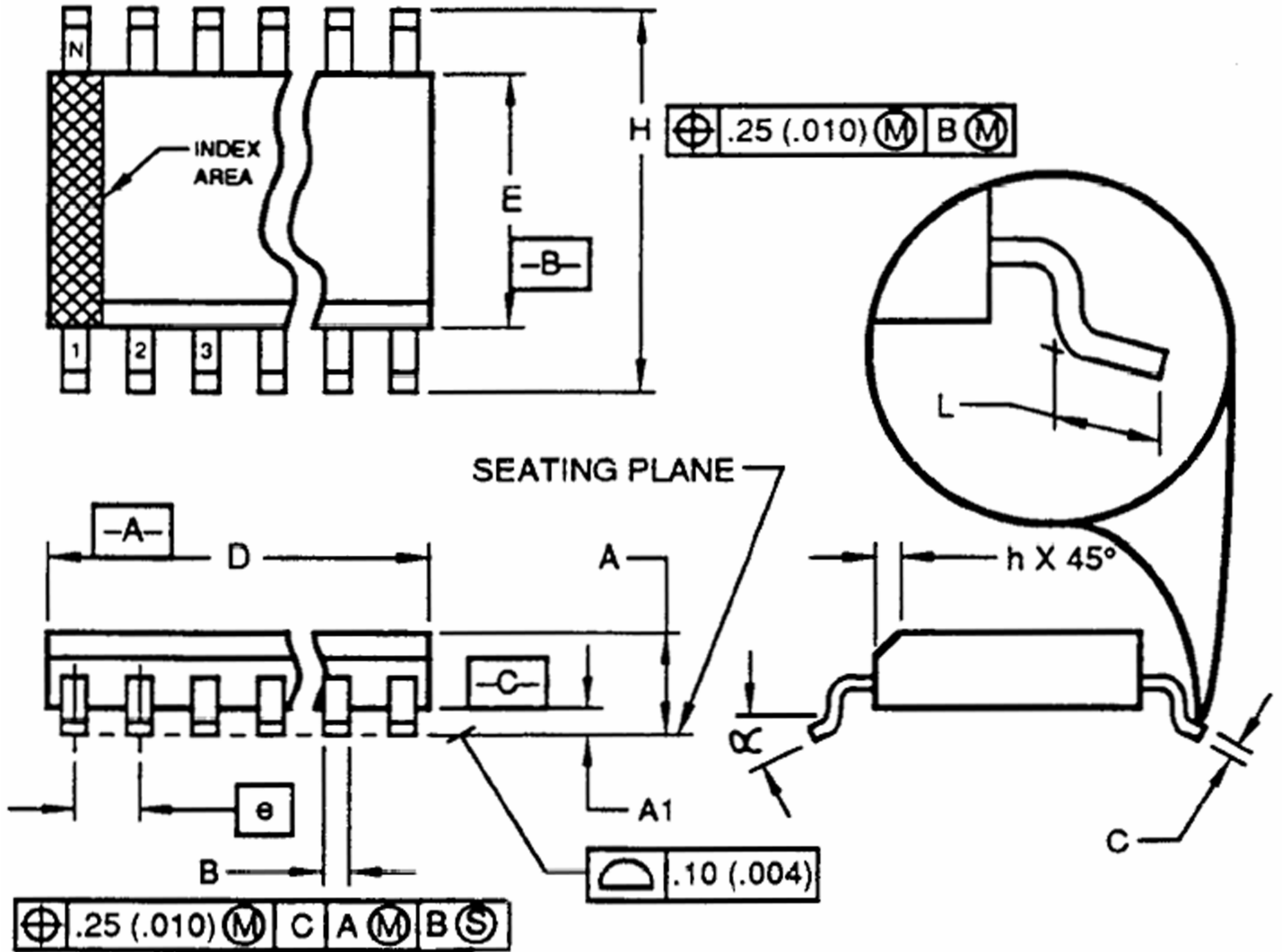
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT6315-S	28 Pins, SOP, 300mil	PT6315-S



PACKAGE INFORMATION

28 PINS, SOP, 300 MIL





Symbol	Min.	Nom.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	17.70		18.10
E	7.40		7.60
e	1.27 bsc.		
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
a	0°		8°

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5-1982.
2. Dimension "D" does not include mold flash , protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15mm (0.006 in) per side.
3. Dimension "E" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. "L" is the length of the terminal for soldering to a substrate.
6. "N" is the number of terminal positions. (N=28)
7. The lead width "B" as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in).
8. Controlling dimension: MILLIMETER.
9. Refer to JEDEC MS-013 Variation AE

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REVISION HISTORY

Date	Revision #:	Reference #:	Remarks
Sept. 21, 2000	01	PT6315-S-S v1.0	App #: 000911
Oct. 2000	02	PT6315-S-S v1.1	App #:001006 Mod #: #: 001005
July 16, 2001	03	PT6315-S-Sv1.3	App #: 010712 Mod #.: 010712
November, 2001	04	PT6315-S-Sv1.4	App #: 011116 Mod #: 011107
December 14, 2001	05	PT6315-S-Sv1.5	App #: 011213 Mod #: 010210
June 2002	06	PT6315-S-Sv1.6	App #: 020606 Mod #: 020606
July 2002	07	PT6315-S-Sv1.7	App #: 020713 Mod #: 020708
January 6, 2004	08	PT6315-S-Sv1.8	Req #: 040103 Mod #: 040108 App #: 040108
September, 14, 2005	09	PT6315-S V1.9	Req #: 050901 Mod #: 050904 App #: 050903