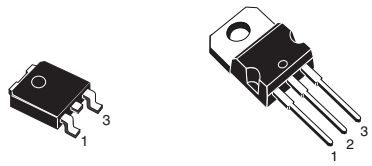
STD40NF10
STP40NF10

N-channel 100V - 0.025Ω - 50A TO-220 / DPAK
Low gate charge STripFET™ II Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ Max	I_D
STD40NF10	100V	<0.028Ω	50A
STP40NF10	100V	<0.028Ω	50A

- Exceptional dv/dt capability
- Low gate charge
- 100% avalanche tested



DPAK TO-220

Application

- Switching applications

Description

This Power MOSFET is the latest development of STMicroelectronics unique "single feature size" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps allowing remarkable manufacturing reproducibility.

Figure 1. Internal schematic diagram

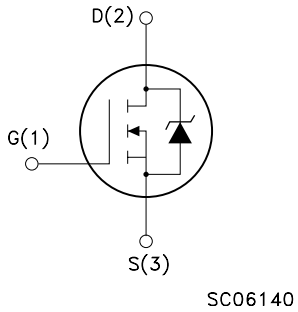


Table 1. Device summary

Order codes	Marking	Package	Packaging
STP40NF10	P40NF10	TO-220	Tube
STD40NF10	D40NF10	DPAK	Tape & reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	DPAK	
V_{DS}	Drain-source voltage (v_{gs} = 0)	100		V
V_{GS}	Gate- source voltage	±20		V
I_D (1)	Drain current (continuous) at T_C = 25°C	50		A
I_D	Drain current (continuous) at T_C = 100°C	35		A
I_{DM} (2)	Drain current (pulsed)	200		A
P_{TOT}	Total dissipation at T_C = 25°C	150	125	W
	Derating factor	1	0.83	W/°C
dv/dt(3)	Peak diode recovery voltage slope	27		V/ns
E_{AS} (4)	Single pulse avalanche energy	385		mj
T_{stg}	Storage temperature	– 55 to 175		°C
T_j	Max. operating junction temperature			

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3. I_{SD} ≤50A, di/dt ≤600A/µs, V_{DD} ≤$V_{(BR)DSS}$, T_j ≤$T_{JMAX.}$
4. Starting T_j= 25°C, I_D= 50A, V_{DD}=25V

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	DPAK	
$R_{thj\text{-}case}$	Thermal resistance junction-case Max	1	1.2	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient Max	62.5		°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	100			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS}=Max rating,T_C=125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 25A		0.025	0.028	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15V, I_D=28A		22		S
C_{iss}	Input capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		2180		pF
C_{oss}	Output capacitance			298		pF
C_{rss}	Reverse transfer capacitance			83.7		pF
Q_g	Total gate charge	V_{DD} = 50V, I_D = 40A, V_{GS} = 10V *(see Figure 17)*		46.5	62	nC
Q_{gs}	Gate-source charge			13.3		nC
Q_{gd}	Gate-drain charge			17.5	22.5	nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 50V, I_D = 25A R_G = 4.7Ω V_{GS} = 10V *(see Figure 16)*		21 46		ns ns
$t_{d(off)}$ t_f	Turn-off-delay time Fall time	V_{DD} = 27V, I_D = 40A, R_G = 4.7Ω, V_{GS} = 10V *(see Figure 16)*		54 13		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current				80	A
I_{SDM} (1)	Source-drain current (pulsed)				320	A
V_{SD} (2)	Forward on voltage	I_{SD} = 50A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 50A, V_{DD} = 25V di/dt = 100A/µs, T_j = 150°C *(see Figure 18)*		80 250 6.4		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

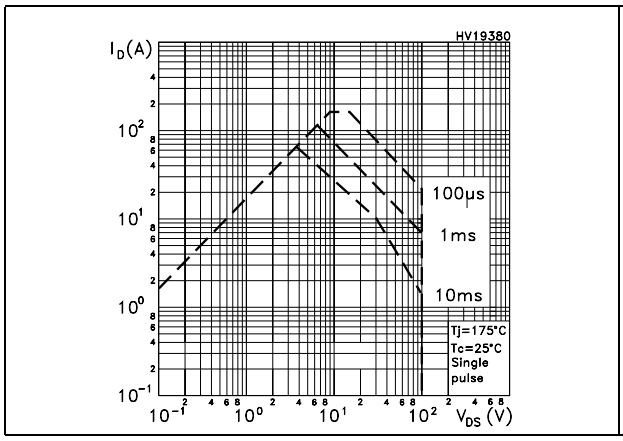


Figure 3. Thermal impedance for TO-220

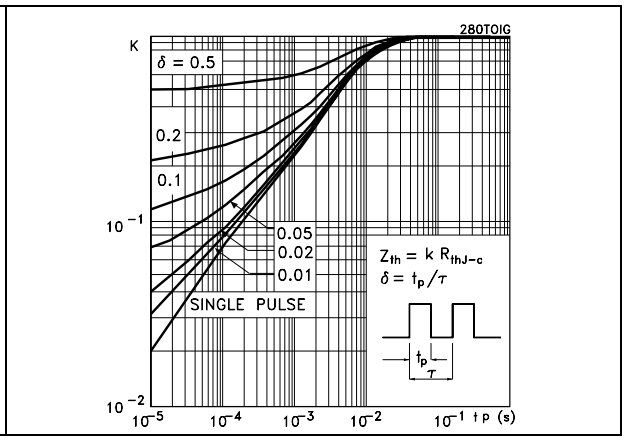


Figure 4. Safe operating area for DPAK

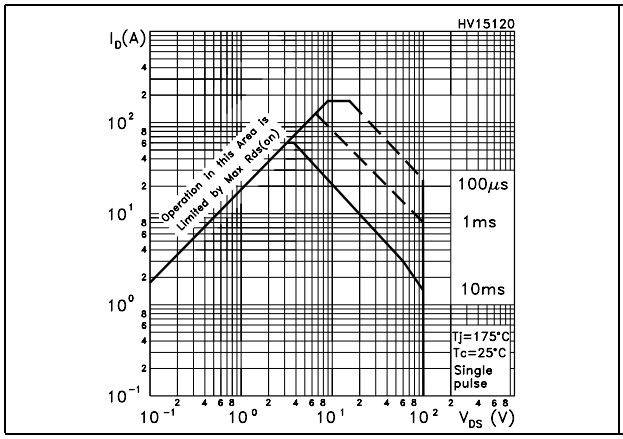


Figure 5. Thermal impedance for DPAK

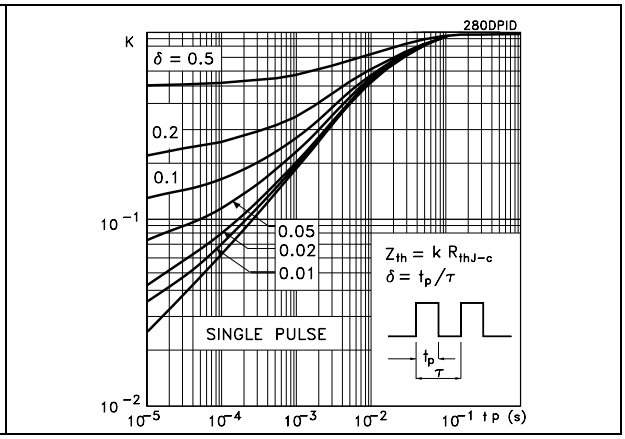


Figure 6. Output characteristics

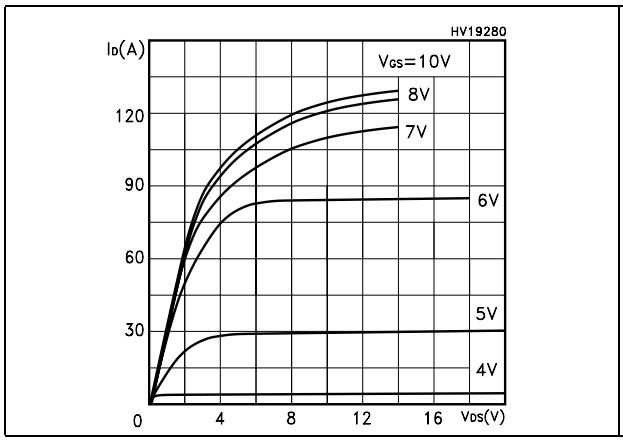


Figure 7. Transfer characteristics

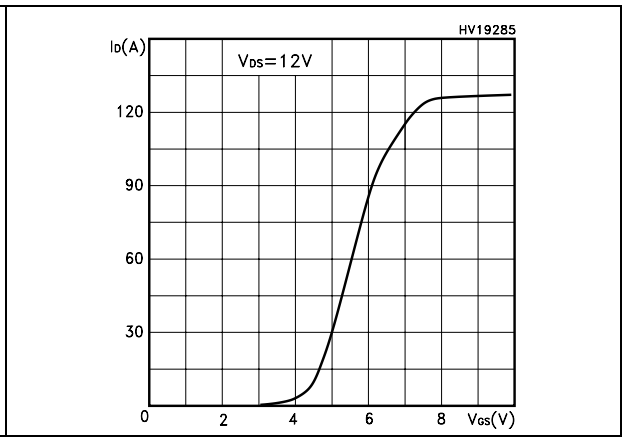


Figure 8. Transconductance

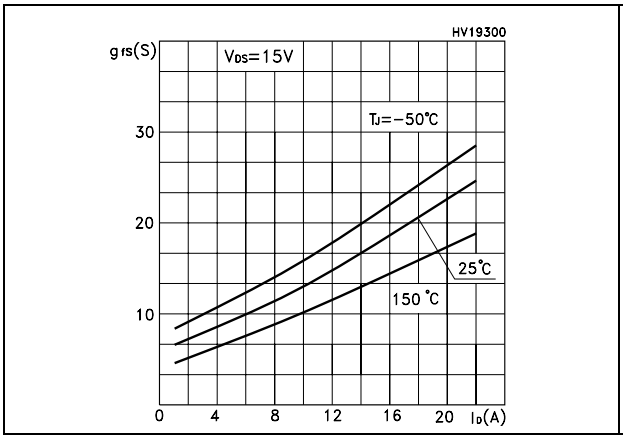


Figure 9. Static drain-source on resistance

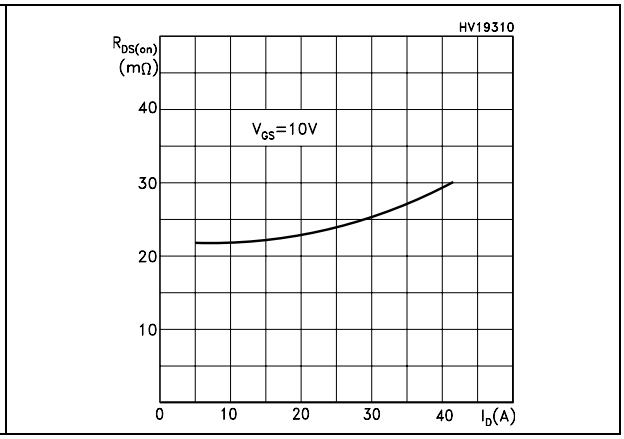


Figure 10. Gate charge vs. gate-source voltage

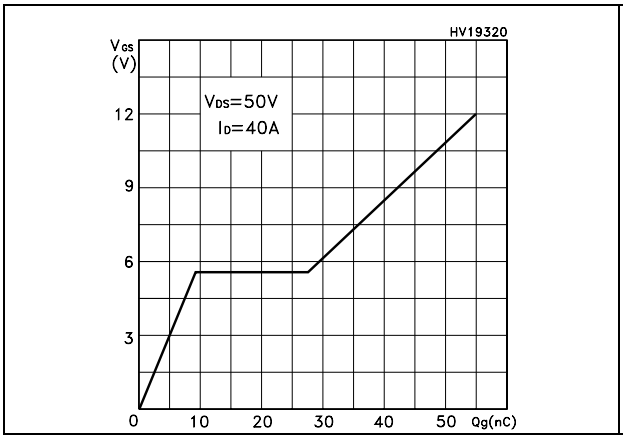


Figure 11. Capacitance variations

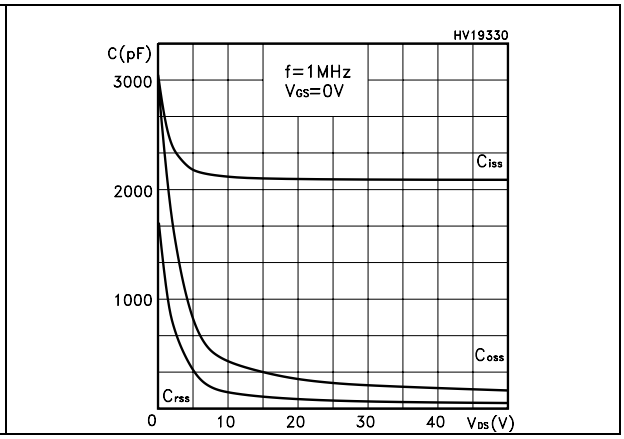


Figure 12. Normalized gate threshold voltage vs. temperature

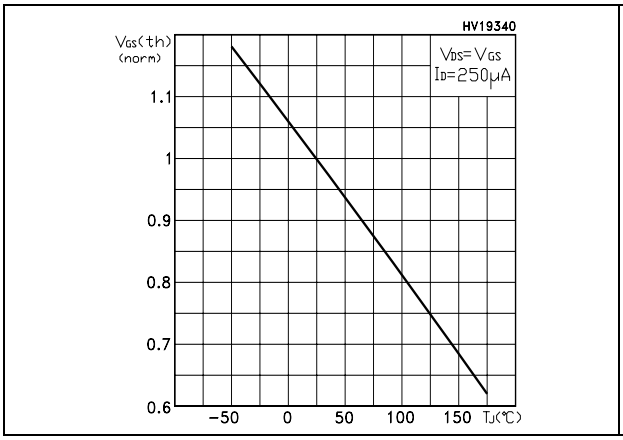


Figure 13. Normalized on resistance vs. temperature

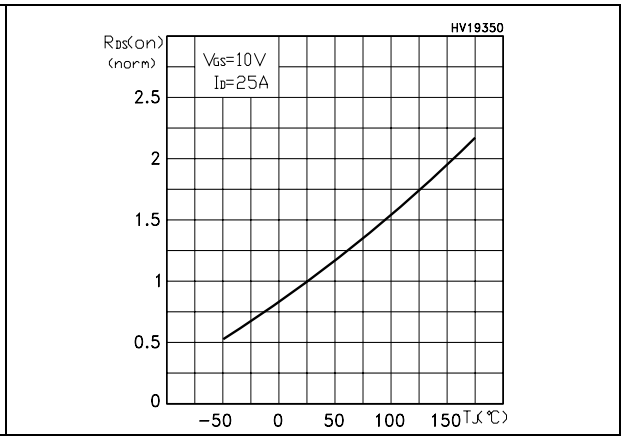


Figure 14. Source-drain diode forward characteristics

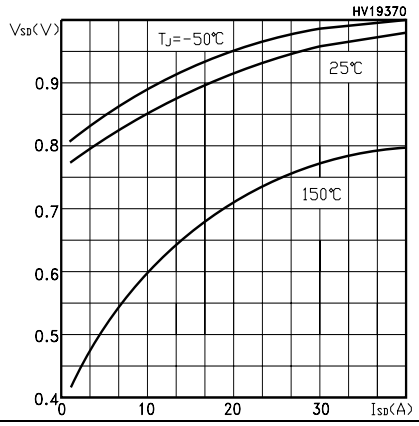
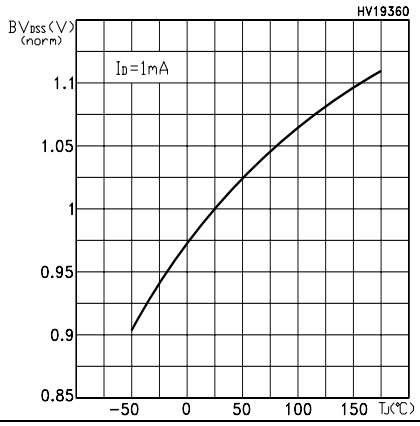


Figure 15. Normalized breakdown voltage vs. tj



3 Test circuit

Figure 16. Switching times test circuit for resistive load

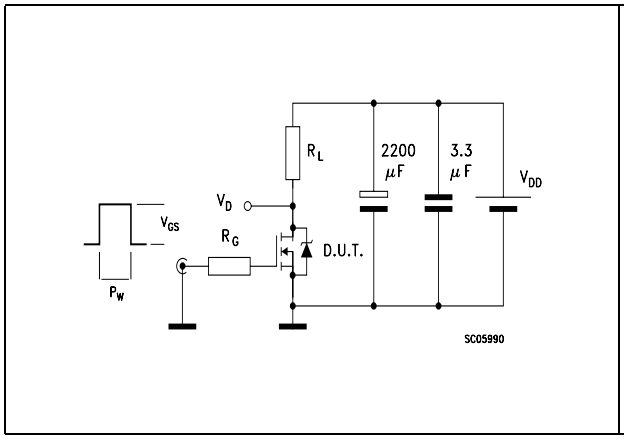


Figure 17. Gate charge test circuit

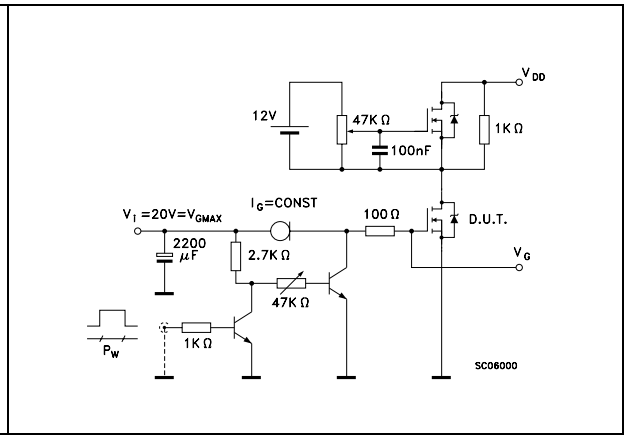


Figure 18. Test circuit for inductive load switching and diode recovery times

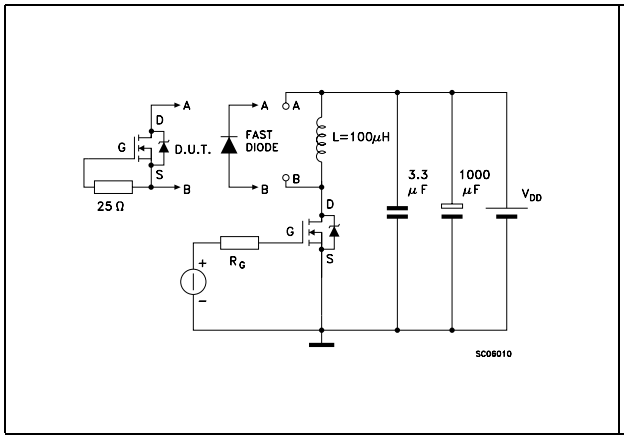


Figure 19. Unclamped Inductive load test circuit

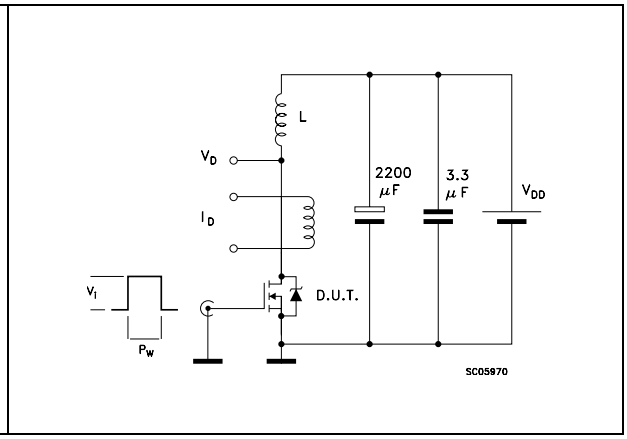


Figure 20. Unclamped inductive waveform

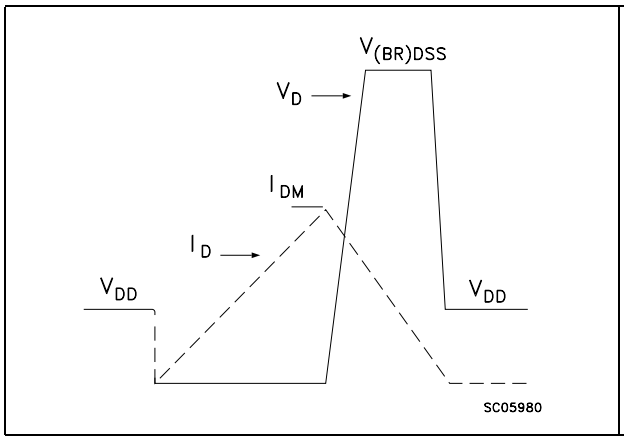
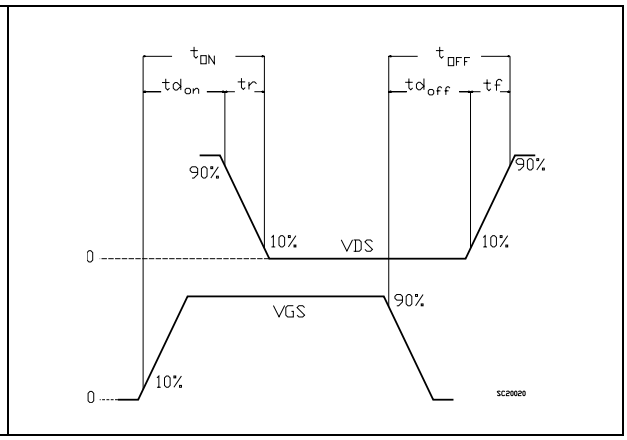


Figure 21. Switching time waveform

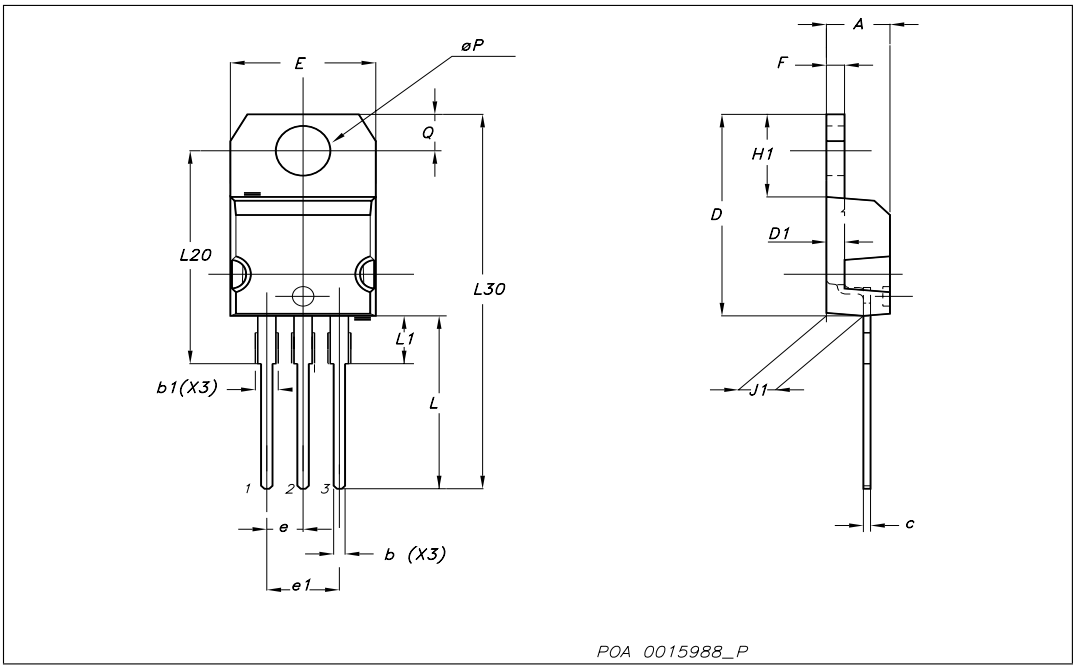


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : *www.st.com*

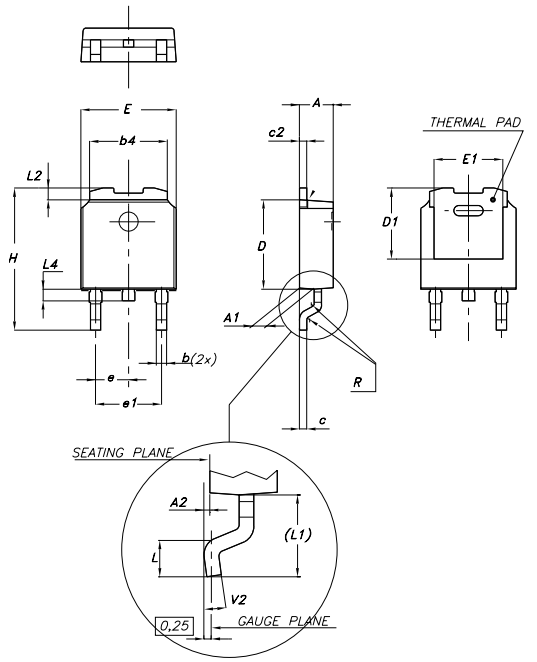
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



DPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



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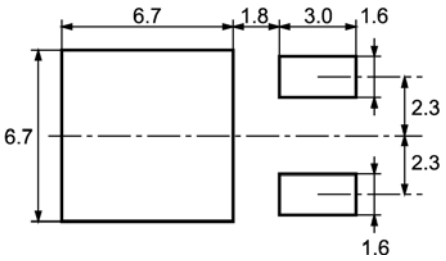
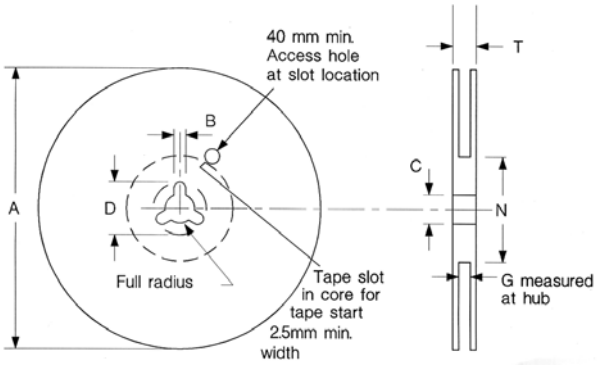
5 Packaging mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



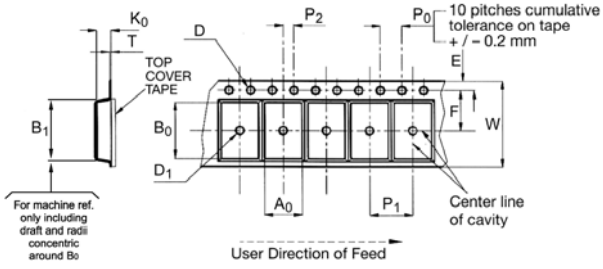
REEL MECHANICAL DATA

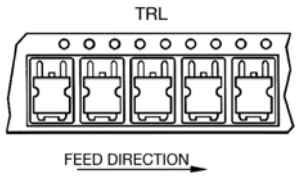
DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

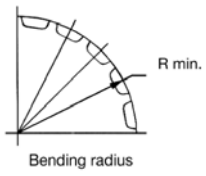
BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641







6 Revision history

Table 8. Document revision history

Date	Revision	Changes
16-Dec-2004	1	First version.
17-Aug-2006	2	The document has been reformatted.
31-Jan-2007	3	Typo mistake on *Table 2*.
19-Sep-2007	4	Added DPAK

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