

-500mA / -40V Digital transistor (with built-in resistor)

DTB114TK

●Applications

Inverter, interface, driver

●Features

- 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors.
- 2) The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input, and parasitic effects are almost completely eliminated.
- 3) Only the on / off conditions need to be set for operation, making the device design easy.
- 4) Higher mounting densities can be achieved.

●Structure

PNP epitaxial planar silicon transistor
(Resistor built-in type)

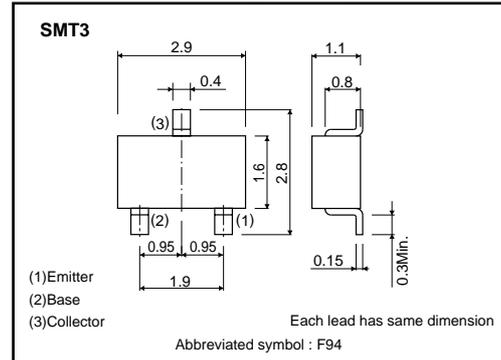
●Packaging specifications

	Package	SMT3
	Packaging type	Taping
	Code	T146
Part No.	Basic ordering unit (pieces)	3000
DTB114TK		○

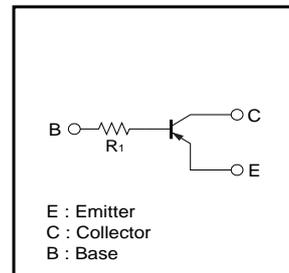
●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Collector-base voltage	V _{CB0}	-50	V
Collector-emitter voltage	V _{CE0}	-40	V
Emitter-base voltage	V _{EB0}	-5	V
Collector current	I _c	-500	mA
Collector power dissipation	P _c	200	mW
Junction temperature	T _j	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

●External dimensions (Unit : mm)



●Circuit schematic



R₁=10kΩ

Transistors

●External characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV_{CBO}	-50	-	-	V	$I_C = -50\mu A$
Collector-emitter breakdown voltage	BV_{CEO}	-40	-	-	V	$I_C = -1mA$
Emitter-base breakdown voltage	BV_{EBO}	-5	-	-	V	$I_E = -50\mu A$
Collector cutoff current	I_{CBO}	-	-	-0.5	μA	$V_{CB} = -50V$
Emitter cutoff current	I_{EBO}	-	-	-0.5	μA	$V_{EB} = -4V$
Collector-emitter saturation voltage	$V_{CE(sat)}$	-	-	-0.3	V	$I_C/I_B = -50mA/-2.5mA$
DC current transfer ratio	h_{FE}	100	250	600	-	$I_C = -50mA, V_{CE} = -5V$
Input resistance	R_1	7	10	13	$k\Omega$	-
Transition frequency	f_t *	-	200	-	MHz	$V_{CE} = -10V, I_E = 50mA, f = 100MHz$

* Characteristics of built-in transistor

●Electrical characteristics curves

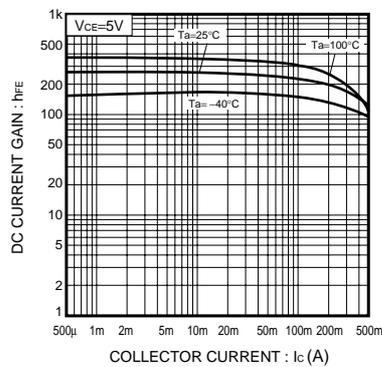


Fig.1 DC current gain vs. Collector current

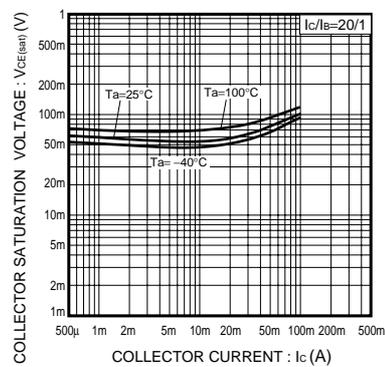


Fig.2 Collector-emitter saturation voltage vs. Collector current

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