

Features

- Zero input-output propagation delay, adjustable by capacitive load on FBK input
- Multiple configurations, see “Available CY2308 Configurations” on page 3
- Multiple low skew outputs
- Two banks of four outputs, three-stateable by two select inputs
- 10 MHz to 133 MHz operating range
- 75 ps typical cycle-to-cycle jitter (15 pF, 66 MHz)
- Space saving 16-pin 150 mil SOIC package or 16-pin TSSOP
- 3.3V operation
- Industrial Temperature available

Functional Description

The CY2308 is a 3.3V Zero Delay Buffer designed to distribute high speed clocks in PC, workstation, datacom, telecom, and other high performance applications.

The part has an on-chip PLL that locks to an input clock presented on the REF pin. The PLL feedback is driven into the FBK pin and obtained from one of the outputs. The input-to-output skew is less than 350 ps and output-to-output skew is less than 200 ps.

The CY2308 has two banks of four outputs each that is controlled by the Select inputs as shown in the table “Select

Input Decoding” on page 2”. If all output clocks are not required, Bank B is three-stated. The input clock is directly applied to the output for chip and system testing purposes by the select inputs.

The CY2308 PLL enters a power down state when there are no rising edges on the REF input. In this mode, all outputs are three-stated and the PLL is turned off resulting in less than 50 μ A of current draw. The PLL shuts down in two additional cases as shown in the table “Select Input Decoding” on page 2.

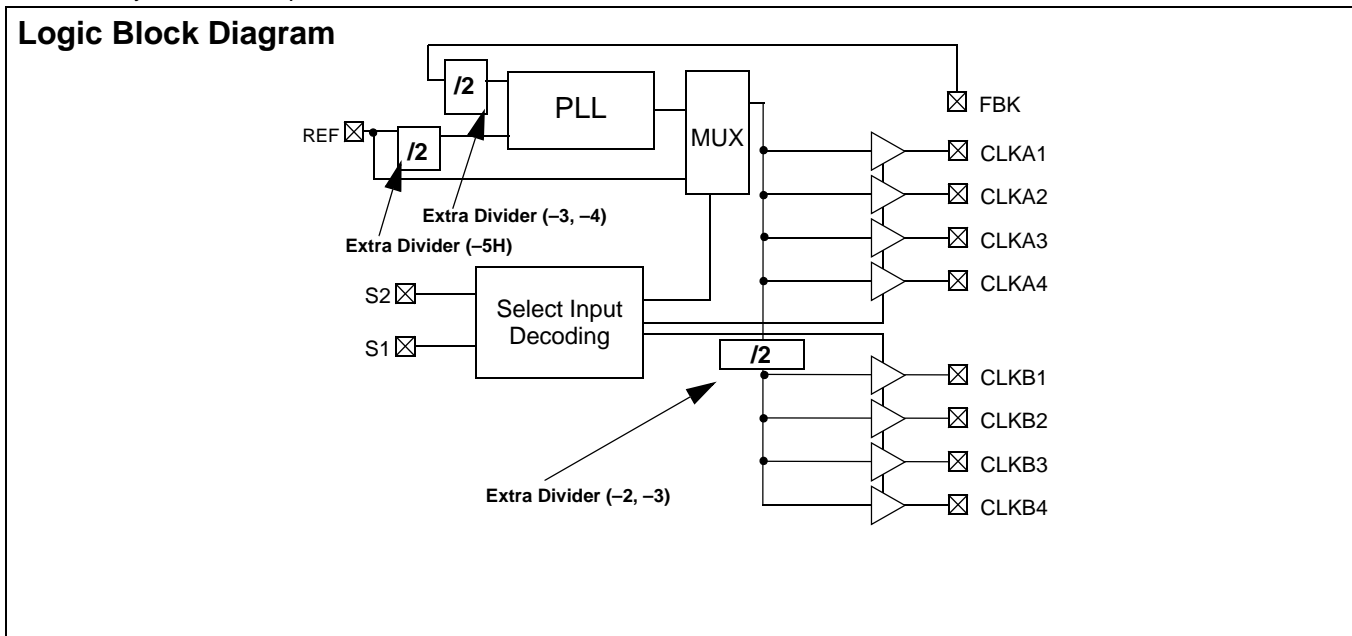
Multiple CY2308 devices accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is less than 700 ps.

The CY2308 is available in five different configurations as shown in the table “Available CY2308 Configurations” on page 3. The CY2308-1 is the base part where the output frequencies equal the reference if there is no counter in the feedback path. The CY2308-1H is the high drive version of the -1 and rise and fall times on this device are much faster.

The CY2308-2 enables the user to obtain 2X and 1X frequencies on each output bank. The exact configuration and output frequencies depend on the output that drives the feedback pin. The CY2308-3 enables the user to obtain 4X and 2X frequencies on the outputs.

The CY2308-4 enables the user to obtain 2X clocks on all outputs. Thus, the part is extremely versatile and is used in a variety of applications.

The CY2308-5H is a high drive version with REF/2 on both banks.



Pinouts

Figure 1. Pin Diagram - 16 Pin SOIC

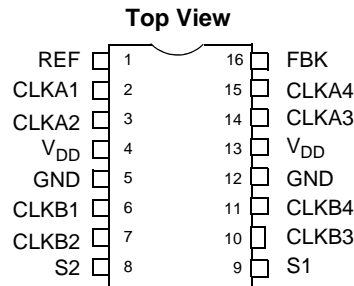


Table 1. Pin Definitions - 16 Pin SOIC

| Pin | Signal | Description |
|-----|----------------------|--|
| 1 | REF ^[1] | Input reference frequency, 5V tolerant input |
| 2 | CLKA1 ^[2] | Clock output, Bank A |
| 3 | CLKA2 ^[2] | Clock output, Bank A |
| 4 | V _{DD} | 3.3V supply |
| 5 | GND | Ground |
| 6 | CLKB1 ^[2] | Clock output, Bank B |
| 7 | CLKB2 ^[2] | Clock output, Bank B |
| 8 | S2 ^[3] | Select input, bit 2 |
| 9 | S1 ^[3] | Select input, bit 1 |
| 10 | CLKB3 ^[2] | Clock output, Bank B |
| 11 | CLKB4 ^[2] | Clock output, Bank B |
| 12 | GND | Ground |
| 13 | V _{DD} | 3.3V supply |
| 14 | CLKA3 ^[2] | Clock output, Bank A |
| 15 | CLKA4 ^[2] | Clock output, Bank A |
| 16 | FBK | PLL feedback input |

Select Input Decoding

| S2 | S1 | CLOCK A1–A4 | CLOCK B1–B4 | Output Source | PLL Shutdown |
|----|----|-----------------------|-----------------------|---------------|--------------|
| 0 | 0 | Tri-State | Tri-State | PLL | Y |
| 0 | 1 | Driven | Tri-State | PLL | N |
| 1 | 0 | Driven ^[4] | Driven ^[4] | Reference | Y |
| 1 | 1 | Driven | Driven | PLL | N |

Notes

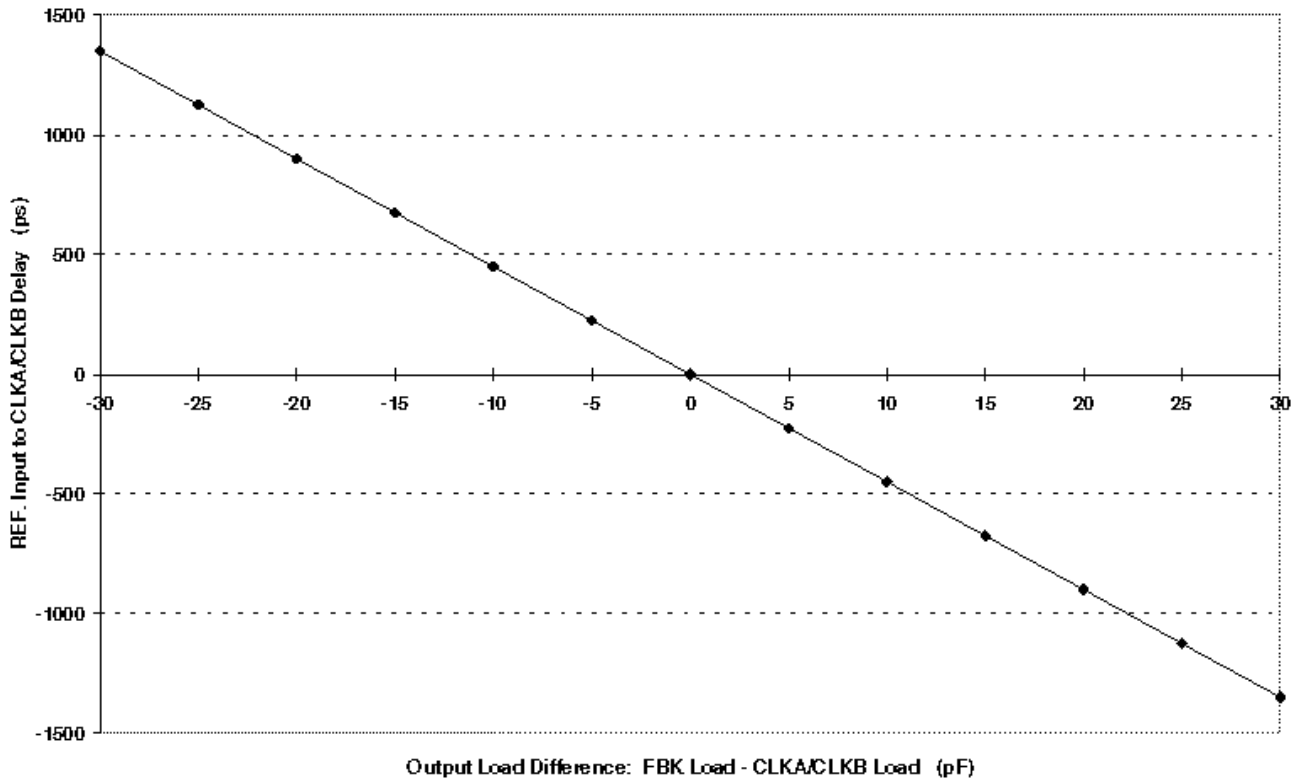
1. Weak pull down.
2. Weak pull down on all outputs.
3. Weak pull ups on these inputs.
4. Outputs inverted on 2308–2 and 2308–3 in bypass mode, S2 = 1 and S1 = 0.

Available CY2308 Configurations

| Device | Feedback From | Bank A Frequency | Bank B Frequency |
|-----------|------------------|------------------|---------------------------------------|
| CY2308-1 | Bank A or Bank B | Reference | Reference |
| CY2308-1H | Bank A or Bank B | Reference | Reference |
| CY2308-2 | Bank A | Reference | Reference/2 |
| CY2308-2 | Bank B | 2 X Reference | Reference |
| CY2308-3 | Bank A | 2 X Reference | Reference or Reference ^[5] |
| CY2308-3 | Bank B | 4 X Reference | 2 X Reference |
| CY2308-4 | Bank A or Bank B | 2 X Reference | 2 X Reference |
| CY2308-5H | Bank A or Bank B | Reference /2 | Reference /2 |

Zero Delay and Skew Control

Table 2. REF. Input to CLKA/CLKB Delay Versus Difference in Loading between FBK pin and CLKA/CLKB Pins



To close the feedback loop of the CY2308, the FBK pin is driven from any of the eight available output pins. The output driving the FBK pin drives a total load of 7 pF plus any additional load that it drives. The relative loading of this output to the remaining outputs adjusts the input-output delay. This is shown in the [Table 2](#).

For applications requiring zero input-output delay, all outputs including the one providing feedback is equally loaded.

If input-output delay adjustments are required, use the [Zero Delay and Skew Control](#) graph to calculate loading differences between the feedback output and remaining outputs.

For zero output-output skew, outputs are loaded equally. For further information on using CY2308, refer to the application note “CY2308: Zero Delay Buffer.”

Note

5. Output phase is indeterminant (0° or 180° from input clock). If phase integrity is required, use the CY2308-2.

Maximum Ratings

| | | | |
|---|--------------------------|---|-----------------|
| Supply Voltage to Ground Potential..... | -0.5V to +7.0V | Storage Temperature | -65°C to +150°C |
| DC Input Voltage (Except Ref) | -0.5V to $V_{DD} + 0.5V$ | Junction Temperature | 150°C |
| DC Input Voltage REF | -0.5 to 7V | Static Discharge Voltage (MIL-STD-883, Method 3015)..... | >2000V |

Operating Conditions for Commercial Temperature Devices

| Parameter | Description | Min | Max | Unit |
|-----------|--|------|-----|------|
| V_{DD} | Supply Voltage | 3.0 | 3.6 | V |
| T_A | Operating Temperature (Ambient Temperature) | 0 | 70 | °C |
| C_L | Load Capacitance, below 100 MHz | - | 30 | pF |
| | Load Capacitance, from 100 MHz to 133 MHz | - | 15 | pF |
| C_{IN} | Input Capacitance ^[6] | - | 7 | pF |
| t_{PU} | Power up time for all V_{DDs} to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | 50 | ms |

Electrical Characteristics for Commercial Temperature Devices

| Parameter | Description | Test Conditions | Min | Max | Unit |
|--------------------|------------------------------------|---|-----|--------------------|---------|
| V_{IL} | Input LOW Voltage | | - | 0.8 | V |
| V_{IH} | Input HIGH Voltage | | 2.0 | - | V |
| I_{IL} | Input LOW Current | $V_{IN} = 0V$ | - | 50.0 | μA |
| I_{IH} | Input HIGH Current | $V_{IN} = V_{DD}$ | - | 100.0 | μA |
| V_{OL} | Output LOW Voltage ^[7] | $I_{OL} = 8\text{ mA } (-1, -2, -3, -4)$ $I_{OL} = 12\text{ mA } (-1H, -5H)$ | - | 0.4 | V |
| V_{OH} | Output HIGH Voltage ^[7] | $I_{OH} = -8\text{ mA } (-1, -2, -3, -4)$ $I_{OH} = -12\text{ mA } (-1H, -5H)$ | 2.4 | - | V |
| I_{DD} (PD mode) | Power Down Supply Current | REF = 0 MHz | - | 12.0 | μA |
| I_{DD} | Supply Current | Unloaded outputs, 100 MHz REF, Select inputs at V_{DD} or GND | - | 45.0 | mA |
| | | | - | 70.0 (-1H, -5H) | mA |
| | | Unloaded outputs, 66 MHz REF (-1, -2, -3, -4) | - | 32.0 | mA |
| | | Unloaded outputs, 33 MHz REF (-1, -2, -3, -4) | - | 18.0 | mA |

Note

- 6. Applies to both Ref Clock and FBK.
- 7. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics for Commercial Temperature Devices ^[8]

| Parameter | Name | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------|---|---|------|------|-------|------|
| t ₁ | Output Frequency | 30-pF load, All devices | 10 | – | 100 | MHz |
| t ₁ | Output Frequency | 20-pF load, –1H, –5H devices ^[9] | 10 | – | 133.3 | MHz |
| t ₁ | Output Frequency | 15-pF load, –1, –2, –3, –4 devices | 10 | – | 133.3 | MHz |
| | Duty Cycle ^[7] = t ₂ ÷ t ₁ (–1, –2, –3, –4, –1H, –5H) | Measured at 1.4V, F _{OUT} = 66.66 MHz 30-pF load | 40.0 | 50.0 | 60.0 | % |
| | Duty Cycle ^[7] = t ₂ ÷ t ₁ (–1, –2, –3, –4, –1H, –5H) | Measured at 1.4V, F _{OUT} <50.0 MHz 15-pF load | 45.0 | 50.0 | 55.0 | % |
| t ₃ | Rise Time ^[7] (–1, –2, –3, –4) | Measured between 0.8V and 2.0V, 30-pF load | – | – | 2.20 | ns |
| t ₃ | Rise Time ^[7] (–1, –2, –3, –4) | Measured between 0.8V and 2.0V, 15-pF load | – | – | 1.50 | ns |
| t ₃ | Rise Time ^[7] (–1H, –5H) | Measured between 0.8V and 2.0V, 30-pF load | – | – | 1.50 | ns |
| t ₄ | Fall Time ^[7] (–1, –2, –3, –4) | Measured between 0.8V and 2.0V, 30-pF load | – | – | 2.20 | ns |
| t ₄ | Fall Time ^[7] (–1, –2, –3, –4) | Measured between 0.8V and 2.0V, 15-pF load | – | – | 1.50 | ns |
| t ₄ | Fall Time ^[7] (–1H, –5H) | Measured between 0.8V and 2.0V, 30-pF load | – | – | 1.25 | ns |
| t ₅ | Output to Output Skew on same Bank (–1, –2, –3, –4) ^[7] | All outputs equally loaded | – | – | 200 | ps |
| | Output to Output Skew (–1H, –5H) | All outputs equally loaded | – | – | 200 | ps |
| | Output Bank A to Output Bank B Skew (–1, –4, –5H) | All outputs equally loaded | – | – | 200 | ps |
| | Output Bank A to Output Bank B Skew (–2, –3) | All outputs equally loaded | – | – | 400 | ps |
| t ₆ | Delay, REF Rising Edge to FBK Rising Edge ^[7] | Measured at V _{DD} /2 | – | 0 | ±250 | ps |
| t ₇ | Device to Device Skew ^[7] | Measured at V _{DD} /2 on the FBK pins of devices | – | 0 | 700 | ps |
| t ₈ | Output Slew Rate ^[7] | Measured between 0.8V and 2.0V on –1H, –5H device using Test Circuit 2 | 1 | – | | V/ns |
| t _J | Cycle to Cycle Jitter ^[7] (–1, –1H, –4, –5H) | Measured at 66.67 MHz, loaded outputs, 15-pF load | – | 75 | 200 | ps |
| | | Measured at 66.67 MHz, loaded outputs, 30-pF load | – | – | 200 | ps |
| | | Measured at 133.3 MHz, loaded outputs, 15-pF load | – | – | 100 | ps |
| t _J | Cycle to Cycle Jitter ^[7] (–2, –3) | Measured at 66.67 MHz, loaded outputs 30-pF load | – | – | 400 | ps |
| | | Measured at 66.67 MHz, loaded outputs 15-pF load | – | – | 400 | ps |
| t _{LOCK} | PLL Lock Time ^[7] | Stable power supply, valid clocks presented on REF and FBK pins | – | – | 1.0 | ms |

Notes

8. All parameters are specified with loaded outputs.
9. CY2308–5H has maximum input frequency of 133.33 MHz and maximum output of 66.67 MHz.

Operating Conditions for Industrial Temperature Devices

| Parameter | Description | Min | Max | Unit |
|-----------------|--|------|-----|------|
| V _{DD} | Supply Voltage | 3.0 | 3.6 | V |
| T _A | Operating Temperature (Ambient Temperature) | -40 | 85 | °C |
| C _L | Load Capacitance, below 100 MHz | - | 30 | pF |
| | Load Capacitance, from 100 MHz to 133 MHz | - | 15 | pF |
| C _{IN} | Input Capacitance ^[6] | - | 7 | pF |
| t _{PU} | Power-up time for all V _{DD} S to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | 50 | ms |

Electrical Characteristics for Industrial Temperature Devices

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---------------------------|------------------------------------|---|-----|-------------|------|
| V _{IL} | Input LOW Voltage | | - | 0.8 | V |
| V _{IH} | Input HIGH Voltage | | 2.0 | - | V |
| I _{IL} | Input LOW Current | V _{IN} = 0V | - | 50.0 | μA |
| I _{IH} | Input HIGH Current | V _{IN} = V _{DD} | - | 100.0 | μA |
| V _{OL} | Output LOW Voltage ^[7] | I _{OL} = 8 mA (-1, -2, -3, -4) I _{OL} = 12 mA (-1H, -5H) | - | 0.4 | V |
| V _{OH} | Output HIGH Voltage ^[7] | I _{OH} = -8 mA (-1, -2, -3, -4) I _{OH} = -12 mA (-1H, -5H) | 2.4 | - | V |
| I _{DD} (PD mode) | Power Down Supply Current | REF = 0 MHz | - | 25.0 | μA |
| I _{DD} | Supply Current | Unloaded outputs, 100 MHz, Select inputs at V _{DD} or GND | - | 45.0 | mA |
| | | | - | 70(-1H,-5H) | mA |
| | | Unloaded outputs, 66 MHz REF (-1, -2, -3, -4) | - | 35.0 | mA |
| | | Unloaded outputs, 66 MHz REF (-1, -2, -3, -4) | - | 20.0 | mA |

Switching Characteristics for Industrial Temperature Devices ^[8]

| Parameter | Name | Test Conditions | Min | Typ | Max | Unit |
|-------------------|---|---|------|------|-------|------|
| t ₁ | Output Frequency | 30 pF load, All devices | 10 | – | 100 | MHz |
| t ₁ | Output Frequency | 20 pF load, –1H, –5H devices ^[9] | 10 | – | 133.3 | MHz |
| t ₁ | Output Frequency | 15 pF load, –1, –2, –3, –4 devices | 10 | – | 133.3 | MHz |
| | Duty Cycle ^[7] = t ₂ ÷ t ₁ (–1, –2, –3, –4, –1H, –5H) | Measured at 1.4V, F _{OUT} = 66.66 MHz 30 pF load | 40.0 | 50.0 | 60.0 | % |
| | Duty Cycle ^[7] = t ₂ ÷ t ₁ (–1, –2, –3, –4, –1H, –5H) | Measured at 1.4V, F _{OUT} <50.0 MHz 15 pF load | 45.0 | 50.0 | 55.0 | % |
| t ₃ | Rise Time ^[7] (–1, –2, –3, –4) | Measured between 0.8V and 2.0V, 30 pF load | – | – | 2.50 | ns |
| t ₃ | Rise Time ^[7] (–1, –2, –3, –4) | Measured between 0.8V and 2.0V, 15 pF load | – | – | 1.50 | ns |
| t ₃ | Rise Time ^[7] (–1H, –5H) | Measured between 0.8V and 2.0V, 30 pF load | – | – | 1.50 | ns |
| t ₄ | Fall Time ^[7] (–1, –2, –3, –4) | Measured between 0.8V and 2.0V, 30 pF load | – | – | 2.50 | ns |
| t ₄ | Fall Time ^[7] (–1, –2, –3, –4) | Measured between 0.8V and 2.0V, 15 pF load | – | – | 1.50 | ns |
| t ₄ | Fall Time ^[7] (–1H, –5H) | Measured between 0.8V and 2.0V, 30 pF load | – | – | 1.25 | ns |
| t ₅ | Output to Output Skew on same Bank (–1, –2, –3, –4) ^[7] | All outputs equally loaded | – | – | 200 | ps |
| | Output to Output Skew (–1H, –5H) | All outputs equally loaded | – | – | 200 | ps |
| | Output Bank A to Output Bank B Skew (–1, –4, –5H) | All outputs equally loaded | – | – | 200 | ps |
| | Output Bank A to Output Bank B Skew (–2, –3) | All outputs equally loaded | – | – | 400 | ps |
| t ₆ | Delay, REF Rising Edge to FBK Rising Edge ^[7] | Measured at V _{DD} /2 | – | 0 | ±250 | ps |
| t ₇ | Device to Device Skew ^[7] | Measured at V _{DD} /2 on the FBK pins of devices | – | 0 | 700 | ps |
| t ₈ | Output Slew Rate ^[7] | Measured between 0.8V and 2.0V on –1H, –5H device using Test Circuit 2 | 1 | – | – | V/ns |
| t _J | Cycle to Cycle Jitter ^[7] (–1, –1H, –4, –5H) | Measured at 66.67 MHz, loaded outputs, 15 pF load | – | 75 | 200 | ps |
| | | Measured at 66.67 MHz, loaded outputs, 30 pF load | – | – | 200 | ps |
| | | Measured at 133.3 MHz, loaded outputs, 15 pF load | – | – | 100 | ps |
| t _J | Cycle to Cycle Jitter ^[7] (–2, –3) | Measured at 66.67 MHz, loaded outputs 30 pF load | – | – | 400 | ps |
| | | Measured at 66.67 MHz, loaded outputs 15 pF load | – | – | 400 | ps |
| t _{LOCK} | PLL Lock Time ^[7] | Stable power supply, valid clocks presented on REF and FBK pins | – | – | 1.0 | ms |

Switching Waveforms

Figure 2. Duty Cycle Timing

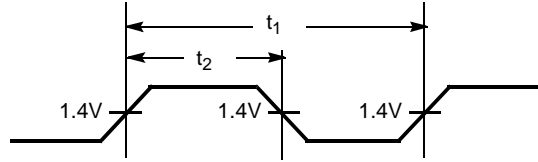


Figure 3. All Outputs Rise/Fall Time

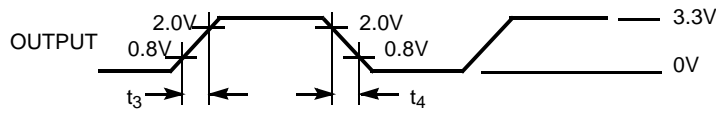


Figure 4. Output-Output Skew

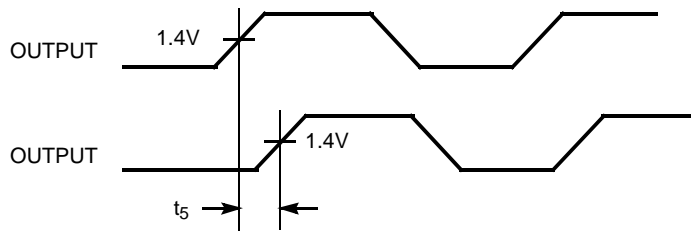


Figure 5. Input-Output Propagation Delay

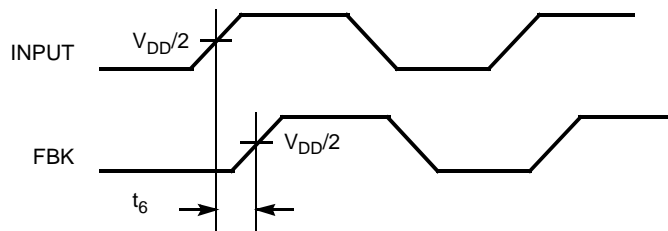
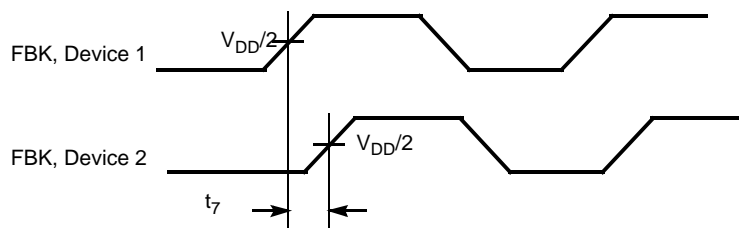
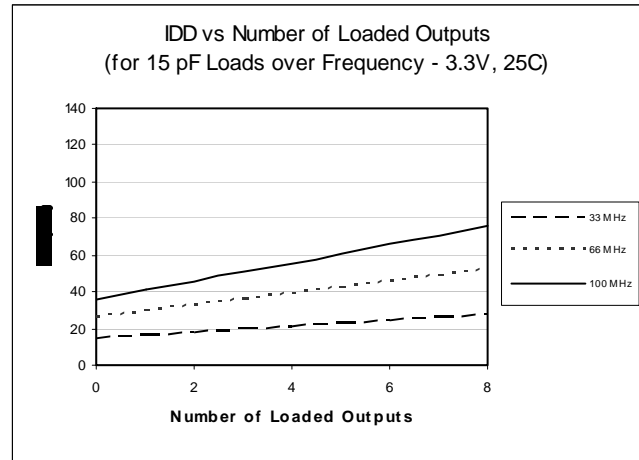
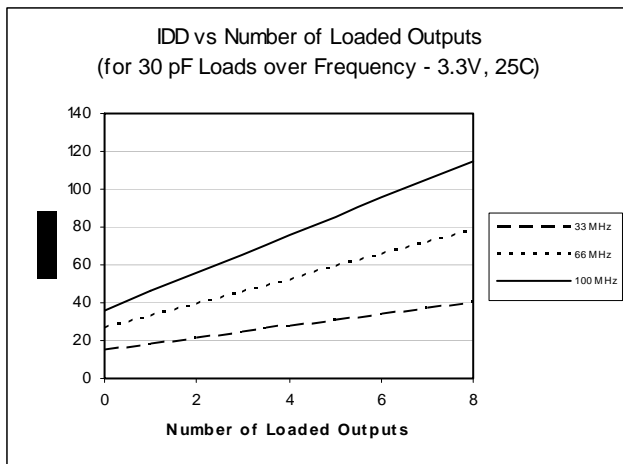
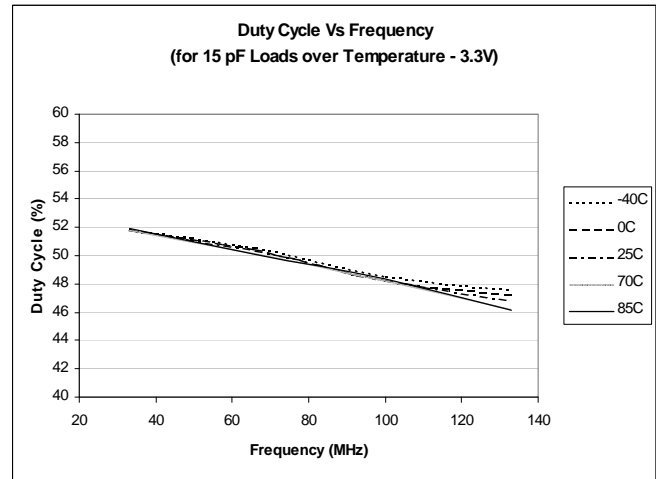
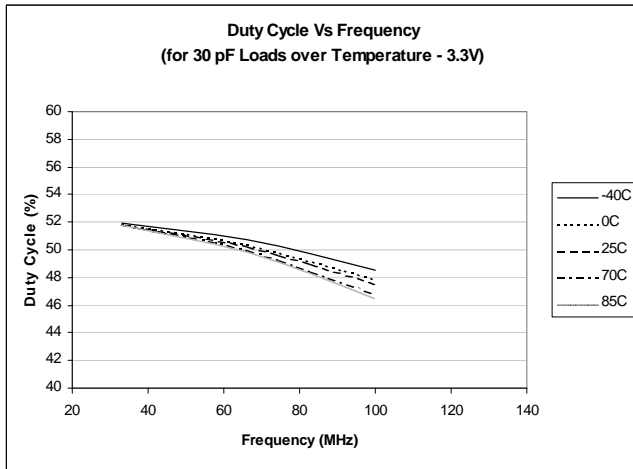
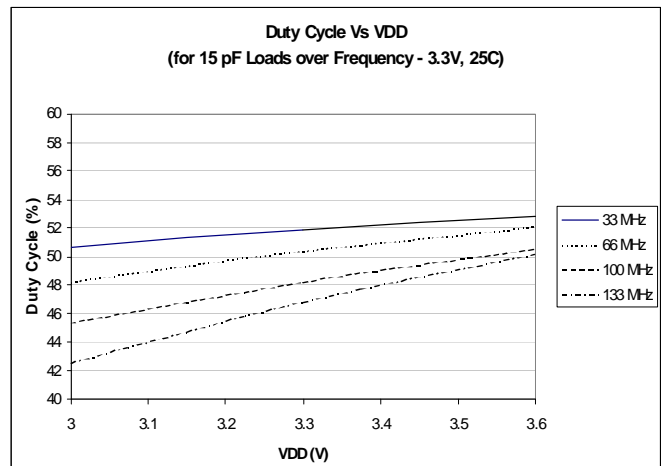
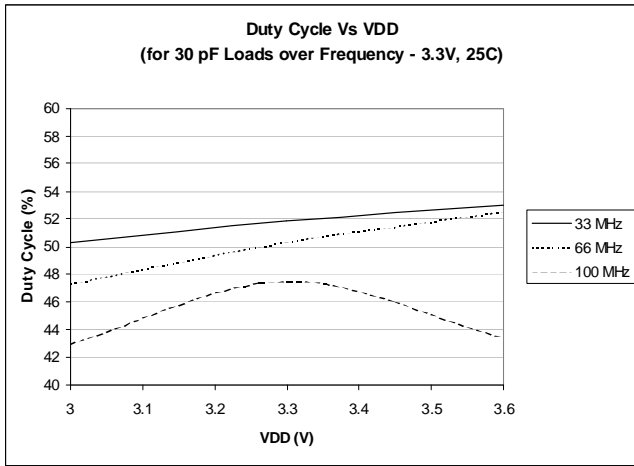


Figure 6. Device-Device Skew



Typical Duty Cycle^[10] and I_{DD} Trends^[11] for CY2308-1,2,3,4

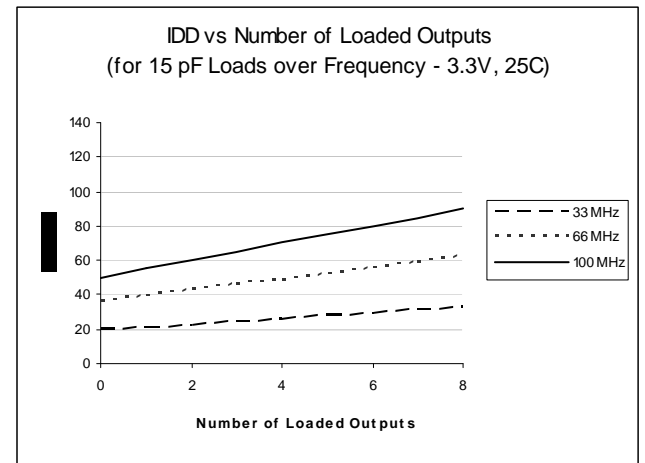
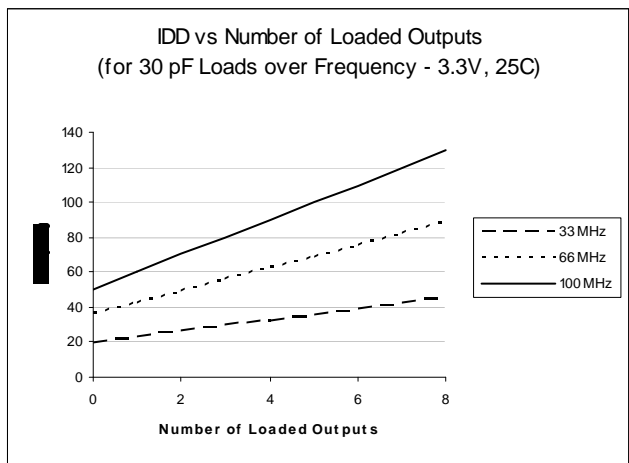
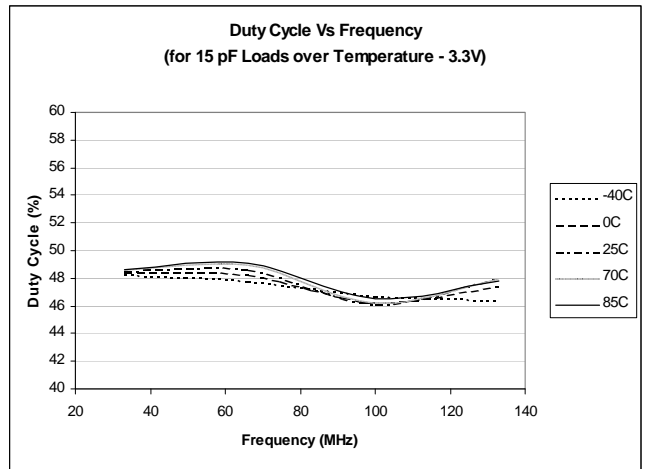
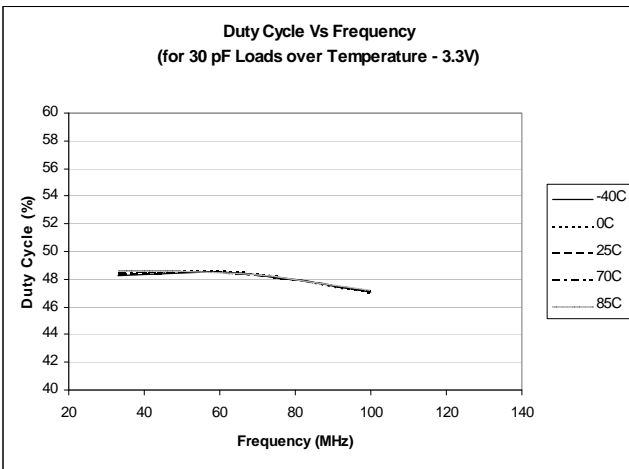
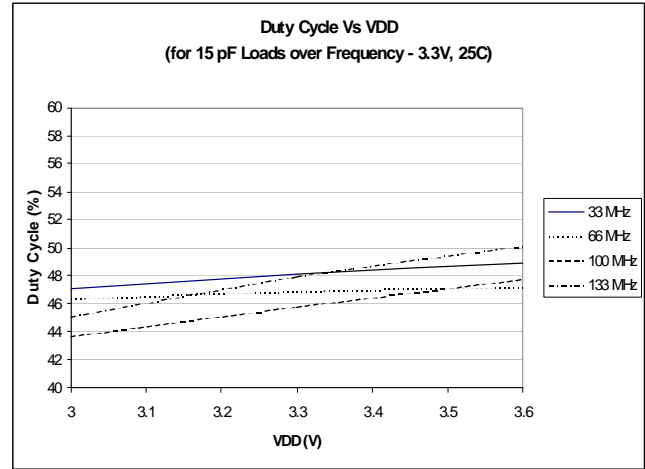
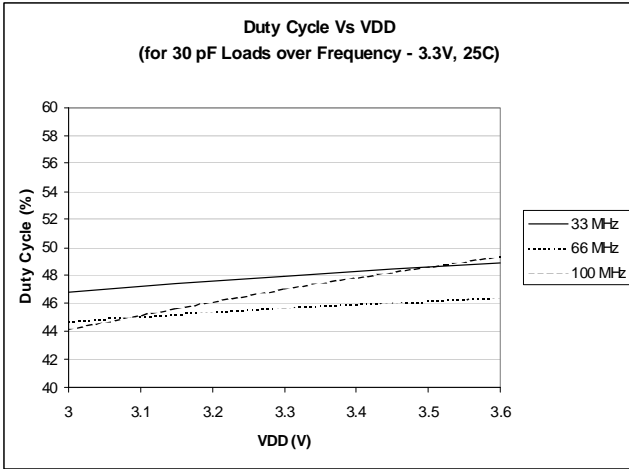


Notes

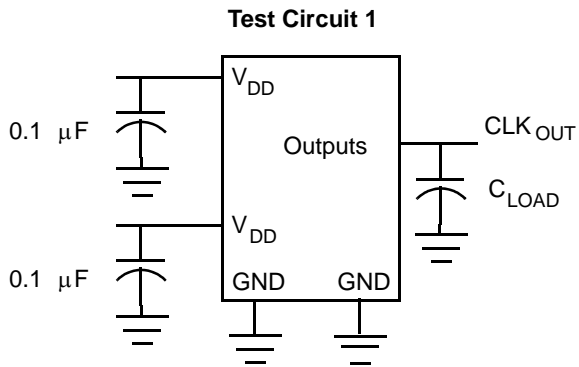
10. Duty Cycle is taken from typical chip measured at 1.4V.

11. I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the unloaded current.
(n = number of outputs; C = Capacitance load per output (F); V = Voltage Supply (V); f = frequency (Hz)).

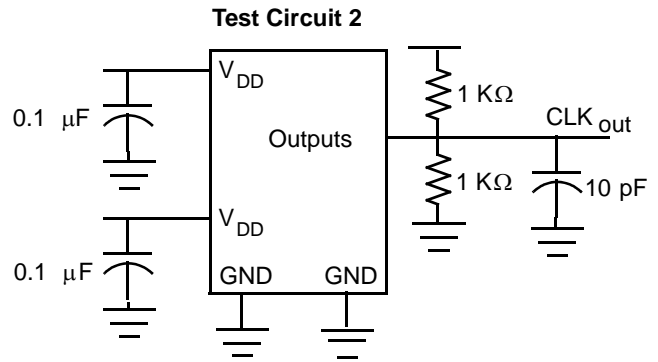
Typical Duty Cycle^[10] and I_{DD} Trends^[11] for CY2308–1H, 5H



Test Circuits



Test Circuit for all parameters except t_b



Test Circuit for t_b , Output slew rate on -1H, -5 device

Ordering Information

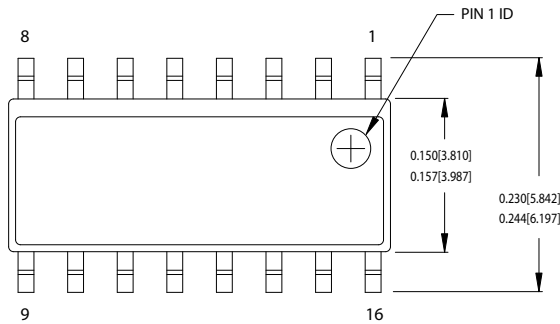
| Ordering Code | Package Type | Operating Range |
|----------------|--------------------------------------|-----------------|
| CY2308SC-1 | 16-pin 150 mil SOIC | Commercial |
| CY2308SC-1T | 16-pin 150 mil SOIC - Tape and Reel | Commercial |
| CY2308SI-1 | 16-pin 150 mil SOIC | Industrial |
| CY2308SI-1T | 16-pin 150 mil SOIC - Tape and Reel | Industrial |
| CY2308SC-1H | 16-pin 150 mil SOIC | Commercial |
| CY2308SC-1HT | 16-pin 150 mil SOIC - Tape and Reel | Commercial |
| CY2308SI-1H | 16-pin 150 mil SOIC | Industrial |
| CY2308SI-1HT | 16-pin 150 mil SOIC - Tape and Reel | Industrial |
| CY2308ZC-1H | 16-pin 150 mil TSSOP | Commercial |
| CY2308ZC-1HT | 16-pin 150 mil TSSOP - Tape and Reel | Commercial |
| CY2308ZI-1H | 16-pin 150 mil TSSOP | Industrial |
| CY2308ZI-1HT | 16-pin 150 mil TSSOP - Tape and Reel | Industrial |
| CY2308SC-2 | 16-pin 150 mil SOIC | Commercial |
| CY2308SC-2T | 16-pin 150 mil SOIC - Tape and Reel | Commercial |
| CY2308SI-2 | 16-pin 150 mil SOIC | Industrial |
| CY2308SI-2T | 16-pin 150 mil SOIC - Tape and Reel | Industrial |
| CY2308SC-3 | 16-pin 150 mil SOIC | Commercial |
| CY2308SC-3T | 16-pin 150 mil SOIC - Tape and Reel | Commercial |
| CY2308SC-4 | 16-pin 150 mil SOIC | Commercial |
| CY2308SC-4T | 16-pin 150 mil SOIC - Tape and Reel | Commercial |
| CY2308SI-4 | 16-pin 150 mil SOIC | Industrial |
| CY2308SI-4T | 16-pin 150 mil SOIC - Tape and Reel | Industrial |
| CY2308SC-5HT | 16-pin 150 mil SOIC - Tape and Reel | Commercial |
| Pb-Free | | |
| CY2308SXC-1 | 16-pin 150 mil SOIC | Commercial |
| CY2308SXC-1T | 16-pin 150 mil SOIC - Tape and Reel | Commercial |
| CY2308SXI-1 | 16-pin 150 mil SOIC | Industrial |
| CY2308SXI-1T | 16-pin 150 mil SOIC - Tape and Reel | Industrial |
| CY2308SXC-1H | 16-pin 150 mil SOIC | Commercial |
| CY2308SXC-1HT | 16-pin 150 mil SOIC - Tape and Reel | Commercial |
| CY2308SXI-1H | 16-pin 150 mil SOIC | Industrial |
| CY2308SXI-1HT | 16-pin 150 mil SOIC - Tape and Reel | Industrial |
| CY2308ZXC-1H | 16-pin 150 mil TSSOP | Commercial |
| CY2308ZXC-1HT | 16-pin 150 mil TSSOP - Tape and Reel | Commercial |
| CY2308ZXI-1H | 16-pin 150 mil TSSOP | Industrial |
| CY2308ZXI-1HT | 16-pin 150 mil TSSOP - Tape and Reel | Industrial |
| CY2308SXC-2 | 16-pin 150 mil SOIC | Commercial |
| CY2308SXC-2T | 16-pin 150 mil SOIC - Tape and Reel | Commercial |
| CY2308SXI-2 | 16-pin 150 mil SOIC | Industrial |
| CY2308SXI-2T | 16-pin 150 mil SOIC - Tape and Reel | Industrial |
| CY2308SXC-3 | 16-pin 150 mil SOIC | Commercial |
| CY2308SXC-3T | 16-pin 150 mil SOIC - Tape and Reel | Commercial |

Ordering Information (continued)

| Ordering Code | Package Type | Operating Range |
|---------------|-------------------------------------|-----------------|
| CY2308SXI-3 | 16-pin 150 mil SOIC | Industrial |
| CY2308SXI-3T | 16-pin 150 mil SOIC - Tape and Reel | Industrial |
| CY2308SXC-4 | 16-pin 150 mil SOIC | Commercial |
| CY2308SXC-4T | 16-pin 150 mil SOIC - Tape and Reel | Commercial |
| CY2308SXI-4 | 16-pin 150 mil SOIC | Industrial |
| CY2308SXI-4T | 16-pin 150 mil SOIC - Tape and Reel | Industrial |
| CY2308SXC-5H | 16-pin 150 mil SOIC | Commercial |
| CY2308SXC-5HT | 16-pin 150 mil SOIC - Tape and Reel | Commercial |
| CY2308SXI-5H | 16-pin 150 mil SOIC | Industrial |
| CY2308SXI-5HT | 16-pin 150 mil SOIC - Tape and Reel | Industrial |

Package Drawings and Dimensions

16-Pin (150 Mil) SOIC S16.15



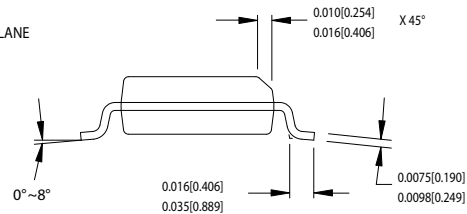
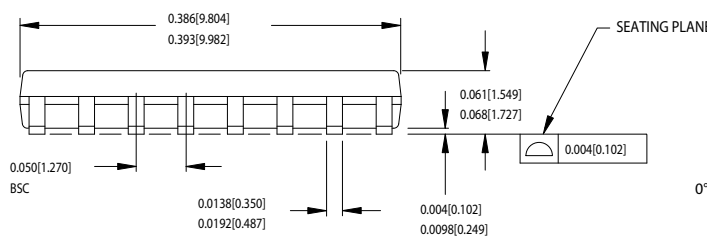
DIMENSIONS IN INCHES[MM] MIN.

MAX.

REFERENCE JEDEC MS-012

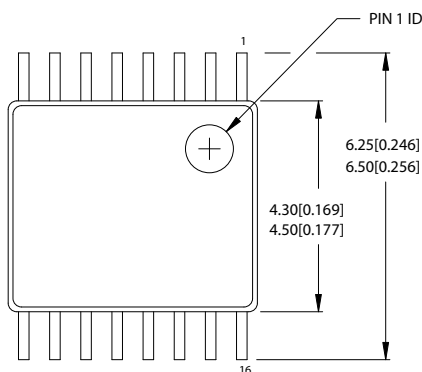
PACKAGE WEIGHT 0.15gms

| PART # | |
|---------|----------------|
| S16.15 | STANDARD PKG. |
| SZ16.15 | LEAD FREE PKG. |



51-85068-B

16-Pin TSSOP 4.40 MM Body Z16.173

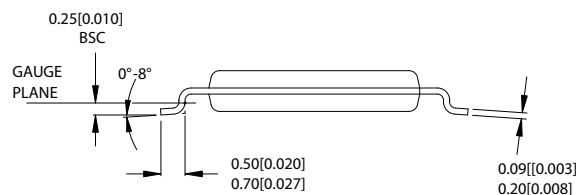
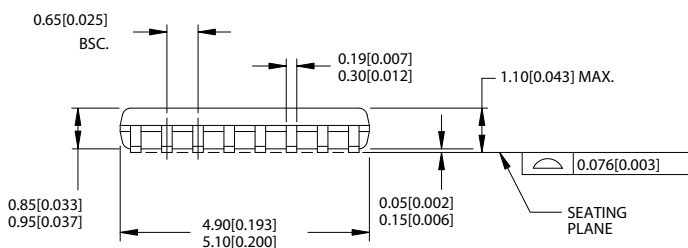


DIMENSIONS IN MM[INCHES] MIN.
MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05 gms

| PART # | |
|---------|----------------|
| Z16.173 | STANDARD PKG. |
| Z16.173 | LEAD FREE PKG. |



51-85091-A

Document History Page

| Document Title: CY2308 3.3V Zero Delay Buffer | | | | |
|---|---------|------------|-----------------|---|
| Document Number: 38-07146 | | | | |
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 110255 | 12/17/01 | SZV | Changed from Specification number: 38-00528 to 38-07146 |
| *A | 118722 | 10/31/02 | RGL | Added Note 1 in page 2. |
| *B | 121832 | 12/14/02 | RBI | Power up requirements added to Operating Conditions Information |
| *C | 235854 | See ECN | RGL | Added Pb-Free Devices |
| *D | 310594 | See ECN | RGL | Removed obsolete parts in the ordering information table Specified typical value for cycle-to-cycle jitter |
| *E | 1344343 | See ECN | KVM/VED | Brought the Ordering Information Table up to date: removed three obsolete parts and added two parts Changed titles to tables that are specific to commercial and industrial temperature ranges |

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