High-Speed USB 2.0 (480Mbps) DPST Switch with Overvoltage Protection (OVP) and Dedicated Charger Port Detection

ISL54227

ISL54227

The Intersil ISL54227 is a single supply, dual SPST (Single Pole/Single Throw) switch that is configured as a DPST. It can operate from a single 2.7V to 5.25V supply. The part was designed for switching or isolating a USB high-speed source or a USB high-speed and full-speed source in portable battery powered products.

The 3.5Ω SPST switches were specifically designed to pass USB full speed and USB high speed data signals. They have high bandwidth and low capacitance to pass USB high speed data signals with minimal distortion.The device has two logic control input pins (OE and LP) to control the SPST switches.

The ISL54227 has OVP detection circuitry on the COM pins to open the SPST switches when the voltage at these pins exceeds 3.8V or goes negative by -0.45V. It isolates fault voltages up to +5.25V or down to -5V from getting passed to the other side of the switch, thereby protecting the USB down-stream transceiver. It has an alarm indicator output pin ($\overline{ALM}$) to indicate when the part is in the overvoltage condition.

The part has an interrupt ($\overline{INT}$) output pin to indicate a 1 to 1 (high/high) state on the COM lines to inform the µprocessor when entering a dedicated charging port mode of operation.

The ISL54227 is available in 10 Ld 1.8mmx1.4mm µTQFN and 10 Ld 3mmx3mm TDFN packages. It operates over a temperature range of -40 to +85°C.

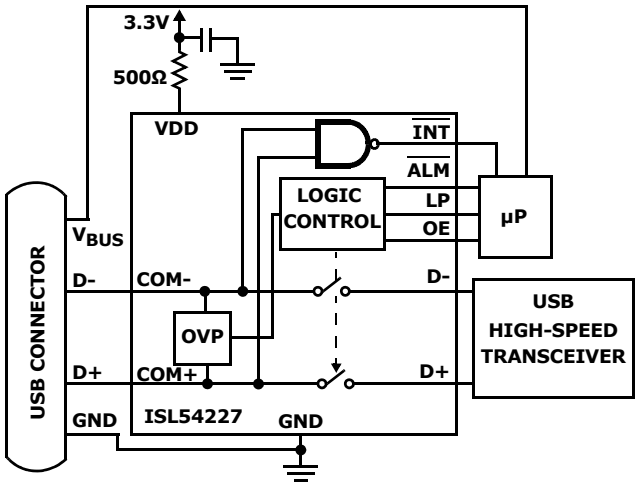
Features

- High-Speed (480Mbps) and Full-Speed (12Mbps) Signaling Capability per USB 2.0
- 1.8V Logic Compatible (2.7V to +3.6V supply)
- Alarm Overvoltage Indicator Output
- Charger Interrupt Indicator Output
- Low Power State
- Power OFF Protection
- COM Pins Overvoltage Detection and Protection for +5.25V and -5V Fault Voltages
- -3dB Frequency 790MHz
- Low ON Capacitance @ 240MHz 2pF
- Low ON-Resistance 3.5Ω
- Single Supply Operation (V_{DD}) . . . . . 2.7V to 5.25V
- Available in µTQFN and TDFN Packages
- Pb-Free (RoHS Compliant)
- Compliant with USB 2.0 Short Circuit and Overvoltage Requirements without Additional External Components

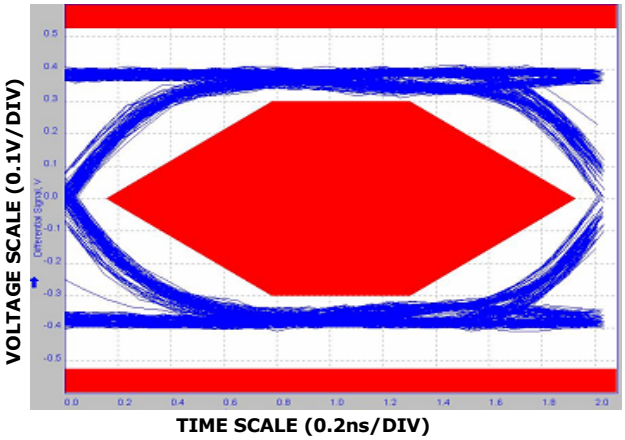
Applications* (see page 16)

- MP3 and other Personal Media Players
- Cellular/Mobile Phones, PDA's
- Digital Cameras and Camcorders
- USB Switching

Typical Application

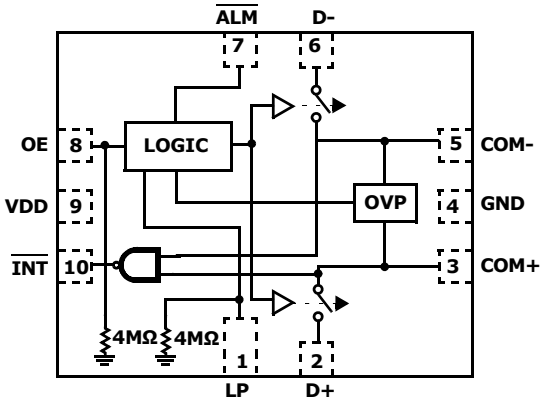


USB 2.0 HS Eye Pattern with Switches in the Signal Path

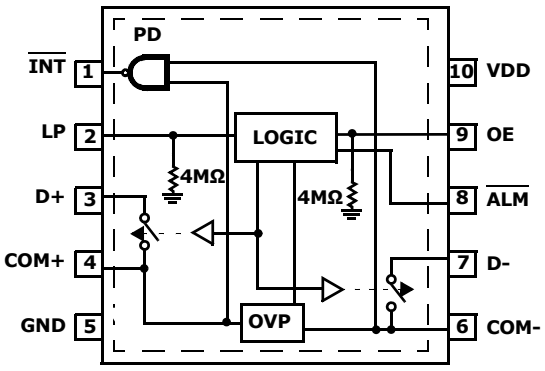


Pin Configurations

ISL54227
(10 LD 1.8X1.4 µTQFN)
TOP VIEW



ISL54227
(10 LD 3X3 TDFN)
TOP VIEW



NOTE:

1. Switches Shown for OE = "0".

Pin Descriptions

µTQFN	TDFN	PIN NAME	DESCRIPTION
1	2	LP	Low Power Input
2	3	D+	USB Data Port
3	4	COM+	USB Data Port
4	5	GND	Ground Connection
5	6	COM-	USB Data Port
6	7	D-	USB Data Port
7	8	$\overline{ALM}$	OTV ALARM Interrupt Output
8	9	OE	Switch Enable
9	10	VDD	Power Supply
10	1	$\overline{INT}$	Charger Mode Interrupt Output
-	PD	PD	Thermal Pad. Tie to Ground or Float

Truth Table

INPUT			OUTPUT			
SIGNAL AT COM PINS	LP	OE	D-, D+	$\overline{INT}$	$\overline{ALM}$	STATE
0V to 3.6V	0	0	OFF	High	High	Normal
0V to 3.6V	0	1	ON	High	High	Normal
0V to 3.6V	1	0	OFF	High	High	Low Power
Overvoltage Range 3.65V to 5.25V -0.29V to -5V	0	1	OFF	High	Low	OVP
COM Pins Tied Together	0	0	OFF	Low	High	Charger Port (CP)
COM Pins Tied Together	1	0	OFF	Low	High	Charger Port (Low Power)

Logic "0" when ≤ 0.5V, Logic "1" when ≥ 1.4V with a 2.7V to 3.6V Supply.

TABLE 1. OVP TRIP POINT VOLTAGE

SYSTEM VOLTAGE CONDITIONS				TRIP POINT	
CODEC SUPPLY	SWITCH SUPPLY (V_{DD})	COMs SHORTED TO	PROTECTED	MIN	MAX
2.7V to 3.3V	2.7V to 5.25V	VBUS	Yes	3.62V	3.95V
2.7V to 3.3V	2.7V to 5.25V	-5V	Yes	-0.6V	-0.29V

Ordering Information

PART NUMBER (Note 5)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54227IRUZ-T (Notes 2, 4)	U1	-40 to +85	10 Ld 1.8 x 1.4mm µTQFN (Tape and Reel)	L10.1.8x1.4A
ISL54227IRUZ-T7A (Notes 2, 4)	U1	-40 to +85	10 Ld 1.8 x 1.4mm µTQFN (Tape and Reel)	L10.1.8x1.4A
ISL54227IRTZ (Note 3)	4227	-40 to +85	10 Ld 3x3 TDFN	L10.3x3A
ISL54227IRTZ-T (Notes 2, 3)	4227	-40 to +85	10 Ld 3x3 TDFN (Tape and Reel)	L10.3x3A
ISL54227IRTZEVAL1Z	Evaluation Board			

NOTES:

2. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. For Moisture Sensitivity Level (MSL), please see device information page for ISL54227. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

VDD to GND . . . . . -0.3 to 6.5V
VDD to COMx. 10.5V
COMx to Dx 8.6V
Input Voltages
D+, D- . . . . . -0.3V to 6.5V
COM+, COM- . . . . . -5V to 6.5V
OE, LP . . . . . -0.3 to 6.5V
Continuous Current (COM-/D-, COM+/D+) . . . . . ±40mA
Peak Current (COM-/D-, COM+/D+)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA
ESD Rating:
Human Body Model (Tested per JESD22-A114-F). . . . >2kV
Machine Model (Tested per JESD22-A115-A). . . . . >150V
Charged Device Model (Tested per JESD22-C101-D) . >2kV
Latch-up (Tested per JEDEC; Class II Level A) . . . . at +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld µTQFN Package (Note 6, 9)	210	165
10 Ld TDFN Package (Notes 7, 8)	58	22

Maximum Junction Temperature (Plastic Package). . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Normal Operating Conditions

Temperature Range . . . . . -40°C to +85°C
V_{DD} Supply Voltage Range . . . . . 2.7V to 5.25V
Logic Control Input Voltage . . . . . 0V to 5.25V
Analog Signal Range, V_{DD} = 2.7V to 5.25V . . . . . 0V to 3.6V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
8. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
9. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications - 2.7V to 5.25V Supply Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{LP} = GND, V_{OEH} = 1.4V, V_{OEL} = 0.5V, (Note 10), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 11, 12)	TYP	MAX (Notes 11, 12)	UNITS
ANALOG SWITCH CHARACTERISTICS						
ON-Resistance, r_{ON} (High-Speed)	V_{DD} = 2.7V, OE = 1.4V, I_{Dx} = 17mA, V_{COM+} or V_{COM-} = 0V to 400mV (see Figure 2, Note 15)	25	-	3.5	5	Ω
		Full	-	-	**7**	Ω
r_{ON} Matching Between Channels, Δr_{ON} (High-Speed)	V_{DD} = 2.7V, OE = 1.4V, I_{Dx} = 17mA, V_{COM+} or V_{COM-} = Voltage at max r_{ON}, (Notes 14, 15)	25	-	0.2	0.45	Ω
		Full	-	-	**0.55**	Ω
r_{ON} Flatness, $R_{FLAT(ON)}$ (High-Speed)	V_{DD} = 2.7V, OE = 1.4V, I_{Dx} = 17mA, V_{COM+} or V_{COM-} = 0V to 400mV, (Notes 13, 15)	25	-	0.26	1	Ω
		Full	-	-	**1.2**	Ω
ON-Resistance, r_{ON}	V_{DD} = 3.3V, OE = 1.4V, I_{COMx} = 17mA, V_{COM+} or V_{COM-} = 3.3V (see Figure 2, Note 15)	+25	-	6.8	17	Ω
		Full	-	-	**22**	Ω
OFF Leakage Current, $I_{Dx(OFF)}$	V_{DD} = 5.25V, OE = 0V, V_{Dx} = 0.3V, 3.3V, V_{COMX} = 3.3V, 0.3V	25	-20	1	20	nA
		Full	**-**	30	**-**	nA
ON Leakage Current, $I_{Dx(ON)}$	V_{DD} = 5.25V, OE = 5.25V, V_{Dx} = 0.3V, 3.3V, V_{COMX} = 0.3V, 3.3V	25	-9	-	9	µA
		Full	**-12**	-	**12**	µA
Power OFF Leakage Current, I_{COM+}, I_{COM-}	V_{DD} = 0V, V_{COM+} = 5.25V, V_{COM-} = 5.25V, OE = 0V	25	-	-	11	µA
Power OFF Logic Current, I_{OE}	V_{DD} = 0V, OE = 5.25V	25	-	-	22	µA
Power OFF D+/D- Current, I_{D+}, I_{D-}	V_{DD} = 0V, OE = V_{DD}, V_{D+} = V_{D-} = 5.25V	25	-	-	1	µA

Electrical Specifications - 2.7V to 5.25V Supply Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{LP} = GND, V_{OEH} = 1.4V, V_{OEL} = 0.5V, (Note 10), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 11, 12)	TYP	MAX (Notes 11, 12)	UNITS
Overvoltage Protection Detection						
Positive Fault-Protection Trip Threshold, V_{PFP}	V_{DD} = 2.7V to 5.25V, OE = V_{DD} (See Table 1 on page 2)	25	3.62	3.8	3.95	V
Negative Fault-Protection Trip Threshold, V_{NFP}	V_{DD} = 2.7V to 5.25V, OE = V_{DD} (See Table 1 on page 2)	25	-0.6	-0.45	-0.29	V
OFF Persistance Time Fault Protection Response Time	Negative OVP Response: V_{DD} = 2.7V, SEL = 0V or V_{DD}, OE/ALM = V_{DD}, V_{Dx} = 0V to -5V, RL = 1.5kΩ	25	-	102		ns
	Positive OVP Response: V_{DD} = 2.7V, SEL = 0V or V_{DD}, OE/ALM = V_{DD}, V_{Dx} = 0V to 5.25V, RL = 1.5kΩ	25	-	2		µs
ON Persistance Time Fault Protection Recovery Time	V_{DD} = 2.7V, OE = V_{DD}, V_{Dx} = 0V to 5.25V or 0V to -5V, RL = 1.5kΩ	25	-	45		µs
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{DD} = 3.3V, V_{INPUT} = 3V, R_L = 50Ω, C_L = 50pF (see Figure 1)	25	-	160	-	ns
Turn-OFF Time, t_{OFF}	V_{DD} = 3.3V, V_{INPUT} = 3V, R_L = 50Ω, C_L = 50pF (see Figure 1)	25	-	60	-	ns
Skew, ($t_{SKEWOUT}$ - t_{SKEWIN})	V_{DD} = 3.3V, OE = 3.3V, R_L = 45Ω, C_L = 10pF, t_R = t_F = 500ps at 480Mbps, (Duty Cycle = 50%) (see Figure 5)	25	-	50	-	ps
Rise/Fall Degradation (Propagation Delay), t_{PD}	V_{DD} = 3.3V, OE = 3.3V, R_L = 45Ω, C_L = 10pF, (see Figure 5)	25	-	250	-	ps
Crosstalk	V_{DD} = 3.3V, R_L = 50Ω, f = 240MHz (see Figure 4)	25	-	-39	-	dB
OFF-Isolation	V_{DD} = 3.3V, OE = 0V, R_L = 50Ω, f = 240MHz	25	-	-23	-	dB
-3dB Bandwidth	Signal = 0dBm, 0.86VDC offset, R_L = 50Ω	25	-	790	-	MHz
OFF Capacitance, C_{OFF}	f = 1MHz, V_{DD} = 3.3V, LP = 0V, OE = 0V (see Figure 3)	25	-	2.5	-	pF
COM ON Capacitance, $C_{(ON)}$	f = 1MHz, V_{DD} = 3.3V, LP = 0V, OE = 3.3V, (see Figure 3)	25	-	4	-	pF
COM ON Capacitance, $C_{(ON)}$	f = 240MHz, V_{DD} = 3.3V, LP = 0V, OE = 3.3V	25	-	2	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range, V_{DD}		Full	**2.7**		**5.25**	V
Positive Supply Current, I_{DD}	V_{DD} = 5.25V, OE = 5.25V, LP = GND	25	-	45	56	µA
		Full	-	-	**59**	µA
Positive Supply Current, I_{DD}	V_{DD} = 3.6V, OE = 3.6V, LP = GND	25	-	23	30	µA
		Full	-	-	**34**	µA
Positive Supply Current, I_{DD} (Low Power State)	V_{DD} = 3.6V, OE = 0V, LP = V_{DD}	25	-	5	6	µA
		Full	-	-	**10**	µA

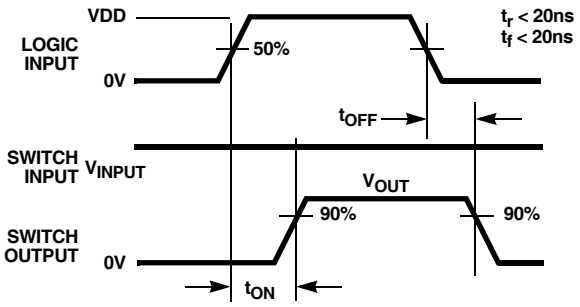
Electrical Specifications - 2.7V to 5.25V Supply Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{LP} = GND, V_{OEH} = 1.4V, V_{OEL} = 0.5V, (Note 10), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 11, 12)	TYP	MAX (Notes 11, 12)	UNITS
Positive Supply Current, I_{DD}	V_{DD} = 4.3V, OE = 2.6V, LP = GND	25	-	35	45	µA
		Full	-	-	**50**	µA
Positive Supply Current, I_{DD}	V_{DD} = 3.6V, OE = 1.4V, LP = GND	25	-	25	32	µA
		Full	-	-	**38**	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{OEL}, V_{LPL}	V_{DD} = 2.7V to 3.6V	Full	-	-	**0.5**	V
Input Voltage High, V_{OEH}, V_{LPH}	V_{DD} = 2.7V to 3.6V	Full	**1.4**	-	-	V
Input Voltage Low, V_{OEL}, V_{LPL}	V_{DD} = 3.7V to 4.2V	Full	-	-	**0.7**	V
Input Voltage High, V_{OEH}, V_{LPH}	V_{DD} = 3.7V to 4.2	Full	**1.7**	-	-	V
Input Voltage Low, V_{OEL}, V_{LPL}	V_{DD} = 4.3V to 5.25V	Full	-	-	**0.8**	V
Input Voltage High, V_{OEH}, V_{LPH}	V_{DD} = 4.3V to 5.25V	Full	**2.0**	-	-	V
Input Current, I_{OEL}, I_{LPL}	V_{DD} = 5.25V, OE = 0V, LP = 0V	Full	-	-8.2	-	nA
Input Current, I_{OEH}, I_{LPH}	V_{DD} = 5.25V, OE = 5.25V, LP = 5.25V, 4MΩ Pull-down	Full	-	1.4	-	µA

NOTES:

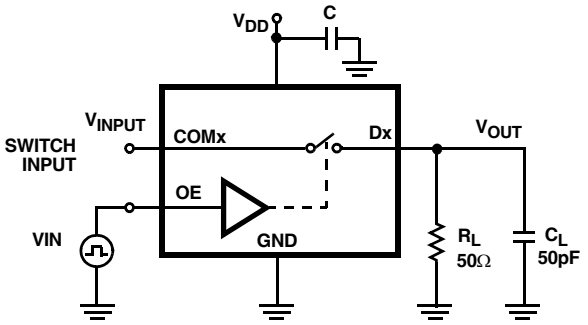
10. V_{LOGIC} = Input voltage to perform proper function.
11. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
12. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
13. Flatness is defined as the difference between maximum and minimum value of ON-resistance over the specified analog signal range.
14. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value.
15. Limits established by characterization and are not production tested.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS

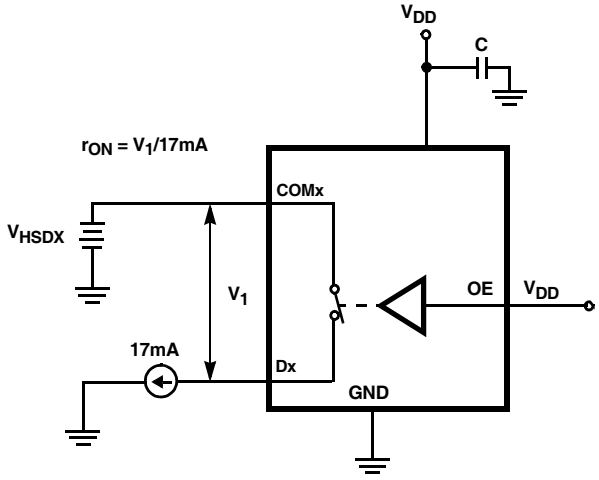


Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(INPUT)} \frac{R_L}{R_L + r_{ON}}$$

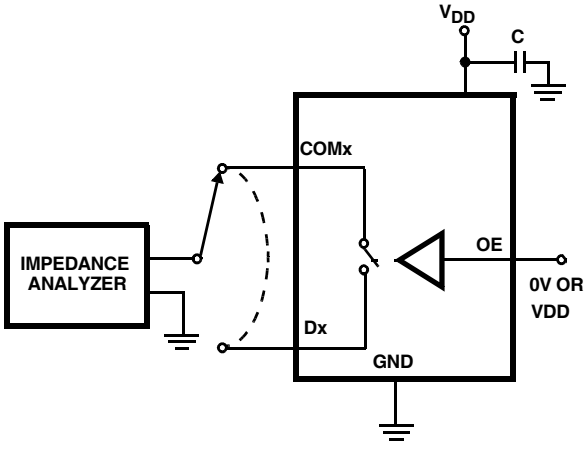
FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES



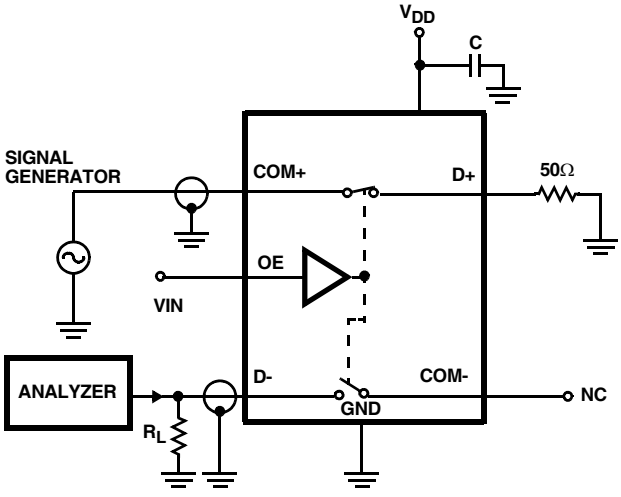
Repeat test for all switches.

FIGURE 2. r_{ON} TEST CIRCUIT



Repeat test for all switches.

FIGURE 3. CAPACITANCE TEST CIRCUIT



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 4. CROSSTALK TEST CIRCUIT

Test Circuits and Waveforms (Continued)

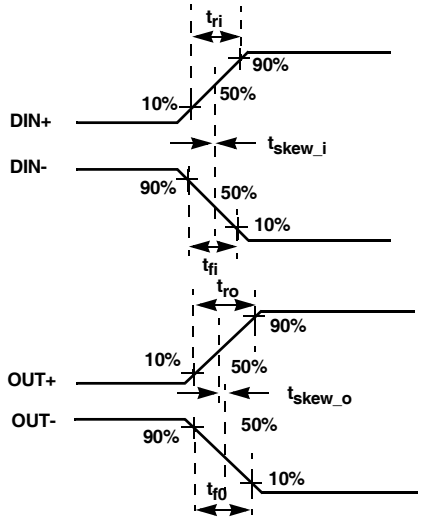
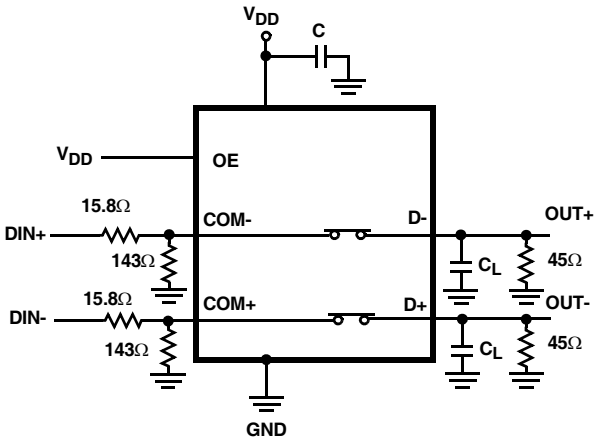


FIGURE 5A. MEASUREMENT POINTS



|tro - tri| Delay Due to Switch for Rising Input and Rising Output Signals.

|tfo - tfi| Delay Due to Switch for Falling Input and Falling Output Signals.

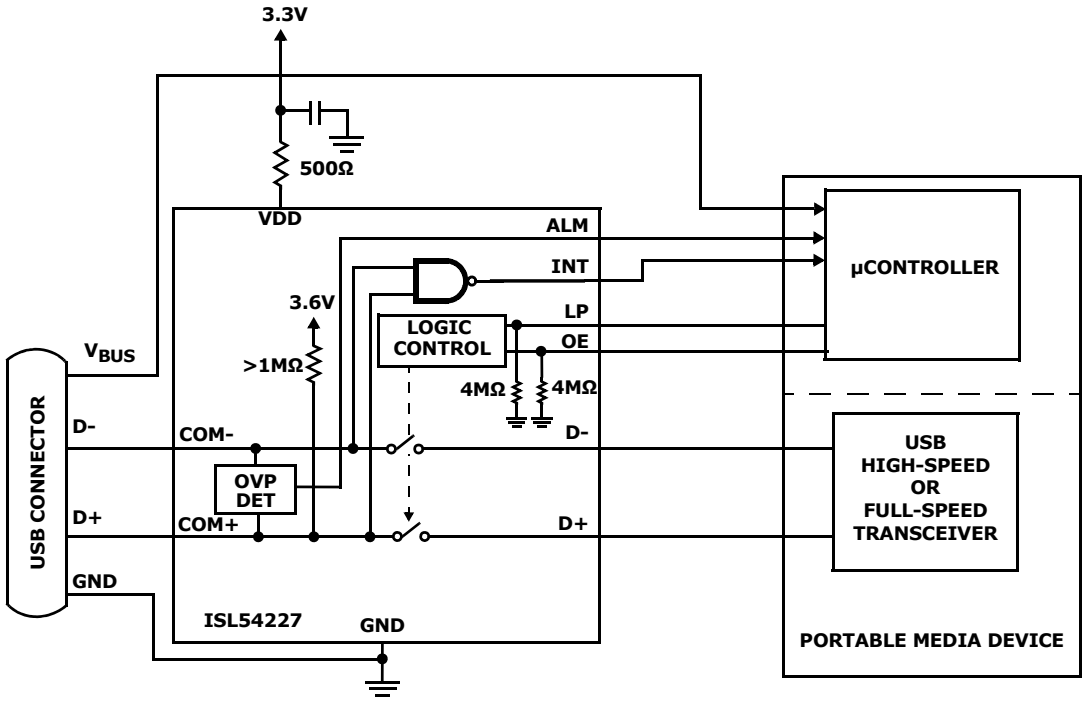
|tskew_0| Change in Skew through the Switch for Output Signals.

|tskew_i| Change in Skew through the Switch for Input Signals.

FIGURE 5B. TEST CIRCUIT

FIGURE 5. SKEW TEST

Application Block Diagram



Detailed Description

The ISL54227 device is a dual single pole/single throw (SPST) analog switch configured as a DPST that operates from a single DC power supply in the range of 2.7V to 5.25V.

It was designed for switching a USB high-speed or full-speed source in portable battery powered products. It is offered in small µTQFN and TDFN packages for use in MP3 players, cameras, PDAs, cellphones, and other personal media players.

The part consists of two 3.5Ω high-speed SPST switches. These switches have high bandwidth and low capacitance to pass USB high-speed (480Mbps) differential data signals with minimal edge and phase distortion. They can also swing from 0V to 3.6V to pass USB full speed (12Mbps) differential data signals with minimal distortion.

The device has a single logic control pin (OE) to open and close the two SPST switches. The part has an LP control pin to put the part in a low power state.

The part contains special over voltage protection (OVP) circuitry on the COM+ and COM- pins. This circuitry acts to open the SPST switches when the part senses a voltage on the COM pins that is >3.8V (typ) or < -0.45V (typ). It isolates voltages up to 5.25V and down to -5V from getting through to the other side of the switches (D-, D+) to protect the USB down-stream transceiver connected at the D+ and D- pins. It has an alarm ($\overline{ALM}$) interrupt output to indicate when the device has detected and entered the OTV state. This output can be monitored by a µController to indicate a fault condition to the system.

The part has charger port interrupt detection circuitry (CP) on the COM pins that outputs a Low on the $\overline{INT}$ pin to inform the µController or power management circuitry when entering a dedicated charging port mode of operation. The charger mode operation is initiated by driving the OE pin Low and externally connecting the COM pins together which pulls the COM lines High, triggering the INT pin to go Low and the SPST switches to open.

The ISL54227 was designed for MP3 players, cameras, cellphones, and other personal media player applications that need to switch a high-speed or full-speed transceiver source. See this functionality in the "Application Block Diagram" on page 8.

A detailed description of the SPST switches is provided in the following section.

High-Speed (Dx) SPST Switches

The Dx switches are bi-directional switches that can pass USB high-speed and USB full-speed signals when VDD is in the range of 2.7V to 5.25V.

When powered with a 2.7V supply, these switches have a nominal r_{ON} of 3.5Ω over the signal range of 0V to 400mV with a r_{ON} flatness of 0.26Ω. The r_{ON} matching between the switches over this signal range is only 0.2Ω, ensuring minimal impact by the switches to USB high speed signal transitions. As the signal level increases, the r_{ON} switch resistance increases. At signal level of 3.3V, the switch resistance is nominally 6.8Ω. See Figures 9, 10, 11, 12, 13, 14 in the "Typical Performance Curves" beginning on page 11.

The Dx switches were specifically designed to pass USB 2.0 high-speed (480Mbps) differential signals in the range of 0V to 400mV. They have low capacitance and high bandwidth to pass the USB high-speed signals with minimum edge and phase distortion to meet USB 2.0 high speed signal quality specifications. See Figure 15 in the "Typical Performance Curves" on page 13 for USB High-speed Eye Pattern taken with switch in the signal path.

The Dx switches can also pass USB full-speed signals (12Mbps) in the range of 0V to 3.6V with minimal distortion and meet all the USB requirements for USB 2.0 full-speed signaling. See Figure 16 in the "Typical Performance Curves" on page 14 for USB Full-speed Eye Pattern taken with switch in the signal path.

The switches are active (turned ON) whenever the $\overline{OE}$ voltage is logic "1"(High) and the LP voltage is logic "0" (Low) and OFF when the OE voltage is logic "0" (Low) and the LP voltage is logic "0" (Low) or logic "1" (High).

OVERVOLTAGE PROTECTION (OVP)

The maximum normal operating signal range for the Dx switches is from 0V to 3.6V. For normal operation the signal voltage should not be allow to exceed these voltage levels or go below ground by more than -0.3V.

However, in the event that a positive voltage >3.8V (typ) to 5.25V, such as the USB 5V V_{BUS} voltage, gets shorted to one or both of the COM+ and COM- pins or a negative voltage <-0.45V (typ) to -5V gets shorted to one or both of the COM pins, the ISL54227 has OVP circuitry to detect the over voltage condition and open the SPST switches to prevent damage to the USB down-stream transceiver connected at the signal pins (D-, D+).

The OVP and power-off protection circuitry allows the COM pins (COM-, COM+) to be driven up to 5.25V while the V_{DD} supply voltage is in the range of 0V to 5.25V. In this condition, the part draws <100µA of I_{COMx} and I_{DD} current and causes no stress to the IC. In addition the SPST switches are OFF and the fault voltage is isolated from the other side of the switch.

The part has an alarm ($\overline{ALM}$) interrupt output to indicate when the device has detected and entered the OTV state. This output can be monitored by a µController to indicate a fault condition to the system.

External V_{DD} Series Resistor to Limit I_{DD} Current during Negative OVP Condition

A 100Ω to 1kΩ resistor in series with the VDD pin (see Figure 6) is required to limit the IDD current draw from the system power supply rail during a negative OVP fault event.

With a negative -5V fault voltage at both com pins, the graph in Figure 7 shows the IDD current draw for different external resistor values for supply voltages of 2.7V, 3.6V, and 5.25V. Note: With a 500Ω resistor the current draw is limited to around 5mA. When the negative fault voltage is removed the I_{DD} current will return to it's normal operation current of 25µA to 45µA.

The series resistor also provides improved ESD and latch-up immunity. During an overvoltage transient event (such as occurs during system level IEC 61000 ESD testing), substrate currents can be generated in the IC that can trigger parasitic SCR structures to turn ON, creating a low impedance path from the VDD power supply to ground. This will result in a significant amount of current flow in the IC, which can potentially create a latch-up state or permanently damage the IC. The external VDD resistor limits the current during this overstress situation and has been found to prevent latch-up or destructive damage for many overvoltage transient events.

Under normal operation, the low microamp I_{DD} current of the IC produces an insignificant voltage drop across the series resistor resulting in no impact to switch operation or performance.

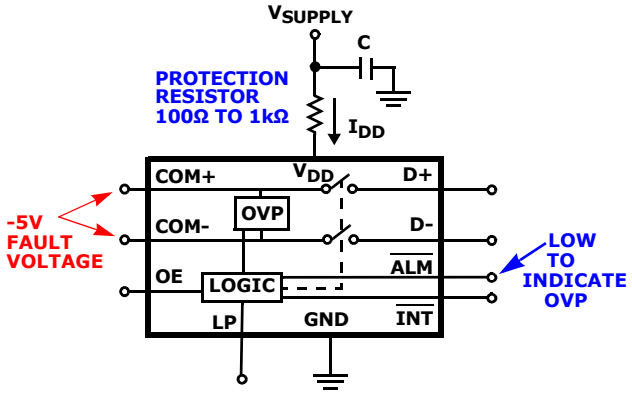


FIGURE 6. V_{DD} SERIES RESISTOR TO LIMIT I_{DD} CURRENT DURING NEGATIVE OVP AND FOR ENHANCED ESD AND LATCH-UP IMMUNITY

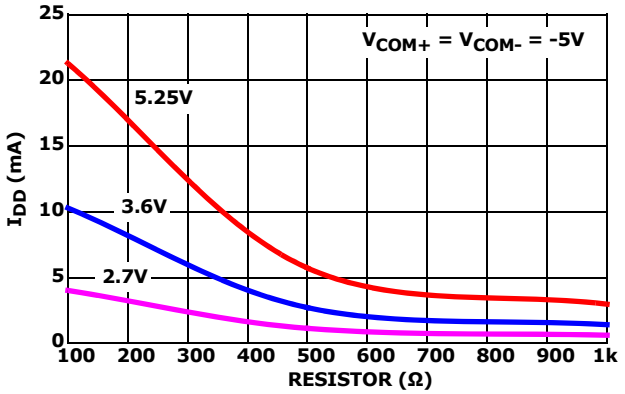


FIGURE 7. NEGATIVE OVP I_{DD} CURRRENT vs RESISTOR VALUE vs V_{SUPPLY}

CHARGER PORT DETECTION

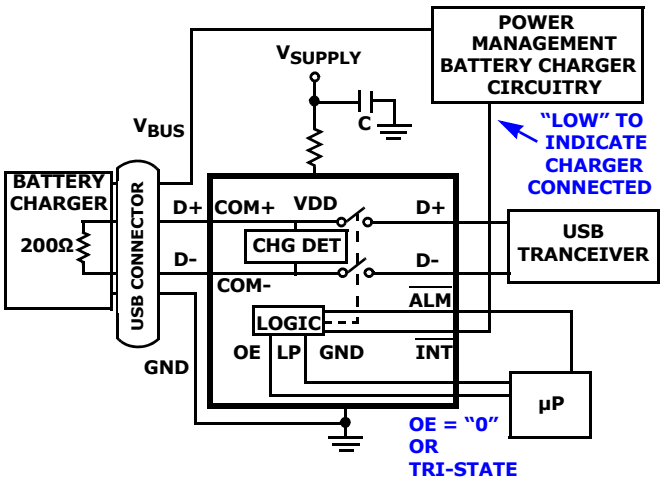


FIGURE 8. CHARGER PORT DETECTION

The ISL54227 has special charger port detection circuitry that monitors the voltage at the com pins to detect when a battery charger has been connected into the USB port (see Figure 8).

When the battery charger is connected into the USB connector, it shorts the COM+ and COM- pins together. The shorting of the pins is sensed by the ISL54227 IC and it pulls the COM+ and COM- lines high and as long as the OE = "0" or is tri-stated by the µP, it will drive its $\overline{INT}$ logic output "Low" to tell the power management circuitry that a battery charger is connected at the port and not a USB host transceiver. The power management circuitry will then use the USB connector V_{BUS} line to charge the battery.

ISL54227 Operation

The following will discuss using the ISL54227 shown in the "Application Block Diagram" on page 8.

POWER

The power supply connected at the VDD pin provides the DC bias voltage required by the ISL54227 part for proper operation. The ISL54227 can be operated with a V_{DD} voltage in the range of 2.7V to 5.25V.

For lowest power consumption you should use the lowest V_{DD} supply.

A 0.01µF or 0.1µF decoupling capacitor should be connected from the VDD pin to ground to filter out any power supply noise from entering the part. The capacitor should be located as close to the VDD pin as possible.

In a typical application, V_{DD} will be in the range of 2.8V to 4.3V and will be connected to the battery or LDO of the portable media device.

LOGIC CONTROL

The state of the ISL54227 device is determined by the voltage at the OE pin, LP pin, and the signal voltage at the COM pins. Refer to "Truth Table" on page 2.

The OE and LP pins are internally pulled low through a 4MΩ resistor to ground and can be tri-stated or left floating.

The ISL54227 is designed to minimize I_{DD} current consumption when the logic control voltage is lower than the V_{DD} supply voltage. With V_{DD} = 3.6V and the OE logic pin is at 1.4V the part typically draws only 25µA. With V_{DD} = 4.3V and the OE logic pin is at 2.6V the part typically draws only 35µA. Driving the logic pin to the V_{DD} supply rail minimizes power consumption.

The OE and LP pin can be driven with a voltage higher than the V_{DD} supply voltage. It can be driven up to 5.25V with a V_{DD} supply in the range of 2.7V to 5.25V.

TABLE 2. LOGIC CONTROL VOLTAGE LEVELS

V_{DD} SUPPLY RANGE	LOGIC = "0" (LOW)		LOGIC = "1" (HIGH)	
	OE	LP	OE	LP
2.7V to 3.6V	≤ 0.5V or floating	≤ 0.5V or floating	≥1.4V	≥1.4V
3.7V to 4.2V	≤ 0.7V or floating	≤ 0.7V or floating	≥1.7V	≥1.7V
4.3V to 5.25V	≤ 0.8V or floating	≤ 0.8V or floating	≥2.0V	≥2.0V

Low Power Mode

If the OE pin = Logic "0", and the LP pin = Logic "1" the switches will turn OFF (high impedance) and the part will be put in a low power mode. In this mode the part draws only 10µA (max) of current across the operating temperature range.

Normal Operation Mode

With a signal level in the range of 0V to 3.6V and with the LP pin = Logic "0" the switches will be ON when the OE pin = Logic "1" and will be OFF (high impedance) when the OE pin = Logic "0".

USB 2.0 V_{BUS} Short Requirments

The USB specification in section 7.1.1 states a USB device must be able to withstand a V_{BUS} short (4.4V to 5.25V) or a -1V short to the D+ or D- signal lines when the device is either powered off or powered on for at least 24 hours.

The ISL54227 part has special power-off protection and OVP detection circuitry to meet these short circuit requirements. This circuitry allows the ISL54227 to provide protection to the USB down-stream transceiver connected at its signal pins (D-, D+) to meet the USB specification short circuit requirements.

The power-off protection and OVP circuitry allows the COM pins (COM-, COM+) to be driven up to 5.25V or down to -5V while the V_{DD} supply voltage is in the range of 0V to 5.25V. In these overvoltage conditions with a 500Ω external V_{DD} resistor the part draws <55µA of current into the COM pins and causes no stress/damage to the IC. In addition all switches are OFF and the shorted V_{BUS} voltage will be isolated from getting through to the other side of the switch channels, thereby protecting the USB transceiver.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

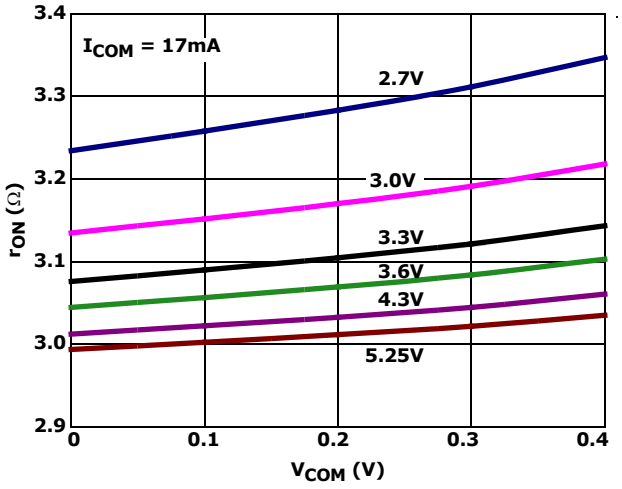


FIGURE 9. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

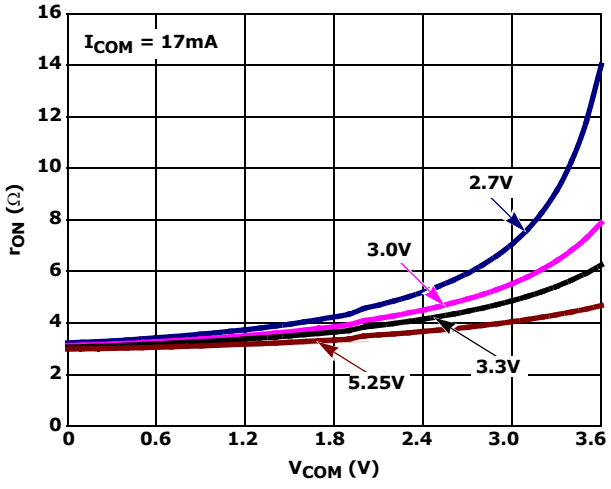


FIGURE 10. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

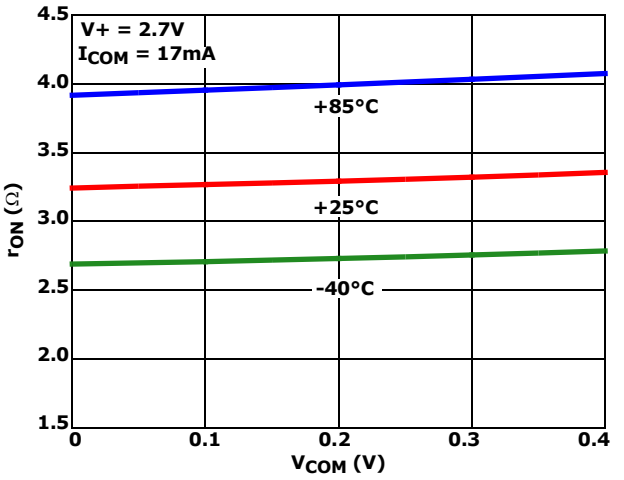


FIGURE 11. ON-RESISTANCE vs SWITCH VOLTAGE

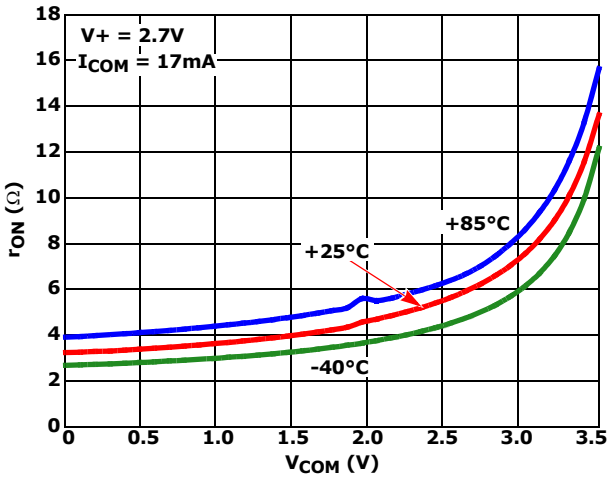


FIGURE 12. ON-RESISTANCE vs SWITCH VOLTAGE

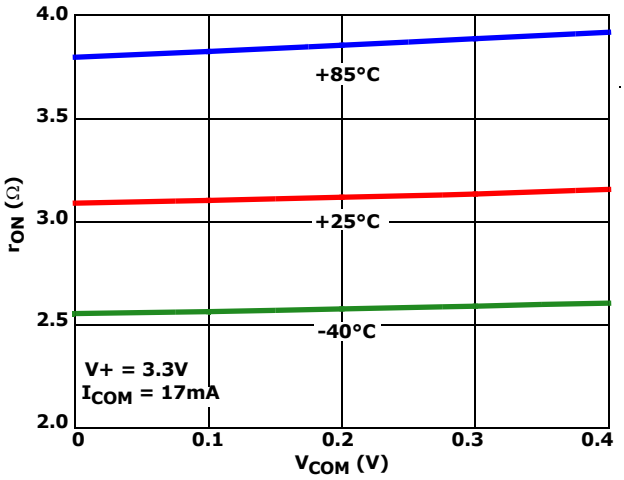


FIGURE 13. ON-RESISTANCE vs SWITCH VOLTAGE

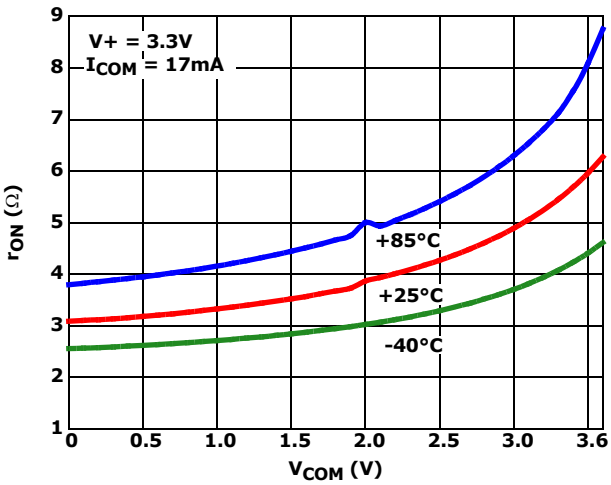


FIGURE 14. ON-RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

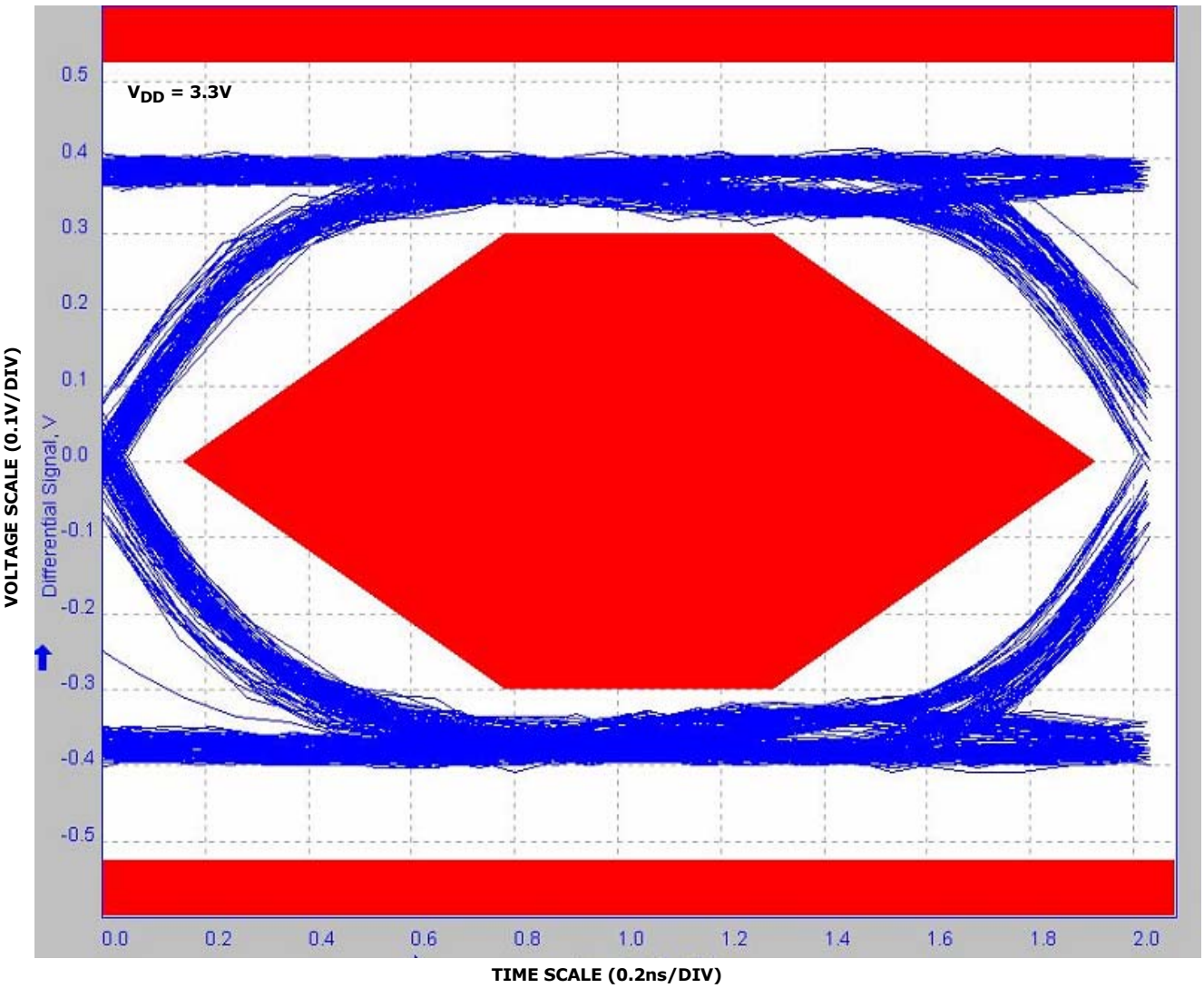


FIGURE 15. EYE PATTERN: 480Mbps WITH USB SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

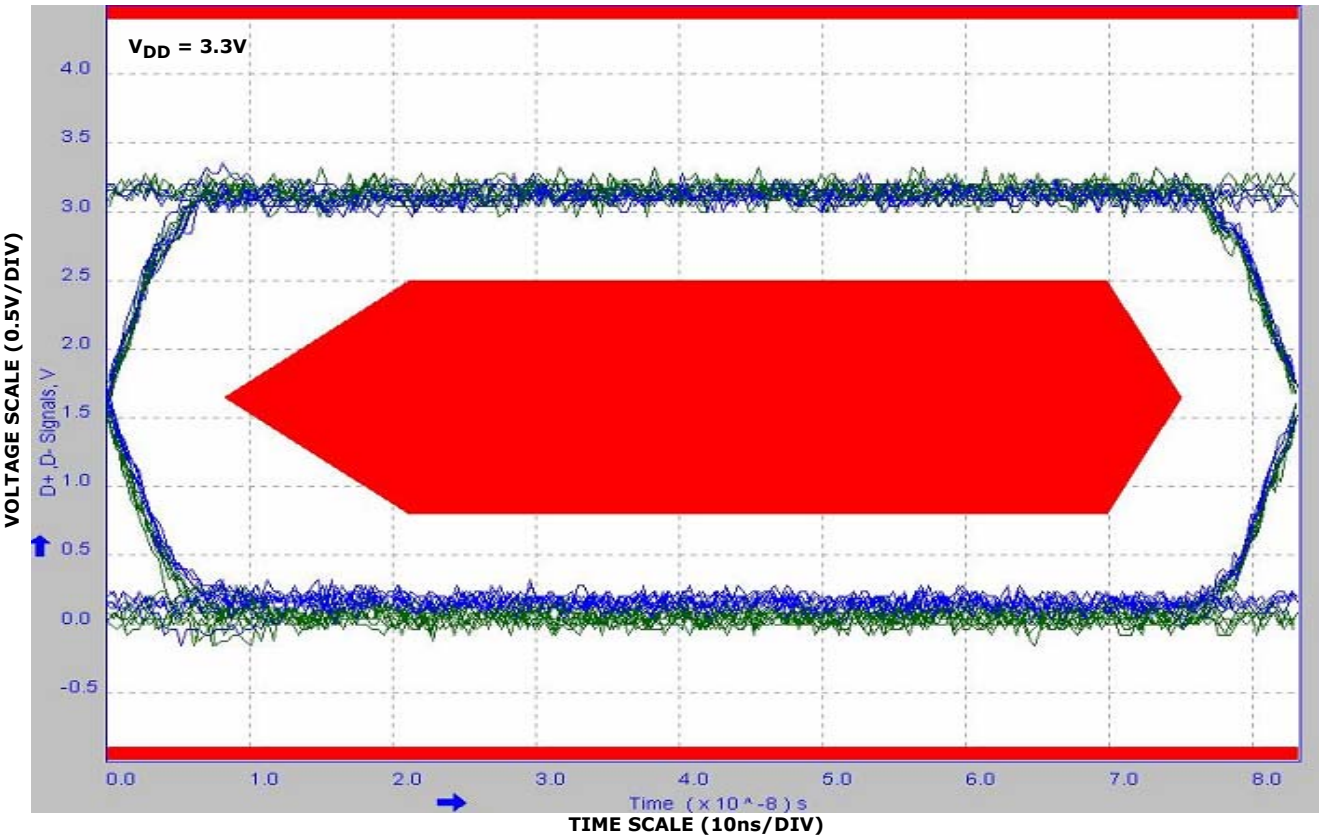


FIGURE 16. EYE PATTERN: 12Mbps WITH USB SWITCHES IN THE SIGNAL PATH

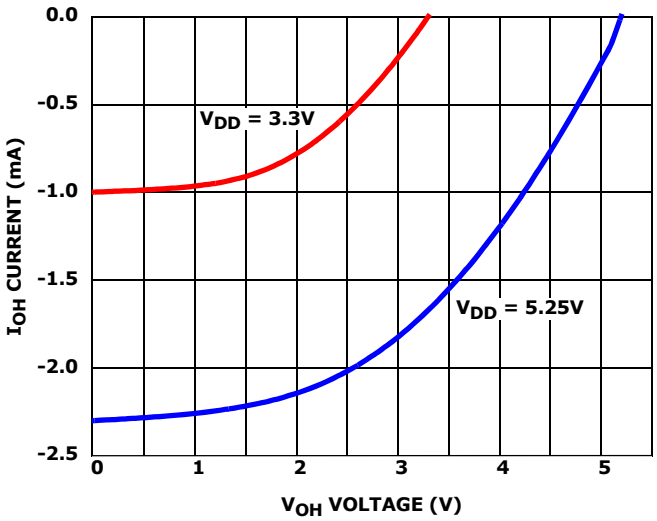


FIGURE 17. I_{OH} vs V_{OH} vs V_{DD} for $\overline{INT}$ and $\overline{ALM}$

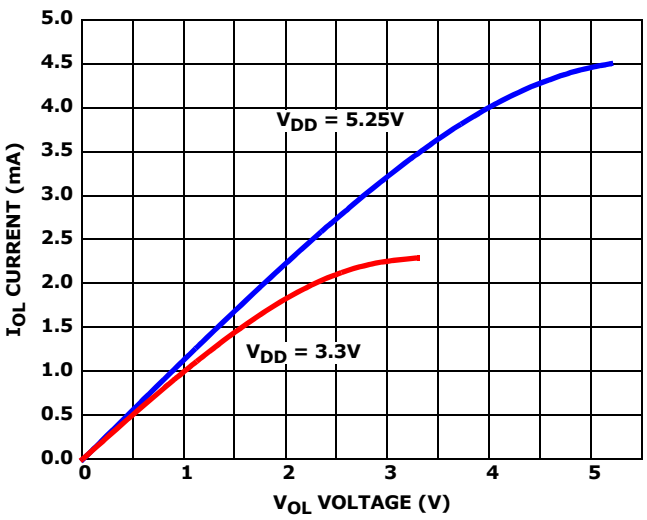


FIGURE 18. I_{OL} vs V_{OL} vs V_{DD} for $\overline{INT}$ and $\overline{ALM}$

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

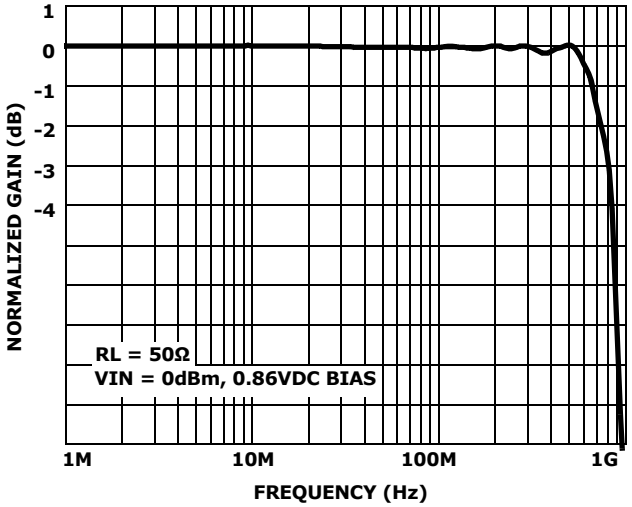


FIGURE 19. FREQUENCY RESPONSE

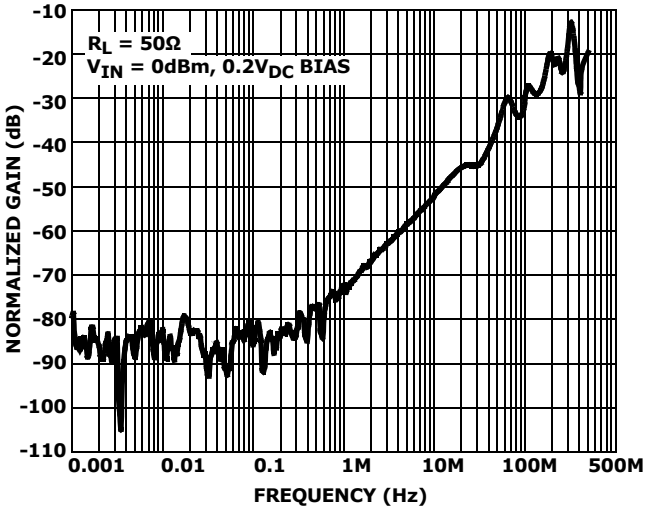


FIGURE 20. OFF-ISOLATION

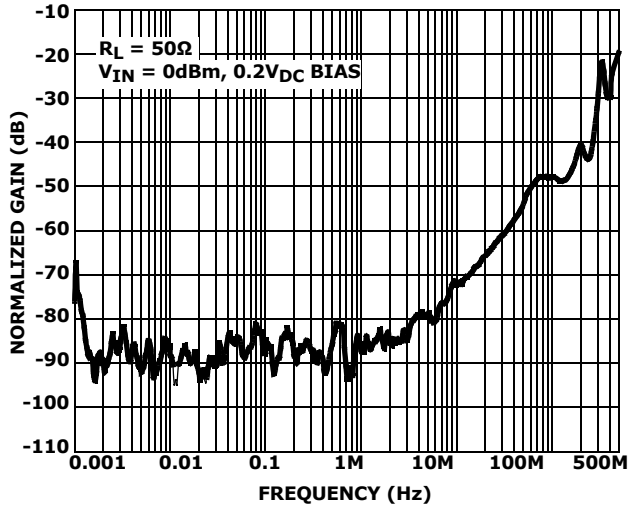


FIGURE 21. CROSSTALK

Die Characteristics

SUBSTRATE AND TDFN THERMAL PAD POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

1297

PROCESS:

Submicron CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
7/2/10	FN7593.0	Initial Release.

Products

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*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL54227

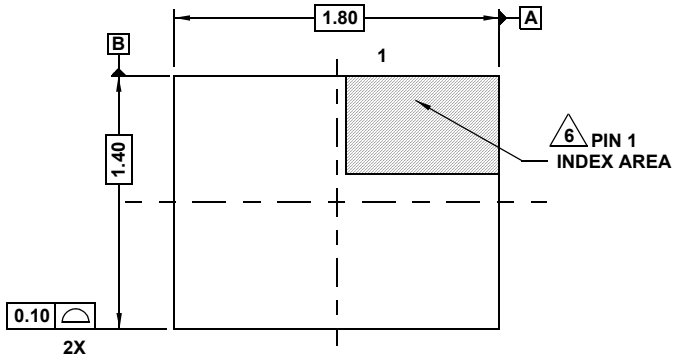
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

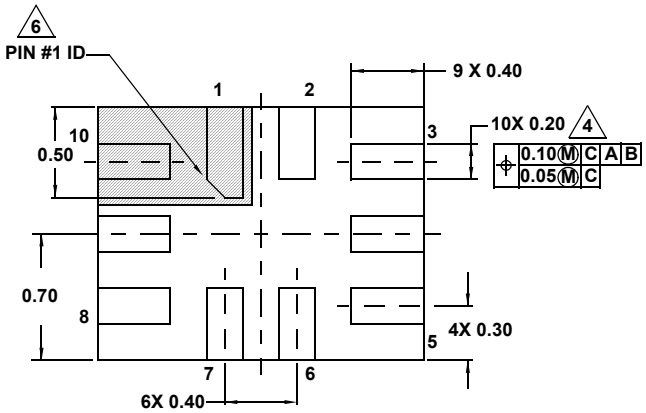
Package Outline Drawing

L10.1.8x1.4A

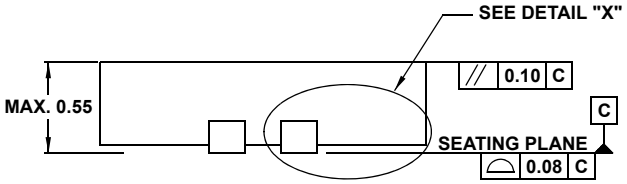
10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 5, 3/10



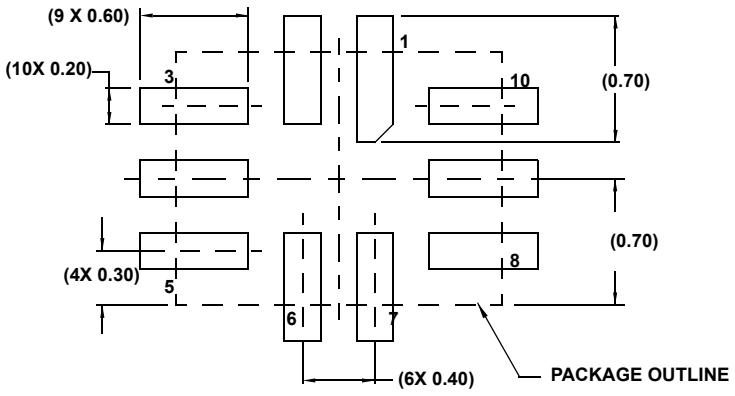
TOP VIEW



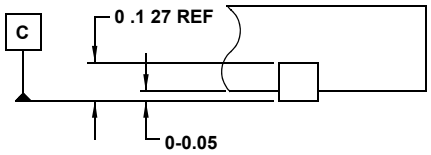
BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN



DETAIL "X"

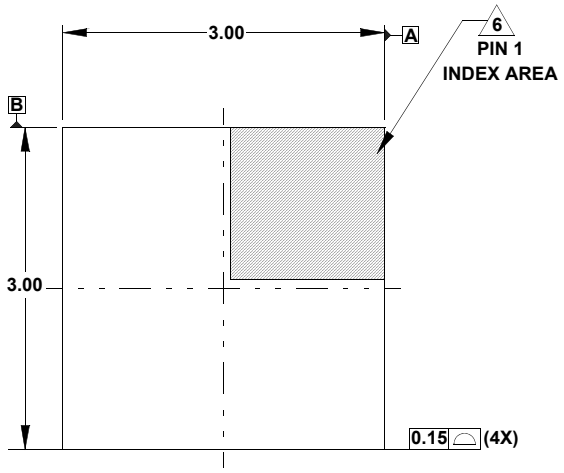
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. JEDEC reference MO-255.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

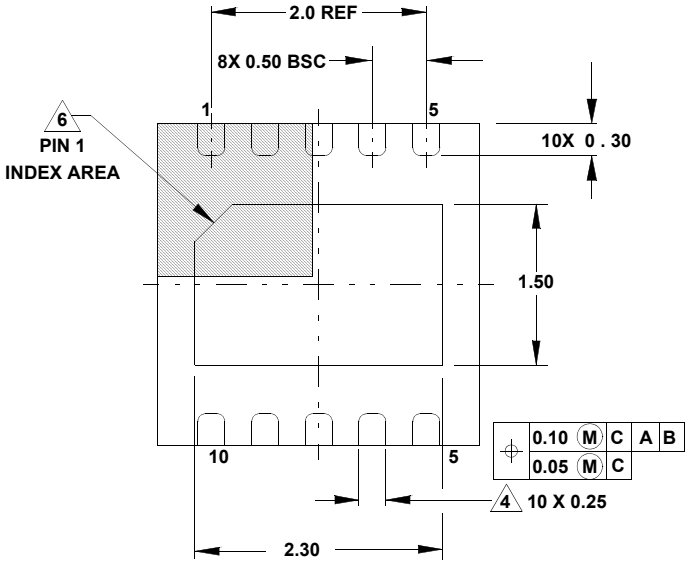
Package Outline Drawing

L10.3x3A

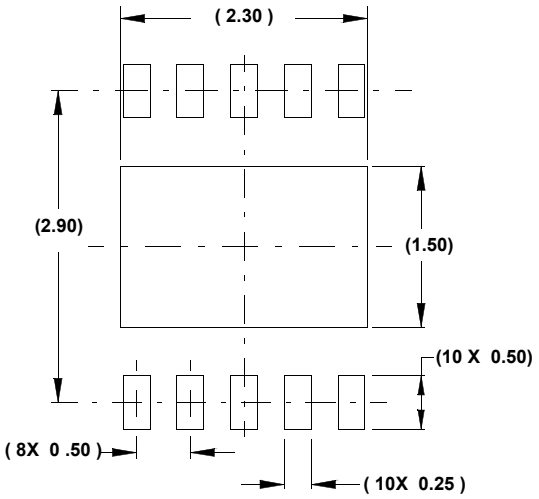
10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 5, 3/10



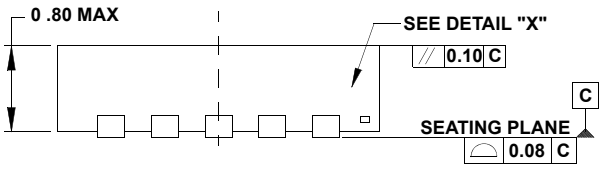
TOP VIEW



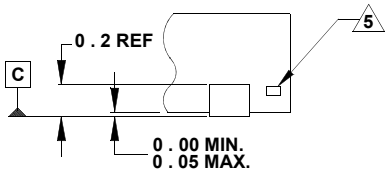
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
   Angular ±2.50°
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229-WEED-3 except exposed pad length (2.30mm).