

Description

The CXG1134AEN is a high power and high Isolation SPDT switch MMIC. This IC can be used in wireless communication systems. The CXG1134AEN can be operated by one CMOS control line. The Sony GaAs J-FET process is used for low insertion loss and on-chip logic circuit.
(Applications : Cellular handsets ; PDC, CDMA)

Features

- ◆ Low insertion loss : 0.25dB @900MHz,
0.35dB @1.9GHz
- ◆ High linearity : IIP3 (typ.) = 70dBm
- ◆ 1 CMOS compatible control line
- ◆ Small package size : 10-pin VSON

Package

10 pin VSON (Plastic)

Structure

GaAs J-FET MMIC

Absolute Maximum Ratings

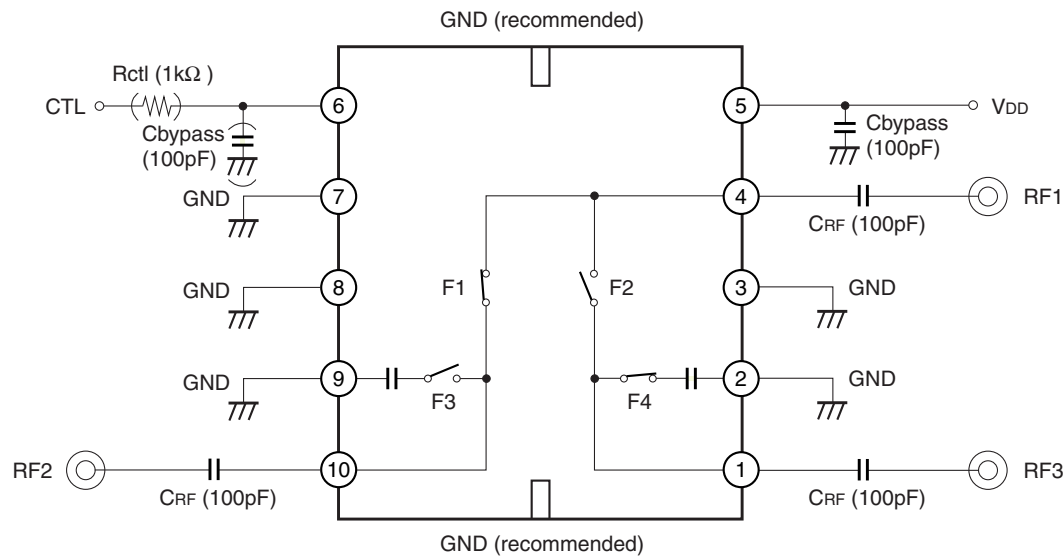
(Ta = 25°C)

◆ Bias voltage	V _{DD}	7	V
◆ Control voltage	V _{ctl}	5	V
◆ Operating temperature	T _{opr}	– 35 to + 85	°C
◆ Storage temperature	T _{stg}	– 65 to + 150	°C

This IC is ESD sensitive device. Special handling precautions are required.

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Block Diagram and Recommended Circuit



When using this IC, the following external parts should be used :

- Rctl : This resistor is used to improve ESD performance. 1kΩ is recommended.
- CRF : This capacitor is used for RF de-coupling and must be used for all applications. 100pF is recommended.
- Cbypass : This capacitor is used for DC line filtering. 100pF is recommended.

Truth Table

On Pass	CTL	F1	F2	F3	F4
RF1 – RF2	H	ON	OFF	OFF	ON
RF1 – RF3	L	OFF	ON	ON	OFF

DC Bias Condition (Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.2	3.0	3.6	V
Vctl (L)	0	—	0.4	V
VDD	2.7	3.0	3.6	V



Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	900MHz		0.25	0.50	dB
Isolation	ISO.	900MHz	28	32		dB
VSWR	VSWR	900MHz		1.2	1.4	—
Harmonics	2fo	*1		− 75	− 60	dBc
	3fo	*1		− 75	− 60	dBc
1dB compression input power	P1dB	V _{DD} = 3.0V, 0/3V control	32	35		dBm
Switching speed	TSW			2	5	μs
Control current	I _{ctl}	V _{ctl} (High) = 3V		10	30	μA
Bias current	I _{DD}	V _{DD} = 3V		50	100	μA

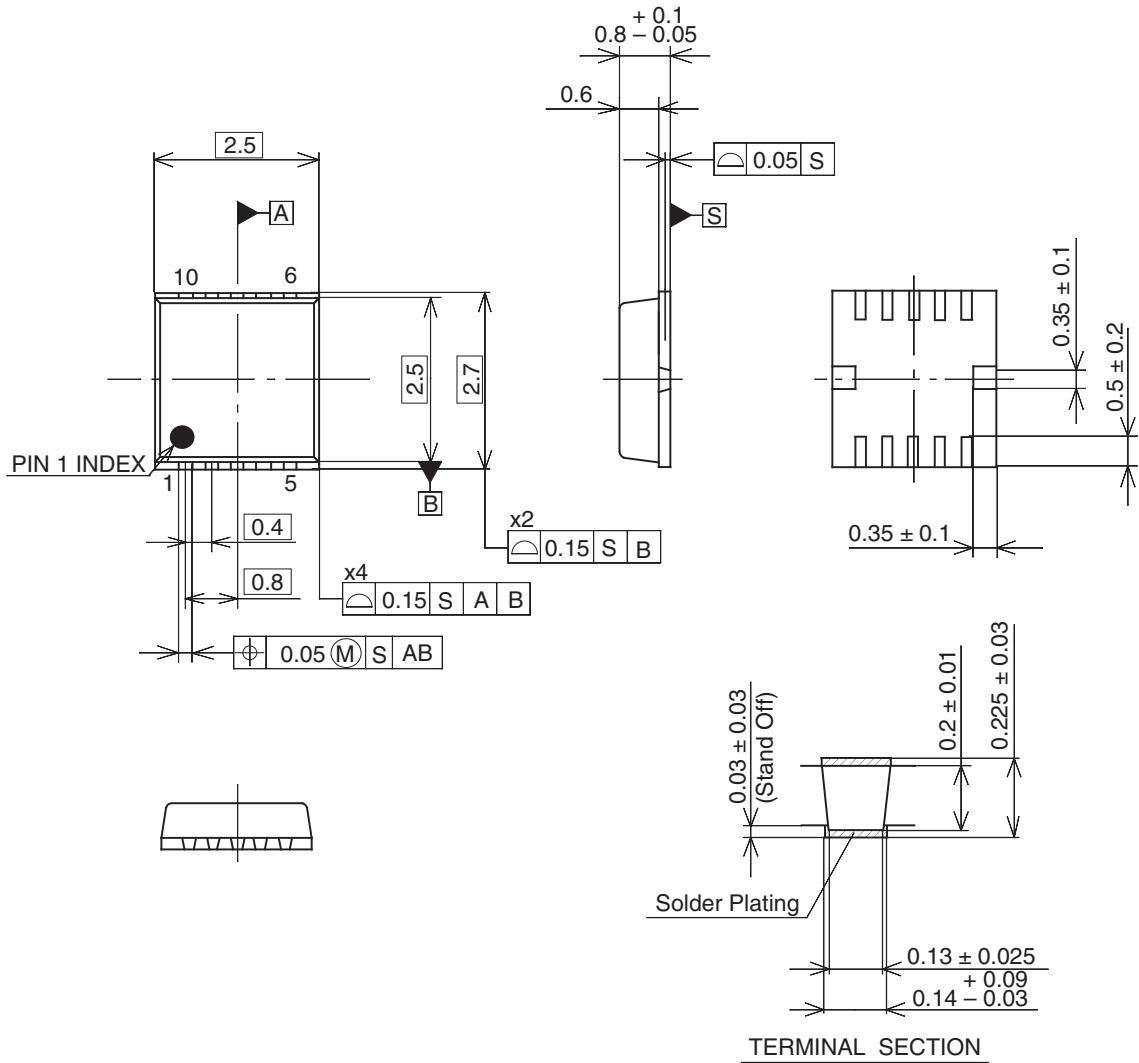
*1 Pin = 30dBm, 900MHz, V_{DD} = 3.0V, 0/3V control



Package Outline

(Unit : mm)

10PIN VSON(PLASTIC)



NOTE:1) The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.

PACKAGE STRUCTURE

SONY CODE	VSON-10P-01
EIAJ CODE	_____
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.013g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm