

# R2A20124AFP/R2A20124ASP

REJ03D0928-0200 Rev.2.00 Aug 03, 2010

# Synchronous Phase Shift Full-Bridge Control IC Series

## **Description**

The R2A20124AFP/R2A20124ASP controls a full-bridge phase shift circuit and secondary synchronous rectification. The R2A20124AFP/R2A20124ASP has adjustable delay time functions which make ZVS of primary side and make loss of body diode of primary switching device minimal.

The R2A20124AFP/R2A20124ASP is based on HA16163/R2A20121. And RAMP slope compensation circuit is builtin as an additional function. Also its output driver circuits are improved to enlarge gate drive output voltage swing from VREF to VCC.

In addition R2A20124AFP has ON/OFF function of synchronous rectification and includes amplifier which detect input current signal.

#### **Features**

- Maximum ratings
  - Supply voltage Vcc: 20 V
  - Operating junction temperature Tj-opr: –40 to +125°C
- Electrical characteristics
  - VFB feedback voltage VFB(-): 1.25 V  $\pm$  2.0%
  - UVLO (Under Voltage Lockout) operation start voltage VH:  $8.4 \text{ V} \pm 0.7 \text{ V}$
  - UVLO operation shutdown voltage VL:  $8.0 \text{ V} \pm 0.6 \text{ V}$
  - UVLO hysteresis voltage dVUVL:  $0.4 \text{ V} \pm 0.1 \text{ V}$
  - Output voltage swing of OUT-A, B, C, D, and E for gate drive: GND to VCC
- Functions

### R2A20124AFP/R2A20124ASP

- Full-bridge phase-shift switching circuit with adjustable delay times
- Pulse by pulse current limit
- Synchronization I/O for the oscillator
- Ramp sloping adjustor
- Error amplifier built-in
- Soft start function

#### R2A20124AFP

- Synchronous rectification on/off control
- Remote on/off control
- Amplified output of current sense input voltage: CS
- · Package lineup
  - Pb-free LQFP-40: R2A20124AFP
  - Pb-free SOP-20: R2A20124ASP

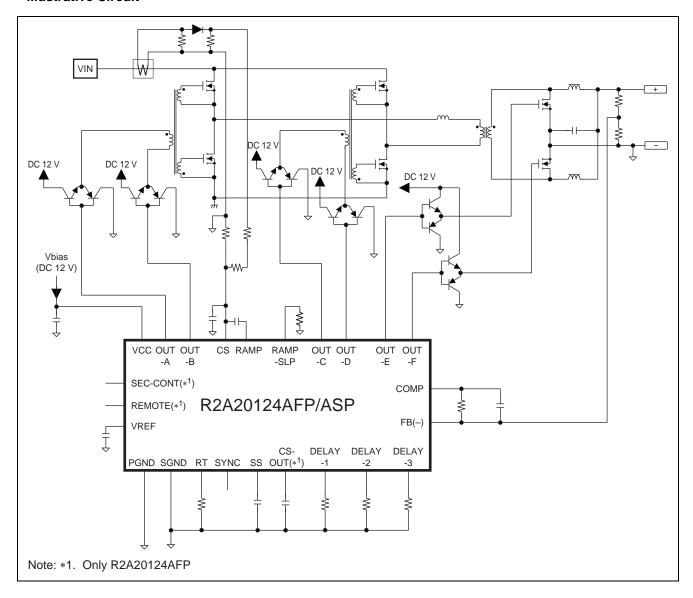
## **Ordering Information**

Part No.	Package Name	Package Code	Taping Spec.
R2A20124AFP-W0	FP-40EV	PLQP0040JB-C	2000 pcs./one taping product
R2A20124AFP-W5			2000 pcs./one taping product
R2A20124AFP-U0			_
R2A20124AFP-U5			_
R2A20124ASP-W0	FP-20DAV	PRSP0020DD-B	2000 pcs./one taping product
R2A20124ASP-W5			2000 pcs./one taping product
R2A20124ASP-U0			_
R2A20124ASP-U5			_

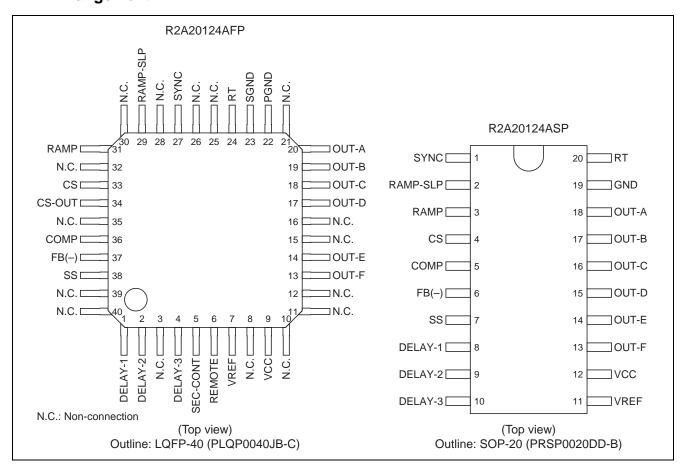
## **Modified Points from R2A20121SP**

- The swing level of the maximum output voltage is changed from VREF to VCC.
- Ramp sloping compensation circuit is added.
- Synchronous rectification control is possible to turned off at light load. (only R2A20124AFP)
- On/off control terminal for Remote is added. (only R2A20124AFP)

## **Illustrative Circuit**



## **Pin Arrangement**

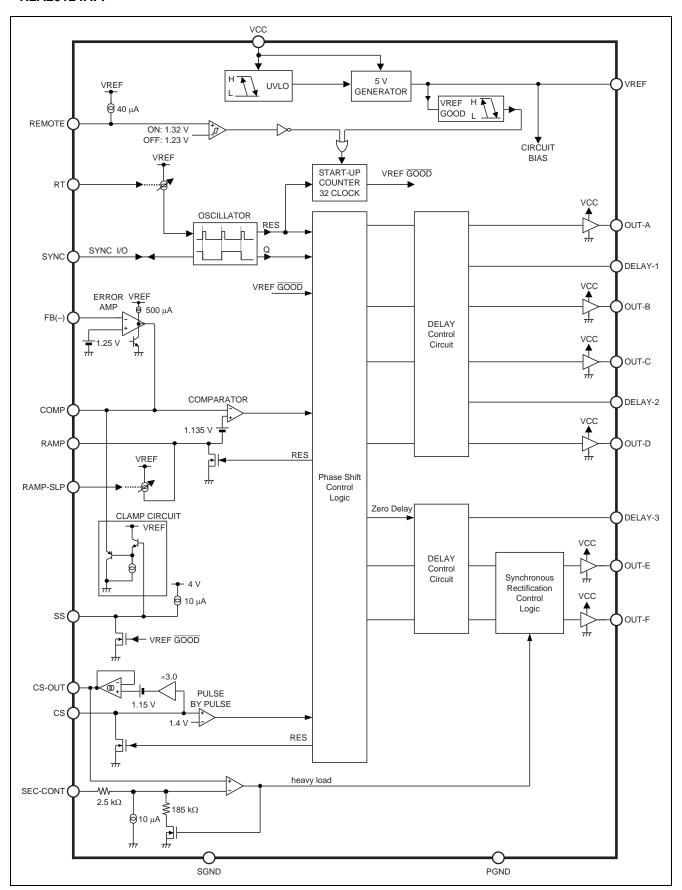


## **Pin Functions**

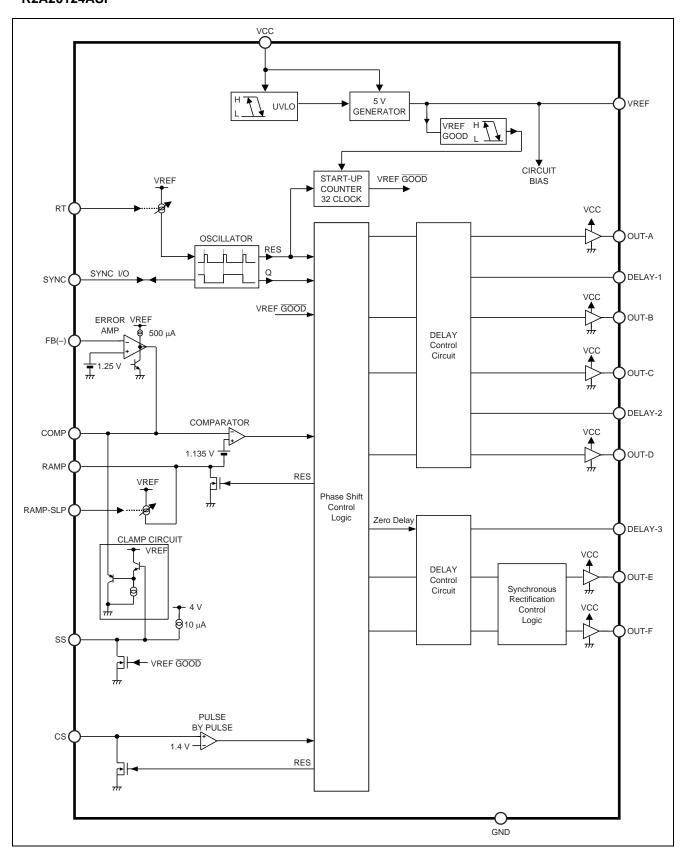
LQFP-40	SOP-20			
Pin No.	Pin No.	Pin Name	Input/Output	Pin Function
1	8	DELAY-1	Input/Output	Delay time adjustor for the full-bridge control signal (OUT-A and B)
2	9	DELAY-2	Input/Output	Delay time adjustor for the full-bridge control signal (OUT-C and D)
4	10	DELAY-3	Input/Output	Delay time adjustor for the secondary control signal (OUT-E and F)
5	_	SEC-CONT	Input	Synchronous rectification on/off control
6	_	REMOTE	Input	Remote on/off control
7	11	VREF	Output	5 V/20 mA output
9	12	VCC	Input	IC power supply input
13	13	OUT-F	Output	Secondary control signal
14	14	OUT-E	Output	Secondary control signal
17	15	OUT-D	Output	Full-bridge control signal
18	16	OUT-C	Output	Full-bridge control signal
19	17	OUT-B	Output	Full-bridge control signal
20	18	OUT-A	Output	Full-bridge control signal
22	_	PGND	_	Ground level for the output signal
23	_	SGND	_	Ground level for the small signal
_	19	GND	_	Ground
24	20	RT	Input/Output	Timing resistor for the oscillator
27	1	SYNC	Input/Output	Synchronization I/O for the oscillator
29	2	RAMP-SLP	Input/Output	Ramp sloping adjustor
31	3	RAMP	Input	Ramp waveform set
33	4	CS	Input	Current sense signal input for OCP
34	_	CS-OUT	Output	Current sense information amplifier output
36	5	COMP	Output	Error amplifier output
37	6	FB(-)	Input	Error amplifier negative input
38	7	SS	Output	Timing capacitor for soft start
3, 8, 10 to 12, 15, 16, 21, 25, 26, 28, 30, 32,	_	N.C.	_	Open
35, 39, 40				

## **Block Diagram**

#### **R2A20124AFP**



### **R2A20124ASP**



## **Absolute Maximum Ratings**

 $(Ta = 25^{\circ}C)$ 

Item	Symbol	Ratings	Unit	Note
Power supply voltage	Vcc	20	V	1
Peak output current	lpk-out	±200	mA	2, 3
DC output current	ldc-out	±50	mA	3, 4
VREF output current	Iref-out	-20	mA	3
COMP sink current	Isink-comp	2	mA	3
DELAY set current	Iset-delay	0.3	mA	3
RT set current	Iset-rt	0.3	mA	3
RAMP-SLP set current	Iset-ramp-slp	0.3	mA	3
VREF terminal voltage	Vter-ref	-0.3 to +6	V	1, 5
Terminal group 1 voltage	Vter-1	-0.3 to (Vref + 0.3)	V	1, 6
Operating junction temperature	Tj-opr	-40 to +125	°C	7
Storage temperature	Tstg	−55 to +150	°C	

- Notes: 1. Rated voltages are with reference to the GND or SGND pin.
  - 2. The Rating shows the transient current when driving a capacitive load.
  - 3. For rated currents, inflow to the IC is indicated by (+), and outflow by (-).
  - 4. Total current of OUT-A, Out-B, OUT-C, OUT-D, OUT-E, and OUT-F must be not exceed ±90 mA.
  - 5. VREF pin voltage must not exceed VCC pin voltage.
  - 6. Terminal group 1 is defined the pins; REMOTE, RAMP-SLP, SEC-CONT, CS, RAMP, COMP, CS-OUT, FB(-), SS, RT, SYNC, and DELAY-1 to 3
  - 7. Theramal resistance θja R2A20124AFP (40-pin); 85.3°C/W Board condition; Glass epoxy 50 mm × 50 mm × 1.6 mm, 10% wiring density. R2A20124ASP (20-pin); 120°C/W Board condition; Glass epoxy 40 mm × 40 mm × 1.6 mm, 10% wiring density.

## **Electrical Characteristics**

 $(Ta=25^{\circ}C,\,Vcc=12\,\,V,\,RT=180\,\,k\Omega,\,Rdelay=51\,\,k\Omega,\,Rramp-slp=27\,\,k\Omega,\,unless\,\,otherwise\,\,specified.)$ 

Item	Symbol	Min	Тур	Max	Unit	Test Conditions	
SUPPLY: R2A20124AFP/ASP							
Start threshold	VH	7.7	8.4	9.1	V		
Shutdown threshold	VL	7.4	8.0	8.6	V		
UVLO hysteresis	dVUVL	0.3	0.4	0.5	V		
Start-up current	Is	_	90	150	μΑ	Vcc = 7.5 V	
Operating current	Icc	_	8	11.5	mA	No load on VREF pin	
VREF: R2A20124AFP/ASP	•				•		
Output voltage	Vref	4.9	5.0	5.1	V		
Line regulation	Vref-line	_	0	10	mV	Vcc= 10 V to 16 V	
Load regulation	Vref-load	_	6	20	mV	Iref= -1 mA to -20 mA	
Temperature stability	dVref/dTa	_	±80*1	_	ppm/°C	Ta = -40°C to 105°C	
OSCILLATOR: R2A20124AFP/ASP	•	•					
Oscillator frequency	fosc	_	200* <sup>1</sup>	_	kHz		
Switching frequency	fsw	85	100	115	kHz	Measured on OUT-A, -B	
Line stability	fsw-line	-1.5	0	1.5	%	Vcc = 10 V to 16 V	
Temperature stability	dfsw/dTa	_	±0.1*1	_	%/°C	Ta = -40°C to 105°C	
RT voltage	$V_{RT}$	2.5	2.7	2.9	V		
SYNC: R2A20124AFP/ASP	•				•		
Input threshold	V <sub>TH-SYNC</sub>	2.5	2.85	3.2	V		
Output high	V <sub>OH-SYNC</sub>	3.5	4.0	_	V	RSYNC = 33 k $\Omega$ to GND * <sup>2</sup>	
Output low	V <sub>OL-SYNC</sub>	_	0.05	0.15	V	RSYNC = $33 \text{ k}\Omega$ to VREF	
Minimum input pulse	T <sub>I-MIN</sub>	50	_	_	ns		
Output pulse width	T <sub>O-SYNC</sub>	_	3.0*1	_	μS		
REMOTE: R2A20124AFP	•				•		
On threshold voltage	V <sub>ON-REMOTE</sub>	1.12	1.32	1.52	V		
Off threshold voltage	V <sub>OFF-REMOTE</sub>	1.04	1.23	1.42	V		
REMOTE hysteresis	dVREMOTE	60	90	120	mV		
Input bias current	I <sub>REMOTE</sub>	-100	-50	_	μΑ	REMOTE = 2 V	
ERROR AMPLIFIER: R2A20124AF	P/ASP						
FB(-) input voltage	V <sub>FB(-)</sub>	1.225	1.250	1.275	V	FB(-) and COMP are shorted	
FB(-) input current	I <sub>FB(-)</sub>	-2.0	0	2.0	μΑ	FB(-) = 1.25 V	
Open-loop DC gain	Av	_	80* <sup>1</sup>	_	dB		
Unity gain bandwidth	BW	_	2* <sup>1</sup>	_	MHz		
Output source current	I <sub>SOURCE</sub>	-650	-500	-390	μΑ	FB(-) = 0.75 V, COMP = 2 V	
Output sink current	I <sub>SINK</sub>	2.0	6.5	_	mA	FB(-) = 1.75 V, COMP = 2 V	
Output high voltage	V <sub>OH-EO</sub>	3.7	3.9	_	V	FB(-) = 0.75 V, COMP; open	
Output low voltage	V <sub>OL-EO</sub>	_	0.1	0.4	V	FB(-) = 1.75 V, COMP; open	
Output clamp voltage *3	V <sub>CLAMP-EO</sub>	-0.16	-0.07	0.0	V	FB(-) = 0.75 V, COMP; open, SS = 1 V	
Notes: 1. Design specification (r	oforonoo data)	•		•		•	

Notes: 1. Design specification (reference data)

2. R2A20124AFP: SGND and PGND

3.  $V_{CLAMP-EO} = V_{COMP} - SS \text{ voltage (1 V)}$ 

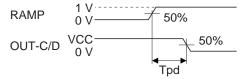
## Electrical Characteristics (cont.)

(Ta = 25°C, Vcc = 12 V, RT = 180 kΩ, Rdelay = 51 kΩ, Rramp-slp = 27 kΩ, unless otherwise specified.)

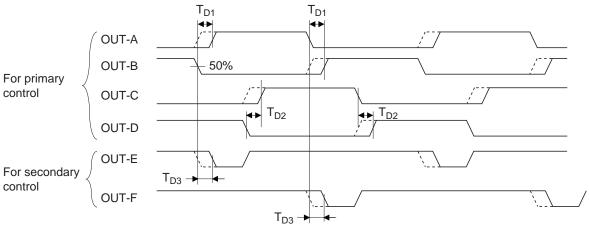
Item	Symbol	Min	Тур	Max	Unit	Test Conditions	
PHASE MODULATOR: R2A20124AFP/ASP							
RAMP offset voltage	V <sub>RAMP</sub>	1.035	1.135	1.235	V		
RAMP source current	Isource-RAMP	-220	-185	-150	μΑ	RAMP = 0.15 V, COMP; open	
RAMP sink current	I <sub>SINK-RAMP</sub>	3	10		mA	RAMP = 0.15 V, COMP = 0 V	
Minimum phase shift	Dmin		0*1*4	_	%	RAMP = 0 V, COMP = 0 V	
Maximum phase shift	Dmax	_	97.0* <sup>1</sup> * <sup>4</sup>		%	RAMP = 0 V, COMP = 2.1 V	
Delay to OUT-C, -D *2	Tpd	_	100	200	ns	COMP = 1.6 V	
RAMP discharge time *1	Tdis	_	80	120	ns	FB(-) = 0.75 V, COMP; open	
RAMP-SLP voltage	V <sub>RAMP-SLP</sub>	2.1	2.3	2.5	>		
DELAY: R2A20124AFP/ASP							
DELAY-1, -2 *3	T <sub>D1, 2</sub>	70	100	130	ns	Delay set R = 51 k $\Omega$	
DELAY-3 *3	T <sub>D3</sub>	45	65	85	ns	Delay set R = 51 k $\Omega$	
DELAY2-1, -2 * <sup>1</sup> * <sup>3</sup>	T <sub>D2_1, _2</sub>	140	220	300	ns	Delay set R = 180 kΩ	
DELAY2-3 * <sup>1</sup> * <sup>3</sup>	T <sub>D2_3</sub>	110	170	230	ns	Delay set R = 180 kΩ	
Terminal voltage	V <sub>D1, 2, 3</sub>	1.9	2.0	2.1	V	Delay set R = 51 kΩ	
SOFT START: R2A20124AFP/ASP							
Source current	I <sub>SS</sub>	-14	-10	-6	μΑ	SS = 1 V	
SS high voltage	V <sub>OH-SS</sub>	3.9	4.0	4.1	V		

Notes: 1. Design specification (reference data)

2. Tpd is defined as;



3.  $T_{D1}$ ,  $T_{D2}$ , and  $T_{D3}$  are defined as;



4. Maximum/Minimum phase shift is defined as;

$$D = \frac{T2}{T1} \times 2 \times 100 \text{ (\%)}$$

$$OUT-A$$

$$OUT-D$$

$$T1$$

$$OUT-C$$

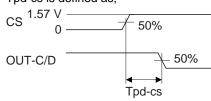
$$T1$$

## **Electrical Characteristics** (cont.)

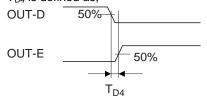
 $(Ta = 25^{\circ}C, Vcc = 12 \text{ V}, RT = 180 \text{ k}\Omega, Rdelay = 51 \text{ k}\Omega, Rramp-slp = 27 \text{ k}\Omega, unless otherwise specified.})$ 

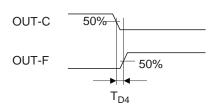
Item	Symbol	Min	Тур	Max	Unit	Test Conditions	
OVER CURRENT PROTECTION: R2A20124AFP/ASP							
Pulse-by-pulse current limit threshold	V <sub>CS-PP</sub>	1.26	1.4	1.54	V	SEC-CONT = 0.3 V (AFP)	
Delay to OUT pins *1	Tpd-cs	_	100	200	ns	CS = 0 V to 1.57 V, SEC-CONT = 0.3 V (AFP)	
CS sink current	I <sub>SINK-CS</sub>	2	5	_	mA	CS = 0.15 V, COMP = 0 V	
OUTPUT: R2A20124AFP/ASP							
High voltage	V <sub>OH-OUT</sub>	11.5	11.9	_	V	IOUT = -2 mA	
Low voltage	V <sub>OL-OUT</sub>	_	0.05	0.2	V	IOUT = 2 mA	
Rise time	tr	_	30	100	ns	COUT = 100 pF	
Fall time	tf	_	30	100	ns	COUT = 100 pF	
Timing offset *2	T <sub>D4</sub>	_	20	140	ns		
POWER INFORMATION AMPLIFIER	R: R2A20124AFP						
Tranceconductance	gm	15	20	25	μS	CS = 0.4 V	
SECONDARY CONTROL: R2A2012	4AFP						
Forced synchronous rectification on voltage	Von-sec-cont	4.6	1	_	>	CS = 1 V	
Forced synchronous rectification off voltage	Voff-sec-cont	_	_	0.4	>	CS = 0 V	
Input bias current-1	I <sub>SEC-CONT1</sub>	5	10	20	μΑ	CS = 0 V, SEC-CONT = 2.1 V	
Input bias current-2	I <sub>SEC-CONT2</sub>	10	20	40	μΑ	CS = 1 V, SEC-CONT = 2.1 V	
Current hysteresis	dl <sub>SEC-CONT</sub>	5	10	20	μΑ		

## Notes: 1. Tpd-cs is defined as;



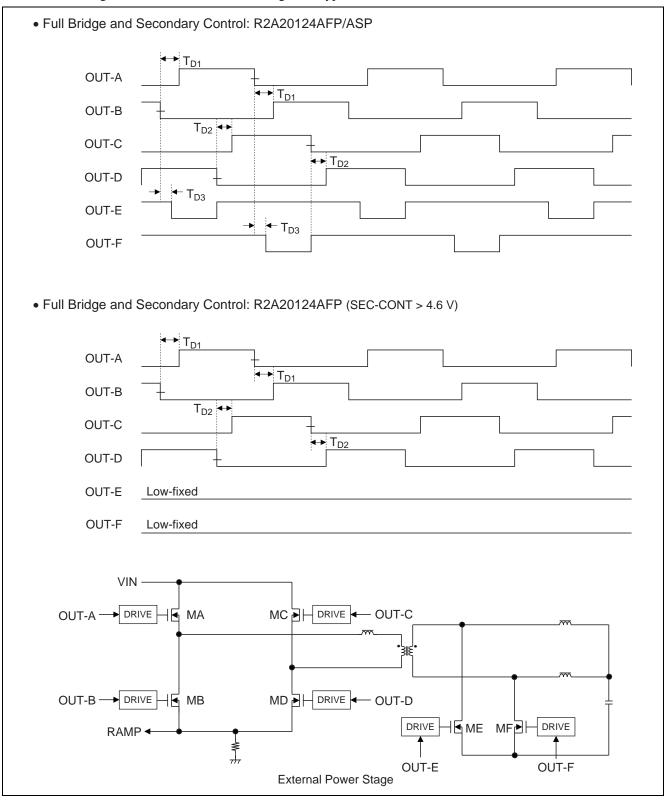
## 2. $T_{D4}$ is defined as;



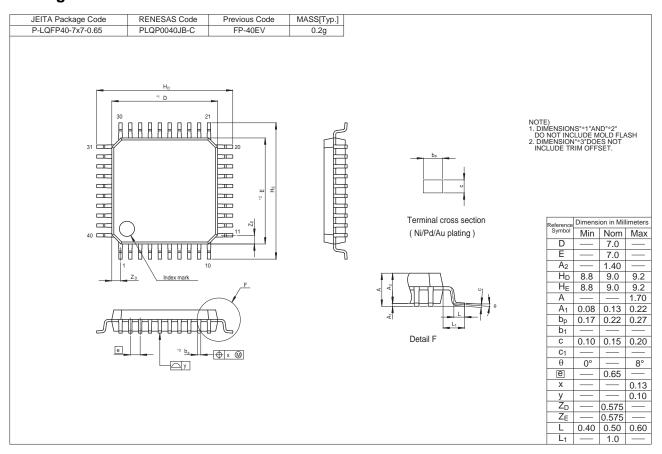


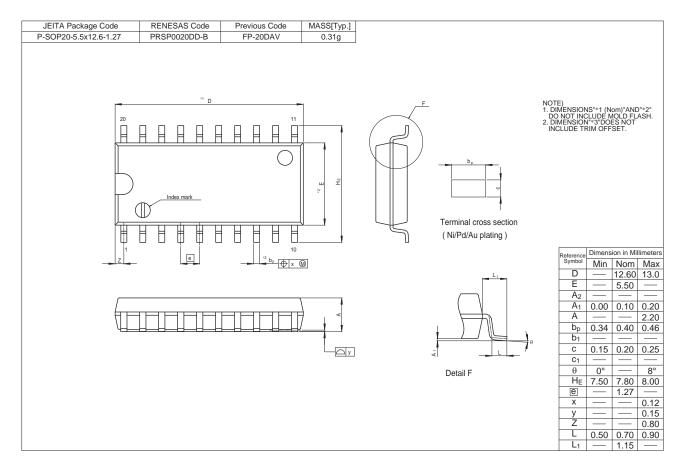
## **Timing Diagram**

Note: All voltage, current, time shown in the diagram is typical value.



## **Package Dimensions**





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