

H5N2501LD, H5N2501LS, H5N2501LM

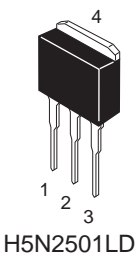
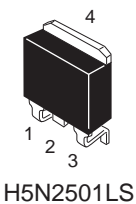
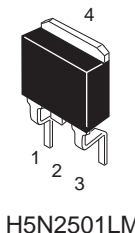
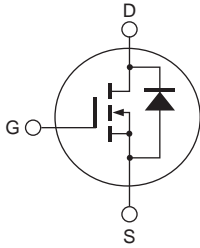
Silicon N Channel MOS FET
High Speed Power Switching

R07DS0056EJ0300
(Previous: REJ03G1250-0200)
Rev.3.00
Jul 23, 2010

Features

- Low on-resistance
 $R_{DS(on)} = 0.14 \Omega$ typ. (at $I_D = 9 \text{ A}$, $V_{GS} = 10 \text{ V}$, $T_a = 25^\circ\text{C}$)
- Low leakage current
- High speed switching

Outline

<p>RENESAS Package code: PRSS0004AE-A (Package name LDKPAK(L))</p>  <p>H5N2501LD</p>	<p>RENESAS Package code: PRSS0004AE-B (Package name LDKPAK(S)-(1))</p>  <p>H5N2501LS</p>	<p>RENESAS Package code: PRSS0004AE-C (Package name LDKPAK(S)-(2))</p>  <p>H5N2501LM</p>
		
<p>1. Gate 2. Drain 3. Source 4. Drain</p>		

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source voltage	V_{DSS}	250	V
Gate to Source voltage	V_{GSS}	± 30	V
Drain current	I_D	18	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	72	A
Body-Drain diode reverse Drain current	I_{DR}	18	A
Avalanche current	I_{AP} ^{Note3}	18	A
Avalanche energy	E_{AR} ^{Note3}	20.25	mJ
Channel dissipation	P_{ch} ^{Note2}	75	W
Channel to case thermal impedance	θ_{ch-c}	1.67	$^\circ\text{C/W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
 2. Value at $T_c = 25^\circ\text{C}$
 3. $STch = 25^\circ\text{C}$, $T_{ch} \leq 150^\circ\text{C}$

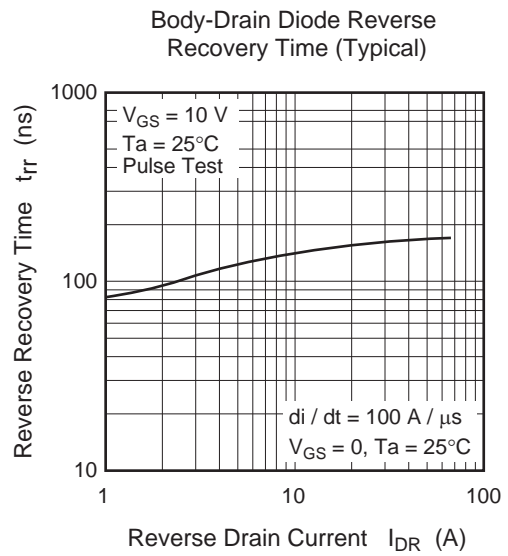
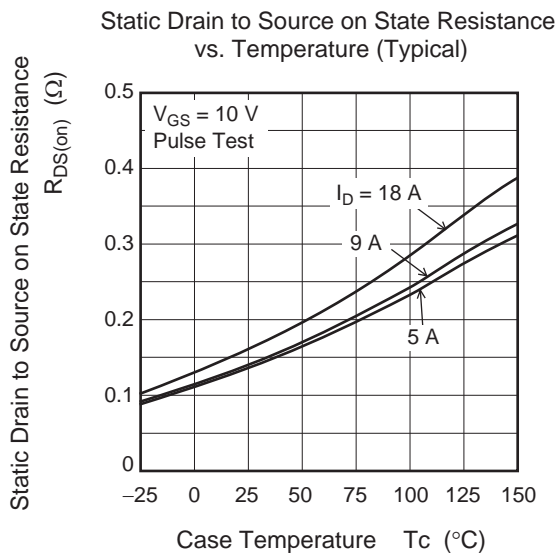
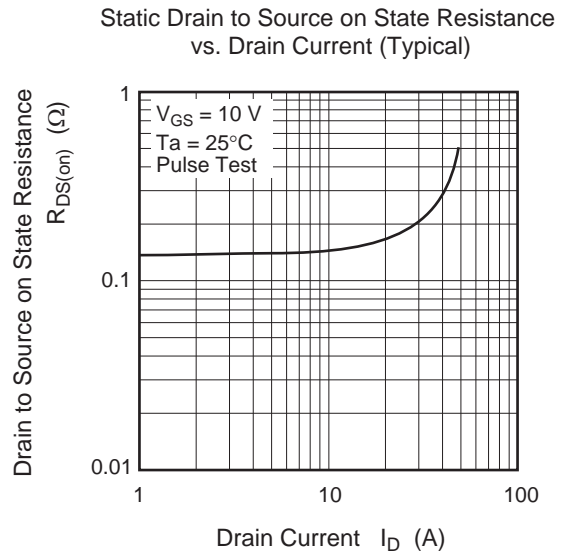
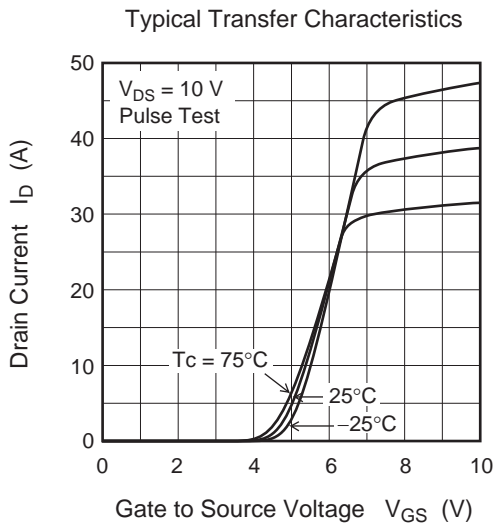
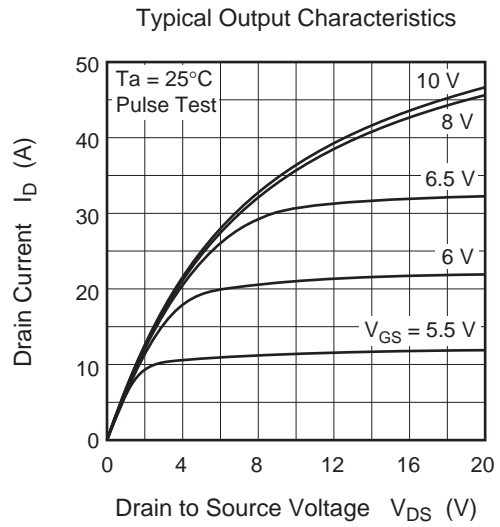
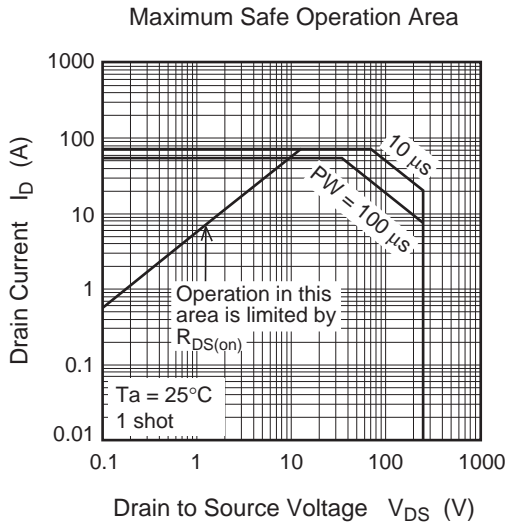
Electrical Characteristics

(Ta = 25°C)

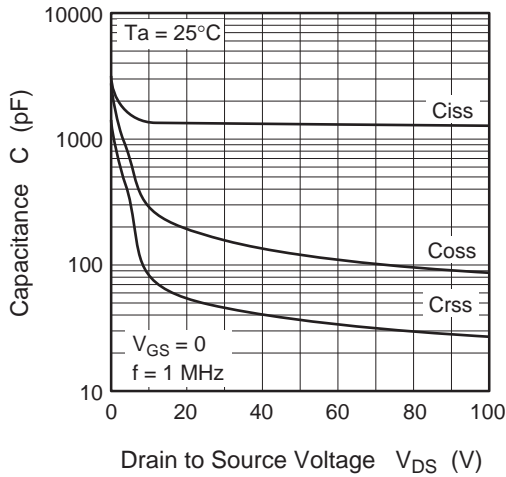
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to Source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Zero Gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 250 \text{ V}$, $V_{GS} = 0$
Gate to Source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Gate to Source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Forward transfer admittance	$ y_{fs} $	8	14	—	S	$I_D = 9 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Static Drain to Source on state resistance	$R_{DS(on)}$	—	0.14	0.18	Ω	$I_D = 9 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	1350	—	pF	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	170	—	pF	
Reverse transfer capacitance	C_{rss}	—	50	—	pF	
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	$I_D = 9 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_L = 13.9 \Omega$ $R_g = 10 \Omega$
Rise time	t_r	—	65	—	ns	
Turn-off delay time	$t_{d(off)}$	—	95	—	ns	
Fall time	t_f	—	18	—	ns	
Total Gate charge	Q_g	—	45	—	nC	$V_{DD} = 200 \text{ V}$ $V_{GS} = 10 \text{ V}$ $I_D = 18 \text{ A}$
Gate to Source charge	Q_{gs}	—	8	—	nC	
Gate to Drain charge	Q_{gd}	—	22	—	nC	
Body-Drain diode forward voltage	V_{DF}	—	0.9	1.4	V	$I_F = 18 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-Drain diode reverse recovery time	t_{rr}	—	160	—	ns	$I_F = 18 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$
Body-Drain diode reverse recovery charge	Q_{rr}	—	1.0	—	μC	

Notes: 4. Pulse test

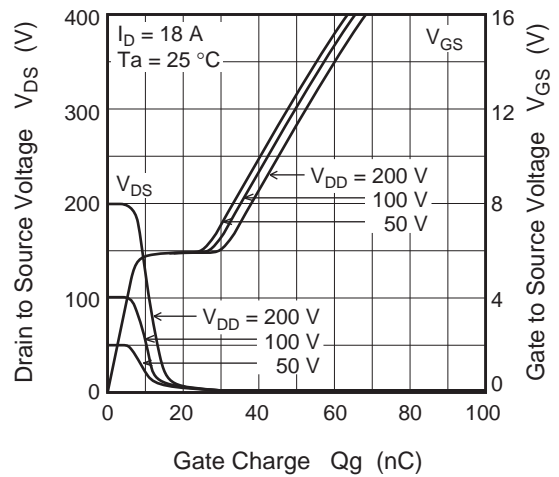
Main Characteristics



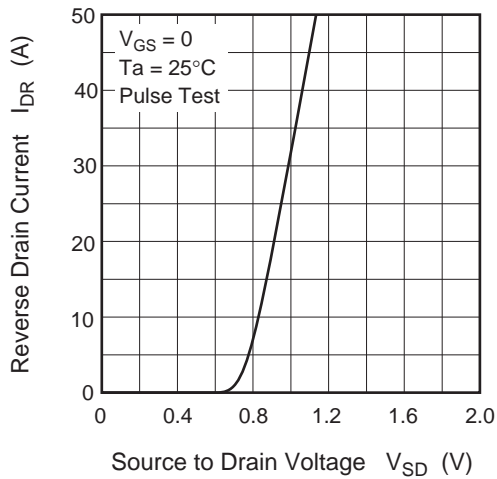
Typical Capacitance vs. Drain to Source Voltage



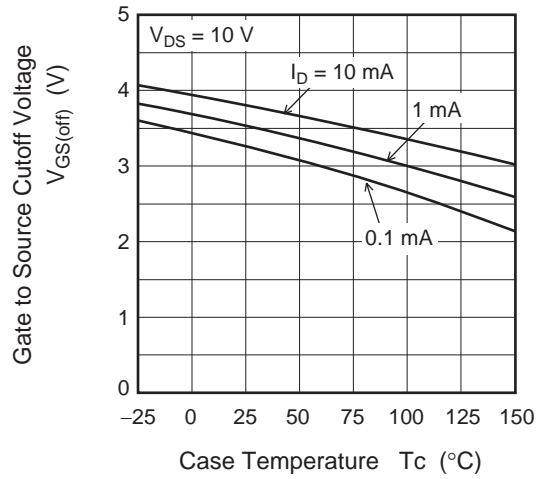
Dynamic Input Characteristics (Typical)



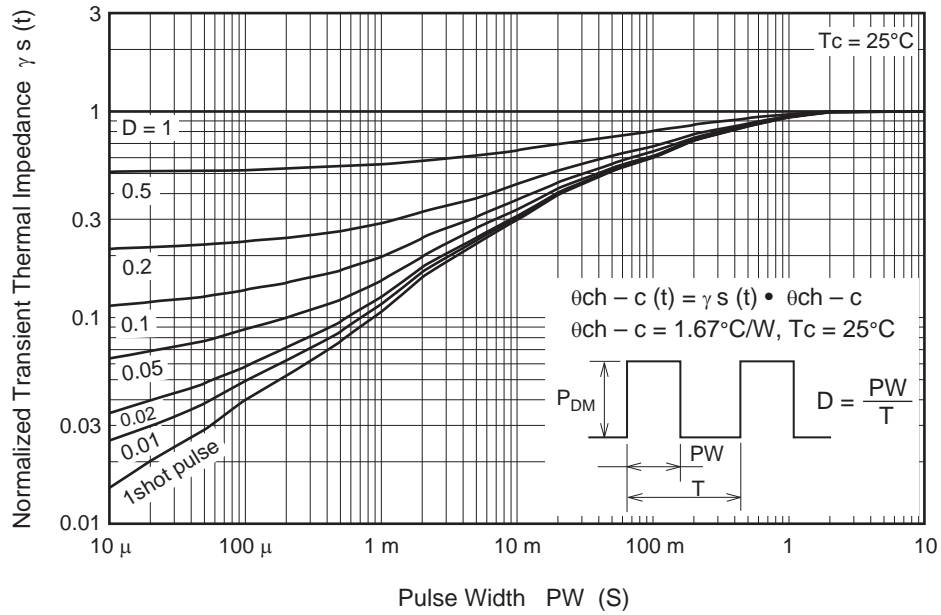
Reverse Drain Current vs. Source to Drain Voltage (Typical)



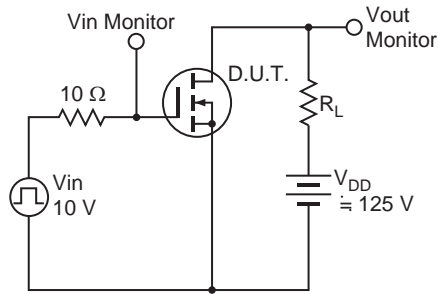
Gate to Source Cutoff Voltage vs. Case Temperature (Typical)



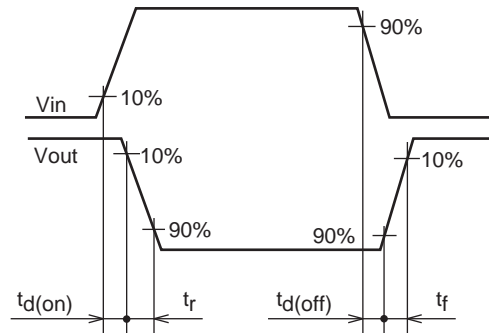
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

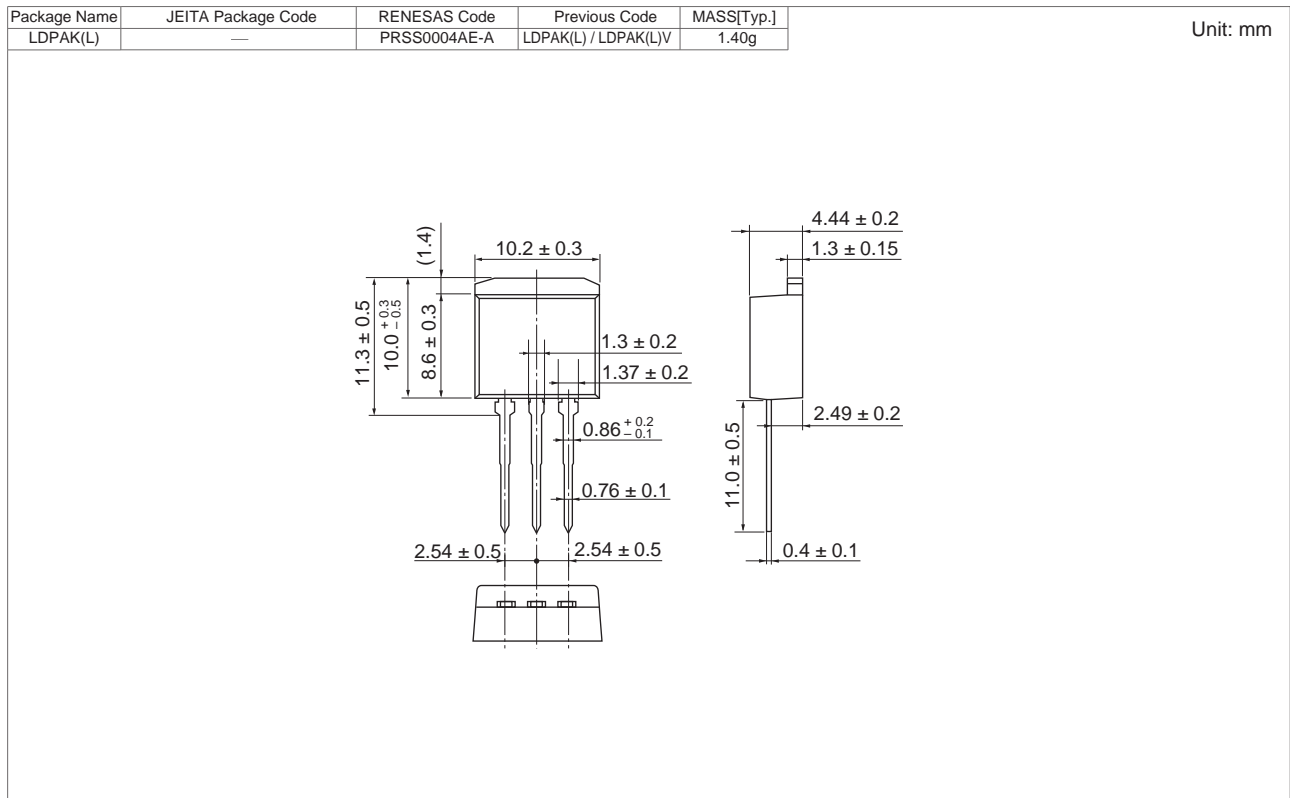


Switching Time Waveform

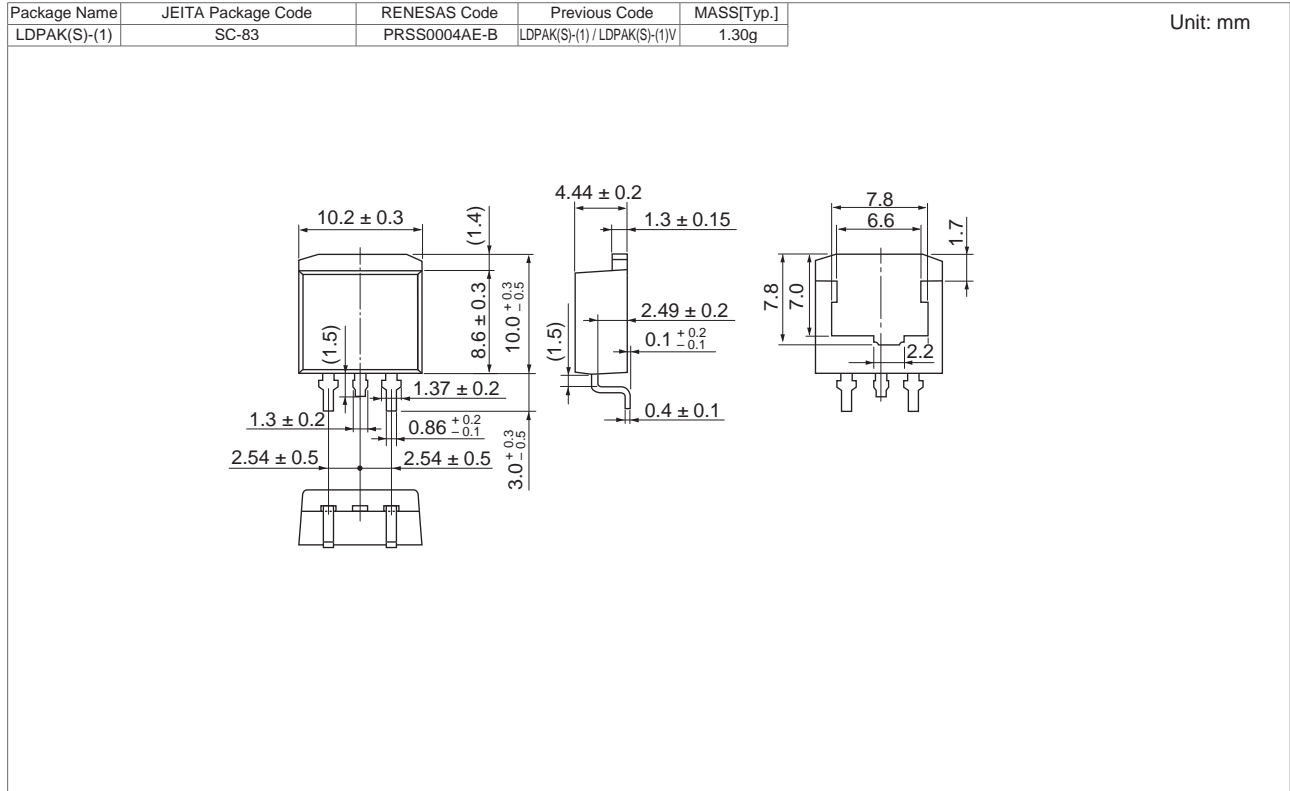


Package Dimensions

• H5N2501LD

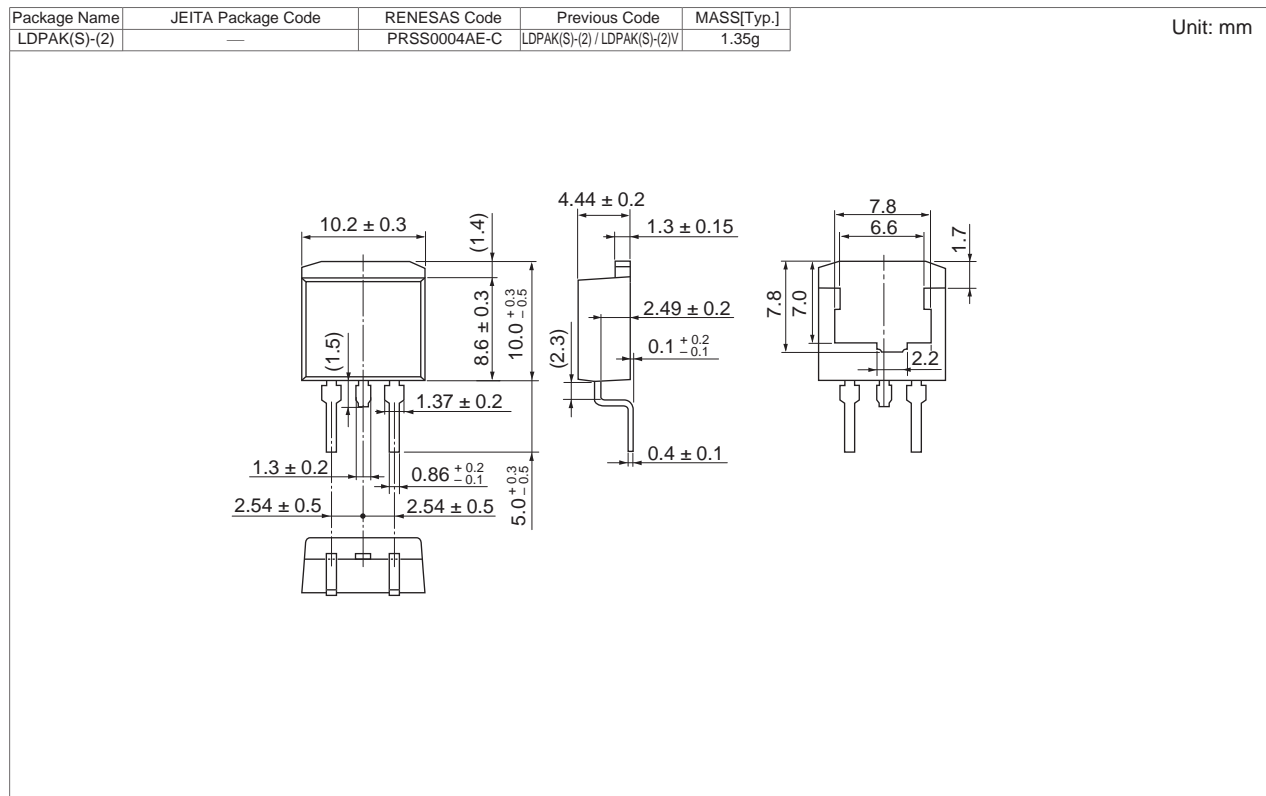


• H5N2501LS



H5N2501LD, H5N2501LS, H5N2501LM

• H5N2501LM



Ordering Information

Part No.	Quantity	Shipping Container
H5N2501LD-E	300 pcs	Box (Tube)
H5N2501LSTL-E	1000 pcs	Taping
H5N2501LMTL-E	1000 pcs	Taping

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