



LOW SKEW, 1-TO-5, DIFFERENTIAL-TO-2.5V, 3.3V LVPECL/ECL FANOUT BUFFER

ICS853014

General Description



The ICS853014 is a low skew, high performance 1-to-5, 2.5V/3.3V Differential-to-LVPECL/ECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS853014 has two selectable clock

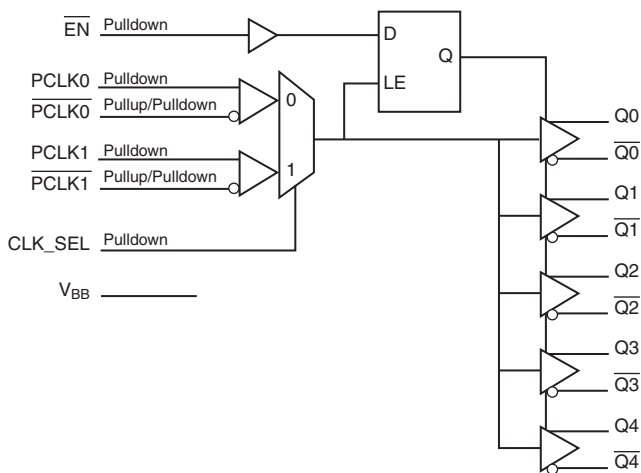
inputs.

Guaranteed output and part-to-part skew characteristics make the ICS853014 ideal for those applications demanding well defined performance and repeatability.

Features

- Five differential LVPECL/ECL outputs
- Two selectable differential LVPECL clock inputs
- PCLKx, $\overline{\text{PCLKx}}$ pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: > 2GHz
- Output skew: 13ps (typical)
- Part-to-part skew: 60ps (typical)
- Propagation delay: 460ps (typical)
- LVPECL mode operating voltage supply range: $V_{CC} = 2.375V$ to $3.8V$, $V_{EE} = 0V$
- ECL mode operating voltage supply range: $V_{CC} = 0V$, $V_{EE} = -3.8V$ to $-2.375V$
- $-40^{\circ}C$ to $85^{\circ}C$ ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment

Q0	1	20	V _{CC}
$\overline{\text{Q0}}$	2	19	$\overline{\text{EN}}$
Q1	3	18	V _{CC}
$\overline{\text{Q1}}$	4	17	$\overline{\text{PCLK1}}$
Q2	5	16	PCLK1
$\overline{\text{Q2}}$	6	15	V _{BB}
Q3	7	14	$\overline{\text{PCLK0}}$
$\overline{\text{Q3}}$	8	13	PCLK0
Q4	9	12	CLK_SEL
$\overline{\text{Q4}}$	10	11	V _{EE}

ICS853014

20-Lead TSSOP

6.5mm x 4.4mm x 0.925mm

package body

G Package

Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, $\overline{Q0}$	Output		Differential output pair. LVPECL/ECL interface levels.
3, 4	Q1, $\overline{Q1}$	Output		Differential output pair. LVPECL/ECL interface levels.
5, 6	Q2, $\overline{Q2}$	Output		Differential output pair. LVPECL/ECL interface levels.
7, 8	Q3, $\overline{Q3}$	Output		Differential output pair. LVPECL/ECL interface levels.
9, 10	Q4, $\overline{Q4}$	Output		Differential output pair. LVPECL/ECL interface levels.
11	V _{EE}	Power		Negative supply pin.
12	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects PCLK1/ $\overline{PCLK1}$ inputs. When LOW, selects PCLK0/ $\overline{PCLK0}$ inputs. LVTTTL / LVCMOS interface levels.
13	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.
14	$\overline{PCLK0}$	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V _{CC} /2 default when left floating.
15	V _{BB}	Output		Bias voltage.
16	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock input.
17	$\overline{PCLK1}$	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V _{CC} /2 default when left floating.
18, 20	V _{CC}	Power		Positive supply pins.
19	\overline{EN}	Input	Pulldown	Synchronizing clock enable. When LOW, clock outputs follow clock input. When HIGH, Qx outputs are forced low, \overline{Qx} outputs are forced high. LVTTTL/LVCMOS interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R _{PULLDOWN}	Input Pulldown Resistor			75		k Ω
R _{VCC/2}	Pullup/Pulldown Resistors			50		k Ω

Function Tables

Table 3A. Control Input Function Table

Inputs			Outputs	
\overline{EN}	CLK_SEL	Selected Source	Q0:Q4	$\overline{Q0:Q4}$
1	0	PCLK0, $\overline{PCLK0}$	Disabled; Low	Disabled; High
1	1	PCLK1, $\overline{PCLK1}$	Disabled; Low	Disabled; High
0	0	PCLK2, $\overline{PCLK2}$	Enabled	Enabled
0	1	PCLK3, $\overline{PCLK3}$	Enabled	Enabled

After \overline{EN} switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in Figure 1.

In the active mode, the state of the outputs are a function of the PCLK0/ $\overline{PCLK0}$ and PCLK1/ $\overline{PCLK1}$ inputs as described in Table 3B.

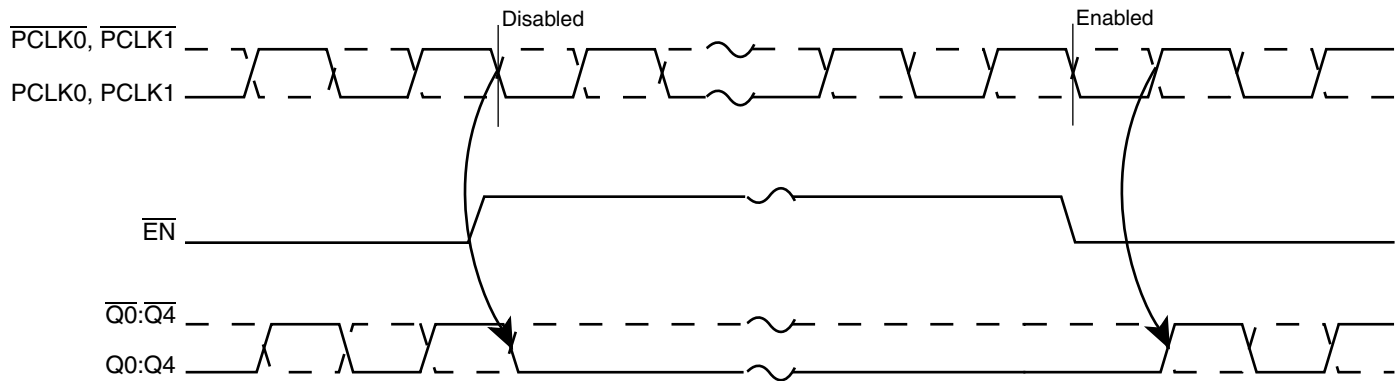


Figure 1. \overline{EN} Timing Diagram

Table 3B. Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
PCLK0 or PCLK1	$\overline{PCLK0}$ or $\overline{PCLK1}$	Q0:Q4	$\overline{Q0:Q4}$		
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-Ended to Differential	Inverting

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V (LVPECL mode, $V_{EE} = 0V$)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, $V_{CC} = 0V$)
Inputs, V_I (LVPECL mode)	-0.5V to $V_{CC} + 0.5V$
Inputs, V_I (ECL mode)	0.5V to $V_{EE} - 0.5V$
Outputs, I_O Continuous Current Surge Current	50mA 100mA
V_{BB} Sink/Source, I_{BB}	$\pm 0.5mA$
Operating Temperature Range, T_A	-40°C to +85°C
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = 2.375V$ to $3.8V$; $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.8	V
I_{EE}	Power Supply Current				85	mA

Table 4B. DC Characteristics, $V_{CC} = 3.3V$; $V_{EE} = 0V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	$-40^{\circ}C$			$25^{\circ}C$			$80^{\circ}C$			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1	2.175	2.275	2.38	2.225	2.295	2.375	2.22	2.295	2.365	V
V_{OL}	Output Low Voltage; NOTE 1	1.405	1.545	1.68	1.425	1.52	1.615	1.44	1.535	1.63	V
V_{IH}	Input High Voltage (Single-ended)	2.075		2.36	2.075		2.36	2.075		2.36	V
V_{IL}	Input Low Voltage (Single-ended)	1.43		1.765	1.43		1.765	1.43		1.765	V
V_{BB}	Output Voltage Reference; NOTE 2	1.86		1.98	1.86		1.98	1.86		1.98	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input High Current	PCLK0, PCLK1 PCLK0, PCLK1		150		150				150	μA
I_{IL}	Input Low Current	PCLK0, PCLK1		-10		-10		-10			μA
		PCLK0, PCLK1		-150		-150		-150			μA

Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$.

NOTE 2: Single-ended input operation is limited. $V_{CC} \geq 3V$ in LVPECL mode.

NOTE 3: Common mode voltage is defined as V_{IH} .

NOTE 4: For single-ended applications, the maximum input voltage for PCLKx, \overline{PCLKx} is $V_{CC} + 0.3V$

Table 4C. LVPECL DC Characteristics, $V_{CC} = 2.5V$; $V_{EE} = 0V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	$-40^{\circ}C$			$25^{\circ}C$			$80^{\circ}C$			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1	1.375	1.475	1.58	1.425	1.495	1.57	1.42	1.495	1.565	V
V_{OL}	Output Low Voltage; NOTE 1	0.605	0.745	0.88	0.625	0.72	0.815	0.64	0.735	0.83	V
V_{IH}	Input High Voltage (Single-ended)	1.275		1.56	1.275		1.56	1.275		1.56	V
V_{IL}	Input Low Voltage (Single-ended)	0.63		0.965	0.63		0.965	0.63		0.965	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input High Current	PCLK0, PCLK1 PCLK0, PCLK1		150		150				150	μA
I_{IL}	Input Low Current	PCLK0, PCLK1		-10		-10		-10			μA
		PCLK0, PCLK1		-150		-150		-150			μA

Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$.

NOTE 2: Common mode voltage is defined as V_{IH} .

NOTE 3: For single-ended applications, the maximum input voltage for PCLKx, \overline{PCLKx} is $V_{CC} + 0.3V$.

Table 4D. ECL DC Characteristics, $V_{CC} = 0V$; $V_{EE} = -3.8V$ to $-2.375V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	$-40^{\circ}C$			$25^{\circ}C$			$80^{\circ}C$			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1	-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.08	-1.005	-0.935	V
V_{OL}	Output Low Voltage; NOTE 1	-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
V_{IH}	Input High Voltage (Single-ended)	-1.225		-0.94	-1.225		-0.94	-1.225		-0.94	V
V_{IL}	Input Low Voltage (Single-ended)	-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
V_{BB}	Output Voltage Reference; NOTE 2	-1.44		-1.32	-1.44		-1.32	-1.44		-1.32	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4	$V_{EE}+1.2$		0	$V_{EE}+1.2$		0	$V_{EE}+1.2$		0	V
I_{IH}	Input High Current	$\overline{PCLK0}, \overline{PCLK1}$		150		150				150	μA
I_{IL}	Input Low Current	$\overline{PCLK0}, \overline{PCLK1}$		-10		-10		-10			μA
		$\overline{PCLK0}, \overline{PCLK1}$		-150		-150		-150			μA

Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$.

NOTE 2: Single-ended input operation is limited. $V_{CC} \geq 3V$ in LVPECL mode.

NOTE 3: Common mode voltage is defined as V_{IH} .

NOTE 4: For single-ended applications, the maximum input voltage for \overline{PCLKx} , \overline{PCLKx} is $V_{CC} + 0.3V$

AC Electrical Characteristics

Table 5. AC Characteristics, $V_{CC} = -3.8V$ to $-2.375V$ or , $V_{CC} = 2.375V$ to $3.8V$; $V_{EE} = 0V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	-40°C			25°C			80°C			Units	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Output Frequency		>2			>2			>2		GHz	
t_{PD}	Propagation Delay; NOTE 1	355	440	525	376	460	550	400	500	595	ps	
$t_{sk(o)}$	Output Skew; NOTE 2, 5		13	25		13	25		13	25	ps	
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 5			105			105			130	ps	
V_{PP}	Peak-to-Peak Input Voltage; NOTE 4	150	800	1800	150	800	1800	150	800	1800	mV	
t_R / t_F	Output Rise/Fall Time	20% to 80%	90	150	210	90	150	210	90	150	210	ps
t_S	Clock Enable Setup Time	100	50		100	50		100	50		ps	
t_H	Clock Enable Hold Time	200	140		200	140		200	140		ps	

All parameters are measured at $f \leq 1GHz$, unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

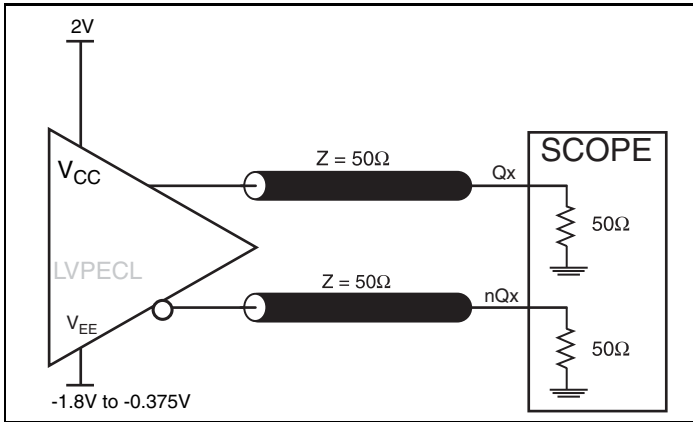
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions.
Using the same type of inputs on each device, the outputs are measured at the differential cross points.

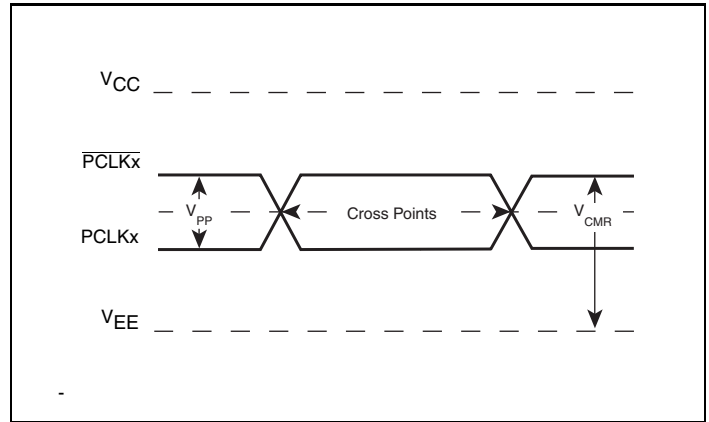
NOTE 4: The VCMR and VPP levels should be such that input low voltage never goes below VEE.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

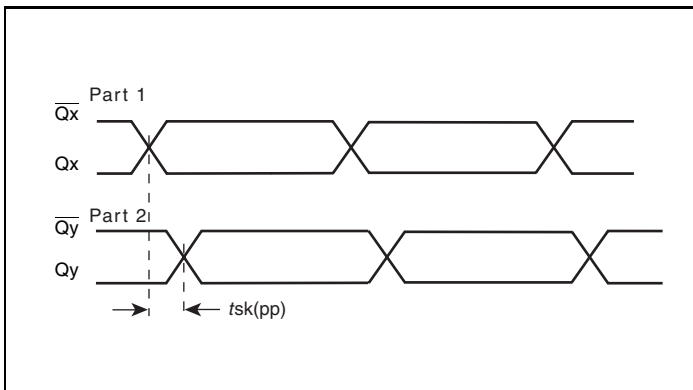
Parameter Measurement Information



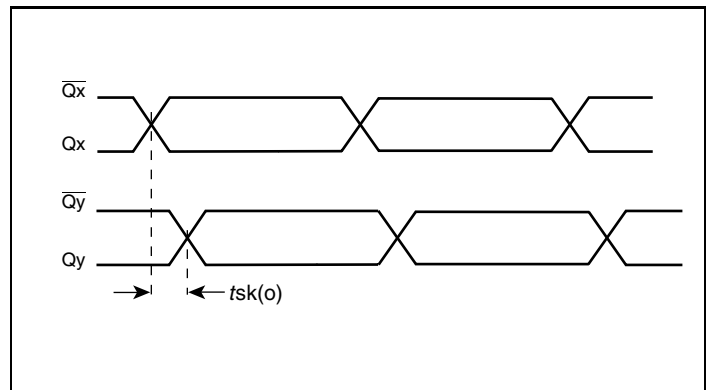
LVPECL Output Load AC Test Circuit



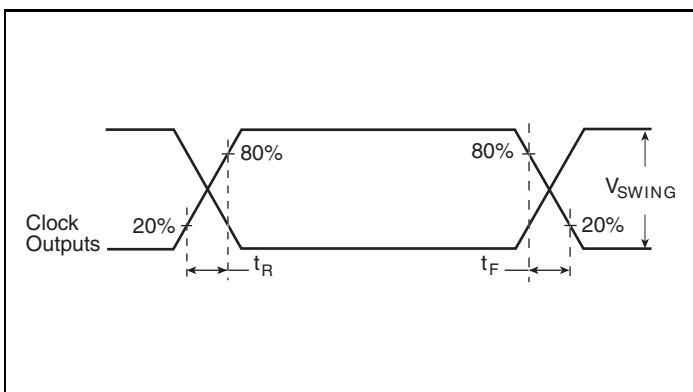
Differential Input Level



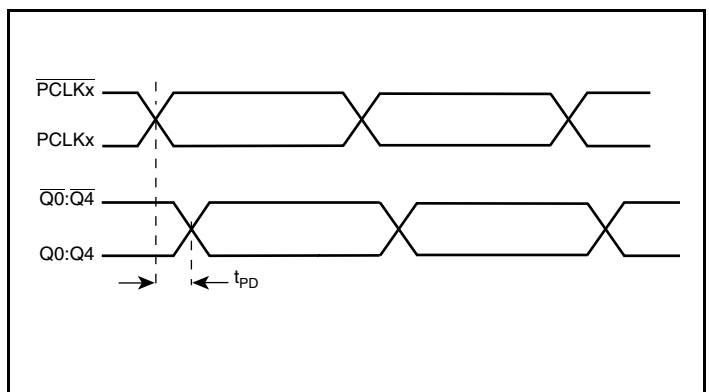
Part-to-Part Skew



Output Skew

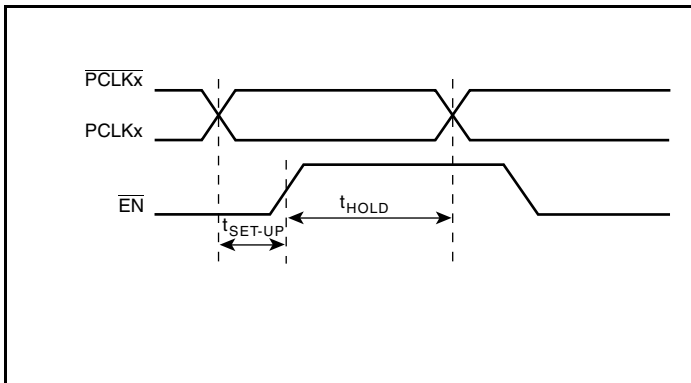


Output Rise/Fall Time



Propagation Delay

Parameter Measurement Information, continued



Setup and Hold Time

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

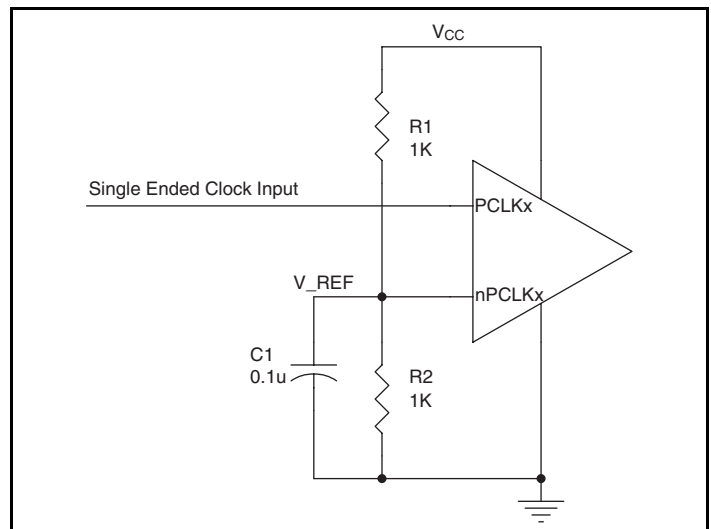


Figure 2. Single-Ended Signal Driving Differential Input

LVPECL Clock Input Interface

The PCLK/PCLK accepts LVPECL, LVDS, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3E show interface examples for the HiPerClockS PCLK/PCLK input driven by the

most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

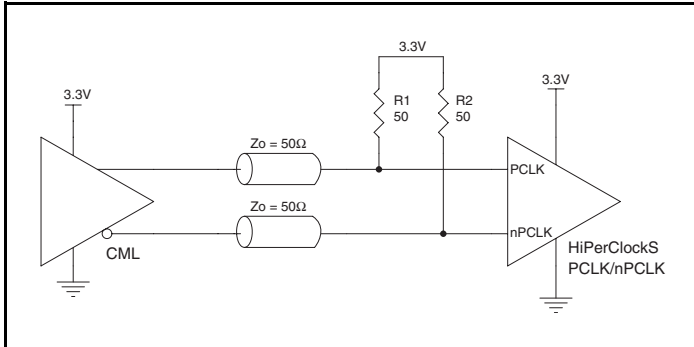


Figure 3A. HiPerClockS PCLK/PCLK Input Driven by an Open Collector CML Driver

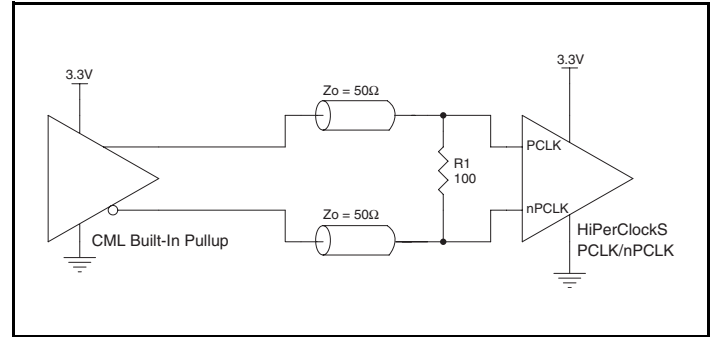


Figure 3B. HiPerClockS PCLK/PCLK Input Driven by a Built-In Pullup CML Driver

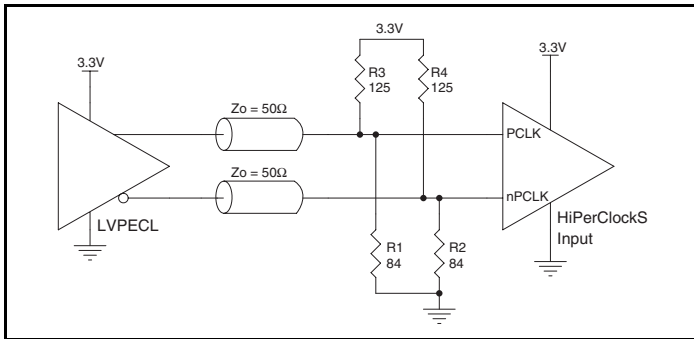


Figure 3C. HiPerClockS PCLK/PCLK Input Driven by a 3.3V LVPECL Driver

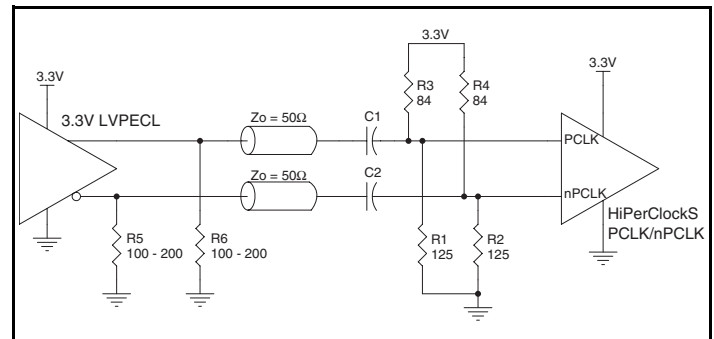


Figure 3D. HiPerClockS PCLK/PCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

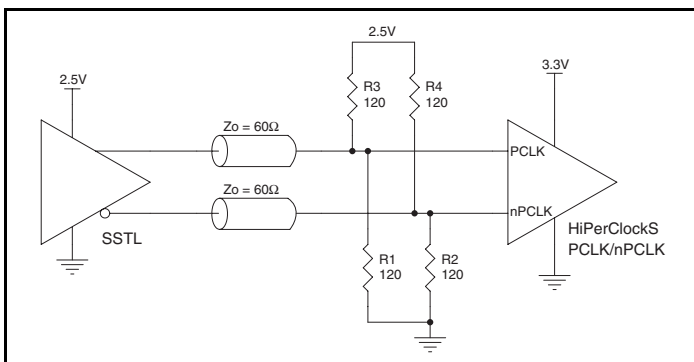


Figure 3E. HiPerClockS PCLK/PCLK Input Driven by an SSTL Driver

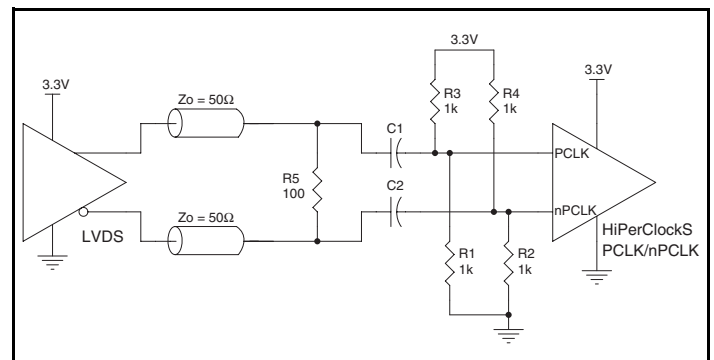


Figure 3F. HiPerClockS PCLK/PCLK Input Driven by a 3.3V LVDS Driver

Recommendations for Unused Output Pins

Inputs:

PCLK/ $\overline{\text{PCLK}}$ INPUTS

For applications not requiring the use of a differential input, both the PCLK and $\overline{\text{PCLK}}$ pins can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from PCLK to ground. For applications

LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and $\overline{\text{FOUT}}$ are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50 Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

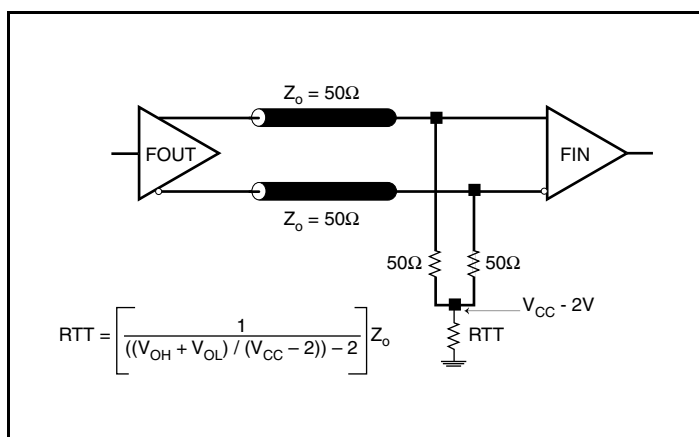


Figure 4A. 3.3V LVPECL Output Termination

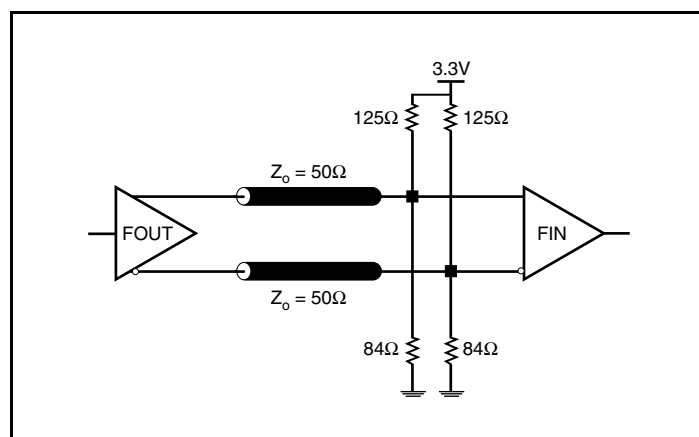


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2V$. For $V_{CC} = 2.5V$, the $V_{CC} - 2V$ is very close to

ground level. The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.

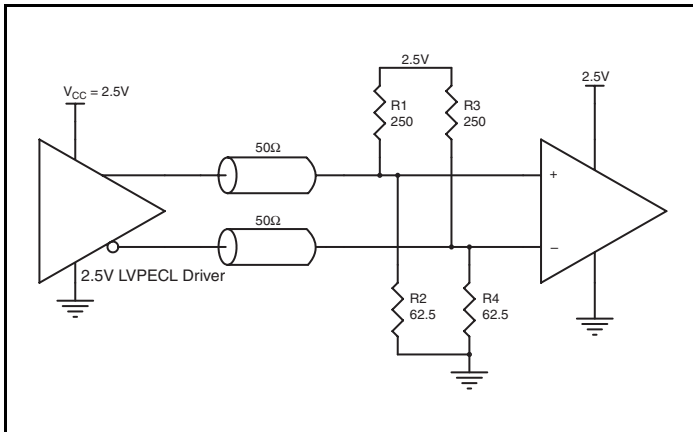


Figure 5A. 2.5V LVPECL Driver Termination Example

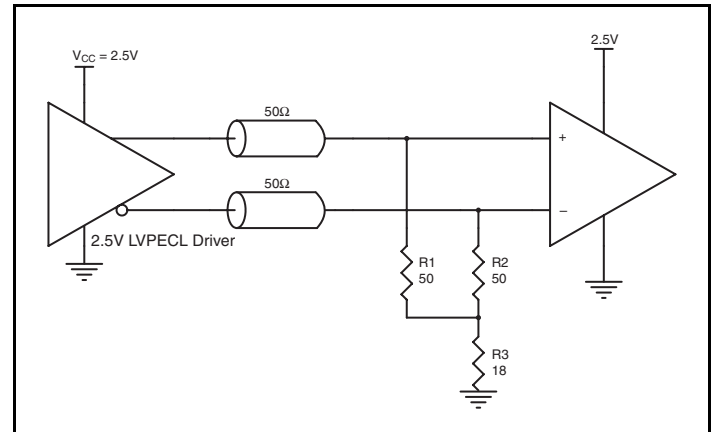


Figure 5B. 2.5V LVPECL Driver Termination Example

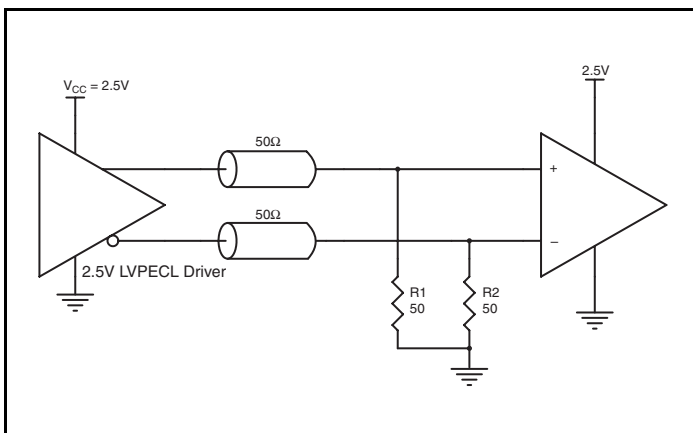


Figure 5C. 2.5V LVPECL Driver Termination Example

Schematic Example

This application note provides general design guide using ICS853014 LVPECL buffer. Figure 6 shows a schematic example of the ICS853014 LVPECL clock buffer. In this example, the input

is driven by an LVPECL driver. CLK_SEL is set at logic high to select PCLK1/PCLK1̄ input.

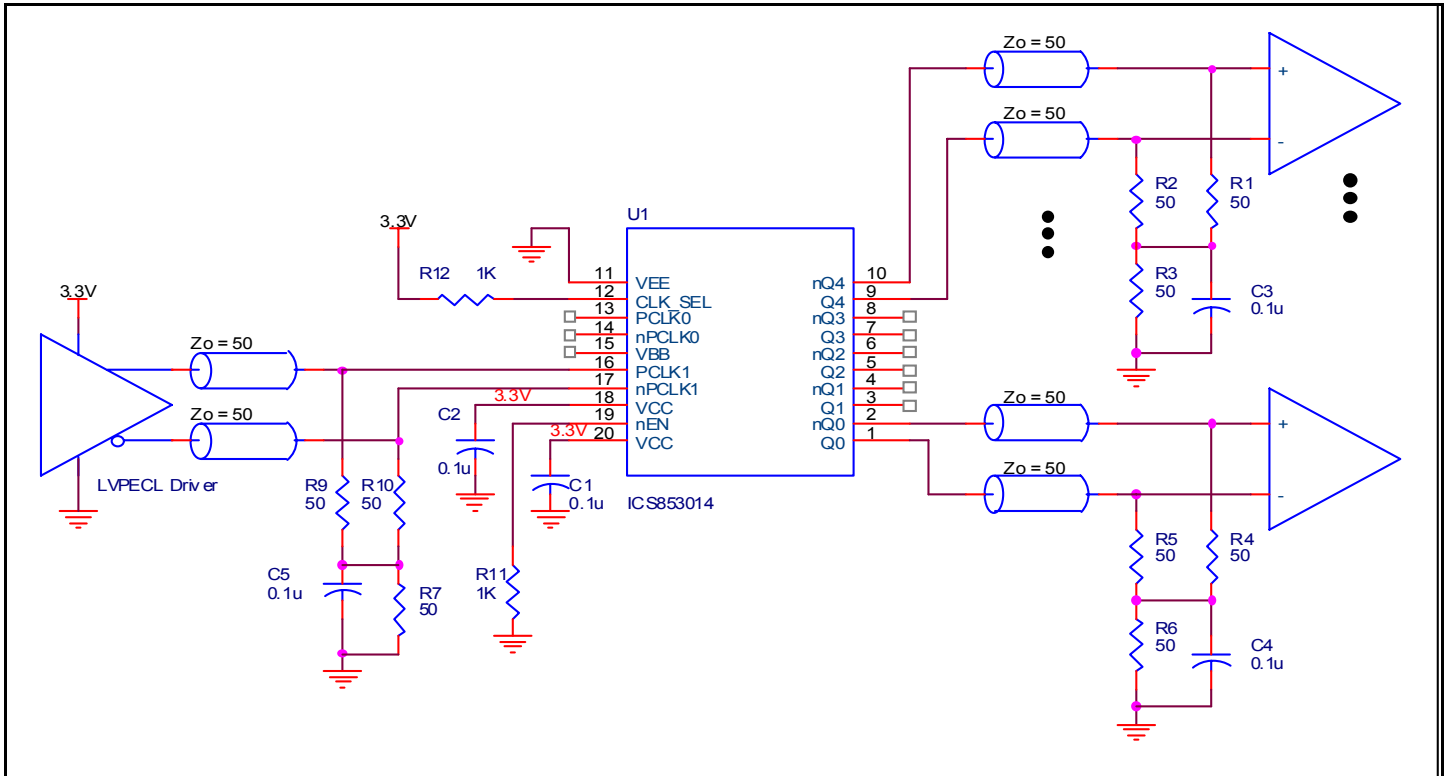


Figure 6. ICS853014 Example LVPECL Clock Output Buffer Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS853014. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS853014 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.8V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.8V * 85mA = 323mW$
- Power (outputs)_{MAX} = **30.94mW/Loaded Output pair**
If all outputs are loaded, the total power is $5 * 30.94mW = 154.7mW$

Total Power_{MAX} (3.8V, with all outputs switching) = $323mW + 154.7mW = 477.7mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming 0 air flow and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.478W * 66.6^\circ C/W = 116.8^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

Linear Feet per Minute	θ_{JA} by Velocity		
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7*.

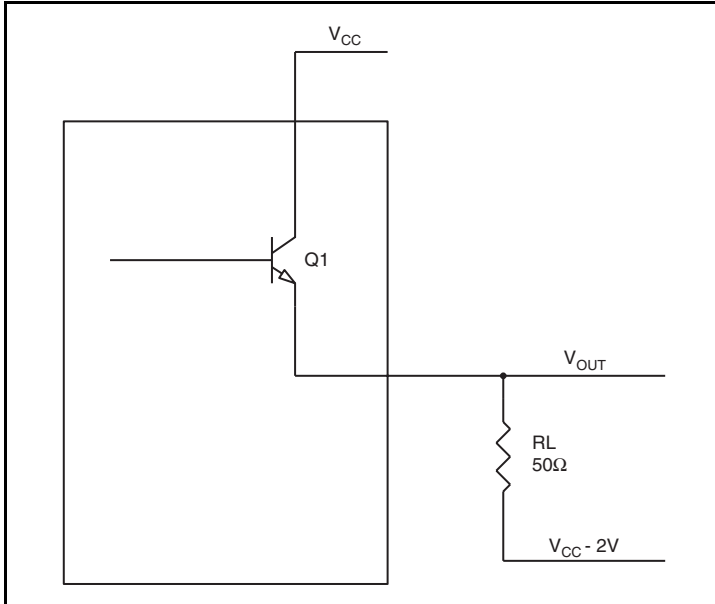


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.935V$
 $(V_{CC_MAX} - V_{OH_MAX}) = 0.935V$
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.67V$
 $(V_{CC_MAX} - V_{OL_MAX}) = 1.67V$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.935V)/50\Omega] * 0.935V = \mathbf{19.92mW}$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.67V)/50\Omega] * 1.67V = \mathbf{11.02mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{30.94mW}$$

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} vs. Air Flow			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

Transistor Count

The transistor count for ICS853014 is: 373

Pin compatible with MC100LVEP14 and SY100EP14U

Package Outline and Package Dimension

Package Outline - G Suffix for 20 Lead TSSOP

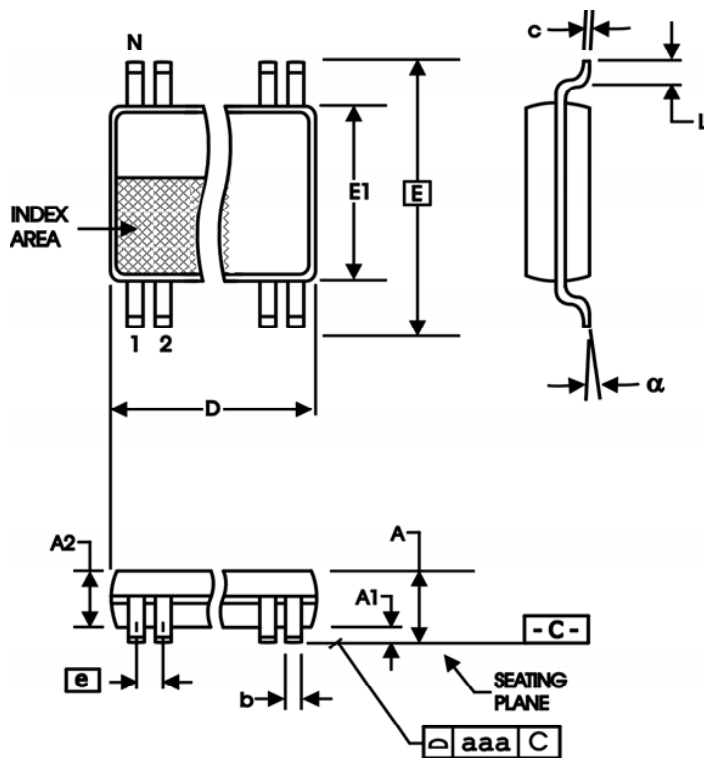


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.90 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS853014BG	ICS853014BG	20 Lead TSSOP	Tube	-40°C to 85°C
ICS853014BGT	ICS853014BG	20 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C
ICS853014BGLF	ICS853014BGL	"Lead-Free" 20 Lead TSSOP	Tube	-40°C to 85°C
CS853014BGLFT	ICS853014BGL	"Lead-Free" 20 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T4B	4	3.3V LVPECL table - V_{OH} values changed @ 85° to 2.22V min. and 2.295V typical from 2.295V min. and 2.33V typical.	9/10/03
	T4C	5	3.3V LVPECL table - V_{OH} values changed @ 85° to 2.22V min. and 2.295V typical from 2.295V min. and 2.33V typical.	
	T4D	5	3.3V LVPECL table - V_{OH} values changed @ 85° to 2.22V min. and 2.295V typical from 2.295V min. and 2.33V typical.	
		8 10	Revised LVPECL Output Termination drawings. Revised Figure 5D.	
C	T4B - T4D	4-5	LVPECL & ECL tables - deleted V_{PP} row.	3/18/04
		6	AC Table - added V_{PP} row and changed max. value from 1200mV to 1800mV.	
C	T9	1	Features Section - added Lead-Free bullet.	5/13/05
		16	Ordering Information Table - added Lead-Free part number.	
D	4A	4	Power Supply DC Characteristics Table - changed I_{EE} from 75mA max. to 85mA max. Updated format throughout the datasheet.	7/6/07
d		1	Corrected block diagram.	11/12/07

ICS853014

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