



## WS74HC164

## 8-Bit Serial-in/Parallel-out Shift Register

### GENERAL DESCRIPTION

74HC164 is fabricated in the high-speed silicon gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices (LS-TTL).

This 8-bit Shift Register has AND-gated serial inputs and clear. Each register bit is a D-type master-slave flip-flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip-flop to the low level at the next clock pulse. A high level on one input enables

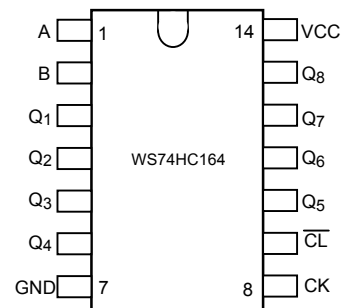
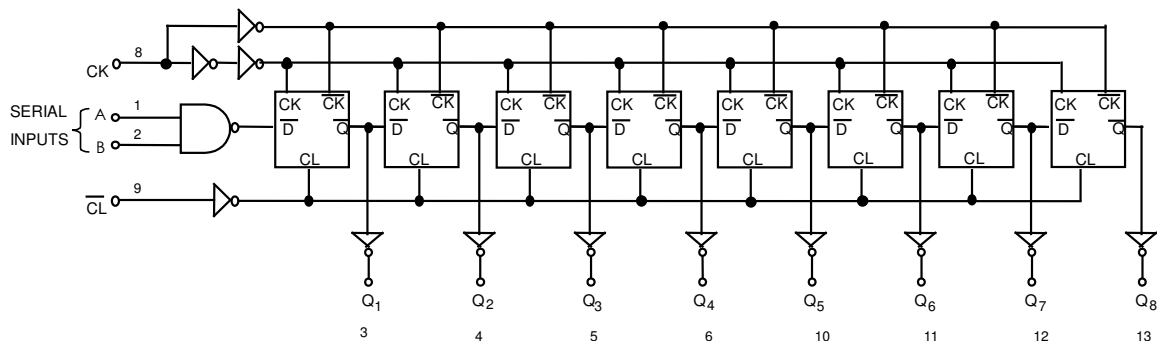
another input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only data meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register during the positive edge of the clock pulse. Clear is independent of the clock and accomplished by a low level at the clear (CL) input.

74HC164 logic is functionally as well as pin-out compatible with the standard LS164. All inputs are protected from ESD damage by internal diode clamps to Vcc and ground.

### FEATURES

- Wide operating supply voltage range: 2-6V.
- Asynchronous master reset CL active at low
- Data serially shifted at the positive edge of clock CK
- Low input current:  $< 1\mu\text{A}$ .
- Low quiescent supply current: 80 $\mu\text{A}$  maximum
- Output driving capability: standard

### LOGIC DIAGRAM



### FUNCTIONAL DESCRIPTION

#### 1. Truth Table

Inputs				Outputs			
$\overline{\text{CL}}$	CK	A	B	Q <sub>1</sub>	Q <sub>2</sub>	...	Q <sub>8</sub>
L	X	X	X	L	L	...	L
H	L	X	X	Q <sub>10</sub>	Q <sub>20</sub>	...	Q <sub>80</sub>
H	↑	H	H	H	Q <sub>1N</sub>	...	Q <sub>7N</sub>
H	↑	L	X	L	Q <sub>1N</sub>	...	Q <sub>7N</sub>
H	↑	X	L	L	Q <sub>1N</sub>	...	Q <sub>7N</sub>

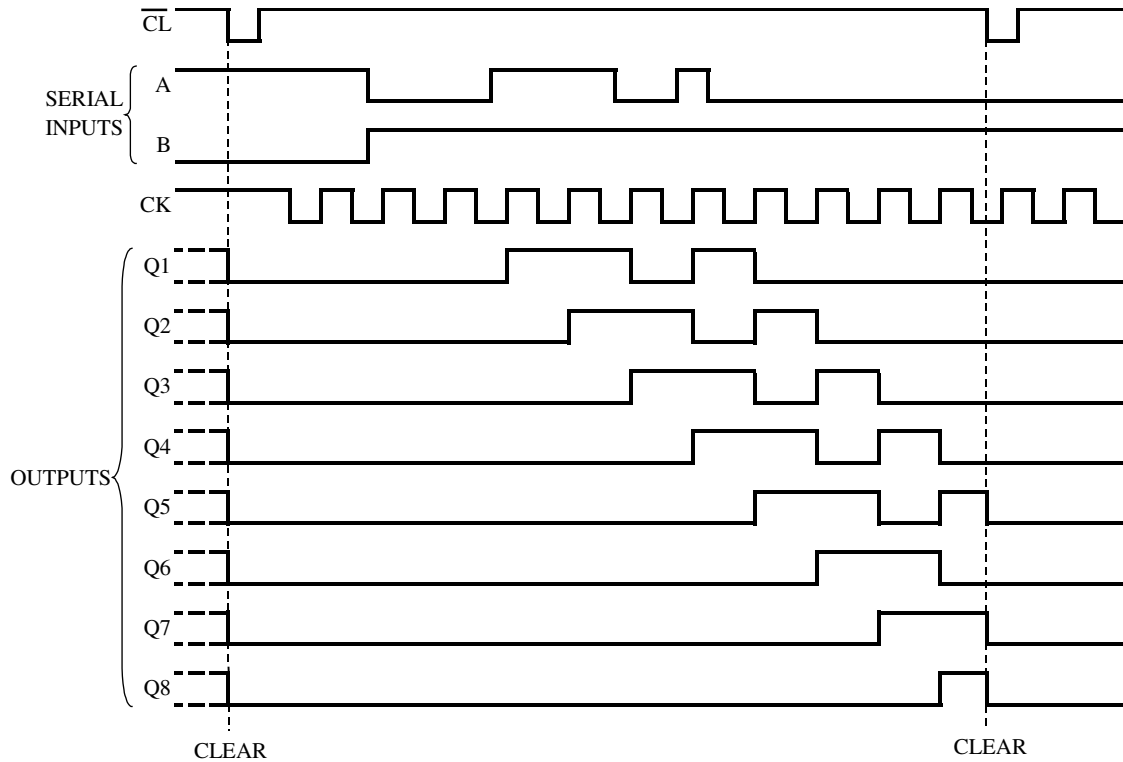
H = High Level (steady state). L = Low Level (steady state)

X = don't care (any input, including transitions)

↑ = Transition from low to high level.

Q<sub>10</sub>, Q<sub>20</sub>, Q<sub>80</sub> = the level of Q<sub>1</sub>, Q<sub>2</sub>, Q<sub>8</sub>, respectively, before the indicated steady state input conditions were established.

Q<sub>1N</sub>, Q<sub>7N</sub> = The level of Q<sub>1</sub> or Q<sub>7</sub> before the most recent ↑ transition of the clock; indicates a one-bit shift.

**2. Logic Waveform**

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Value	Unit
DC supply voltage (V <sub>CC</sub> )	- 0.5 ~ + 7.0	V
DC input or output Voltage (V <sub>IN</sub> , V <sub>OUT</sub> )	-0.5 to V <sub>CC</sub> +0.5	V
DC Current Drain per pin, any output (I <sub>OUT</sub> )	±25	mA
DC Current V <sub>CC</sub> or GND (I <sub>CC</sub> )	±50	mA
Storage Temperature( T <sub>STG</sub> )	-65 ~ +150	°C
Power Dissipation (P <sub>D</sub> )	500	mW

**Note 1:** Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Min.	Typ.	Max.	Unit
DC Supply Voltage (V <sub>CC</sub> )	2	5	6	V
Input / output Voltage (V <sub>IN</sub> , V <sub>OUT</sub> )	0		V <sub>CC</sub>	V
V <sub>IH</sub> High-level Input Voltage	V <sub>CC</sub> = 2 V	1.5		V
	V <sub>CC</sub> = 4.5 V	3.15		
	V <sub>CC</sub> = 6 V	4.2		
V <sub>IL</sub> Low-level Input Voltage	V <sub>CC</sub> = 2 V		0.5	V
	V <sub>CC</sub> = 4.5 V		1.35	
	V <sub>CC</sub> = 6 V		1.8	
Input Rise/Fall Times (t <sub>r</sub> /t <sub>f</sub> )	V <sub>CC</sub> = 2 V		1000	ns
	V <sub>CC</sub> = 4.5 V		500	
	V <sub>CC</sub> = 6 V		400	
Operating Temperature (T <sub>A</sub> )	74HC164	-40	+85	°C

**Note 2:** All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.

**DC ELECTRICAL CHARACTERISTICS**

( apply across temperature range unless otherwise specified)

Parameter	Test Conditions		Vcc	T <sub>A</sub> =25°C		T <sub>A</sub> =-40~85 °C		Unit
				Min.	Typ.	Max.	Min.	
V <sub>OH</sub>	V <sub>I</sub> =V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20uA	2V	1.9	1.998	1.9		V
			4.5V	4.4	4.499	4.4		
			6V	5.9	5.999	5.9		
		I <sub>OH</sub> = -4mA	4.5V	3.98	4.3	3.84		
		I <sub>OH</sub> = -5.2mA	6V	5.48	5.8	5.34		
V <sub>OL</sub>	V <sub>I</sub> =V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = 20uA	2V		0.002	0.1	0.1	V
			4.5V		0.001	0.1	0.1	
			6V		0.001	0.1	0.1	
		I <sub>OH</sub> = 4mA	4.5V		0.17	0.26	0.33	
		I <sub>OH</sub> = 5.2mA	6V		0.15	0.26	0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6V	±0.1	±100		±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6V			8	80	μA
C <sub>i</sub>			2V~6V	3	10		10	pF

**TIMING REQUIREMENTS OVER RECOMMENDED OPERATING TEMPERATURE RANGE  
(unless otherwise noted)**

Parameter		Vcc	T <sub>A</sub> =25°C		T <sub>A</sub> =-40~85 °C		Unit
			Min.	Max.	Min.	Max.	
f <sub>clock</sub>	Clock frequency	2V		6		5	MHz
		4.5V		31		25	
		6V		36		28	
t <sub>w</sub>	Pulse duration	CL low	2V	100		125	ns
			4.5V	20		25	
			6V	17		21	
	CK High or low	2V	80		100		
		4.5V	16		20		
		6V	14		18		
t <sub>s</sub>	Setup time (before CK ↑)	Data	2V	100		125	ns
			4.5V	20		25	
			6V	17		21	
	CL inactive	2V	100		125		
		4.5V	20		25		
		6V	17		21		
t <sub>h</sub>	Hold time (Data after CK ↑)		2V	5		5	ns
			4.5V	5		5	
			6V	5		5	

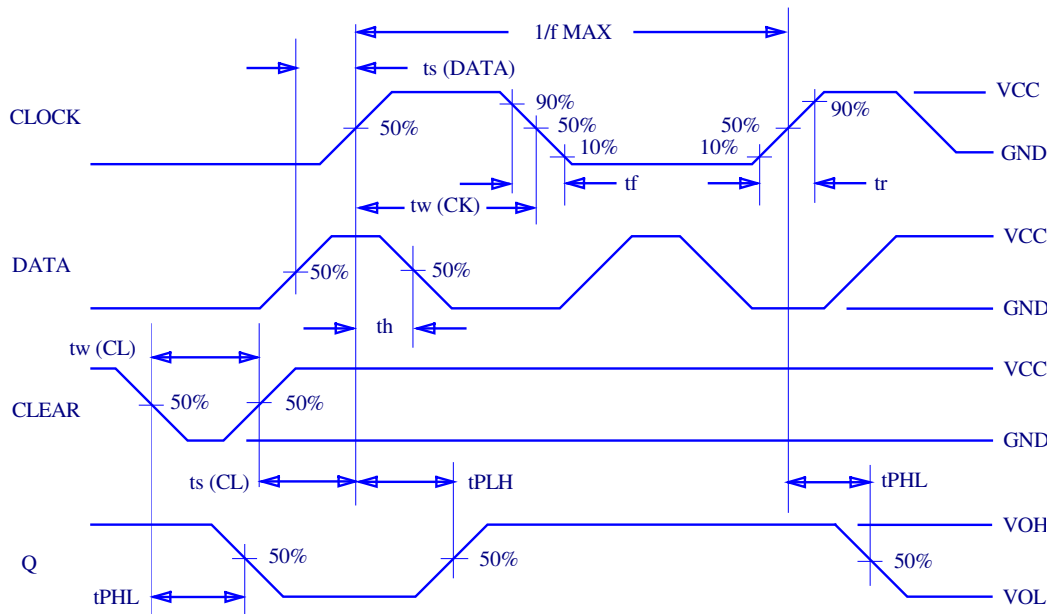
**AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub>=50pF)**

Parameter	From (Input)	To (Output)	Vcc	T <sub>A</sub> =25°C			T <sub>A</sub> =-40~85 °C		Unit
				Min.	Typ.	Max.	Min.	Max.	
f <sub>max</sub>			2V	6	10		5	MHz	
			4.5V	31	54		25		
			6V	36	62		28		
t <sub>PHL</sub>	CL	Any Q	2V		140	205		255	ns
			4.5V		28	41		51	
			6V		24	35		46	
t <sub>pd</sub>	CK	Any Q	2V		115	175		220	ns
			4.5V		23	35		44	
			6V		20	30		38	
t <sub>t</sub>			2V		38	75		95	ns
			4.5V		8	15		19	
			6V		6	13		16	

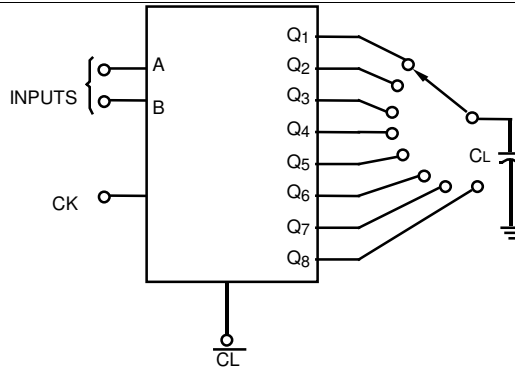
Parameter	Test Conductions	Typ.	Unit
C <sub>pd</sub> Power Dissipation Capacitance	T <sub>A</sub> =25°C, NO LOAD	135	pF

**Note 3 :** C<sub>PD</sub> determines the no load dynamic power consumption ,  $P_D=C_{PD} \cdot V_{CC}^2 \cdot f_i + I_{CC} \cdot V_{CC}$ , and the no load dynamic current consumption,  $I_s = C_{PD} \cdot V_{CC} \cdot f_i + I_{CC}$ .

**AC SWITCHING WAVEFORM AND AC TEST CIRCUIT**



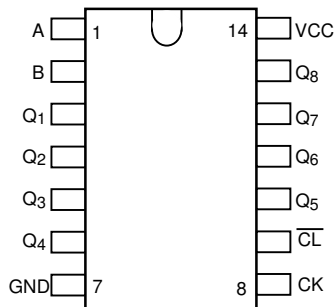
**AC Switching Waveform**



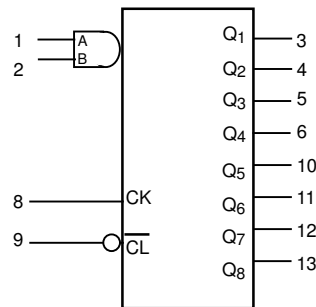
AC Testing Circuit

PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
1, 2	A, B	Data Inputs
3, 4, 5, 6, 10, 11, 12, 13	Q <sub>1</sub> – Q <sub>8</sub>	Outputs
7	GND	Ground (0V)
8	CK	Clock input (active at rising edge)
9	$\overline{CL}$	Master reset input (active at Low)
14	V <sub>CC</sub>	Positive power supply

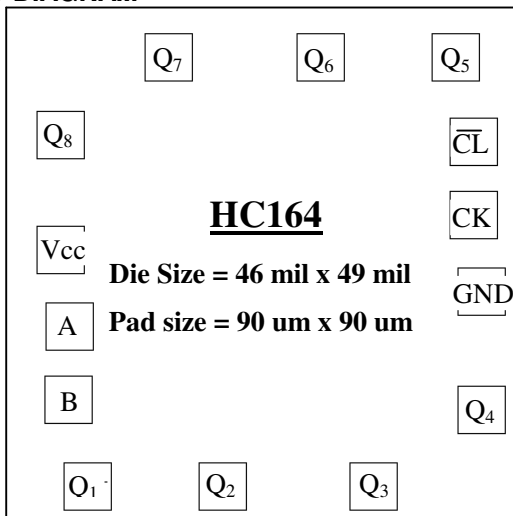


Pin Configuration (DIP14)



Logic Symbol

PAD DIAGRAM



The Coordinate of Each Pad

Q <sub>1</sub> (-395.1, -452.8)	Q <sub>5</sub> (305.0, 362.8)
Q <sub>2</sub> (-138.3, -452.8)	Q <sub>6</sub> ( 48.2, 362.8)
Q <sub>3</sub> ( 149.9, -452.8)	Q <sub>7</sub> (-240.0, 362.8)
Q <sub>4</sub> (355.4, -308.2)	Q <sub>8</sub> (-445.5, 214.6)
GND (355.4, - 82.2)	V <sub>CC</sub> (-445.5, - 3.8)
CK ( 338.7, 61.8)	A (-428.8, -148.8)
$\overline{CL}$ (340.6, 201.8)	B (-430.7, -288.8)

**Note 4:** Substrate should be connected to Vcc or left it open.