# SH7211 Group

## MTU2 Three-Phase Complementary PWM Output Function (Complementary PWM Mode)

### Introduction

This application note presents sample settings for producing three-phase complementary pulse width modulation (PWM) output, with no overlap of the positive and antiphases, using multi-function timer pulse unit 2 (MTU2) of the SH7211.

### Target Device

SH7211

### Contents

# 1. Preface

## 1.1 Specifications

This application note describes how to use the complementary PWM mode function of multi-function timer pulse unit 2 (MTU2) to output three-phase complementary PWM waveforms. Figure 1 shows the configuration.

- Channels 3 and 4 of MTU2 are set to complementary PWM mode (complementary PWM mode 3).
- The PWM positive phase output pins are TIOC3B, TIOC4A, and TIOC4B. The antiphase output pins corresponding to these phase output pins are TIOC3D, TIOC4C, and TIOC4D.
- The PWM output signal is low-active.
- In complementary PWM mode, PWM waveform output incorporates dead time (anti-short periods) to prevent overlap between the positive and antiphases. The dead time is set to 4 µm.
- The PWM carrier cycle is set to 400 µm.
- The PWM duty setting values are updated at an interrupt generated every PWM carrier cycle.
- A toggle waveform synchronized with the PWM carrier half-cycle is output by pin TIOC3A.

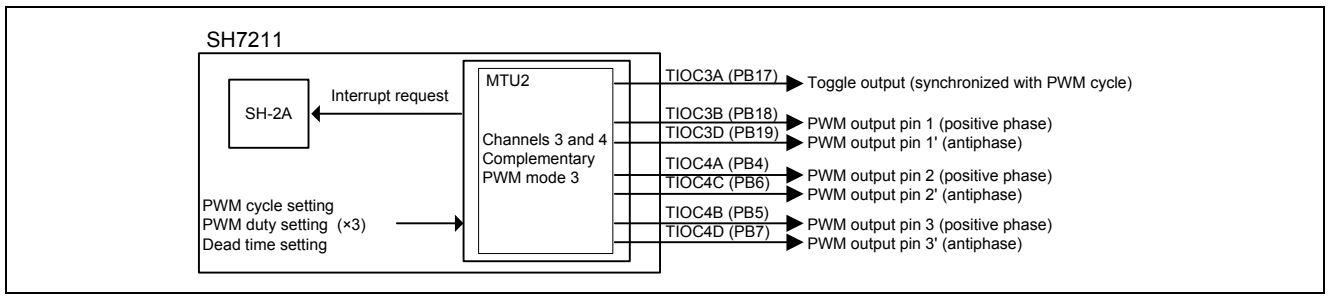


**Figure 1 Three-Phase Complementary PWM Output (Complementary PWM Mode 3)**

## 1.2 Module Used

Channels 3 and 4 of multi-function timer pulse unit 2 (MTU2)

## 1.3 Applicable Conditions

| | |
|---|---|
| MCU: | SH7211 [R5F7211] |
| Operating frequencies: | Internal clock (Iϕ) = 160 MHz |
| | Bus clock (Bϕ) = 40 MHz |
| | Peripheral clock (Pϕ) = 40 MHz |
| | MTU2S clock (Mϕ) = 80 MHz |
| | AD clock (Aϕ) = 40 MHz |
| MCU operating mode: | Single-chip mode |
| Integrated development environment: | Renesas Technology High-performance Embedded Workshop, Ver. 4.05.01.001 |
| C compiler: | Renesas Technology SuperH RISC engine Family C/C++ Compiler Package, Ver. 9.03, Release 00 |
| Compile options: | High-performance Embedded Workshop default settings |
| | (-cpu=sh2a -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo) |

## 2. Description of the Sample Application

In this sample application, the complementary PWM mode function of multi-function timer pulse unit 2 (MTU2) is used.

### 2.1 Operational Overview of Module Used

#### 2.1.1 Multi-Function Timer Pulse Unit 2 (MTU2)

Multi-function timer pulse unit 2 (MTU2) is a multi-function timer unit comprising a 6-channel 16-bit timer. Settings such as compare match or input capture can be made individually for each channel. Channels 3 and 4 can be used for 6-line PWM output control by specifying complementary PWM mode or reset synchronous mode.

For details of MTU2, see the Multi-Function Timer Pulse Unit 2 (MTU2) section in the SH7211 Group Hardware Manual (RJJ09B0338).

Table 1 is an overview of multi-function timer pulse unit 2 (MTU2). Figure 2 is a block diagram of MTU2.

**Table 1 Overview of Multi-Function Timer Pulse Unit 2 (MTU2)**

| Item | Description |
|---|---|
| Number of channels | 16-bit timer × 6 channels (channels 0 to 5) |
| Counter clock | Each channel selectable among eight counter input clocks (four counter input clocks for channel 5) |
| Operation of channels 0 to 5 | • Waveform output at compare match, input capture function, counter clear operation, simultaneous write to multiple timer counters (TCNT), simultaneous clear at compare match or input capture<br>• Synchronous register I/O using counter-synchronous operation, max. 12-phase PWM output through combination with synchronous operation |
| Triggers for A/D converter | • Ability to generate conversion start trigger for A/D converter<br>• Ability to generate interrupt at counter peak/trough and to skip conversion start triggers for A/D converter in complementary PWM mode |
| Buffered operation | • Ability to specify register buffer operation for channels 0, 3, and 4 |
| Operating modes | • Ability to specify PWM mode for channels 0 to 4<br>• Ability to specify phase counting mode independently for channels 1 and 2<br>• Ability to specify 3-phase positive and negative PWM waveform output (total 6 lines) in complementary PWM mode or reset synchronous PWM mode, using linked operation of channels 3 and 4 |
| Interrupt requests | • 28 interrupt sources (compare match, input capture, etc.) |
| Others | • Cascade connection operation<br>• High-speed access via internal 16-bit bus<br>• Support for automatic transfer of register data<br>• Ability to specify module standby mode<br>• Support for dead time compensation counter function using channel 5 |

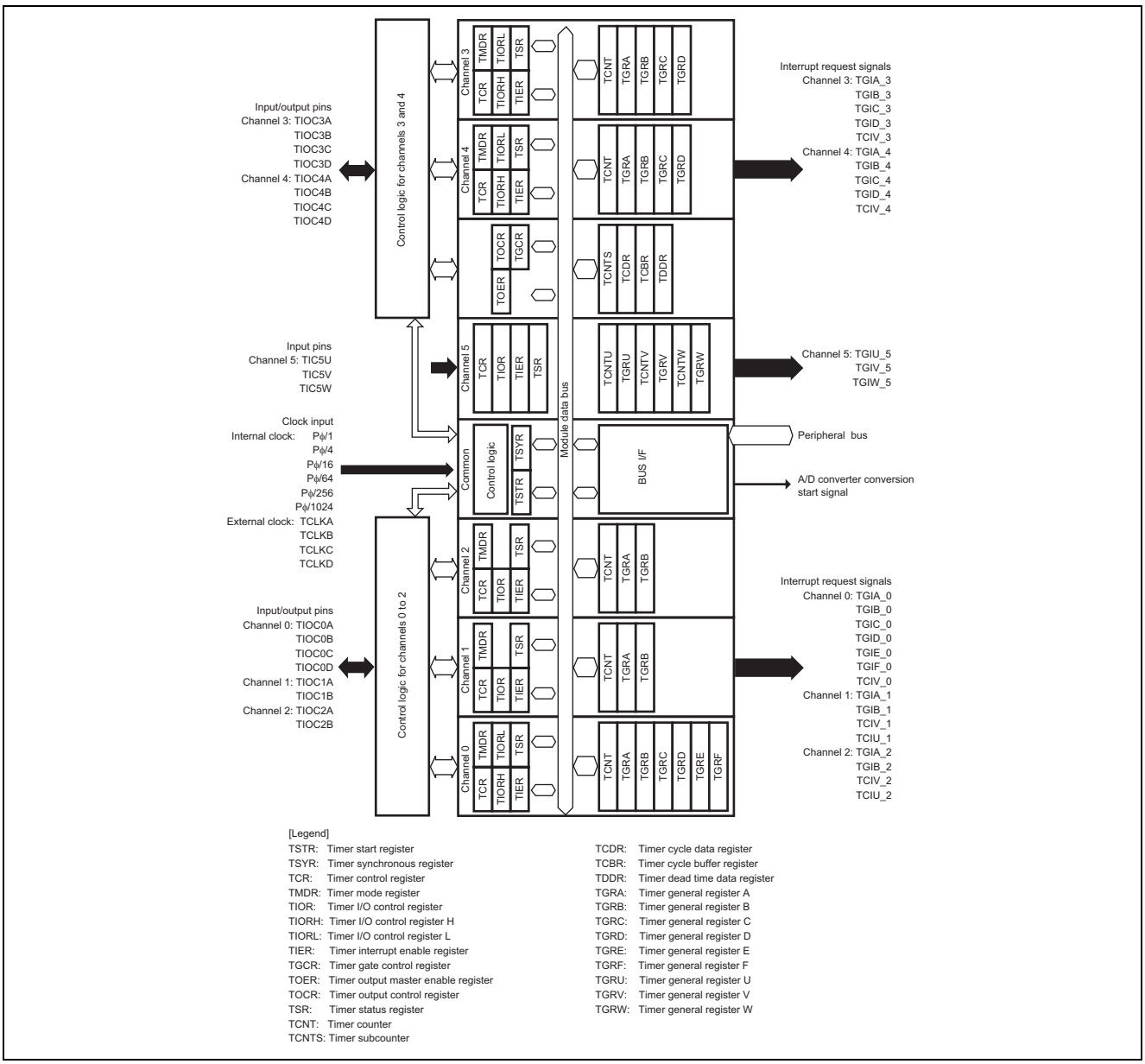


**Figure 2 Block Diagram of MTU2**

### 2.1.2 Complementary PWM mode

Multi-function timer pulse unit 2 (MTU2) can be set to complementary PWM mode, in which channels 3 and 4 are used in combination. In complementary PWM mode, three-phase non-overlapping positive and negative PWM waveforms are output. It is also possible to specify PWM waveform output with no dead time to prevent overlapping. Pins TIOC3B, TIOC3D, TIOC4A, TIOC4B, TIOC4C, and TIOC4D function as PWM output pins in complementary PWM mode. The TIOC3A pin can be set for toggle output synchronized with the PWM cycle.

Figure 3 shows the configuration of channels 3 and 4 of multi-function timer pulse unit 2 (MTU2) in complementary PWM mode.

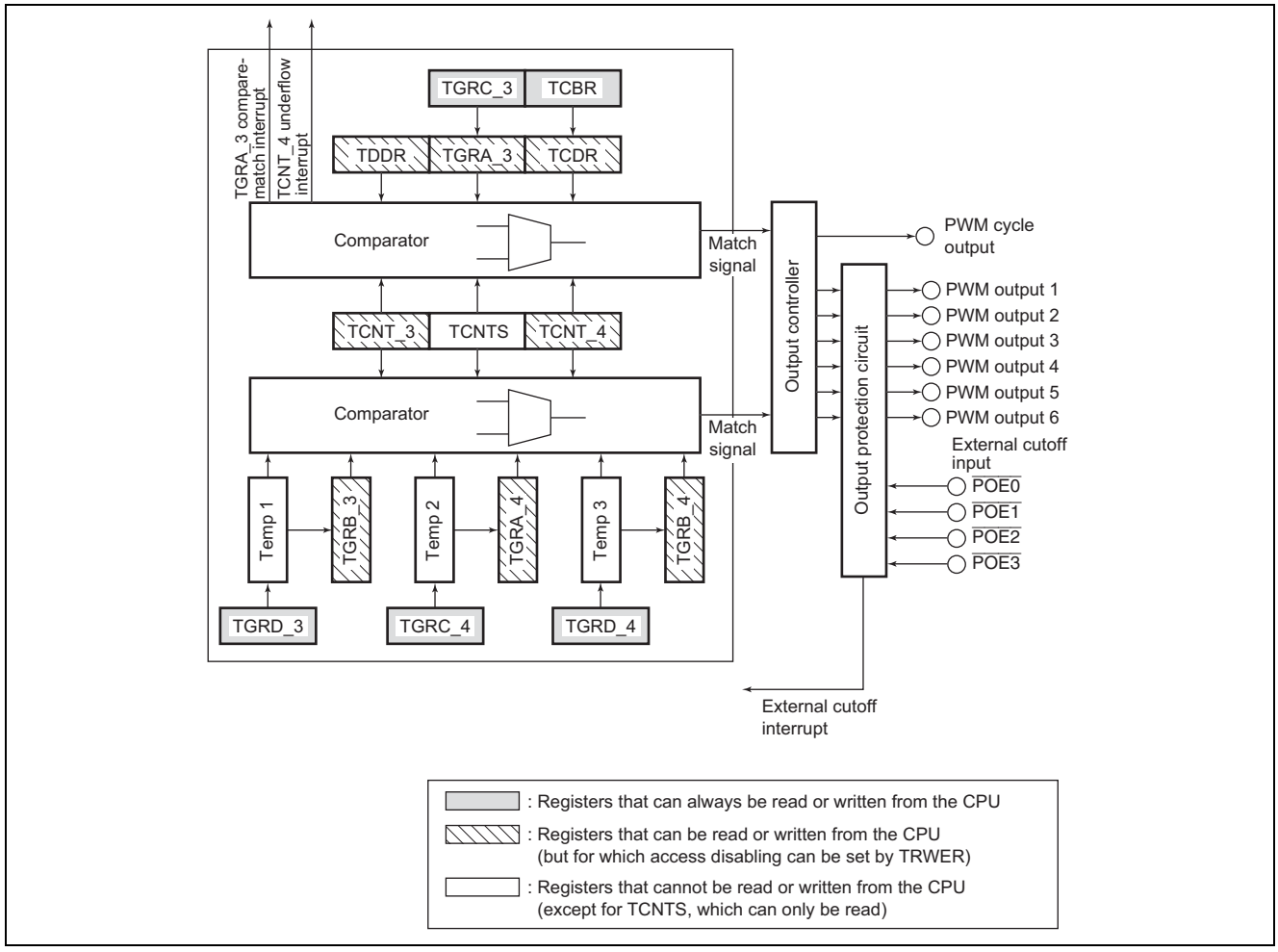


**Figure 3 Block Diagram of Channels 3 and 4 in Complementary PWM Mode**

The channel 3 and channel 4 register functions in complementary PWM mode are described below.

- Timer general register A_3 (TGRA_3) operates as a compare register. The upper limit value for TCNT_3 (1/2 carrier cycle + dead time) is set in TGRA_3. To change the value of this register while the timer is operating, set the new value in timer general register C_3 (TGRC_3).
- Timer general register B_3 (TGRB_3) operates as a compare register. The duty of the PWM waveforms output by pins TIOC3B and TIOC3D is set in TGRB_3. To change the value of this register while the timer is operating, set the new value in timer general register D_3 (TGRD_3).
- Timer general register C_3 (TGRC_3) operates as the buffer register for TGRA_3. While the timer is operating, TGRA_3 is updated to reflect values set in TGRC_3.
- Timer general register D_3 (TGRD_3) operates as the buffer register for TGRB_3. While the timer is operating, TGRB_3 is updated to reflect values set in TGRD_3.
- Timer general register A_4 (TGRA_4) operates as a compare register. The duty of the PWM waveforms output by pins TIOC4A and TIOC4C is set in TGRA_4. To change the value of this register while the timer is operating, set the new value in timer general register C_4 (TGRC_4).
- Timer general register B_4 (TGRB_4) operates as a compare register. The duty of the PWM waveforms output by pins TIOC4B and TIOC4D is set in TGRB_4. To change the value of this register while the timer is operating, set the new value in timer general register D_4 (TGRD_4).
- Timer general register C_4 (TGRC_4) operates as the buffer register for TGRA_4. While the timer is operating, TGRA_4 is updated to reflect values set in TGRC_4.
- Timer general register D_4 (TGRD_4) operates as the buffer register for TGRB_4. While the timer is operating, TGRB_4 is updated to reflect values set in TGRD_4.
- Temporary registers 1, 2, and 3 (Temp1, 2, and 3) occupy a position between the buffer registers and compare registers. Data written to the buffer register is transferred to the temporary register and then to the compare register. The temporary registers cannot be accessed by the CPU.
- Timer counter_3 (TCNT_3) is a 16-bit counter. TCNT_3 starts counting down when a compare match with TGRA_3 occurs, and it starts counting up when a compare match with the timer dead time data register (TDDR) occurs.
- Timer counter_4 (TCNT_4) is a 16-bit counter. TCNT_4 starts counting down when a compare match with the timer cycle data register (TCDR) occurs, and it starts counting up when the value of TCNT_4 reaches H'0000.
- The timer dead time data register (TDDR) is a 16-bit readable/writable register. TDDR specifies the dead time for the PWM waveforms.
- The timer cycle data register (TCDR) is a 16-bit register. TCDR specifies a value equal to one-half the PWM carrier cycle.
- The timer cycle buffer register (TCBR) operates as the buffer register for TCDR. While the timer is operating, TCDR is updated to reflect values set in TCBR.

## 2.2 Operation of the Sample Program

### 2.2.1 Settings for Operation of the Sample Program

In this application note, channels 3 and 4 of the multi-function timer pulse unit 2 (MTU2) are set to complementary PWM mode 3 and three-phase complementary PWM waveforms are output. In addition, toggle output synchronized with the PWM carrier cycle is generated. Table 2 lists the setting conditions for complementary PWM mode operation. Figure 4 shows a sample of output waveforms in complementary PWM mode.

**Table 2 Setting for Operation in Complementary PWM Mode**

| Item | Description |
|---|---|
| Channels in use | Channels 3 and 4 |
| Operating mode | Complementary PWM mode 4 (data transfer at counter peaks and troughs) |
| Functions of pins | • TIOC3A pin: Toggle output synchronized to PWM cycle<br>• TIOC3B pin: PWM output 1 (positive phase waveform)<br>• TIOC3D pin: PWM output 1' (PWM output 1 antiphase waveform)<br>• TIOC4A pin: PWM output 2 (positive phase waveform)<br>• TIOC4C pin: PWM output 2' (PWM output 2 antiphase waveform)<br>• TIOC4B pin: PWM output 3 (positive phase waveform)<br>• TIOC4D pin: PWM output 4' (PWM output 3 antiphase waveform) |
| Active level | • Positive phase output: Low-active output<br>• Antiphase output: Low-active output |
| Counter clock | 10 MHz (4 cycles of Pϕ clock) |
| PWM carrier cycle | 400 μm (carrier frequency: 2.5 kHz) |
| Dead time | 4 μm |
| PWM duty | • For PWM outputs 1, 2, and 3, the initial PWM duty is 50%.<br>• The PWM duty is updated by an interrupt generated at every compare match with TGRA_3. (The setting value is incremented or decremented.) |
| Interrupt | • TGRA_3 compare match interrupt<br>A compare match with TGRA_3 occurs every PWM carrier cycle. |

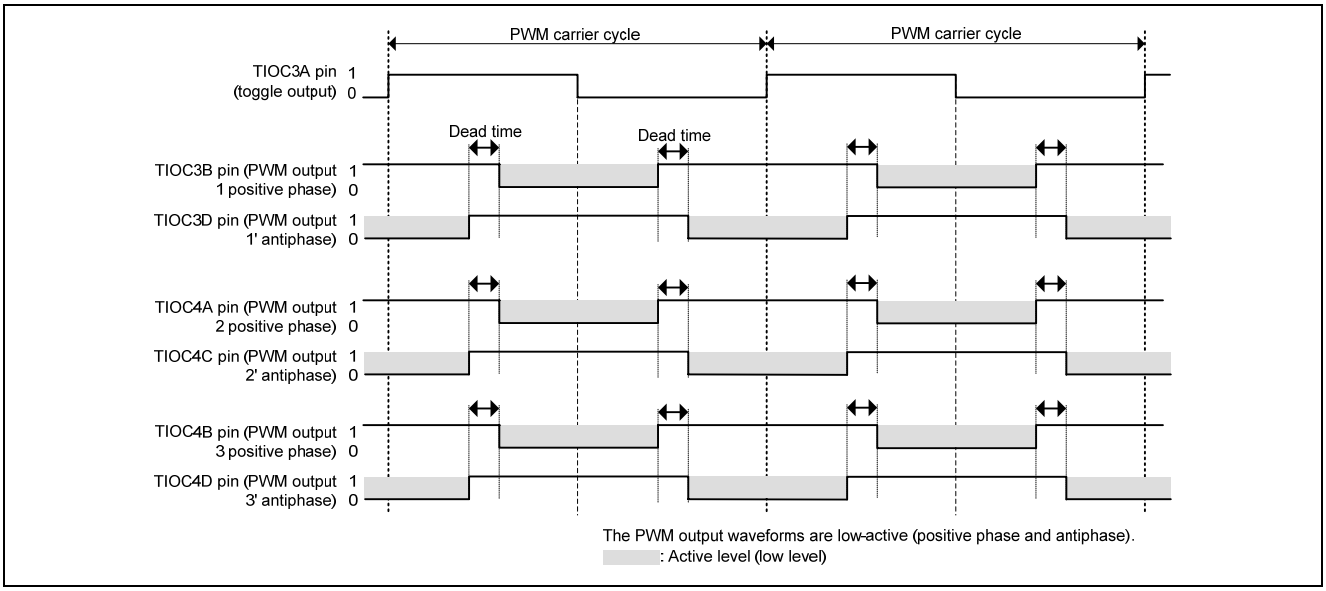


**Figure 4 Output Waveforms in Complementary PWM Mode Operation**

## 2.2.2 Description of Operation by the Sample Program

### (1) Operation of Timer Counters

Figure 5 shows the operation timer counter in complementary PWM mode. Counters TCNT_3 and TCNT_4, which correspond to channel 3 and channel 4, each count up or down. The initial value of counter TCNT_3 is set to the same value as the TDDR register, and the initial value of counter TCNT_4 is set to H'0000. Channels 3 and 4 start timer count operation simultaneously.

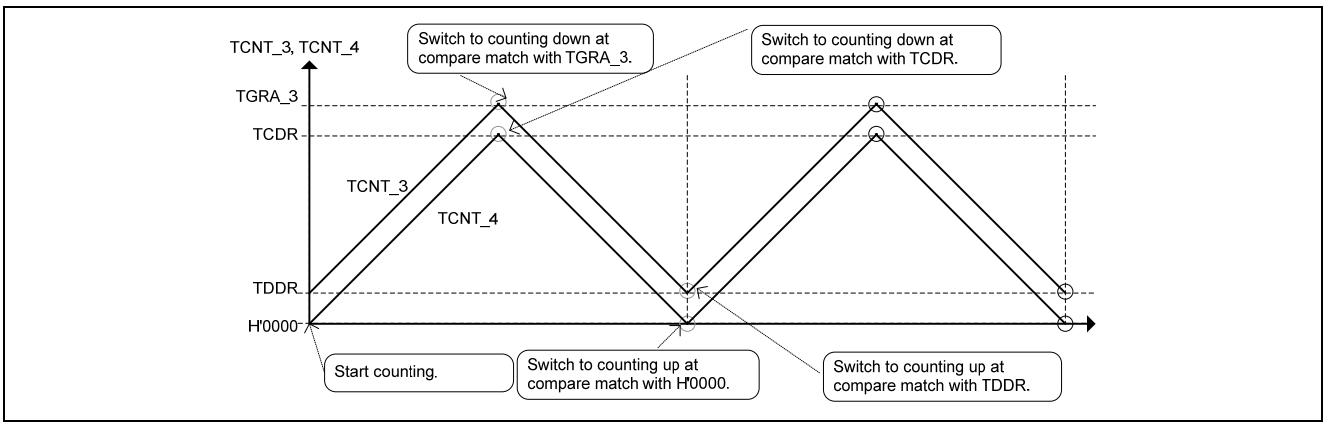


**Figure 5 Operation of Timer Counters**

### (2) PWM Output Waveforms

The three-phase complementary PWM output waveforms are controlled by using the compare match function with timer counters (TCNT_3 and TCNT_4) and compare registers (TGRB_3, TGRA_4, and TGRB_4). When the value of a register matches the value of a counter, positive phase output and antiphase output are generated according to the values set in bits OLSN and OLSP in the timer output control register (TOCR).

Figure 6 shows the output waveforms for single-phase (positive phase, antiphase) complementary PWM output. The positive phase and antiphase output signals are controlled by using the compare match function with timer counters (TCNT_3 and TCNT_4) and a compare register (TGRB_3).

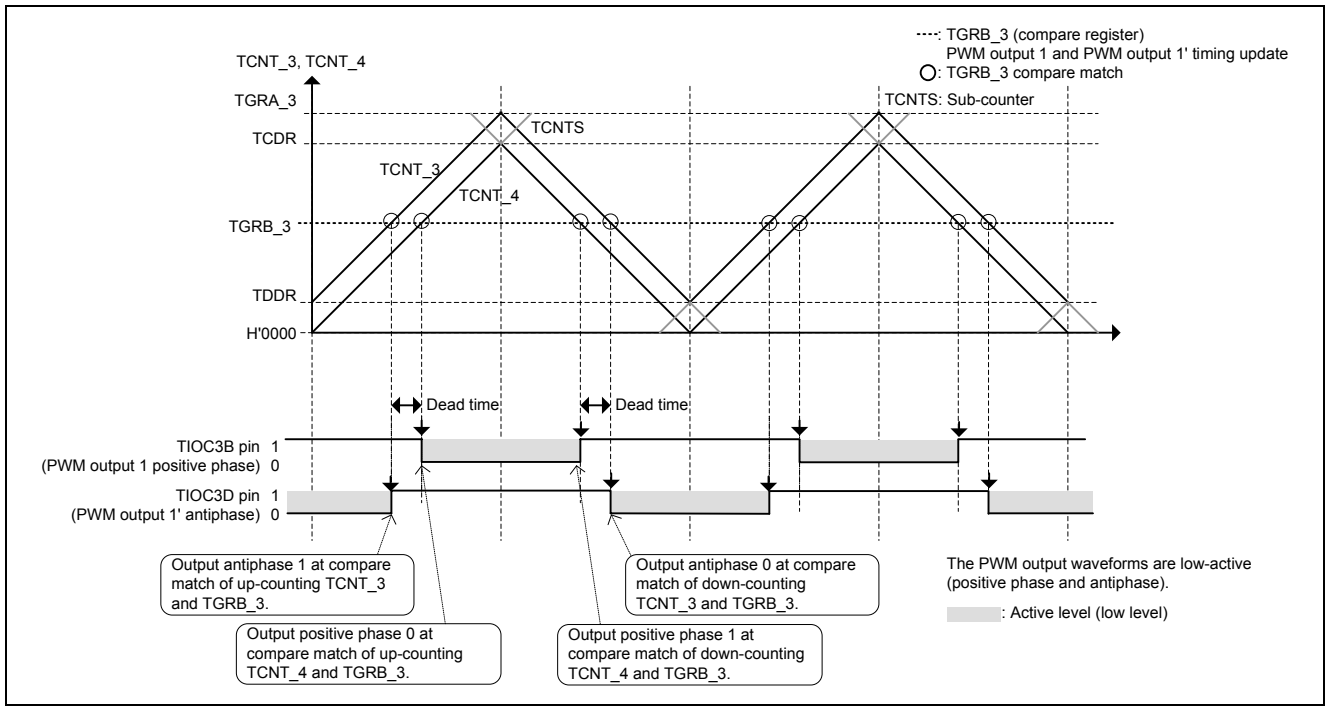


**Figure 6 Complementary PWM Output Waveforms**

### (3) Changing the PWM Duty

Figure 7 shows the PWM duty update timing. In the reference program, the TGRA_3 compare match interrupt (counter peak interrupt) handler makes register settings after incrementing or decrementing the PWM duty setting values. Three buffer registers, TGRD_3, TGRC_4, and TGRD_4, are used to update the PWM duty.

When changing the duty, always set TGRD_4 last. Always execute a write to TGRD_4 after writing updated register data, even if the TGRD_4 data value does not change.

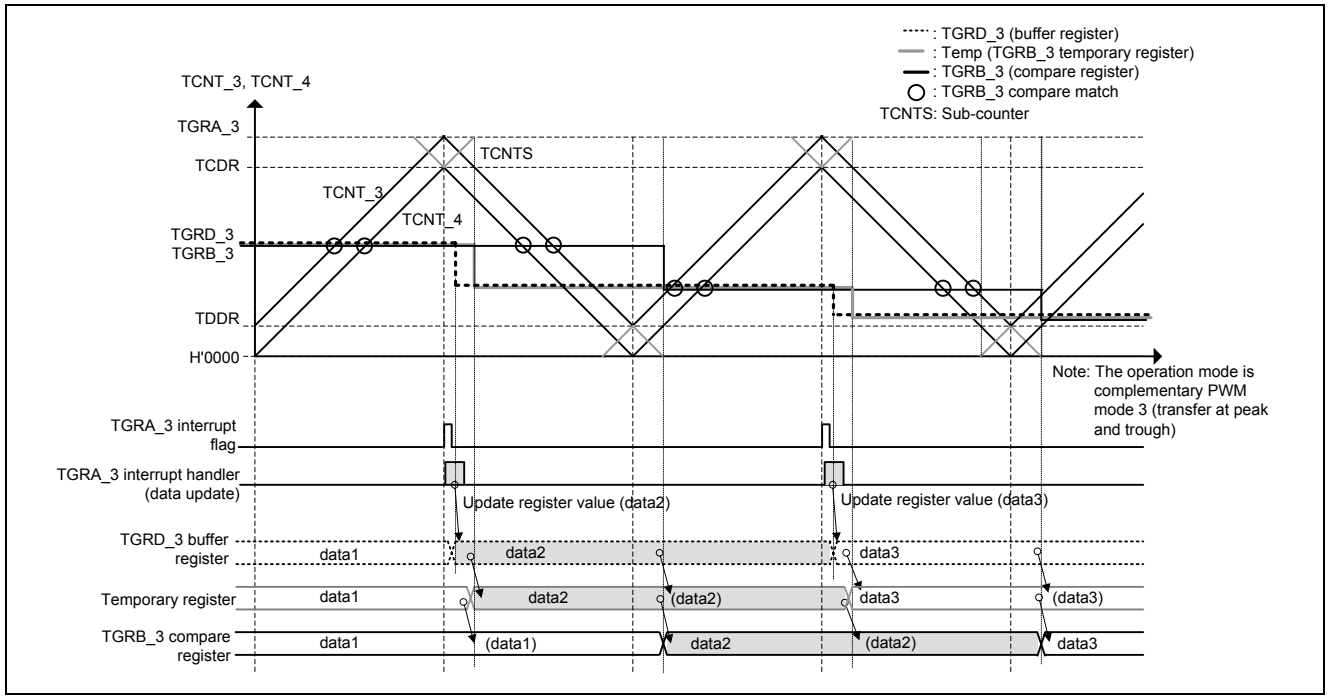


**Figure 7 PWM Duty Update Timing**

### (4) Output Toggling in Synchronization with PWM Cycle

Figure 8 shows the operations for toggling of an output level in synchronization with the PWM cycle. The PSYE bit in the timer output control register (TOCR) is set to 1 to select toggling of an output in synchronization with the PWM carrier cycle. Toggling is of the signal on the TIOC3A pin. The initial value for output is 1.

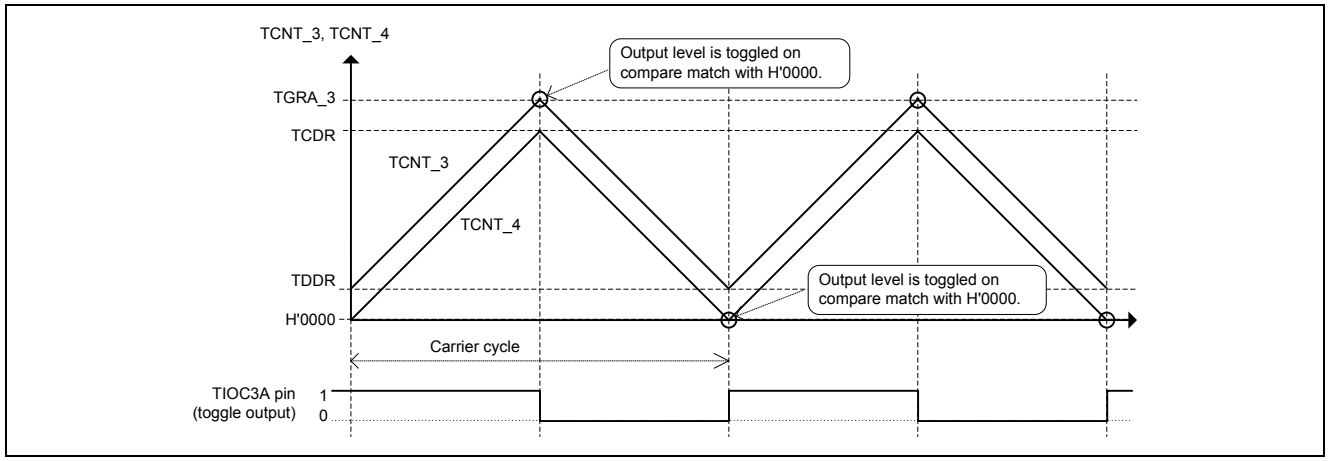


**Figure 8 Operation for Toggling an Output in Synchronization with the PWM Cycle**

### 2.2.3 Example of Output with User-Defined PWM Duty

Table 3 summarizes single-phase positive phase and antiphase output operation, showing the relationship between different PWM duty setting values and the resulting positive phase and antiphase output waveforms.

In complementary PWM mode, the output levels are fixed when the value of the compare register (TGRB_3) is H'0000, with positive phase output in a constant-on state and antiphase output in a constant-off state. The output levels are also fixed when the value of the compare register (TGRB_3) is equal to or greater than the setting value of the TGRA_3 register, with positive phase output in a constant-off state and antiphase output in a constant-on state. Figures 9 and 10 show examples of positive phase and antiphase output waveforms.

Note that when the PWM duty is changed, the new setting value is not written directly to the compare register. Instead, it must be written to the buffer register, after which the compare register is updated via the buffer register.

**Table 3 Example of PWM Duty Settings and Output Waveforms**

| | Output Waveform* | | |
|---|---|---|---|
| **TGRB_3 Register Value** | **Positive Phase Output (TIOC3B Pin)** | **Antiphase Output (TIOC3D Pin)** | **Waveform Figure** |
| TGRB_3 ≥ TGRA_3 | Constant-off state (high) | Constant-on state (low) | Figure 9 (a) |
| Between TGRA_3 and TCDR | Constant-off state (high) | Off waveform output (pulse) | — |
| TGRB_3 = TCDR | Constant-off state (high) | Off waveform output (width of dead time × 2) | Figure 9 (b) |
| Between (TCDR – Td) and TCDR | On waveform output (pulse) | Off waveform output | — |
| TGRB_3 = (TCDR – Td) | On waveform output (width of dead time × 2) | Off waveform output (width of dead time × 4) | Figure 9 (c) |
| Between (TDDR × 2) and (TCDR – Td) | Complementary PWM waveform output | | — |
| TGRB_3 = (TDDR × 2) | Off waveform output (width of dead time × 4) | On waveform output (width of dead time × 2) | Figure 10 (a) |
| Between TDDR and (TDDR × 2) | Off waveform output | On waveform output (pulse) | — |
| TGRB_3 = TDDR | On waveform output (width of dead time × 2) | Constant-off state (high) | Figure 10 (b) |
| Between H'0000 and TDDR | Off waveform output (pulse) | Constant-off state (high) | — |
| TGRB_3 = H'0000 | Constant-on state (low) | Constant-off state (high) | Figure 10 (c) |

Note: * The PWM output active level is set to low. The example is for single-phase (positive phase, antiphase) complementary PWM output.

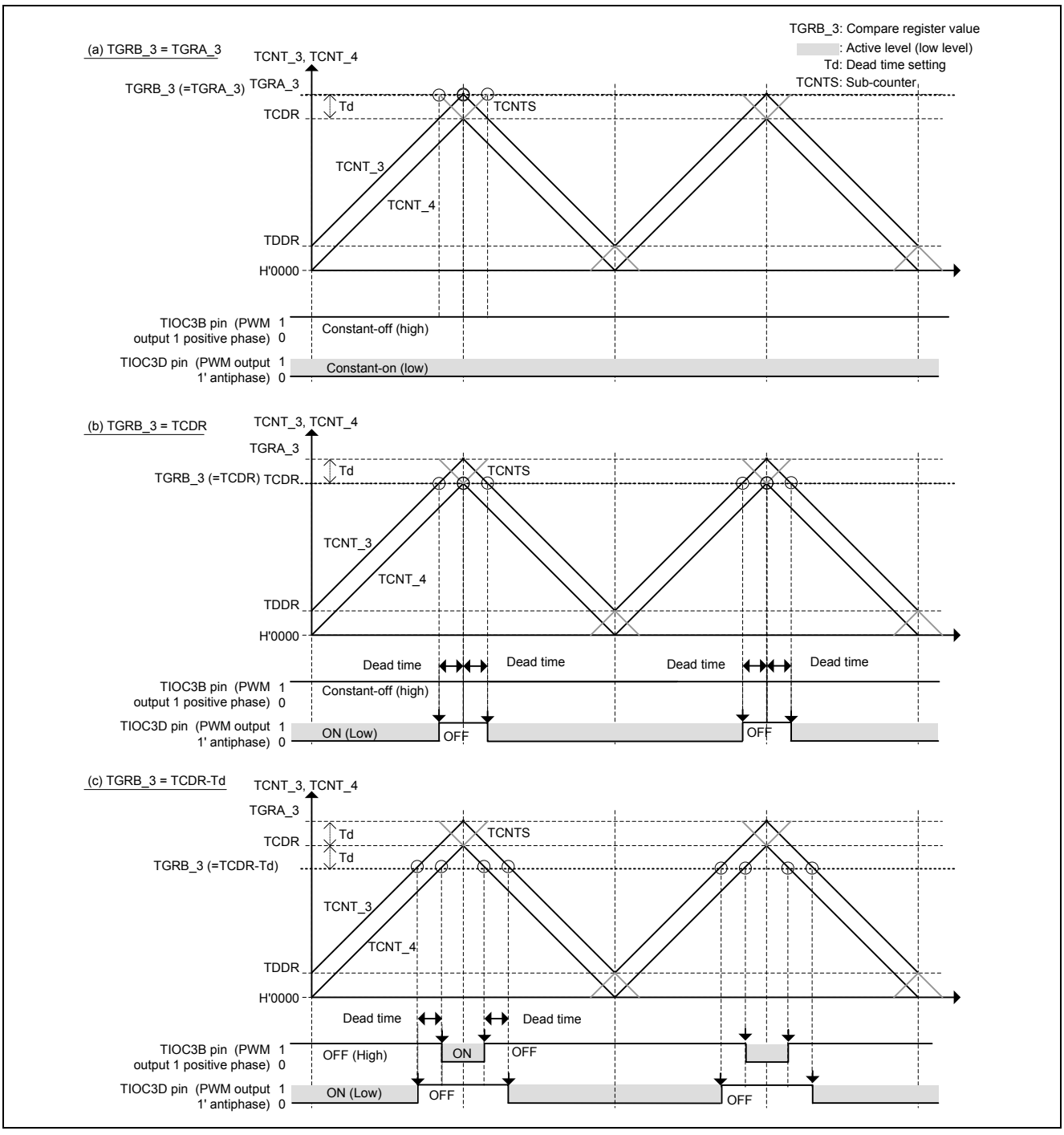


**Figure 9 Examples of PWM Waveform Output (1)**

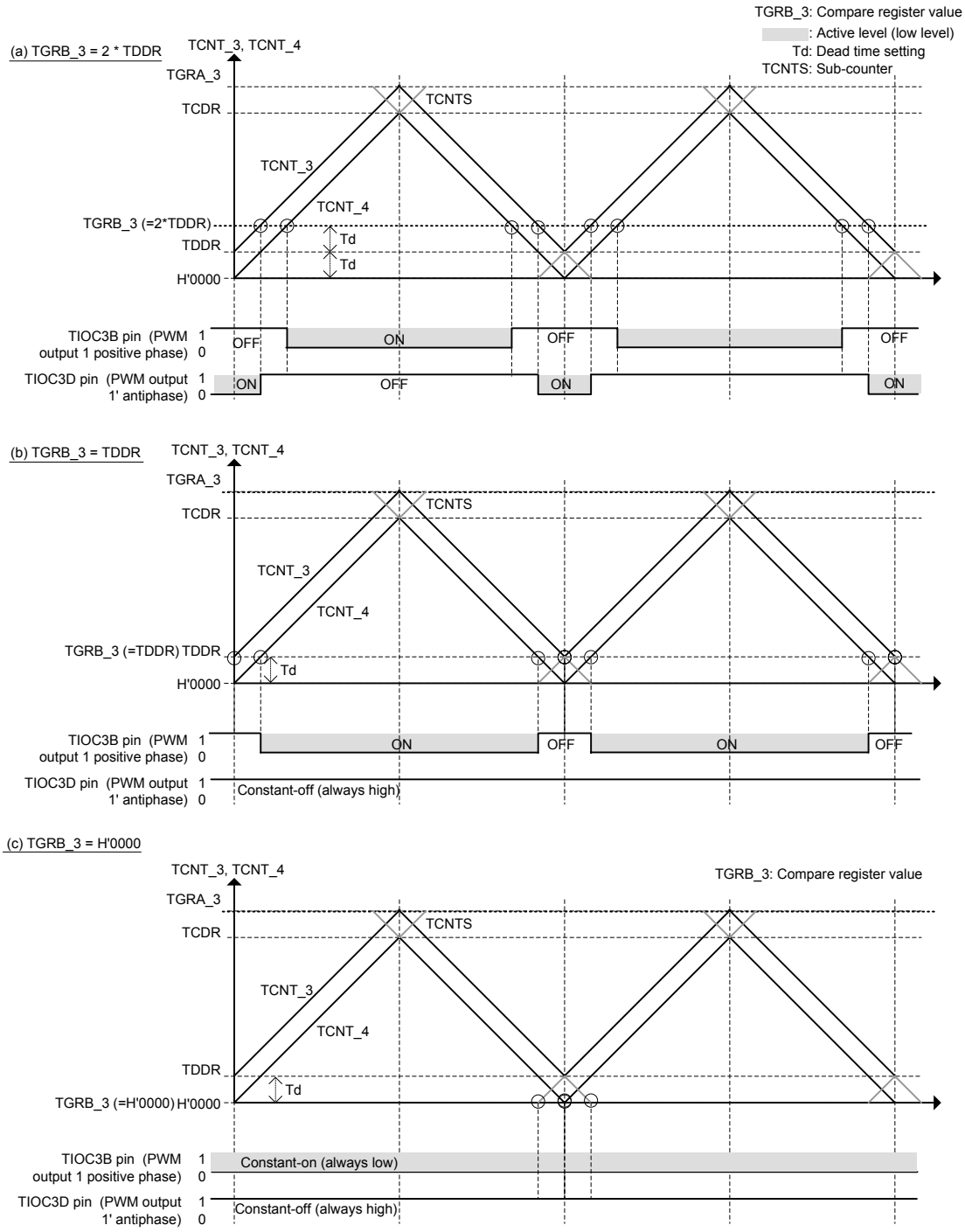


**Figure 10 Examples of PWM Waveform Output (2)**

## 2.3 Configuration of the Sample Program

### 2.3.1 Description of Functions

Table 4 lists functions used in this sample program.

**Table 4 Functions Used**

| Function Name | Label | Description |
|---|---|---|
| Main | main () | Makes initial settings for each module and makes timer start settings for multi-function timer pulse unit 2 (MTU2). |
| Standby setting function | stbcr_init () | Cancels MTU2 module standby. |
| MTU2 initial setting function | mtu2_init () | Makes MTU2 (channels 3 and 4) initial settings. Specifies reset-synchronized PWM mode. |
| PFC initial setting function | pfc_init () | Makes initial settings for the pin function controller (PFC). Sets MTU2-related pins to timer pin function. |
| TGRA_3 interrupt function | int_mtu2_tgia3 () | Handler for the MTU2 (channel 3) TGRA_3 compare match interrupt. Updates the three-phase PWM duty setting values. The interrupt is generated once every PWM carrier cycle (400 μm). |

### 2.3.2 Variable Usage

Table 5 lists the functions used by the sample program.

**Table 5 Variable Usage**

| Label Name | Description | Name of Employing Module |
|---|---|---|
| Dead_time | Dead time setting value (TDDR register setting value) | • mtu2_init () |
| C_cycle | Value equal to 1/2 of PWM carrier cycle (TCBR register setting value) | |
| Pul_cycle | Value equal to 1/2 of PWM carrier cycle + dead time (TGRC_3 register setting value) | |
| Pul_pwm_duty1 | PWM1 output (TIOC3B pin and TIOC3D pin) PWM duty setting value (TGRD_3 register setting value) | • mtu2_init ()<br>• int_mtu2_tgia3 () |
| Pul_pwm_duty2 | PWM2 output (TIOC4A pin and TIOC4C pin) PWM duty setting value (TGRC_4 register setting value) | |
| Pul_pwm_duty3 | PWM3 output (TIOC4B pin and TIOC4D pin) PWM duty setting value (TGRD_4 register setting value) | |

## 2.4 Procedure for Setting the Module Used

The processing sequences of the sample program are shown below.

### 2.4.1 Main Function

Figure 11 shows the processing sequence of the main function.

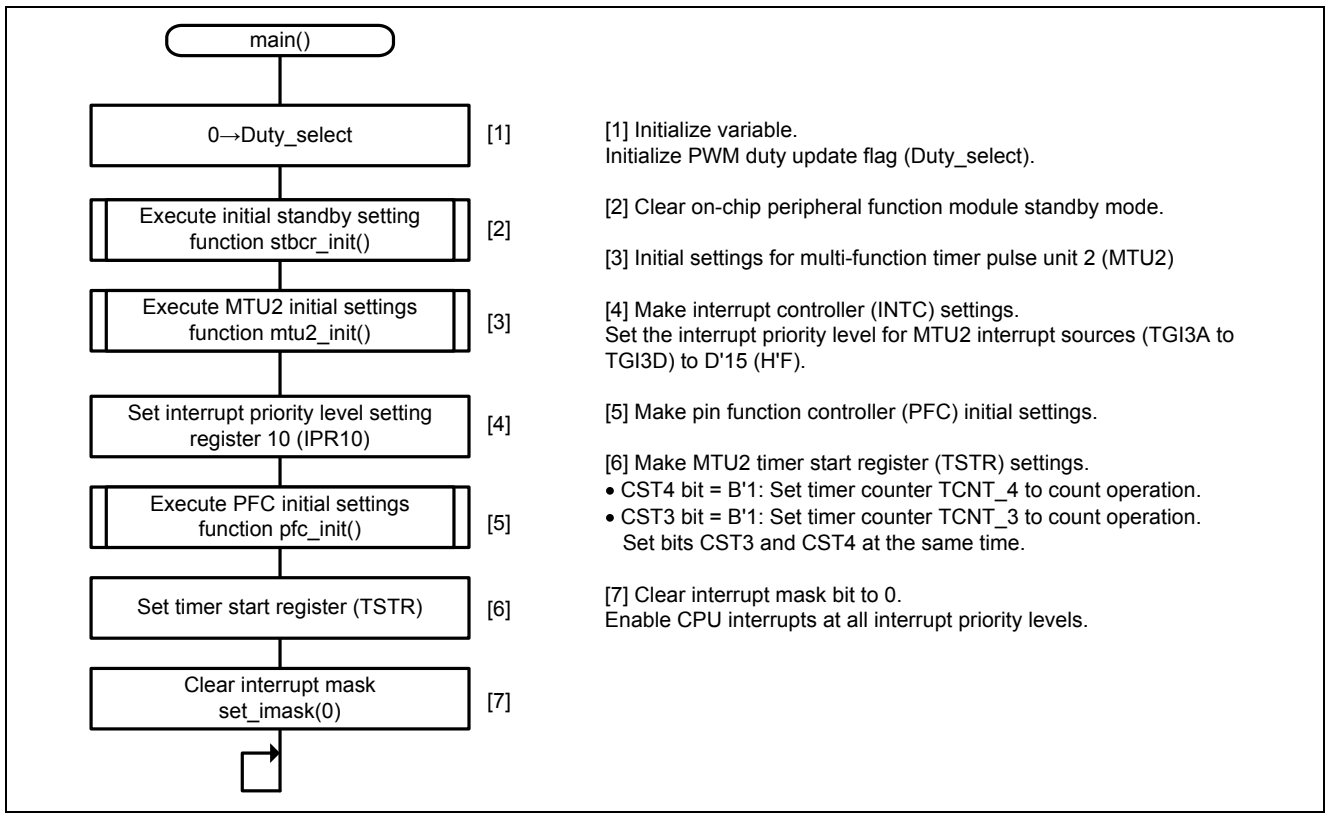


**Figure 11 Processing by Function main**

### 2.4.2 Initialization for Standby

Figure 12 shows the flow of processing for standby processing.

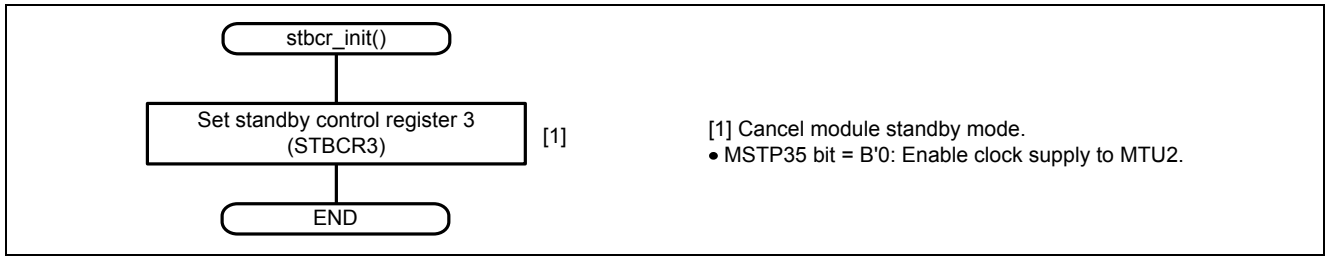


**Figure 12 Initialization: Release from Standby**

### 2.4.3 Initialization of Multi-Function Timer Pulse Unit 2 (MTU2)

Figure 13 shows the processing sequence of the function that makes initial settings for multi-function timer pulse unit 2 (MTU2). Channels 3 and 4 of are set to complementary PWM mode 3.

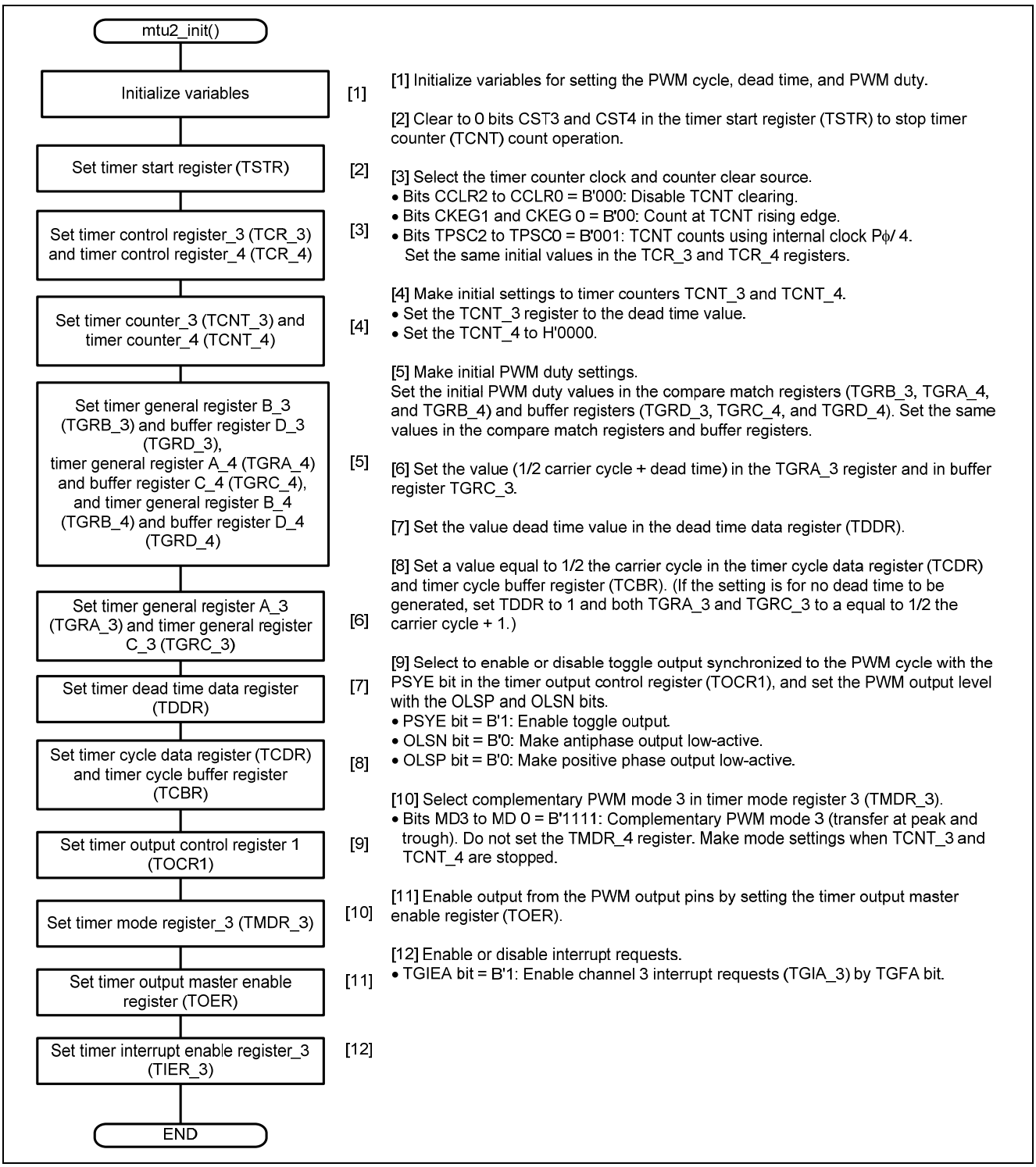


**Figure 13 Initialization of MTU2**

### 2.4.4 Initialization of Pin Function Controller (PFC)

Figure 14 shows the flow for initialization of the PFC.

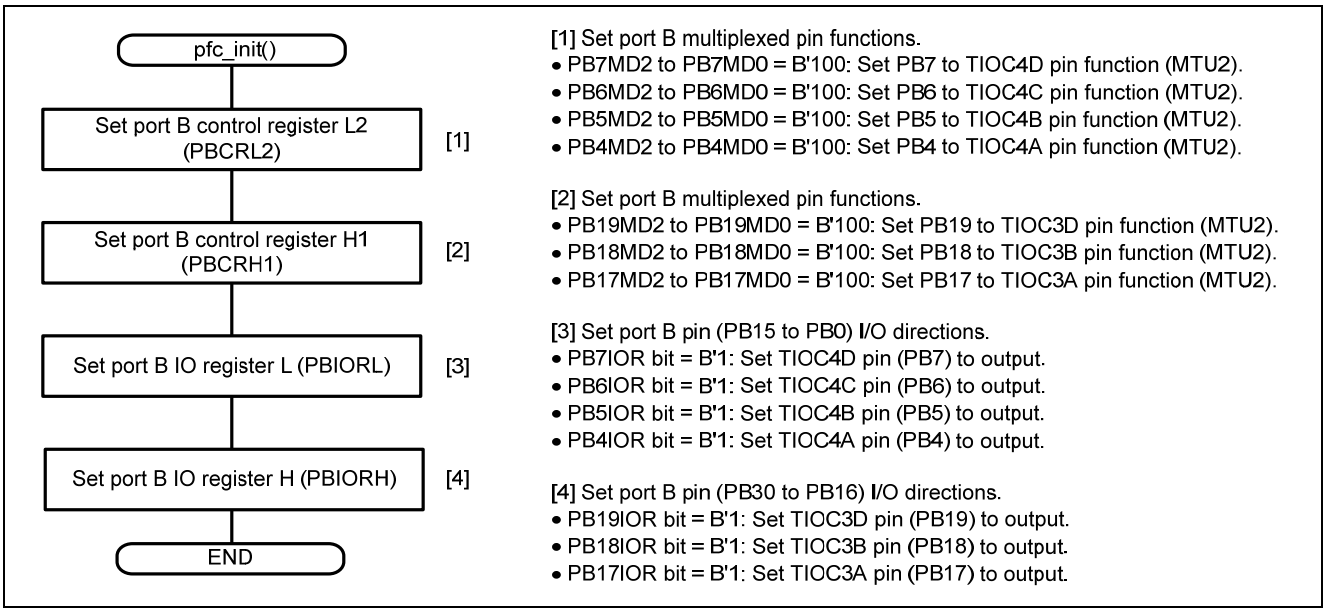


**Figure 14 Initialization of Pin Function Controller (PFC)**

### 2.4.5 Handling of the Compare Match Interrupt

Figure 15 shows the flow for handling the compare match interrupt (TGRA_3) from MTU2.

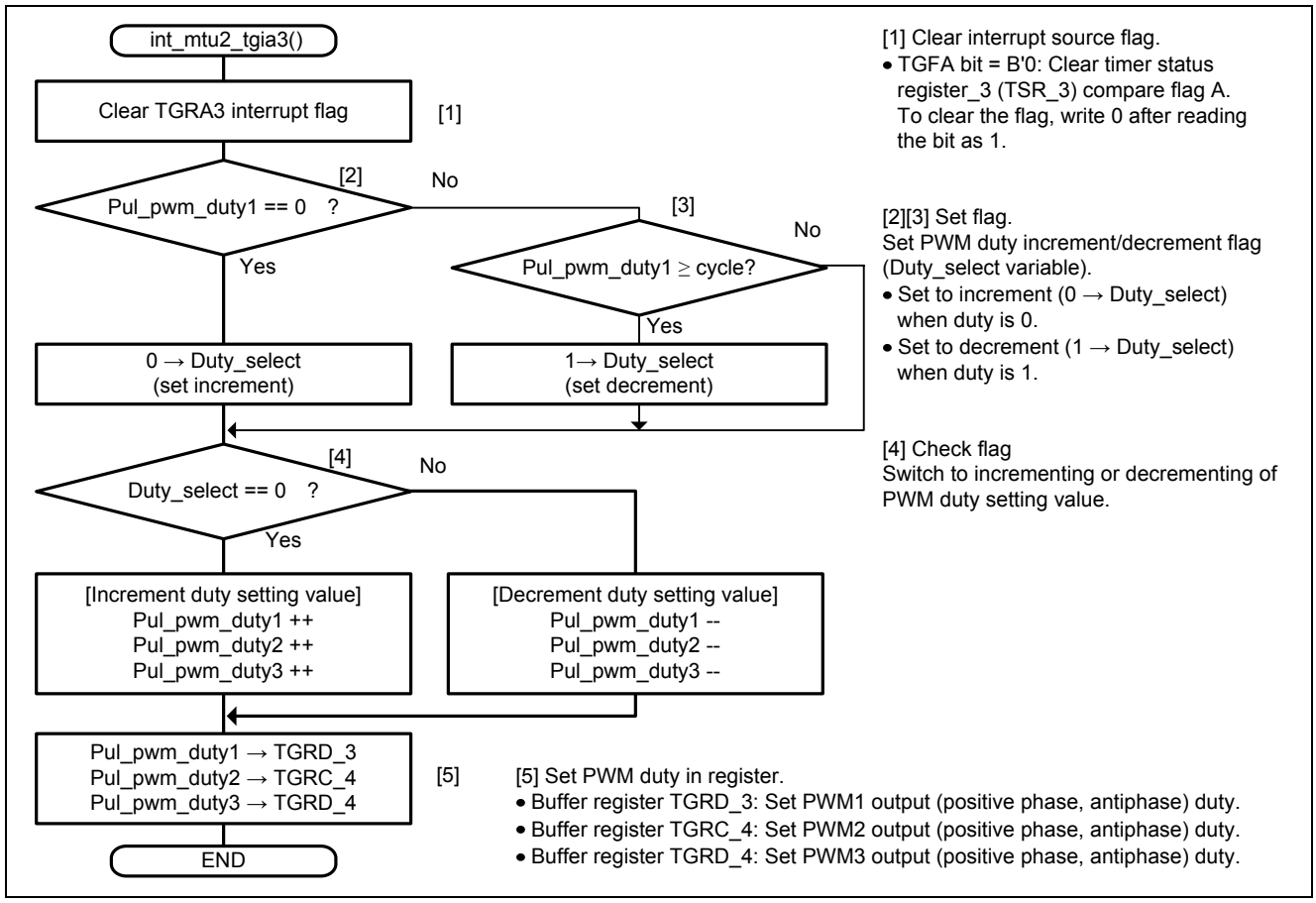


**Figure 15 Interrupt Handling**

## 2.5 Settings of Registers in the Sample Program

The following describes the settings of registers used in the sample program.

### 2.5.1 Clock Pulse Generator (CPG)

Table 6 gives a list of settings for registers of the clock pulse generator (CPG).

**Table 6 Clock Pulse Generator (CPG)**

| Register Name | Address | Setting | Description |
|---|---|---|---|
| Frequency control register (FRQCR) | H'FFFE0010 | H'1303 | Specifies the clock output settings and operating frequency multiplication ratios.<br>• CKOEN = B'1: Fix CK pin low level.<br>• STC1 and STC0 = B'11: PLL circuit 1 × 2<br>• IFC2 to IFC0 = B'000: Internal clock (Iϕ) × 1<br>• RNGS = B'0: High-frequency mode<br>• PFC2 to PFC0 = B'011: Peripheral clock (Pϕ) × 1/4 |

### 2.5.2 Power-Down Mode

Table 7 shows the register settings for power down mode.

**Table 7 Power-Down Mode**

| Register Name | Address | Setting | Description |
|---|---|---|---|
| Standby control register 3 (STBCR3) | H'FFFE0408 | H'5E | Specifies the operation settings for individual modules.<br>• HIZ= B'0: Maintain pin state in software standby mode.<br>• MSTP36 = B'1: Stop clock supply to MTU2S.<br>• MSTP35 = B'0: Operate MTU2.<br>• MSTP34 = B'1: Stop clock supply to POE2.<br>• MSTP33 = B'1: Stop clock supply to IIC3.<br>• MSTP32 = B'1: Stop clock supply to ADC.<br>• MSTP31 = B'1: Stop clock supply to DAC.<br>• MSTP30 = B'0: Operate flash memory. |

### 2.5.3 Multi-Function Timer Pulse Unit 2 (MTU2)

Table 8 gives a list of settings for registers of multi-function timer pulse unit 2 (MTU2).

**Table 8 Multi-Function Timer Pulse Unit 2 (MTU2)**

| Register Name | Address | Value | Description |
|---|---|---|---|
| Timer control register_3 (TCR_3) | H'FFFE4200 | H'01 | TCNT control settings<br>• CCLR2 to CCLR0 = B'000: Disable clearing of TCNT.<br>• CKEG1 and CKEG0 = B'00: Count at rising edge.<br>• TPSC2 to TPSC0 = B'001: TCNT counts using internal clock Pϕ / 4. |
| Timer control register_4 (TCR_4) | H'FFFE4201 | H'01 | TCNT control settings<br>• CCLR2 to CCLR0 = B'000: Disable clearing of TCNT.<br>• CKEG1 and CKEG0 = B'00: Count at rising edge.<br>• TPSC2 to TPSC0 = B'001: TCNT counts using internal clock Pϕ / 4. |
| Timer counter_3 (TCNT_3) | H'FFFE4210 | D'40 | 16 bit counter<br>In complementary PWM mode, set the initial value to match the setting value of the timer dead time data register (TDDR). |
| Timer counter_4 (TCNT_4) | H'FFFE4212 | H'0000 | 16 bit counter<br>Set the initial value to H'0000. |
| Timer general register A_3 (TGRA_3) | H'FFFE4218 | D'2040 | In complementary PWM mode, set the TCNT_3 upper limit to a value of (1/2 carrier cycle + dead time). |
| Timer general register C_3 (TGRC_3) | H'FFFE4224 | | In complementary PWM mode, set the initial value of the TGRA_3 buffer register to match the setting value of the TGRA_3 register. |
| Timer general register B_3 (TGRB_3) | H'FFFE421A | D'1020 | In complementary PWM mode, set the PWM output 1 compare register PWM duty (initial output value). |
| Timer general register D_3 (TGRD_3) | H'FFFE4226 | | In complementary PWM mode, set the initial value of the TGRB_3 buffer register to match the setting value of the TGRB_3 register. New PWM duty values are set in this register. |
| Timer general register A_4 (TGRA_4) | H'FFFE421C | D'1020 | In complementary PWM mode, set the PWM output 2 compare register PWM duty (initial output value). |
| Timer general register C_4 (TGRC_4) | H'FFFE4228 | | In complementary PWM mode, set the initial value of the TGRA_4 buffer register to match the setting value of the TGRA_4 register. New PWM duty values are set in this register. |
| Timer general register B_4 (TGRB_4) | H'FFFE421E | D'1020 | In complementary PWM mode, set the PWM output 3 compare register PWM duty (initial output value). |

| Register Name | Address | Value | Description |
|---|---|---|---|
| Timer general register D_4 (TGRD_4) | H'FFFE422A | D'1020 | In complementary PWM mode, set the initial value of the TGRB_4 buffer register to match the setting value of the TGRB_4 register. New PWM duty values are set in this register. |
| Timer dead time data register (TDDR) | H'FFFE4216 | D'40 | This 16-bit register is only used in complementary PWM mode. Set the offset value (dead time value) for TCNT_4 and TCNT_3. |
| Timer cycle data register (TCDR) | H'FFFE4214 | D'2000 | This register is only used in complementary PWM mode. Set the TCNT_4 upper limit value (1/2 the carrier cycle). |
| Timer cycle buffer register (TCBR) | H'FFFE4222 | | This register is only used in complementary PWM mode. It functions as the buffer register for the TCDR register. Set the same value as that for the TCDR register. |
| Timer output control register 1 (TOCR1) | H'FFFE420E | H'40 | Complementary PWM mode output operation settings<br>• PSYE = B'1: Enable toggle output synchronized with the PWM cycle.<br>• TOCL = B'0: Enable writing to the TOCS, OLSN, and OLSP bits.<br>• TOCS = B'0: Enable TOCR1 setting.<br>• OLSN = B'0: In complementary PWM mode, select the antiphase output level: Initial output = high, active level = low.<br>• OLSP = B'0: In complementary PWM mode, select the positive phase output level: Initial output = high, active level = low. |
| Timer mode register_3 (TMDR_3) | H'FFFE4202 | H'3F | Sets the operation mode (channel 3).<br>• BFB = B'1: Set TGRB and TGRD to buffer operation.<br>• BFA = B'1: Set TGRA and TGRC to buffer operation.<br>• MD3 to MD0 = B'1111: Complementary PWM mode 3 (transfer at peak and trough) |
| Timer mode register_4 (TMDR_4) | H'FFFE4203 | - | Sets the operation mode (channel 4).<br>When channel 3 is set to complementary PWM mode, the settings for channel 4 are ignored and the settings for channel 3 are followed automatically. There is no need to make setting to this register. Leave the initial values unchanged. |

| Register Name | Address | Value | Description |
|---|---|---|---|
| Timer output master enable register (TOER) | H'FFFE420A | H'FF | Specifies the output settings for the MTU2 output pins.<br>• OE4D = B'1: Enable MTU2 output on TIOC4D pin.<br>• OE4C = B'1: Enable MTU2 output on TIOC4C pin.<br>• OE3D = B'1: Enable MTU2 output on TIOC3D pin.<br>• OE4B = B'1: Enable MTU2 output on TIOC4B pin.<br>• OE4A = B'1: Enable MTU2 output on TIOC4A pin.<br>• OE3B = B'1: Enable MTU2 output on TIOC3B pin. |
| Timer interrupt enable register_3 (TIER_3) | H'FFFE4208 | H'01 | Enables or disables interrupt requests.<br>• TGIEA= B'1: Enable interrupt requests (TGIA) by TGFA bit. |
| Timer start register (TSTR) | H'FFFE4280 | H'C0 | Starts or stops TCNT operation for channels 0 to 4.<br>• CST4 = B'1: Start TCNT_4 count operation.<br>• CST3 = B'1: Start TCNT_3 count operation.<br>Stop count operation by TCNT_2, TCNT_1, and TCNT_0. Make counter operation bit settings for TCNT_4 and TCNT_3 at the same time. |

### 2.5.4 Interrupt Controller (INTC)

Table 9 gives a list of settings for registers of the interrupt controller (INTC).

**Table 9 Interrupt Controller (INTC)**

| Register Name | Address | Setting | Description |
|---|---|---|---|
| Interrupt priority level setting register 10 (IPR10) | H'FFFE0C08 | H'00F0 | Sets interrupt priority levels (level 0 to 15).<br>• Bits 15 to 12 = B'0000: MTU2 (TGI2A and TGI2B) interrupt level = 0<br>• Bits 11 to 8 = B'0000: MTU2 (TCI2V and TCI2U) interrupt level = 0<br>• Bits 7 to 4 = B'1111: MTU3 (TGI3A to TGI3D) interrupt level = 15<br>• Bits 3 to 0 = B'0000: MTU3 (TCI3V) interrupt level = 0<br>The TGI3A interrupt is used by the reference program. |

### 2.5.5 Pin Function Controller (PFC)

Table 10 gives a list of settings for registers of the pin function controller (PFC).

**Table 10 Pin Function Controller (PFC)**

| Register Name | Address | Setting | Description |
|---|---|---|---|
| Port B control register L2 (PBCRL2) | H'FFFE3894 | H'4444 | Sets port B multiplexed pin functions.<br>• PB7MD2 to PB7MD0 = B'100: Set PB7 to TIOC4D I/O (MTU2).<br>• PB6MD2 to PB6MD0 = B'100: Set PB6 to TIOC4C I/O (MTU2).<br>• PB5MD2 to PB5MD0 = B'100: Set PB5 to TIOC4B I/O (MTU2).<br>• PB4MD2 to PB4MD0 = B'100: Set PB4 to TIOC4A I/O (MTU2). |
| Port B control register H1 (PBCRH1) | H'FFFE388E | H'4440 | Sets port B multiplexed pin functions.<br>• PB19MD2 to PB19MD0 = B'100: Set PB19 to TIOC3D I/O (MTU2).<br>• PB18MD2 to PB18MD0 = B'100: Set PB18 to TIOC3C I/O (MTU2).<br>• PB17MD2 to PB17MD0 = B'100: Set PB17 to TIOC3B I/O (MTU2).<br>• PB16MD2 to PB16MD0 = B'000: Set PB16 to TIOC3A I/O (MTU2). |
| Port B I/O register H (PBIORH) | H'FFFE3884 | H'000E | Sets port B pin I/O directions.<br>• PB19IOR = B'1: Set PB19 (TIOC3D) as an output pin.<br>• PB18IOR = B'1: Set PB18 (TIOC3B) as an output pin.<br>• PB17IOR = B'1: Set PB17 (TIOC3A) as an output pin.<br>• PB16IOR = B'0: Set PB16 (port) as an input pin.<br>Set all the others to B'0: All input pins. |
| Port B I/O register L (PBIORL) | H'FFFE3886 | H'00F0 | Sets port B pin I/O directions.<br>• PB7IOR = B'1: Set PB7 (TIOC4D) as an output pin.<br>• PB6IOR = B'1: Set PB6 (TIOC4C) as an output pin.<br>• PB5IOR = B'1: Set PB5 (TIOC4B) as an output pin.<br>• PB4IOR = B'1: Set PB4 (TIOC4A) as an output pin.<br>Set all the others to B'0: All input pins. |

## 3. Documents for Reference

- Hardware Manual
  SH7211 Group Hardware Manual [RJJ09B0338]
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Software Manual
  SH-2A/SH2A-FPU Software Manual [RJJ09B0086]
  (The latest version can be downloaded from the Renesas Technology Web site.)

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