STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCTNAME BU7964GUW

FUNCTION Serial Interface for Mobile Devices Application

MSDL3(Mobile Shrink Data Link 3) Deserializer LSI

FEATURES
·Maximum transmission rate of highspeed differential interface MSDL3 is 1350Mbps.
·Support LCD interface with 24bit parallel RGB video mode.
·Pixel clock frequency is 4~45MHz

1. Absolute maximum

Parameter	Symbol	Rated values	Unit	Remarks
Power supply voltage for DVDD	DVDD	-0.3 ~ +2.5	V	
Power supply voltage for MSVDD	MSVDD	-0.3 ~ +2.5	V	
Input voltage	VIN	-0.3 ~ DVDD+0.3	V	I/O terminals of IOVDD line
		-0.3 ~ MSVDD+0.3	V	I/O terminals of MSVDD line
Input current	IIN	-10 ~ +10	mA	
Package power dissipation	Pd	300 *	mW	Without board mounted
Preservation temperature	Tstg	-55 ~ +125	°C	

*When it uses by Ta=25°C or higher, reduce by 3.0 mW/°C (for a single package).

2. Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Supply voltage for DVDD	VDVDD	1.65	1.80	1.95	V	VDVDD=VMSVDD
Supply voltage for MSVDD	VMSVDD	1.65	1.80	1.95	V	
SubLVDS data rate	DR	120	-	450	Mbps/ch	
Operating temperature range	Topr	-30	25	+85	°C	

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3. ELECTRICAL CHARACTERISTICS

3.1 CMOS INOUT CHARACTERISTICS

Ta=25℃, DVDD=MSVDD=1.80V, DGND=MSGND=0.00V, unless otherwise noted

Parameter	Symbol	Min	Typ	Max	Unit	Conditions	
'L' input voltage1	VIL1	DGND	-	0.3×DVDD	V	XSD, PLL_BW[1:0], LS[1:0], F_XS terminals	
'H' input voltage1	VIH1	0.7×DVDD	-	DVDD	V		
'L' output voltage1	VOL1	DGND	-	0.3×DVDD	V	IO=1mA	F_XS=L, PCLK,CPO, PD[26:0] terminals
'H' output voltage1	VOH1	0.7×DVDD	-	DVDD	V	IO=-1mA	
'L' output voltage2	VOL2	DGND	-	0.3×DVDD	V	IO=3mA	F_XS=H, PCLK,CPO, PD[26:0] terminals
'H' output voltage2	VOH2	0.7×DVDD	-	DVDD	V	IO=-3mA	
'L' output voltage3	VOL3	DGND	-	0.15×DVDD	V	IO=100uA	PCLK,CPO, PD[26:0] terminals
'H' output voltage3	VOH3	0.85×DVDD	-	DVDD	V	IO=-100uA	
PCLK frequency1	fPCLK1	4.0	-	15.0	MHz	LS[1:0]=LL	PCLK terminals
PCLK frequency2	fPCLK2	8.0	-	30.0	MHz	LS[1:0]=LH	
PCLK frequency3	fPCLK3	12.0	-	45.0	MHz	LS[1:0]=HL	
PCLK duty cycle	DPCLKO	45	50	55	%	PCLK terminals, CL=10pF	
Data setup to PCLK	tDSO	9.0	-	-	ns	PD[26:0] terminals, CL=10pF	
Data hold to PCLK	tDHO	9.0	-	-	ns		

3.2 MSDL3 RX CHARACTERISTICS

Ta=25℃, DVDD=MSVDD=1.80V, DGND=MSGND=0.00V, unless otherwise noted

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Differential voltage range	Vdiff_rx	70	100	200	mVpp	
Common mode voltage range	Vcm_rx	0.6	0.9	1.2	V	
RX pull down current	Ipull_rx	12	30	90	μA	
Threshold voltage of RX link detection	Vlink_rx	0.2	0.3	0.4	V	
SubLVDS data rate	DR_rx	120	-	450	Mbps/ch	

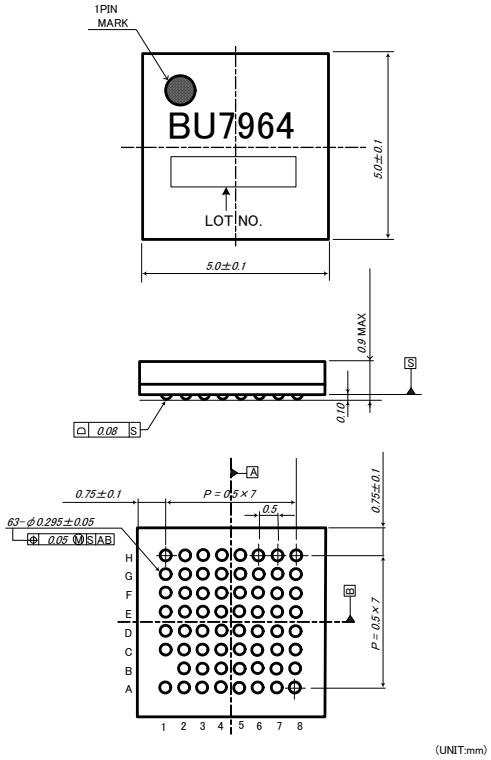
3.3 CURRENT COMSUMPTION

Ta=25℃, DVDD=MSVDD=1.80V, DGND=MSGND=0.00V, unless otherwise noted

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Shutdown current	Iop_sht_ r x	-	0.2	10.0	μA	XSD=L
Standby current	Iop_stb_ r x	-	41.8	90.0	μA	XSD=H
Active current of 1ch27bit format	Iop_act_ r x1	-	17.6	24.0	mA	LS[1:0]=LL, PLL_BW[1:0]=HL, fPCLK=15MHz, CL=10pF, *1
Active current of 2ch27bit format	Iop_act_ r x2	-	28.0	36.8	mA	LS[1:0]=LH, PLL_BW[1:0]=HL, fPCLK=30MHz, CL=10pF, *1
Active current of 3ch27bit format	Iop_act_ r x3	-	36.0	48.6	mA	LS[1:0]=HL, PLL_BW[1:0]=HL, fPCLK=45MHz, CL=10pF, *1

*1 : Total operating current(IDVDD+IMSVDD) with PD[26:0] outputs toggling 0x2AAAAAA and 0x5555555.

4. PACKAGE VIEW

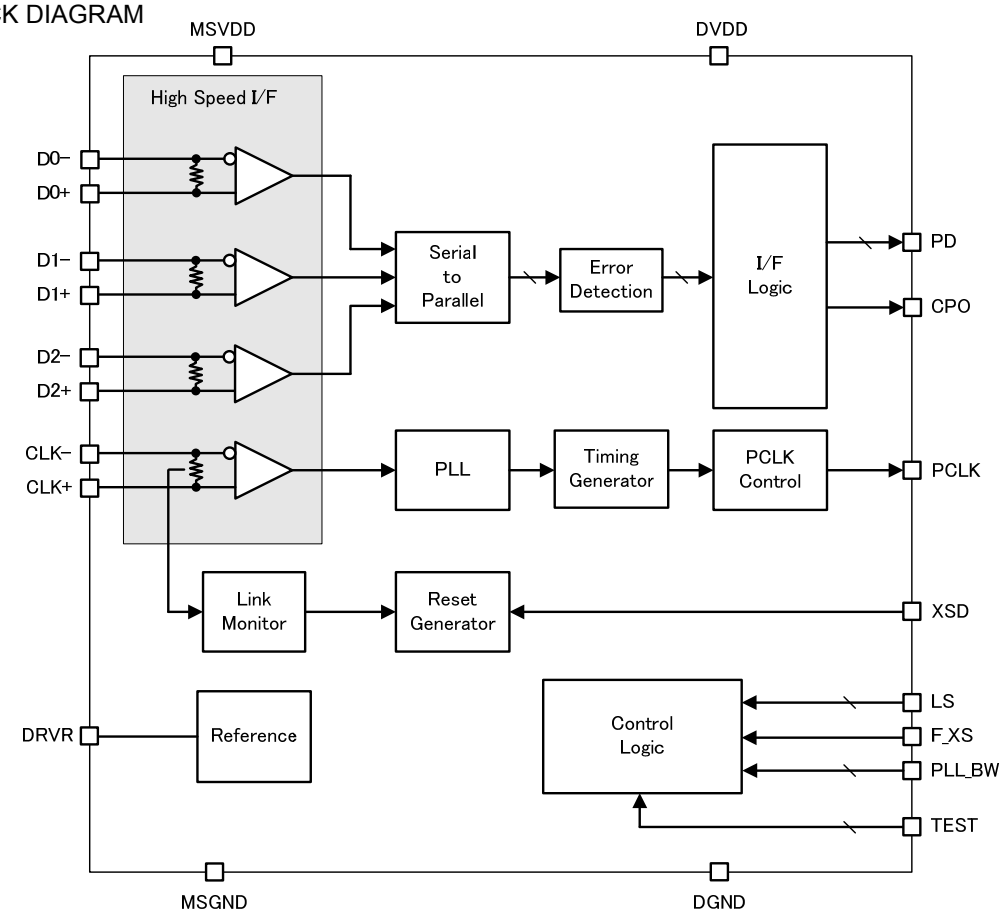


VBGA063W050

5. PIN LIST

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
A1	TEST0	D1	PD23	G1	LS1
A2	PD19	D2	PD21	G2	PLL_BW1
A3	PD17	D3	N. C.	G3	D2−
A4	PD16	D4	DGND	G4	D1−
A5	PD14	D5	DGND	G5	CLK−
A6	PD13	D6	DVDD	G6	D0−
A7	PD10	D7	PD4	G7	N. C.
A8	CPO	D8	PD5	G8	PD0
B1		E1	PD25	H1	N. C.
B2	PCLK	E2	PD24	H2	N. C.
B3	PD18	E3	DVDD	H3	D2+
B4	PD15	E4	DGND	H4	D1+
B5	PD12	E5	MSGND	H5	CLK+
B6	PD11	E6	N. C.	H6	D0+
B7	PD9	E7	PD1	H7	DRVR
B8	PD8	E8	PD3	H8	TEST1
C1	PD22	F1	PD26		
C2	PD20	F2	LS0		
C3	PLL_BW0	F3	MSVDD		
C4	DVDD	F4	MSGND		
C5	N. C.	F5	MSVDD		
C6	F_XS	F6	N. C.		
C7	PD7	F7	XSD		
C8	PD6	F8	PD2		

6. SYSTEM BLOCK DIAGRAM



7. USAGE PRECAUTIONS

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operatingconditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals

In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

(13) Rush current at power supply turning on

Because the rush current might flow momentarily in CMOS IC when internal logic is irregular at the power supply Note the capacity of the power supply coupling, the power supply, and width and drawing the GND pattern wiring.

(14) Rush current of the order of turning on the power supply

Because the rush current might flow momentarily by the order of turning on the power supply and the delay in IC with two or more power supplies Note the capacity of the power supply coupling, the power supply, and width and drawing the GND pattern wiring.

Notes

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