Delta Sheet

XC164CM-8FF to XC164CS

16bit

Microcontrollers

Never stop thinking.

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XC164CM

16-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

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Revision History:	**2004-03**	V1.0D3
Previous Version:	2003-02	V1.0D2

Page	**Subjects (major changes since last revision)**
	This document has the status draft. All changes to previous version are marked with change bars. Only major changes are listed below. Especially formal changes and typos are not listed.
3-4	**Setting reset configurations**: depending on the mode now 2-4 pins are used to select a reset configuration. Pin P1H5 is additionally used for setting reset configurations. All configuration pins have an integrated pull up. No integrated pull down any more. The configuration is latched with the rising edge of RSTIN. Please read pages 3 to 4 carefully.
8	There was a line mismatch in the table of Port3.

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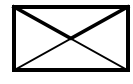

1 Delta Sheet XC164CM-8FF to XC164CS-16FF

1.1 Blockdiagram XC164CM-8F

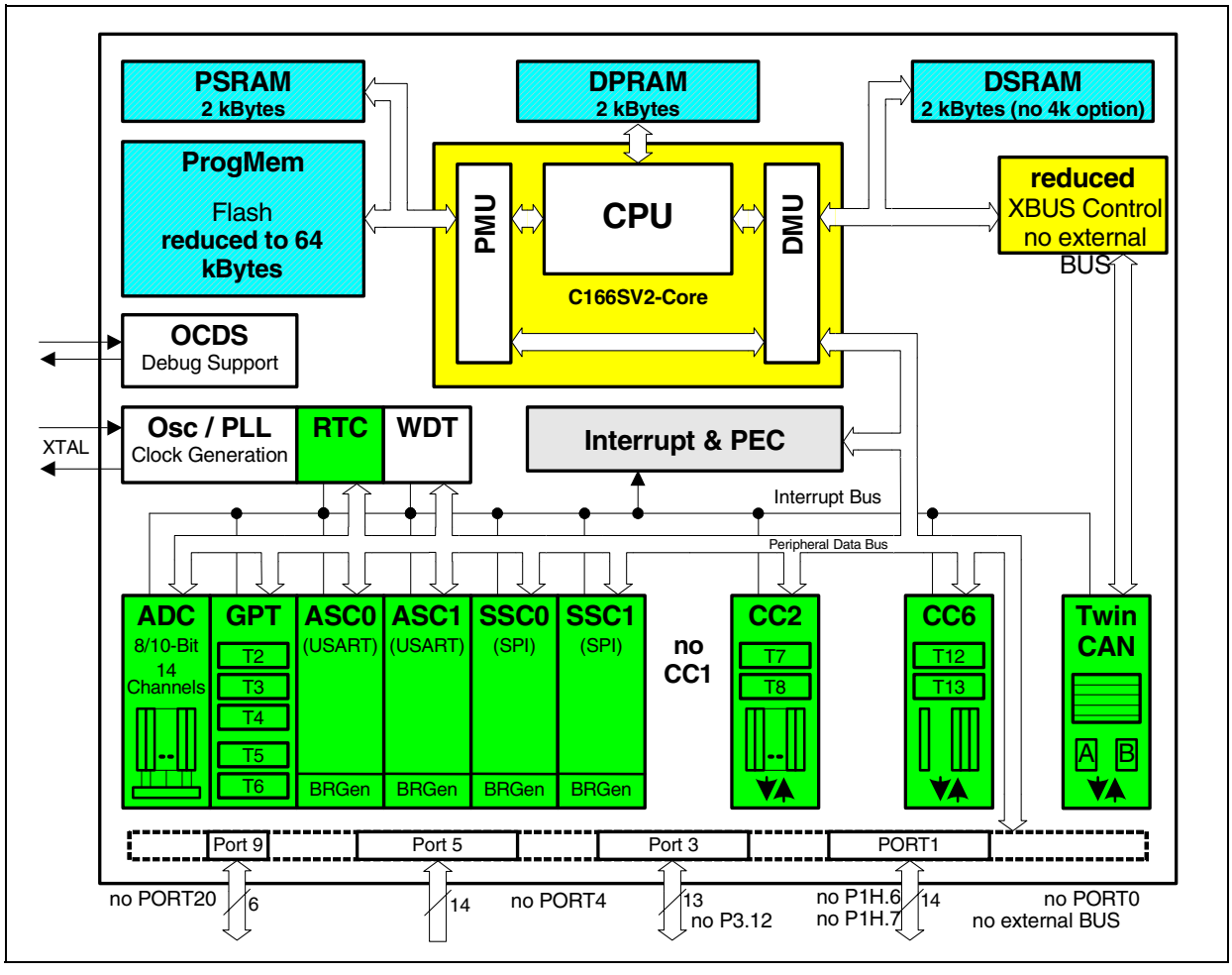

Figure 1 Blockdiagram XC164CM-8FF with deltas to XC164CS-16FF

1.2 Delta Feature Table XC164CS-16FF to XC164CM-8FF

Table 1 List of feature differences

Feature	XC164CS-16FF	intermediate EES	XC164CM-8FF
Program Flash Memory	128kB C00000-C1FFFF	128kB C00000-C1FFFF	64kB C00000-C0FFFF
Program SRAM	2kB E00000-E07FFF	2kB E00000-E07FFF	2kB E00000-E07FFF
Data SRAM	2kB (4kB option) 00C000-00C7FF	4kB 00C000-00CFFF	2kB 00C000-00C7FF

Table 1 List of feature differences

Feature	XC164CS-16FF	intermediate EES	XC164CM-8FF
Package	TQFP100	TQFP64	TQFP64
CAPCOM1	on chip available, no IOs, for interrupt generation only	on chip available, no IOs, for interrupt generation only	no CAPCOM1 module on chip
CAPCOM2	fully available with all 16 channels, 12 IOs CC16-27IO, Double-register-compare on 8 channels	fully available with all 16 channels, 10 IOs CC16-25IO, Double-register-compare on 8 channels	fully available with all 16 channels, 10 IOs CC16-25IO, Double-register-compare on 8 channels
CAN	IO pins on port 9 or 4 alternatively	IO pins on port9 only	IO pins on port9 only
External BUS	available	not available, single chip mode only	not available, single chip mode only
Port0	P0L.0-7, P0H0-7	no Port0 pins, no reset configuration with port0 functions possible	no Port0 pins, reset configurations via P9, P1 and $\overline{\text{TRST}}$
Port1	P1L.0-7, P1H0-7	P1L.0-7, P1H0-**5,** no P1H6-7, no external bus functions	P1L.0-7, P1H0-**5,** no P1H6-7, no external bus functions
Port3	P3.1-13, P3.15	P3.1-11, P3.13, P3.15, no pin P3.12	P3.1-11, P3.13, P3.15, no pin P3.12
Port4	P4.0-7	no Port 4 pins	no Port 4 pins
Port5	P5.0-7, P5.10-15	all pins available, no changes on Port5	all pins available, no changes on Port5
Port20	P20.0-5, P20.12	no Port 20 pins, reset configurations via P9 possible	no Port 20 pins, reset configurations via P9, P1 and $\overline{\text{TRST}}$
TRST	enables JTAG	enables JTAG	enables JTAG and configuration pins sensing during reset

Table 2 List of differences in setting configuration modes during reset

Feature	XC164CS-16FF	intermediate EES	XC164CM-8FF
integrated pull up (PU) /down (PD) during reset	$\overline{EA}$ PU, $\overline{RD}$ PU, ALE PD	P9.5 PU, P9.4 PD	P1H5 PU, P1H4 PU P9.5 PU, P9.4 PU
Standard start from internal memory at C00000	$\overline{EA}$=1,$\overline{RD}$=1,ALE=0 default	P9.5=1, P9.4=0 ($\overline{EA}$ is always 1) default	$\overline{TRST}$=**1**[1)] P1H5=x, P1H4=x P9.5 =1, P9.4=1 default
Bootstrap loader ASC	$\overline{EA}$=1,$\overline{RD}$=**0**, ALE=0 $\overline{EA}$=0, P0.5-2=1011	P9.5=**0**, P9.4=0 ($\overline{EA}$ is always 1)	$\overline{TRST}$ = **1** P1H5=x, P1H4=x P9.5=**0,** P9.4=1
Bootstrap loader CAN	$\overline{EA}$=1,$\overline{RD}$=**0**,ALE=**1** $\overline{EA}$=0, P0.5-2=1001	P9.5=**0**, P9.4=**1** ($\overline{EA}$ is always 1)	$\overline{TRST}$ = **1** P1H5=x, P1H4=1 P9.5=1**,** P9.4=**0**
Adapt mode	$\overline{EA}$=**0** P0.1=**0**	not possible	$\overline{TRST}$ = **1** P1H5=1, P1H4=1 P9.5=**0,** P9.4=**0**
Alternate start internal from C10000	$\overline{EA}$=1,$\overline{RD}$=1,ALE=**1**	P9.5=1, P9.4=**1** ($\overline{EA}$ is always 1)	not supported

1) In XC164CM this mode is used for start from internal memory at C00000 in conjunction with OCDS. Standard start from internal memory at C00000 is always performed if $\overline{TRST}$=0 during reset.

Note: Bold means: to be set with external pull resistor.

1.3 Bootstrap Loader, Adapt Mode, and Test Mode Settings XC164CM

All system start up configurations are locked or enabled by $\overline{\text{TRST}}$. If pin $\overline{\text{TRST}}$ is pulled low for all the time, then OCDS (including JTAG) and all non standard system start up configurations are always disabled.
For all applications it is recommended to have $\overline{\text{TRST}}$ pulled low for normal operation.

1.3.1 Enabling Non Standard System Start Up Configurations

If at the end of reset pin $\overline{\text{TRST}}$ is getting high, then pins P1H.5 (pin 6), P1H.4 (5), P9.5 (48), and P9.4 (47) are used to select one of the non standard system start up configurations. This setting is latched with the rising edge of $\overline{\text{RSTIN}}$.

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Table 3 Mode Selection Overview

P1H.5	P1H.4	P9.5	P9.4	**Selected Mode**
x	x	1	1	Start internal: default setting, internal start from address C00000 . To be used for internal start from C00000 with OCDS debuggers (0011, 0111, 1011, 1111)
x	x	0	1	BSL-ASC: Bootstrap loader ASC
x	1	1	0	BSL-CAN: Bootstrap loader CAN
1	1	0	0	Adapt Mode: all pins are tristate used for connecting an incircuit emulator
0	0	0	0	Test modes do not use any of these settings. In order to avoid such settings do not pull down P1H4 or P1H5 during reset and $\overline{\text{TRST}}$=1
0	0	1	0	
0	1	0	0	
1	0	0	0	
1	0	1	0	

1.3.2 Enabling Normal Operation

If at the end of reset $\overline{\text{TRST}}$ is low, then always the default system start up configuration is selected and the configuration 1111 is latched. Code execution is starting from address C0 0000. For safety aspects keep $\overline{\text{TRST}}$ low for normal operation.

1.3.3 Enabling OCDS During Normal Operation

If only $\overline{\text{TRST}}$ is getting high while $\overline{\text{RSTIN}}$ remains low, then the microcontroller does not perform a reset but the JTAG interface is getting enabled.

1.4 Pin Configuration and Definition

The pins of the XC164CM are described in detail in **Table 4**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package. E*) and C*) mark pins to be used as alternate external interrupt inputs, C*) marks pins that can have CAN interface lines assigned to them.

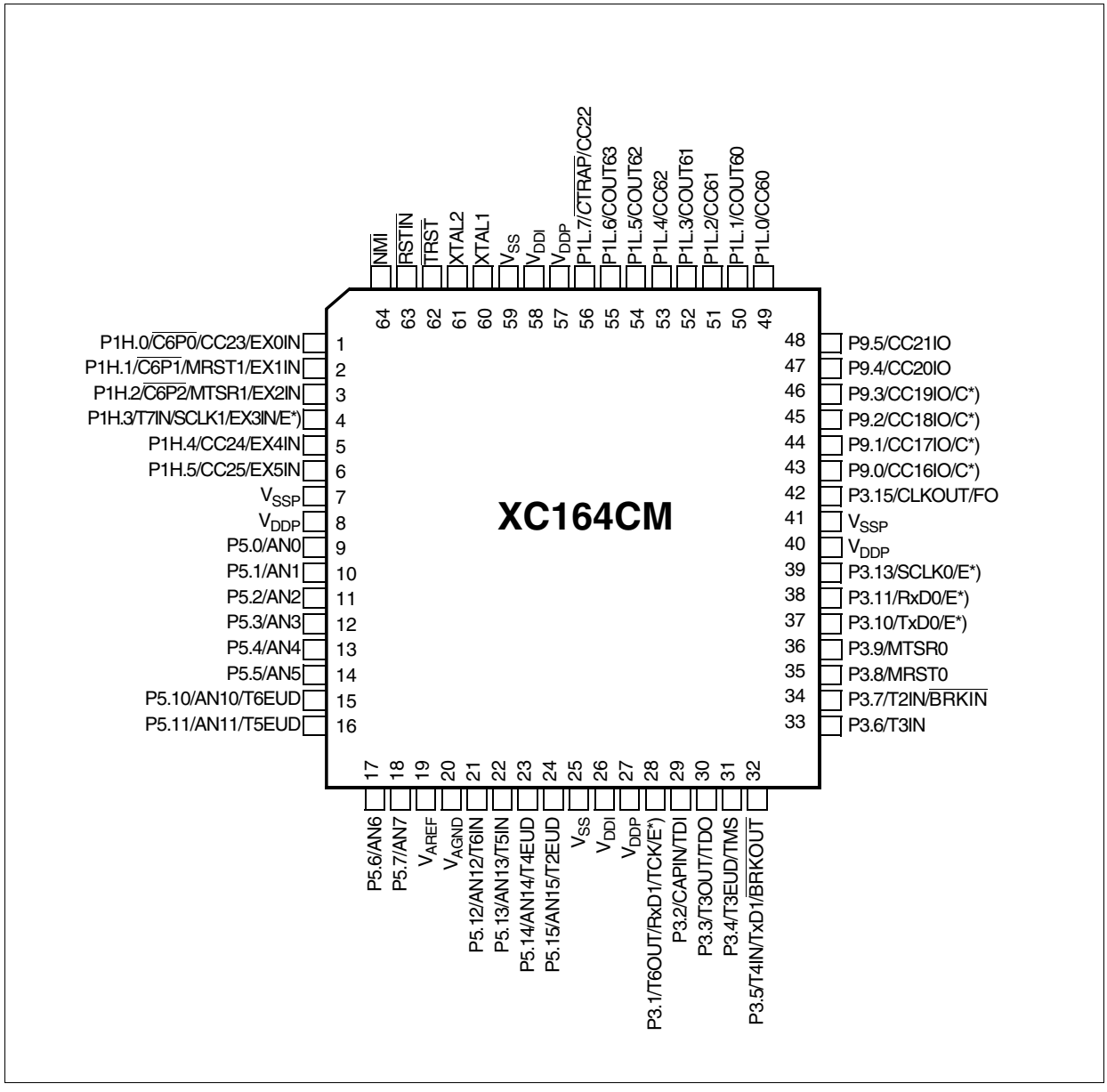

Figure 2 Pin Configuration (top view)

Table 4 Pin Definitions and Functions

Symbol	Pin Num.	Input Outp.	Function
$\overline{\text{RSTIN}}$	63	I	Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the XC164CM. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. *Note: The reset duration must be sufficient to let the hardware configuration signals settle. External circuitry must guarantee low level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached the operating range.*
$\overline{\text{NMI}}$	64	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the XC164CM into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.
P9	43-48	IO	Port 9 is a 6-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 9 is selectable (standard or special). The following Port 9 pins also serve for alternate functions:[1)]
P9.0	43	I/O	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp.,
		I	CAN2_RxD CAN Node 2 Receive Data Input,
		I	EX7IN Fast External Interrupt 7 Input (alternate pin B)
P9.1	44	I/O	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp.,
		O	CAN2_TxD CAN Node 2 Transmit Data Output,
		I	EX6IN Fast External Interrupt 6 Input (alternate pin B)
P9.2	45	I/O	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp.,
		I	CAN1_RxD CAN Node 1 Receive Data Input,
		I	EX7IN Fast External Interrupt 7 Input (alternate pin A)
P9.3	46	I/O	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp.,
		O	CAN1_TxD CAN Node 1 Transmit Data Output,
		I	EX6IN Fast External Interrupt 6 Input (alternate pin A)
P9.4	47	I/O	CC20IO CAPCOM2: CC20 Capture Inp./Compare Outp.[2)]
P9.5	48	I/O	CC21IO CAPCOM2: CC21 Capture Inp./Compare Outp.[2)]

Table 4 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function	
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. Each pin can be programmed for input (output driver in high-impedance state) or output. The PORT1 pins serve for the following functions:	
P1L.0	49	I/O	CC60	CAPCOM6: Input / Output of Channel 0
P1L.1	50	O	COUT60	CAPCOM6: Output of Channel 0
P1L.2	51	I/O	CC61	CAPCOM6: Input / Output of Channel 1
P1L.3	52	O	COUT61	CAPCOM6: Output of Channel 1
P1L.4	53	I/O	CC62	CAPCOM6: Input / Output of Channel 2
P1L.5	54	O	COUT62	CAPCOM6: Output of Channel 2
P1L.6	55	O	COUT63	Output of 10-bit Compare Channel
P1L.7	56	I	$\overline{\text{CTRAP}}$	CAPCOM6: Trap Input
			$\overline{\text{CTRAP}}$ is an input pin with an internal pullup resistor. A low level on this pin switches the CAPCOM6 compare outputs to the logic level defined by software (if enabled).	
		I/O	$\overline{\text{CC22IO}}$	CAPCOM2: CC22 Capture Inp./Compare Outp.
P1H.0	1	I	$\overline{\text{CC6POS0}}$	CAPCOM6: Position 0 Input,
		I	EX0IN	Fast External Interrupt 0 Input (default pin),
		I/O	$\overline{\text{CC23IO}}$	CAPCOM2: CC23 Capture Inp./Compare Outp.
P1H.1	2	I	$\overline{\text{CC6POS1}}$	CAPCOM6: Position 1 Input,
		I	EX1IN	Fast External Interrupt 1 Input (default pin),
		I/O	$\overline{\text{MRST1}}$	SSC1 Master-Receive/Slave-Transmit In/Out.
P1H.2	3	I	$\overline{\text{CC6POS2}}$	CAPCOM6: Position 2 Input,
		I	EX2IN	Fast External Interrupt 2 Input (default pin),
		I/O	MTSR1	SSC1 Master-Transmit/Slave-Receive Out/Inp.
P1H.3	4	I	T7IN	CAPCOM2: Timer T7 Count Input,
		I/O	SCLK1	SSC1 Master Clock Output / Slave Clock Input,
		I	EX3IN	Fast External Interrupt 3 Input (default pin),
P1H.4	5	I/O	CC24IO	CAPCOM2: CC24 Capture Inp./Compare Outp.,
		I	EX4IN	Fast External Interrupt 4 Input (default pin)[2)]
P1H.5	6	I/O	CC25IO	CAPCOM2: CC25 Capture Inp./Compare Outp.,
		I	EX5IN	Fast External Interrupt 5 Input (default pin)[2)]
XTAL2	61	O	XTAL2:	Output of the oscillator amplifier circuit
XTAL1	60	I	XTAL1:	Input to the oscillator amplifier and input to the internal clock generator
			To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.	

Table 4 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function	
P3		IO	Port 3 is a 13-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 3 is selectable (standard or special). The following Port 3 pins also serve for alternate functions:	
P3.1	28	O	T6OUT	GPT2 Timer T6 Toggle Latch Output,
		I/O	RxD1	ASC1 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX1IN	Fast External Interrupt 1 Input (alternate pin A),
		I	TCK	Debug System: JTAG Clock Input
P3.2	29	I	CAPIN	GPT2 Register CAPREL Capture Input,
		I	TDI	Debug System: JTAG Data In
P3.3	30	O	T3OUT	GPT1 Timer T3 Toggle Latch Output,
		O	TDO	Debug System: JTAG Data Out
P3.4	31	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input,
		I	TMS	Debug System: JTAG Test Mode Selection
P3.5	32	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp
		O	TxD1	ASC1 Clock/Data Output (Async./Sync.),
		O	$\overline{\text{BRKOUT}}$	Debug System: Break Out
P3.6	33	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	34	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp
		I	$\overline{\text{BRKIN}}$	Debug System: Break In
P3.8	35	I/O	MRST0	SSC0 Master-Receive/Slave-Transmit In/Out.
P3.9	36	I/O	MTSR0	SSC0 Master-Transmit/Slave-Receive Out/In.
P3.10	37	O	TxD0	ASC0 Clock/Data Output (Async./Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin B)
P3.11	38	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin A)
P3.13	39	I/O	SCLK0	SSC0 Master Clock Output / Slave Clock Input.,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin A)
P3.15	42	O	CLKOUT	System Clock Output (=CPU Clock),
		O	FOUT	Programmable Frequency Output
$\overline{\text{TRST}}$	62	I	Test-System Reset Input. A high level at this pin activates the XC164CM's debug system and/or the non default configuration functions on ports 1 and 9. For normal system operation, pin $\overline{\text{TRST}}$ should be held low.	

Table 4 Pin Definitions and Functions (cont'd)

Symbol	Pin Num.	Input Outp.	Function
P5		I	Port 5 is a 14-bit input-only port. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	9	I	AN0
P5.1	10	I	AN1
P5.2	11	I	AN2
P5.3	12	I	AN3
P5.4	13	I	AN4
P5.5	14	I	AN5
P5.10	15	I	AN10, T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl. Inp.
P5.11	16	I	AN11, T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.6	17	I	AN6
P5.7	18	I	AN7
P5.12	21	I	AN12, T6IN GPT2 Timer T6 Count/Gate Input
P5.13	22	I	AN13, T5IN GPT2 Timer T5 Count/Gate Input
P5.14	23	I	AN14, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	24	I	AN15, T2EUD GPT1 Timer T2 Ext. Up/Down Ctrl. Inp.
V_{AREF}	19	-	Reference voltage for the A/D converter.
V_{AGND}	20	-	Reference ground for the A/D converter.
V_{DDI}	26, 58	-	Core Supply Voltage (On-Chip Modules): +2.5 V during normal operation and idle mode. Please refer to the **Operating Conditions**
V_{DDP}	8, 27, 40, 57	-	Pad Supply Voltage (Pin Output Drivers): +5 V during normal operation and idle mode. Please refer to the **Operating Conditions**
V_{SS}	7, 25, 41, 59	-	Ground. Connect decoupling capacitors to adjacent V_{DDx}/V_{SS} pin pairs as close as possible to the pins. All V_{SS} pins must be connected to the ground-line or ground-plane.

1) The CAN interface lines are assigned to port P9 under software control.

2) If at the end of an external reset $\overline{\text{TRST}}$ was high these pins are used for sensing configuration settings and integrated pull up devices are activated during reset.

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