

PROTECTION PRODUCTS - RailClamp®
Description

RailClamps are surge rated diode arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to data and transmission lines from overvoltage caused by **ESD** (electrostatic discharge), **CDE** (Cable Discharge Events), and **EFT** (electrical fast transients).

The unique design incorporates surge rated, low capacitance steering diodes and a TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. The internal TVS diode prevents over-voltage on the power line, protecting any downstream components.

The low capacitance array configuration allows the user to protect three high-speed data or transmission lines. The low inductance construction minimizes voltage overshoot during high current surges. This device is optimized for ESD protection of USB OTG and SIM interfaces. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Features

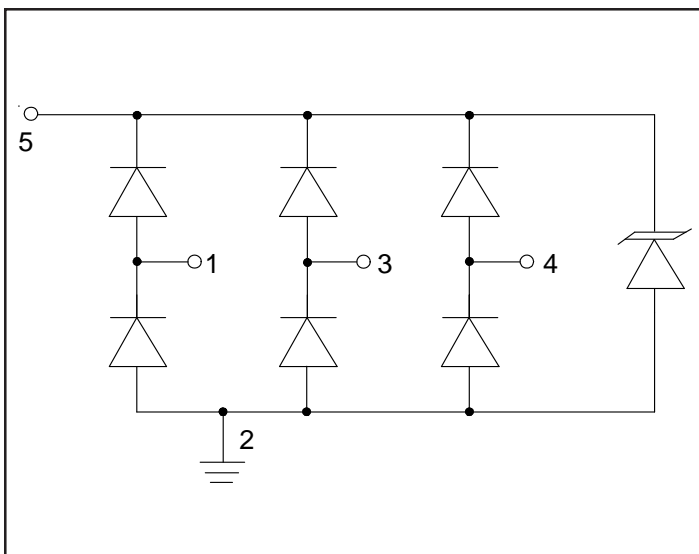
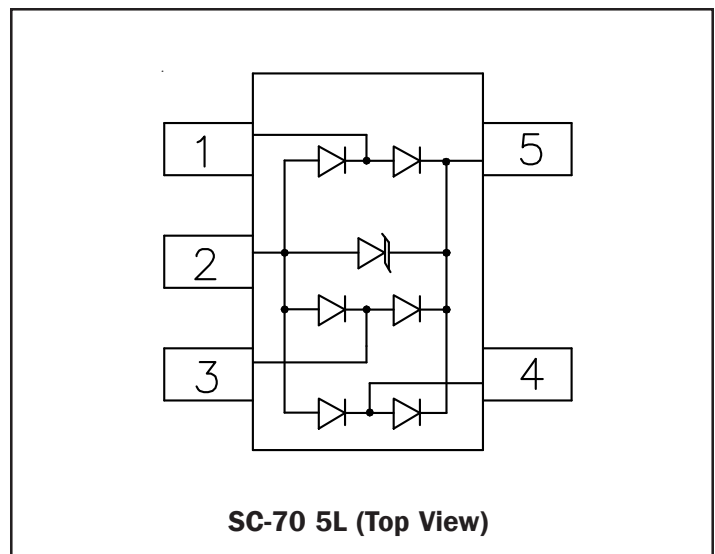
- ◆ Transient protection for high-speed data lines to **IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)**
- ◆ **IEC 61000-4-4 (EFT) 40A (5/50ns)**
- ◆ Array of surge rated diodes with internal TVS Diode
- ◆ Small package saves board space
- ◆ Protects three I/O lines & power line
- ◆ Low capacitance (**$< 3\text{pF}$**) for high-speed interfaces
- ◆ Low clamping voltage
- ◆ Low operating voltage: 5.0V
- ◆ Solid-state silicon-avalanche technology

Mechanical Characteristics

- ◆ EIAJ SC-70 5L package
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Lead Finish: Matte Tin
- ◆ Pb-Free, Halogen Free, RoHS/WEEE Compliant
- ◆ Marking : F53
- ◆ Packaging : Tape and Reel

Applications

- ◆ USB OTG interfaces
- ◆ SIM Ports
- ◆ Video Graphics Cards
- ◆ Personal Digital Assistants (PDAs)
- ◆ Monitors and Flat Panel Displays
- ◆ Portable Electronics
- ◆ Microcontroller Input Protection

Circuit Diagram

Schematic & PIN Configuration


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Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{pk}	150	Watts
Peak Pulse Current ($t_p = 8/20\mu s$)	I_{pp}	6	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	15 8	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C)

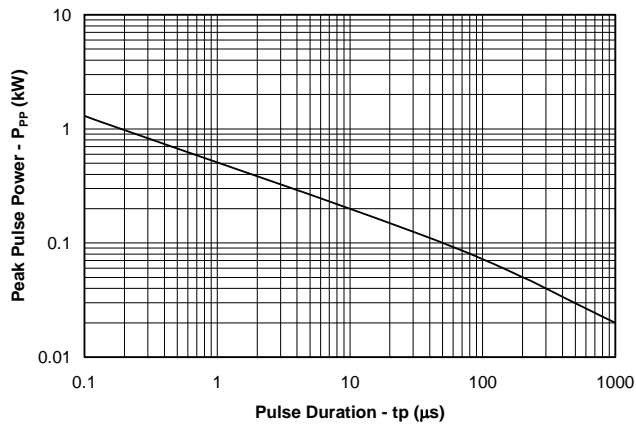
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Pin 5 to 2			5	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$ Pin 5 to 2	6			V
Reverse Leakage Current	I_R	$V_{RWM} = 5V, T=25^\circ C$ Pin 5 to 2			3	μA
Clamping Voltage	V_C	$I_{pp} = 1A, t_p = 8/20\mu s$ Any pin to pin 2			15	V
Clamping Voltage	V_C	$I_{pp} = 6A, t_p = 8/20\mu s$ Any pin to pin 2			25	V
Junction Capacitance	C_J	$V_R = 0V, f = 1MHz$ Any I/O pin to pin 2			3	pF
		$V_R = 0V, f = 1MHz$ Between I/O pins			1.5	pF

Note 1: I/O pins are pin 1, 3, and 4

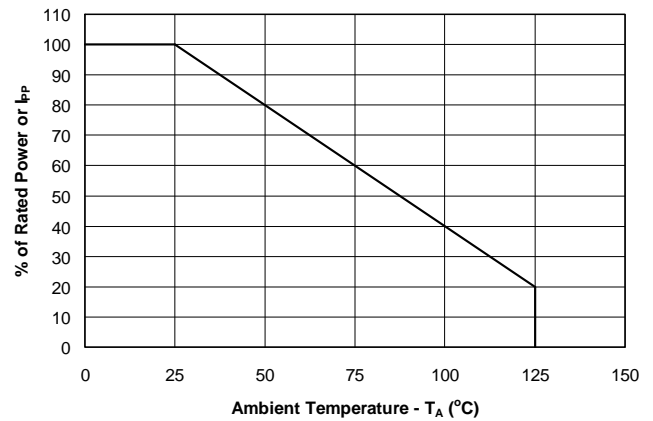
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Typical Characteristics

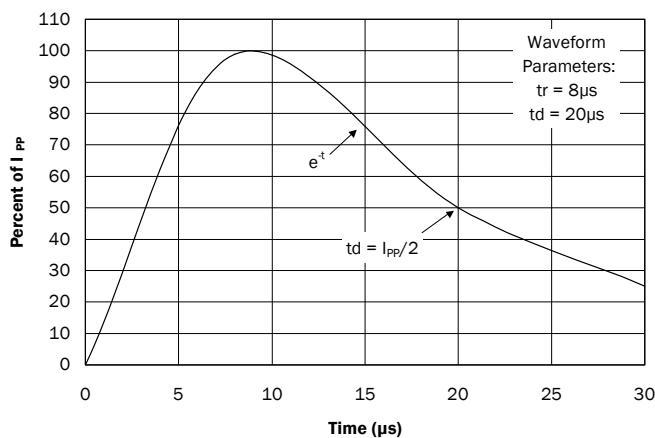
Non-Repetitive Peak Pulse Power vs. Pulse Time



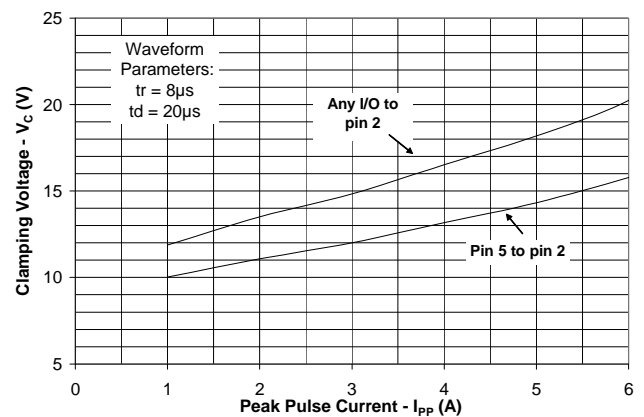
Power Derating Curve



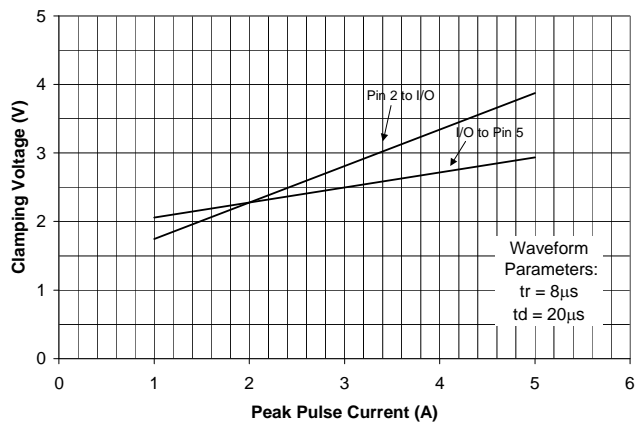
Pulse Waveform



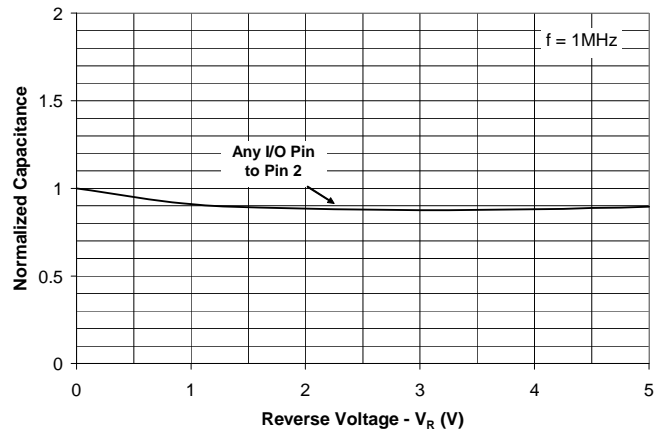
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current

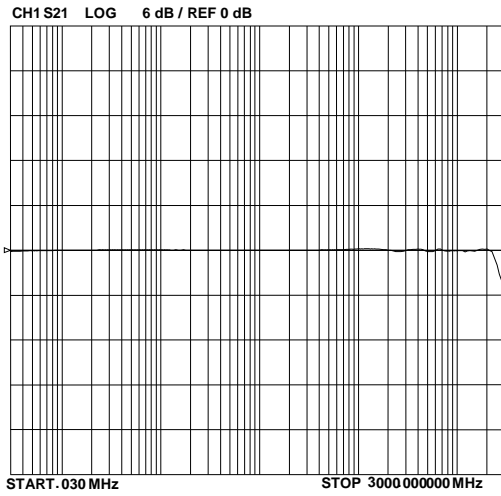


Capacitance vs. Reverse Voltage (Normalized to 0V)

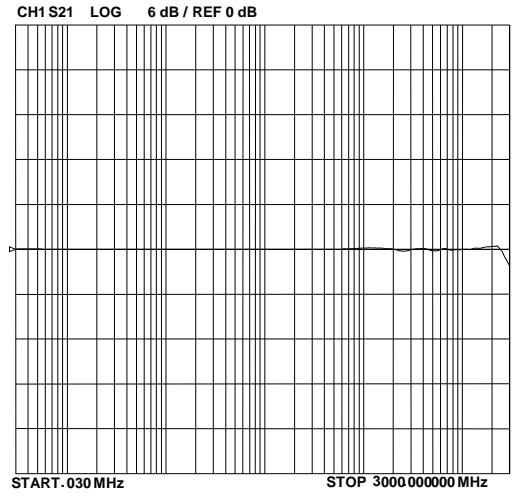


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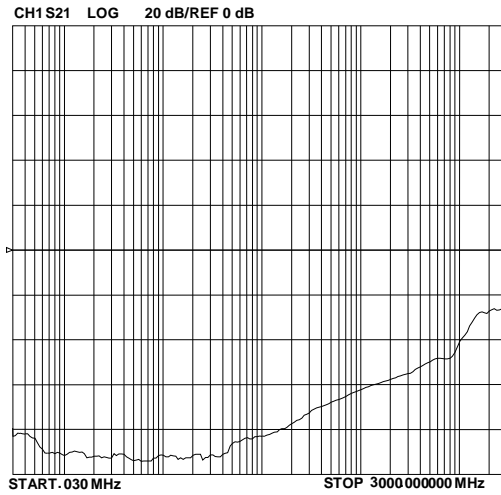
Insertion Loss S21 (I/O to Pin 2)



Insertion Loss S21 (I/O to I/O)



Analog Crosstalk



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Applications Information

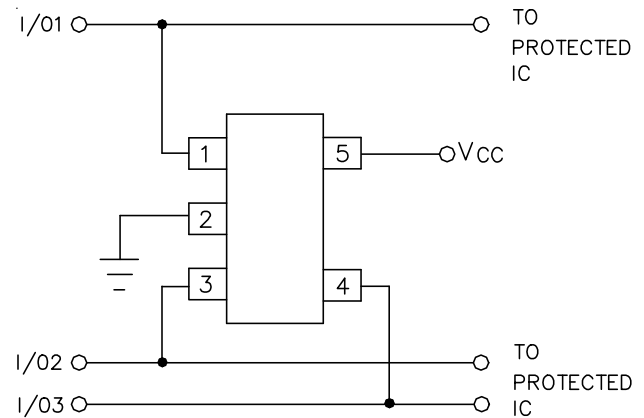
Device Connection Options for Protection of Three High-Speed Data Lines

This device is designed to protect three data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode V_f) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 3, and 4. The negative reference is connected at pin 2. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance. Connect pin 5 directly to the positive supply rail (V_{CC}). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.

Matte Tin Lead Finish

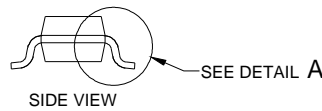
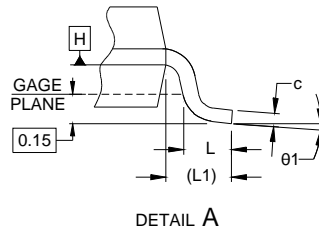
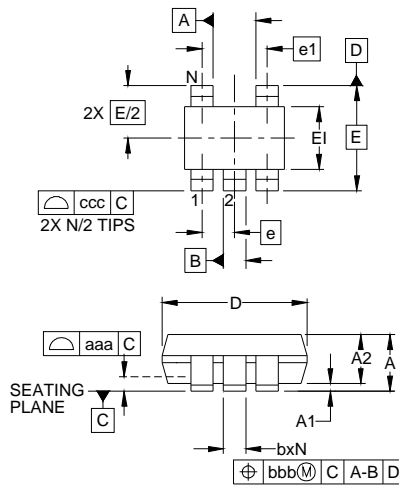
Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Data Line and Power Supply Protection Using V_{CC} as reference



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Outline Drawing - SC70-5L

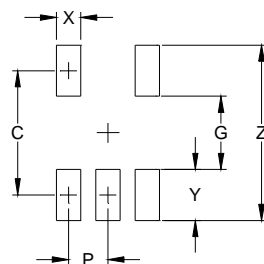


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.004	0.00	-	0.10
A2	.028	.035	.039	0.70	0.90	1.00
b	.006	-	.012	0.15	-	0.30
c	.003	-	.009	0.08	-	0.22
D	.075	.079	.083	1.90	2.00	2.10
E1	.045	.049	.053	1.15	1.25	1.35
E	.083 BSC			2.10 BSC		
e	.026 BSC			0.65 BSC		
e1	.051			1.30 BSC		
L	.010	.014	.018	0.26	0.36	0.46
L1	(0.017)			(0.42)		
N	5			5		
theta1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.012			0.30		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-203, VARIATION AA.

Land Pattern - SC70-5L



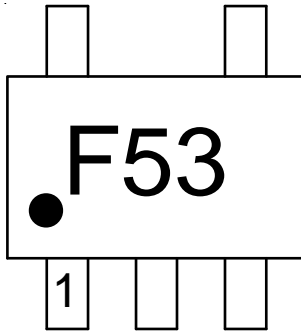
DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.073)	(1.85)
G	.039	1.00
P	.026	0.65
X	.016	0.40
Y	.033	0.85
Z	.106	2.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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Marking Codes

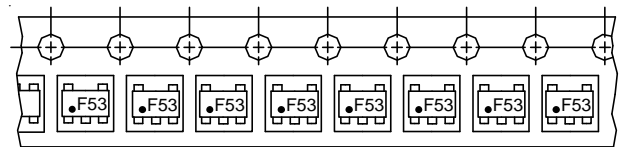
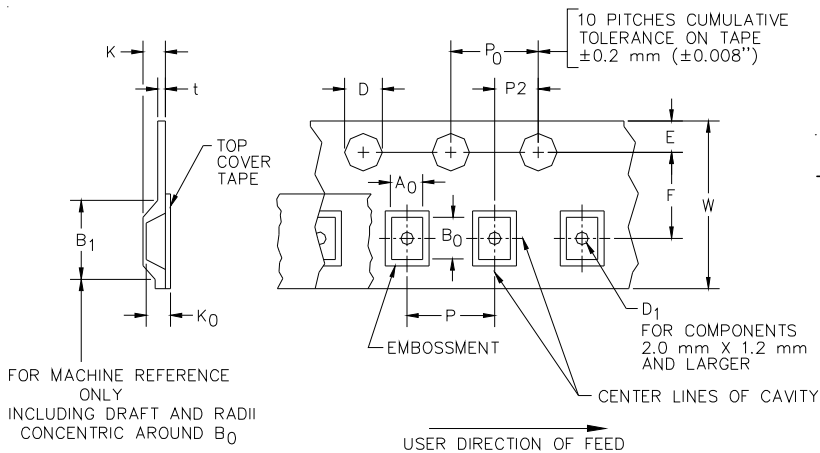


Ordering Information

Part Number	Lead Finish	Qty per Reel	Reel Size
RClamp0503F.TCT	Matte Tin	3,000	7 Inch

RailClamp and RClamp are registered marks of Semtech Corporation

Tape and Reel Specification



Device Orientation in Tape

Tape Width	B, (Max)	D	D1 (MIN)	E	F	K (MAX)	P	P0	P2	T(MAX)	W
8 mm	4.2 mm (.165)	1.5 + 0.1 mm - 0.0 mm (0.59 +.005 - .000)	1.0 mm (.039)	1.750±.10 mm (.069±.004)	3.5±0.05 mm (.138±.002)	2.4 mm (.094)	4.0±0.1 mm (.157±.004)	4.0±0.1 mm (.157±.004)	2.0±0.05mm (.079±.002)	0.4 mm (.016)	8.3 mm (.312±.012)

Contact Information

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