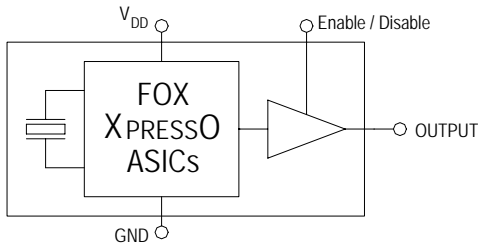


LVPECL 7 x 5mm 3.3V 50ppm XO Freq: 312.5MHz

Features

- ✔ Low Jitter
- ✔ Low Cost
- ✔ Tri-State Enable / Disable Feature
- ✔ Industry Standard Package
- ✔ Gold over Nickel Termination Finish



Electrical Characteristics

Parameters	Symbol	Condition	Maximum Value (unless otherwise noted)
Frequency Range	F _O		312.5 MHz
Frequency Stability 1			50 ppm
Temperature Range	T _O T _{STG}	Standard operating Storage	-40°C to +85°C -55°C to +125°C
Supply Voltage	V _{DD}	Standard	3.3V ± 5%
Input Current	I _{DD}	Standard Load	120 mA
Output Load	Differential	Standard	50 ohms into V _{DD} -2.0V _{DC}
Start-Up Time	T _S		10 mS
Output Enable / Disable Time			100 nS
Moisture Sensitivity Level	MSL		1
Termination Finish			Au

Note 1 – Stability is inclusive of 25°C tolerance, operating temperature range, input voltage change, load change, aging, shock and vibration.

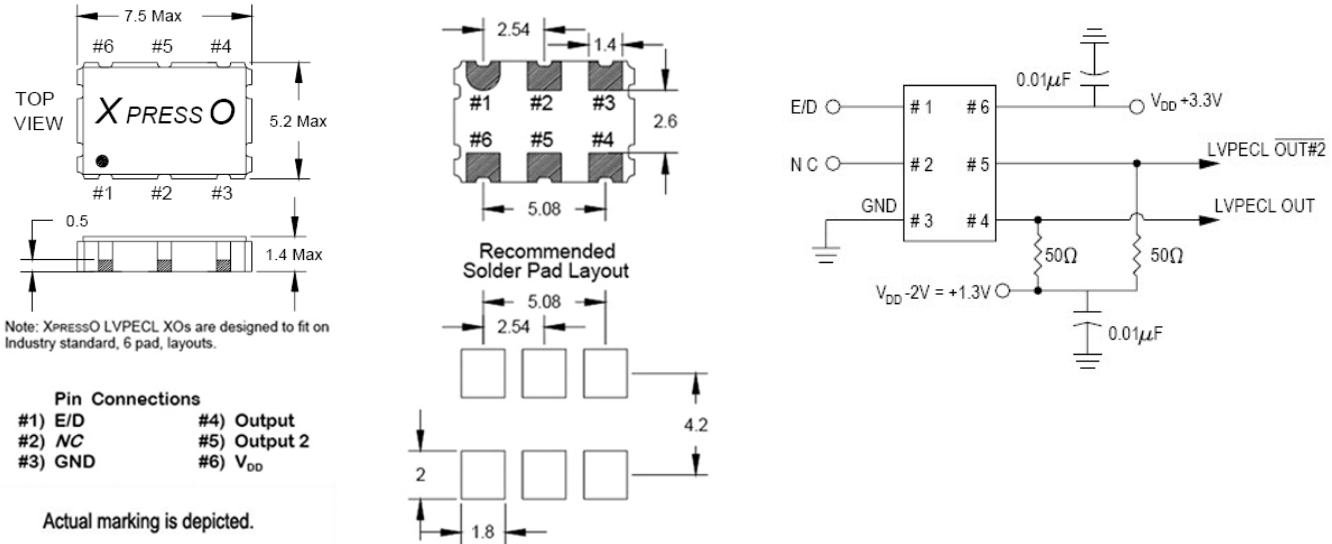
Output Wave Characteristics

Parameters	Symbol	Condition	Maximum Value
Output LOW Voltage	V _{OL}	Standard Load	1.35V ~ 1.65V
Output HIGH Voltage	V _{OH}	Standard Load	2.055V ~ 2.405V
Output Symmetry		@ 50% V _{p-p} Level	45% ~ 55%
Output Enable (PIN # 1) Voltage	V _{IH}		≥70% V _{DD}
Output Disable (PIN # 1) Voltage	V _{IL}		≤ 30% V _{DD}
Cycle Rise Time	T _R	20% ~ 80% V _{p-p}	400 pS
Cycle Fall Time	T _F	80% ~ 20% V _{p-p}	400 pS

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LVPECL 7 x 5mm 3.3V 50ppm XO Freq: 312.5MHz

Dimensional Drawing & Pad Layout



Drawing is for reference to critical specifications defined by size measurements. Certain non-critical visual attributes, such as side castellations, reference pin shape, etc. may vary

Phase Jitter & Time Interval Error (TIE) (Typical Measurements)

Frequency	Phase Jitter (12kHz to 20MHz)	TIE (Sigma of Jitter Distribution)	Units
312.5 MHz	0.86	3.5	pS RMS

Phase Jitter is integrated from HP3048 Phase Noise Measurement System; measured directly into 50 ohm input; V_{DD} = 3.3V.

TIE was measured on LeCroy LC684 Digital Storage Scope, directly into 50 ohm input, with Amherst M1 software; V_{DD} = 3.3V.

Per *MJSQ spec (Methodologies for Jitter and Signal Quality specifications)*

Random & Deterministic Jitter Composition (Typical Measurements)

Frequency	Random (Rj) (pS RMS)	Deterministic (Dj) (pS P-P)	Total Jitter (Tj) (14 x Rj) + Dj
312.5 MHz	1.29	9.3	27.7 pS

Rj and Dj, measured on LeCroy LC684 Digital Storage Scope, directly into 50 ohm input, with Amherst M1 software.

Per *MJSQ spec (Methodologies for Jitter and Signal Quality specifications)*

Pin Functional Description

Pin #	Name	Type	Function
1	E / D ¹	Logic	Enable / Disable Control of Output (0 = Disabled)
2	NC ²		No Connection – Leave Open
3	GND	Ground	Electrical Ground for V _{DD}
4	Output	Output	LVPECL Oscillator Output
5	Output 2	Output	Complementary LVPECL Output
6	V _{DD} ³	Power	Power Supply Source Voltage

- NOTES:**
- Includes pull-up resistor to V_{DD} to provide output when the pin (1) is No Connect. (Also see note 2)
 - An optional pin # 2 Enable / disable is available.
 - Installation should include a 0.01µF bypass capacitor placed between V_{DD} (Pin 6) and GND (Pin 3) to minimize power supply line noise.



for **ETHERNET**

Model: FXO-PC735RGB-312

LVPECL 7 x 5mm 3.3V 50ppm XO Freq: 312.5MHz

