

# PRELIMINARY

# **CY2XF32**

# High Performance CMOS Oscillator with Frequency Margining - Pin Control

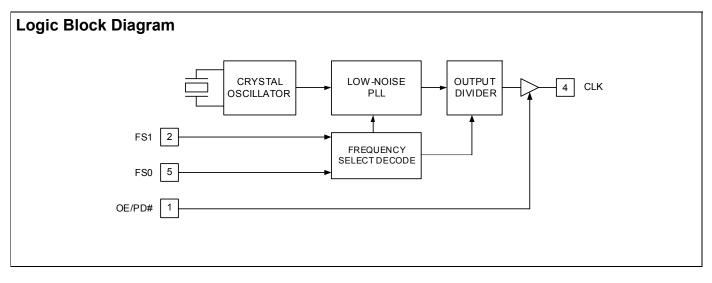
### Features

- Crystal Oscillator with CMOS Output
- Output Frequency from 8 MHz to 200 MHz
- Two Frequency Margining Control Pins (FS0, FS1)
- Output Enable or Power Down Function
- Factory Configured or Field Programmable
- Integrated Phase-Locked Loop (PLL)
- Supply Voltage: 3.3V or 2.5V
- Pb-free Package: 5.0 x 3.2 mm LCC
- Commercial and Industrial Temperature Ranges

# **Functional Description**

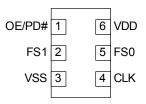
The CY2XF32 is a high performance and high frequency Crystal Oscillator (XO). It uses a Cypress proprietary low noise PLL to synthesize the frequency from an integrated crystal. The output frequency can be changed via two select pins, allowing easy frequency margin testing in applications.

The CY2XF32 is available as a factory configured device or as a field programmable device.



### **Pinouts**





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San Jose, CA 95134-1709 • 408-943-2600 Revised September 18, 2009



#### Table 1. Pin Definitions - 6 Pin Ceramic LCC

| Pin  | Name     | I/O Type    | Description  |
|------|----------|-------------|--|
| 1    | OE/PD#   | CMOS Input  | Output Enable or Power Down: Functionality is a programming option; see Table 3 and Table 4 for details. |
| 2, 5 | FS1, FS0 | CMOS Input  | Frequency Select.  |
| 4    | CLK      | CMOS Output | Clock Output.  |
| 6    | VDD      | Power       | Supply Voltage: 2.5V or 3.3V.  |
| 3    | VSS      | Power       | Ground.  |

### **Functional Description**

The FS0 and FS1 pins select between four different output frequencies, as shown in Table 2. Frequency margining is a common application for this feature. One frequency is used for the standard operating mode of the device, while the other frequencies are available for margin testing, either during product development or in system manufacturing test.

#### Table 2. Frequency Select

| FS1 | FS0 | Output Frequency |
|-----|-----|------------------|
| 0   | 0   | Frequency 0      |
| 0   | 1   | Frequency 1      |
| 1   | 0   | Frequency 2      |
| 1   | 1   | Frequency 3      |

When changing the output frequency, the frequency transition is not guaranteed to be smooth. There can be frequency excursions beyond the start frequency and the new frequency. Glitches and runt pulses are possible, and time must be allowed for the PLL to relock.

Pin 1 is programmed to function as either OE (output enable) or PD# (power down, active low). The OE function is used to enable or disable the CLK output very quickly, but it does not reduce core power consumption. The PD# function puts the device into a low power state, but the wake up takes longer because the PLL must reacquire lock. Details are shown in Table 3 and Table 4.

#### Table 3. Output Enable Operation

| OE | PLL & Xtal Oscillator | Output Buffer |
|----|-----------------------|---------------|
| 0  | Active                | Off           |
| 1  | Active                | On            |

#### Table 4. Power Down Operation

| PD# | PLL & Xtal Oscillator | Output Buffer |
|-----|-----------------------|---------------|
| 0   | Off                   | Off           |
| 1   | Active                | On            |

## **Programming Description**

The CY2XF32 is a programmable device. Before being used in an application, it must be programmed with the output frequencies and other variables described in a later section. Two different device types are available, each with its own programming flow. They are described below.

#### Field Programmable CY2XF32F

Field programmable devices are shipped unprogrammed and must be programmed before being installed on a printed circuit board (PCB). Customers use CyberClocks<sup>™</sup> Online Software to specify the device configuration and generate a JEDEC (extension .jed) programming file. Programming of samples and prototype quantities is available using a Cypress programmer. Third party vendors manufacture programmers for small to large volume applications. Cypress's value added distribution partners also provide programming services. Field programmable devices are designated with an "F" in the part number. They are intended for quick prototyping and inventory reduction. The CY2XF32 is one time programmable (OTP).

The software is located at www.cyberclocksonline.com.

#### Factory Configured CY2XF32

For ready-to-use devices, the CY2XF32 is available with no field programming required. All requests are submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, the user receives a new part number, samples, and data sheet with the programmed values. This part number is used for additional sample requests and production orders.



# **Programming Variables**

#### **Output Frequencies**

The CY2XF32 is programmed with up to four independent output frequencies, which are then selected using the FS0 and FS1 pins. The device can synthesize frequencies to a resolution of one part per million (ppm), but the actual accuracy of the output frequency is limited by the accuracy of the integrated reference crystal.

### Pin 1: Output Enable or Power Down (OE/PD#)

Pin 1 is programmed as either Output Enable (OE) or Power Down (PD#).

### Supply Voltage

A programming option optimizes the CY2XF32 for either 2.5V or 3.3V supply voltage. A device programmed for a particular supply voltage is not guaranteed to meet specifications when operated at the other voltage.

### Industrial versus Commercial Device Performance

Industrial and commercial devices have different internal crystals. This has a potentially significant impact on performance levels for applications requiring the lowest possible phase noise. CyberClocks Online Software displays expected performance for both options.

#### Table 5. Device Programming Variables

| Variable                                     |  |  |  |  |
|--|--|--|--|--|
| Output Frequency 0 (Power on default)        |  |  |  |  |
| Output Frequency 1                           |  |  |  |  |
| Output Frequency 2                           |  |  |  |  |
| Output Frequency 3                           |  |  |  |  |
| Pin 1 Functionality (OE or PD#)              |  |  |  |  |
| Supply Voltage (2.5V or 3.3V)                |  |  |  |  |
| Temperature Range (Commercial or Industrial) |  |  |  |  |





# **Absolute Maximum Conditions**

| Parameter                      | Description                             | Condition                   | Min  | Max                  | Unit |
|--------------------------------|---|-----------------------------|------|----------------------|------|
| V <sub>DD</sub>                | Supply Voltage                          |                             | -0.5 | 4.4                  | V    |
| V <sub>IN</sub> <sup>[1]</sup> | Input Voltage, DC                       | Relative to V <sub>SS</sub> | -0.5 | V <sub>DD</sub> +0.5 | V    |
| Τ <sub>S</sub>                 | Temperature, Storage                    | Non operating               | -55  | 135                  | °C   |
| TJ                             | Temperature, Junction                   |                             | -40  | 135                  | °C   |
| ESD <sub>HBM</sub>             | ESD Protection (Human Body Model)       | JEDEC STD 22-A114-B         | 2000 | -                    | V    |
| $\Theta_{JA}^{[2]}$            | Thermal Resistance, Junction to Ambient | 0 m/s airflow               |      | 64                   | °C/W |

# **Operating Conditions**

| Parameter         | Description   | Min   | Тур | Max   | Unit |
|-------------------|---|-------|-----|-------|------|
| V <sub>DD</sub>   | 3.3V Supply Voltage Range   | 3.135 | 3.3 | 3.465 | V    |
|                   | 2.5V Supply Voltage Range   | 2.375 | 2.5 | 2.625 | V    |
| T <sub>PU</sub>   | Power Up Time for $V_{DD}$ to Reach Minimum Specified Voltage (Power Ramp is Monotonic) | 0.05  | _   | 500   | ms   |
| T <sub>A</sub>    | Ambient Temperature, Commercial   | 0     | -   | 70    | °C   |
|                   | Ambient Temperature, Industrial   | -40   | _   | 85    | °C   |
| C <sub>LOAD</sub> | Load Capacitance at CLK (>100 MHz)  | _     | -   | 10    | pF   |
|                   | Load Capacitance at CLK (≤100 MHz)  | _     | _   | 15    | pF   |

# **DC Electrical Characteristics**

| Parameter                       | Description                        | Condition   | Min                 | Тур | Max                 | Unit |
|---------------------------------|------------------------------------|---|---------------------|-----|---------------------|------|
| I <sub>DD</sub>                 | Operating Supply Current           | V <sub>DD</sub> = 3.465V, OE/PD# = V <sub>DD</sub> , output<br>unloaded | -                   | -   | 110                 | mA   |
| I <sub>SB</sub>                 | Standby Supply Current             | PD# = V <sub>SS</sub>   | -                   | -   | 200                 | μA   |
| V <sub>OH</sub>                 | Output High Voltage                | V <sub>DD</sub> = min, I <sub>OH</sub> = –4 mA                          | 0.9*V <sub>DD</sub> | -   | -                   | V    |
| V <sub>OL</sub>                 | Output Low Voltage                 | V <sub>DD</sub> = max, I <sub>OL</sub> = 4 mA                           | -                   | -   | 0.1*V <sub>DD</sub> | V    |
| I <sub>OZ</sub>                 | Output Leakage Current             | OE/PD# = V <sub>SS</sub>  | -35                 | -   | 35                  | μA   |
| V <sub>IH</sub>                 | Input High Voltage                 |   | 0.7*V <sub>DD</sub> | -   | -                   | V    |
| V <sub>IL</sub>                 | Input Low Voltage                  |   | -                   | —   | 0.3*V <sub>DD</sub> | V    |
| I <sub>IH0</sub>                | Input High Current, OE/PD# Pin     | Input = V <sub>DD</sub>   | -                   | -   | 115                 | μA   |
| I <sub>IH1</sub>                | Input High Current, FS0 & FS1 Pins | Input = V <sub>DD</sub>   | -                   | -   | 10                  | μA   |
| I <sub>ILO</sub>                | Input Low Current, OE/PD# Pin      | Input = V <sub>SS</sub>   | -50                 | -   | -                   | μA   |
| I <sub>IL1</sub>                | Input Low Current, FS0 & FS1 Pin   | Input = V <sub>SS</sub>   | -20                 | -   | -                   | μA   |
| C <sub>IN0</sub> [3]            | Input Capacitance, OE/PD# Pin      |   | -                   | 15  | -                   | pF   |
| C <sub>IN1</sub> <sup>[3]</sup> | Input Capacitance, FS0 & FS1 Pin   |   | _                   | 4   | -                   | pF   |

#### Notes

- The voltage on any input or I/O pin cannot exceed the power pin during power up.
   Simulated. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has four layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.
   Not 100% tested, guaranteed by design and characterization.



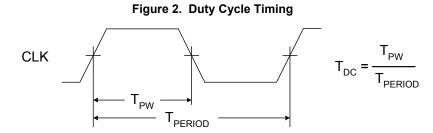
# AC Electrical Characteristics<sup>[3]</sup>

| Parameter         | Description  | Condition   | Min | Тур | Max | Unit |
|-------------------|--|---|-----|-----|-----|------|
| F <sub>OUT</sub>  | Output Frequency <sup>[5]</sup>                        |   | 8   | -   | 200 | MHz  |
| FSC               | Frequency Stability, Commercial Devices <sup>[4]</sup> | $T_A = 0^{\circ}C$ to $70^{\circ}C$   | _   | -   | ±35 | ppm  |
| FSI               | Frequency Stability, Industrial Devices <sup>[4]</sup> | $T_A = -40^{\circ}C \text{ to } 85^{\circ}C$  | -   | -   | ±55 | ppm  |
| AG                | Aging, 10 Years  |   | _   | -   | ±15 | ppm  |
| T <sub>DC</sub>   | Output Duty Cycle                                      | Measured at V <sub>DD</sub> /2; see Figure 2  | 45  | 50  | 55  | %    |
| T <sub>R</sub>    | Output Rise Time                                       | 20% to 80% of $V_{DD}$ , $C_{LOAD}$ = 15 pF   | _   | 0.7 | 1.5 | ns   |
| T <sub>F</sub>    | Output Fall Time                                       | 80% to 20% of $V_{DD}$ , $C_{LOAD}$ = 15 pF   | _   | 0.8 | 1.5 | ns   |
| Т <sub>ОНZ</sub>  | Output Disable Time                                    | Time from falling edge on OE to stopped outputs (Asynchronous)  | -   | -   | 100 | ns   |
| T <sub>OE</sub>   | Output Enable Time                                     | Time from rising edge on OE to outputs at a valid frequency (Asynchronous)  | _   | -   | 100 | ns   |
| Т <sub>LOCK</sub> | Startup Time   | Time for CLK to reach valid frequency<br>measured from the time<br>V <sub>DD</sub> = V <sub>DD</sub> (min.) or from PD# rising edge | -   | -   | 5   | ms   |
| T <sub>LFS</sub>  | Relock Time  | Time for CLK to reach valid frequency from FS0 or FS1 pin change  | _   | -   | 1   | ms   |

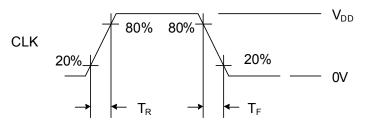
Notes
4. Frequency stability is the maximum variation in frequency from F<sub>0</sub>. It includes initial accuracy, plus variation from temperature and supply voltage.
5. This parameter is specified in CyberClocks Online software.



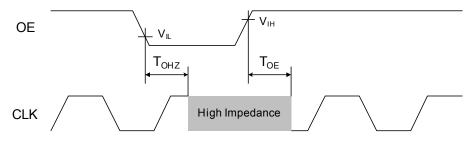
# **Switching Waveforms**



### Figure 3. Output Rise and Fall Time



### Figure 4. Output Enable and Disable Timing

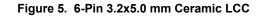


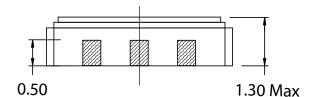


# **Ordering Information**

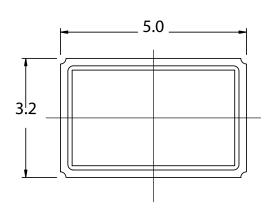
| Part Number <sup>[6]</sup> Configuration |                    | Package Description                   | Product Flow             |  |
|--|--------------------|---------------------------------------|--------------------------|--|
| Pb-Free                                  |                    |                                       |                          |  |
| CY2XF32FLXCT                             | Field Programmable | 6-Pin Ceramic LCC SMD - Tape and Reel | Commercial, 0° to 70°C   |  |
| CY2XF32FLXIT                             | Field Programmable | 6-Pin Ceramic LCC SMD - Tape and Reel | Industrial, –40° to 85°C |  |
| CY2XF32LXCxxxT                           | Factory Configured | 6-Pin Ceramic LCC SMD - Tape and Reel | Commercial, 0° to 70°C   |  |
| CY2XF32LXIxxxT                           | Factory Configured | 6-Pin Ceramic LCC SMD - Tape and Reel | Industrial, –40° to 85°C |  |

# Package Diagram





SIDE VIEW



TOP VIEW

Dimensions in mm General Tolerance: ± 0.15MM Kyocera dwg ref KD-VA6432-A Package Weight ~ 0.12 grams

001-10044-\*\*

0.10 REF.

0.10 R REF.

TYP.

0.32 R

TYP. 1.27

8

INDEX

2.54 TYP.

5

2

0.45 REF.

1

0.64 TYP.

10

9

3

BOTTOM VIEW

TYP. 0.20 R REF.

1.2 TYP.

Note6. "xxx" is a factory assigned code that identifies the programming option.



### **Document History Page**

| Document Title: CY2XF32 High Performance CMOS Oscillator with Frequency Margining - Pin Control<br>Document Number: 001-53147 |         |                    |                    |   |  |  |  |
|---|---------|--------------------|--------------------|---|--|--|--|
| Rev.  | ECN No. | Orig. of<br>Change | Submission<br>Date | Description of Change   |  |  |  |
| **  | 2705753 | KVM/PYRS           | 05/13/09           | New data sheet  |  |  |  |
| *A  | 2734005 | WWZ                | 07/09/2009         | Post to external web  |  |  |  |
| *В  | 2764787 | KVM                |                    | Change I <sub>SB</sub> max from 250 $\mu$ A to 200 $\mu$ A<br>Add max limit for T <sub>R</sub> , T <sub>F</sub> : 1.5 ns<br>Change T <sub>LOCK</sub> max from 10 ms to 5 ms<br>Change T <sub>LFS</sub> max from 10 ms to 1 ms |  |  |  |

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