High Performance CMOS Oscillator with Frequency Margining - Pin Control
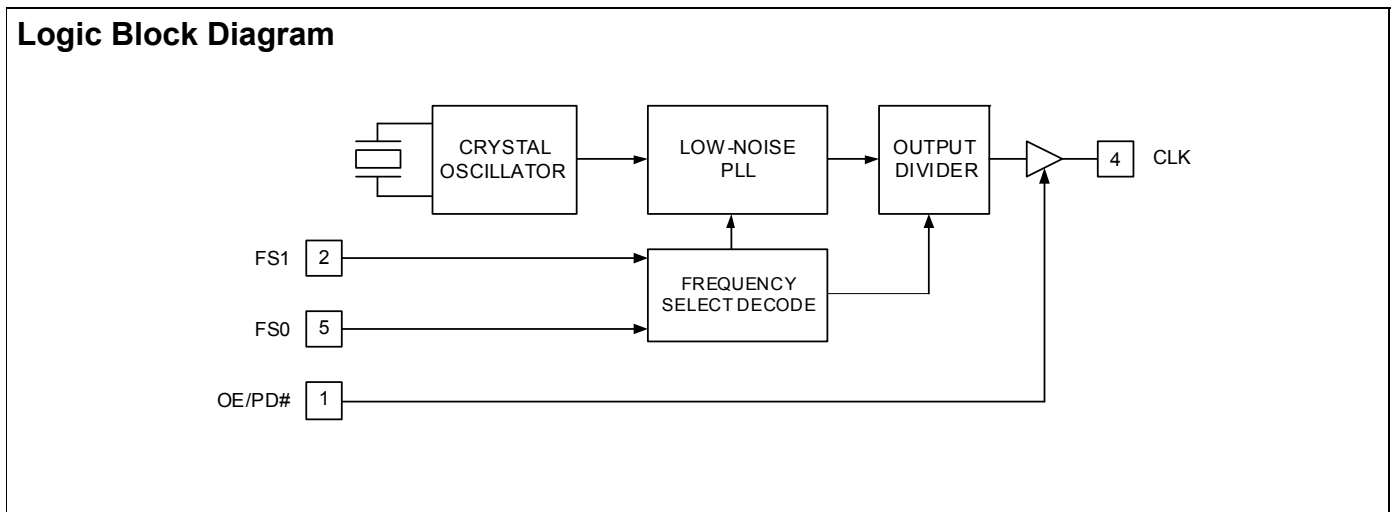
Features

- Crystal Oscillator with CMOS Output
- Output Frequency from 8 MHz to 200 MHz
- Two Frequency Margining Control Pins (FS0, FS1)
- Output Enable or Power Down Function
- Factory Configured or Field Programmable
- Integrated Phase-Locked Loop (PLL)
- Supply Voltage: 3.3V or 2.5V
- Pb-free Package: 5.0 x 3.2 mm LCC
- Commercial and Industrial Temperature Ranges

Functional Description

The CY2XF32 is a high performance and high frequency Crystal Oscillator (XO). It uses a Cypress proprietary low noise PLL to synthesize the frequency from an integrated crystal. The output frequency can be changed via two select pins, allowing easy frequency margin testing in applications.
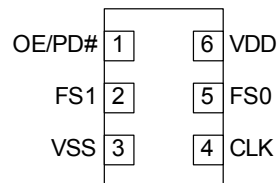
The CY2XF32 is available as a factory configured device or as a field programmable device.

Logic Block Diagram

Pinouts

Figure 1. Pin Diagram - 6 Pin Ceramic LCC

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Table 1. Pin Definitions - 6 Pin Ceramic LCC

Pin	Name	I/O Type	Description
1	OE/PD#	CMOS Input	Output Enable or Power Down: Functionality is a programming option; see Table 3 and Table 4 for details.
2, 5	FS1, FS0	CMOS Input	Frequency Select.
4	CLK	CMOS Output	Clock Output.
6	VDD	Power	Supply Voltage: 2.5V or 3.3V.
3	VSS	Power	Ground.

Functional Description

The FS0 and FS1 pins select between four different output frequencies, as shown in Table 2. Frequency margining is a common application for this feature. One frequency is used for the standard operating mode of the device, while the other frequencies are available for margin testing, either during product development or in system manufacturing test.

Table 2. Frequency Select

FS1	FS0	Output Frequency
0	0	Frequency 0
0	1	Frequency 1
1	0	Frequency 2
1	1	Frequency 3

When changing the output frequency, the frequency transition is not guaranteed to be smooth. There can be frequency excursions beyond the start frequency and the new frequency. Glitches and runt pulses are possible, and time must be allowed for the PLL to relock.

Pin 1 is programmed to function as either OE (output enable) or PD# (power down, active low). The OE function is used to enable or disable the CLK output very quickly, but it does not reduce core power consumption. The PD# function puts the device into a low power state, but the wake up takes longer because the PLL must reacquire lock. Details are shown in Table 3 and Table 4.

Table 3. Output Enable Operation

OE	PLL & Xtal Oscillator	Output Buffer
0	Active	Off
1	Active	On

Table 4. Power Down Operation

PD#	PLL & Xtal Oscillator	Output Buffer
0	Off	Off
1	Active	On

Programming Description

The CY2XF32 is a programmable device. Before being used in an application, it must be programmed with the output frequencies and other variables described in a later section. Two different device types are available, each with its own programming flow. They are described below.

Field Programmable CY2XF32F

Field programmable devices are shipped unprogrammed and must be programmed before being installed on a printed circuit board (PCB). Customers use CyberClocks™ Online Software to specify the device configuration and generate a JEDEC (extension .jed) programming file. Programming of samples and prototype quantities is available using a Cypress programmer. Third party vendors manufacture programmers for small to large volume applications. Cypress's value added distribution partners also provide programming services. Field programmable devices are designated with an "F" in the part number. They are intended for quick prototyping and inventory reduction. The CY2XF32 is one time programmable (OTP).

The software is located at www.cyberclocksonline.com.

Factory Configured CY2XF32

For ready-to-use devices, the CY2XF32 is available with no field programming required. All requests are submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, the user receives a new part number, samples, and data sheet with the programmed values. This part number is used for additional sample requests and production orders.

Programming Variables

Output Frequencies

The CY2XF32 is programmed with up to four independent output frequencies, which are then selected using the FS0 and FS1 pins. The device can synthesize frequencies to a resolution of one part per million (ppm), but the actual accuracy of the output frequency is limited by the accuracy of the integrated reference crystal.

Pin 1: Output Enable or Power Down (OE/PD#)

Pin 1 is programmed as either Output Enable (OE) or Power Down (PD#).

Supply Voltage

A programming option optimizes the CY2XF32 for either 2.5V or 3.3V supply voltage. A device programmed for a particular supply voltage is not guaranteed to meet specifications when operated at the other voltage.

Industrial versus Commercial Device Performance

Industrial and commercial devices have different internal crystals. This has a potentially significant impact on performance levels for applications requiring the lowest possible phase noise. CyberClocks Online Software displays expected performance for both options.

Table 5. Device Programming Variables

Variable
Output Frequency 0 (Power on default)
Output Frequency 1
Output Frequency 2
Output Frequency 3
Pin 1 Functionality (OE or PD#)
Supply Voltage (2.5V or 3.3V)
Temperature Range (Commercial or Industrial)

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply Voltage		−0.5	4.4	V
V_{IN}[1]	Input Voltage, DC	Relative to V_{SS}	−0.5	V_{DD}+0.5	V
T_S	Temperature, Storage	Non operating	−55	135	°C
T_J	Temperature, Junction		−40	135	°C
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC STD 22-A114-B	2000	–	V
Θ_{JA}[2]	Thermal Resistance, Junction to Ambient	0 m/s airflow	64		°C/W

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	3.3V Supply Voltage Range	3.135	3.3	3.465	V
	2.5V Supply Voltage Range	2.375	2.5	2.625	V
T_{PU}	Power Up Time for V_{DD} to Reach Minimum Specified Voltage (Power Ramp is Monotonic)	0.05	–	500	ms
T_A	Ambient Temperature, Commercial	0	–	70	°C
	Ambient Temperature, Industrial	−40	–	85	°C
C_{LOAD}	Load Capacitance at CLK (>100 MHz)	–	–	10	pF
	Load Capacitance at CLK (≤100 MHz)	–	–	15	pF

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{DD}	Operating Supply Current	V_{DD} = 3.465V, OE/PD# = V_{DD}, output unloaded	–	–	110	mA
I_{SB}	Standby Supply Current	PD# = V_{SS}	–	–	200	μA
V_{OH}	Output High Voltage	V_{DD} = min, I_{OH} = −4 mA	0.9*V_{DD}	–	–	V
V_{OL}	Output Low Voltage	V_{DD} = max, I_{OL} = 4 mA	–	–	0.1*V_{DD}	V
I_{OZ}	Output Leakage Current	OE/PD# = V_{SS}	−35	–	35	μA
V_{IH}	Input High Voltage		0.7*V_{DD}	–	–	V
V_{IL}	Input Low Voltage		–	–	0.3*V_{DD}	V
I_{IH0}	Input High Current, OE/PD# Pin	Input = V_{DD}	–	–	115	μA
I_{IH1}	Input High Current, FS0 & FS1 Pins	Input = V_{DD}	–	–	10	μA
I_{IL0}	Input Low Current, OE/PD# Pin	Input = V_{SS}	−50	–	–	μA
I_{IL1}	Input Low Current, FS0 & FS1 Pin	Input = V_{SS}	−20	–	–	μA
C_{IN0}[3]	Input Capacitance, OE/PD# Pin		–	15	–	pF
C_{IN1}[3]	Input Capacitance, FS0 & FS1 Pin		–	4	–	pF

Notes
1. The voltage on any input or I/O pin cannot exceed the power pin during power up.
2. Simulated. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has four layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.
3. Not 100% tested, guaranteed by design and characterization.

[+] Feedback

AC Electrical Characteristics[3]

Parameter	Description	Condition	Min	Typ	Max	Unit
F_{OUT}	Output Frequency[5]		8	–	200	MHz
FSC	Frequency Stability, Commercial Devices[4]	T_A = 0°C to 70°C	–	–	±35	ppm
FSI	Frequency Stability, Industrial Devices[4]	T_A = –40°C to 85°C	–	–	±55	ppm
AG	Aging, 10 Years		–	–	±15	ppm
T_{DC}	Output Duty Cycle	Measured at V_{DD}/2; see Figure 2	45	50	55	%
T_R	Output Rise Time	20% to 80% of V_{DD}, C_{LOAD} = 15 pF	–	0.7	1.5	ns
T_F	Output Fall Time	80% to 20% of V_{DD}, C_{LOAD} = 15 pF	–	0.8	1.5	ns
T_{OHZ}	Output Disable Time	Time from falling edge on OE to stopped outputs (Asynchronous)	–	–	100	ns
T_{OE}	Output Enable Time	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	–	100	ns
T_{LOCK}	Startup Time	Time for CLK to reach valid frequency measured from the time V_{DD} = V_{DD}(min.) or from PD# rising edge	–	–	5	ms
T_{LFS}	Relock Time	Time for CLK to reach valid frequency from FS0 or FS1 pin change	–	–	1	ms

Notes
4. Frequency stability is the maximum variation in frequency from F_0. It includes initial accuracy, plus variation from temperature and supply voltage.
5. This parameter is specified in CyberClocks Online software.

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Switching Waveforms

Figure 2. Duty Cycle Timing

$$T_{DC} = \frac{T_{PW}}{T_{PERIOD}}$$
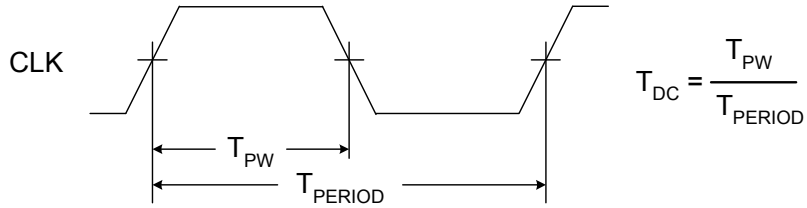
Figure 3. Output Rise and Fall Time
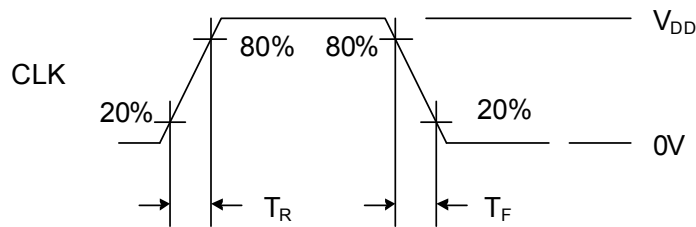
Figure 4. Output Enable and Disable Timing

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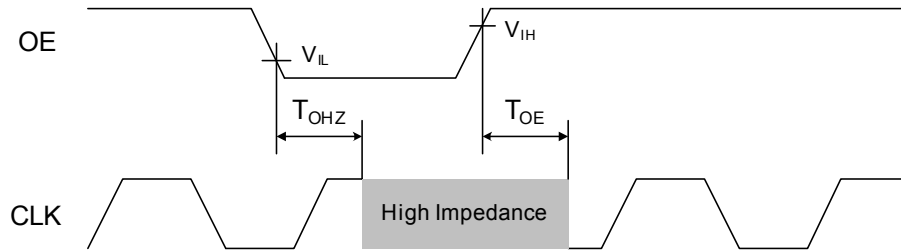
Ordering Information

Part Number[6]	Configuration	Package Description	Product Flow
Pb-Free			
CY2XF32FLXCT	Field Programmable	6-Pin Ceramic LCC SMD - Tape and Reel	Commercial, 0° to 70°C
CY2XF32FLXIT	Field Programmable	6-Pin Ceramic LCC SMD - Tape and Reel	Industrial, –40° to 85°C
CY2XF32LXCxxxT	Factory Configured	6-Pin Ceramic LCC SMD - Tape and Reel	Commercial, 0° to 70°C
CY2XF32LXIxxxT	Factory Configured	6-Pin Ceramic LCC SMD - Tape and Reel	Industrial, –40° to 85°C

Package Diagram

Figure 5. 6-Pin 3.2x5.0 mm Ceramic LCC

SIDE VIEW

TOP VIEW

BOTTOM VIEW
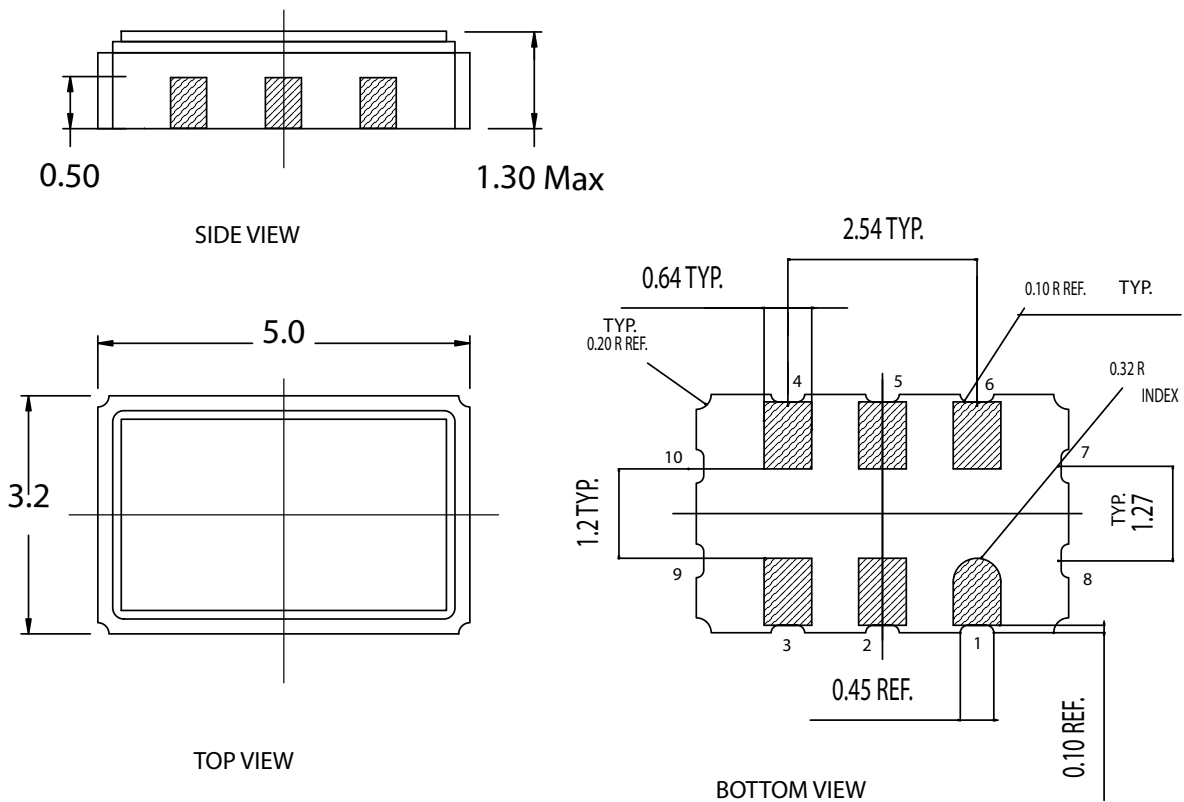
Dimensions in mm
General Tolerance: ± 0.15MM
Kyocera dwg ref KD-VA6432-A
Package Weight ~ 0.12 grams

001-10044-**

Note
6. "xxx" is a factory assigned code that identifies the programming option.

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Document History Page

Document Title: CY2XF32 High Performance CMOS Oscillator with Frequency Margining - Pin Control Document Number: 001-53147				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2705753	KVM/PYRS	05/13/09	New data sheet
*A	2734005	WWZ	07/09/2009	Post to external web
*B	2764787	KVM	09/19/2009	Change I_{SB} max from 250 µA to 200 µA Add max limit for T_R, T_F: 1.5 ns Change T_{LOCK} max from 10 ms to 5 ms Change T_{LFS} max from 10 ms to 1 ms

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