TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOSIII)

TPCS8302

Lithium Ion Battery Applications
Notebook PC Applications
Portable Equipment Applications

- Small footprint due to small and thin package
- Low drain-source ON resistance: $RDS(ON) = 22 \text{ m}\Omega \text{ (typ.)}$
- High forward transfer admittance: $|Y_{fs}| = 12 \text{ S (typ.)}$
- Low leakage current: $IDSS = -10 \mu A (max) (VDS = -20 V)$
- Enhancement mode: $V_{th} = -0.5 \sim -1.2 \text{ V (V}_{DS} = -10 \text{ V, I}_{D} = -200 \text{ }\mu\text{A})$

Absolute Maximum Ratings (Ta = 25°C)

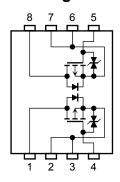
Char	acteristics	Symbol	Rating	Unit	
Drain-source voltage		V_{DSS}	-20	V	
Drain-gate voltag	ge (R _{GS} = 20 kΩ)	V_{DGR}	-20	V	
Gate-source volt	age	V _{GSS}	±12	V	
Dunin aumant	DC (Note 1)	I _D	-5	^	
Drain current	Pulse (Note 1)	I _{DP}	-20	Α	
Drain power	Single-device operation (Note 3a)	P _{D (1)}	1.1		
dissipation (t = 10 s) (Note 2a)	Single-device value at dual operation (Note 3b)	P _{D (2)}	0.75	W	
Drain power dissipation (t = 10 s) (Note 2b)	Single-device operation (Note 3a)	P _{D (1)}	0.6	W	
	Single-device value at dual operation (Note 3b)	P _{D (2)}	0.35		
Single pulse avalanche energy (Note 4)		E _{AS}	32.5	mJ	
Avalanche curre	Avalanche current		-5	Α	
Repetitive avalanche energy Single-device value at dual operation (Note 2a, 3b, 5)		E _{AR}	0.075	mJ	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55 to 150	°C	

Unit: mm

| 0.525| | 0.25±0.05 | 0.65 | 0.25±0.05 | 0.65 | 0.25±0.05 | 0.65 | 0.25±0.05 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.2 | 0.6±0.

Weight: 0.035 g (typ.)

Circuit Configuration



Note: (Note 1), (Note 2), (Note 3), (Note 4) and (Note 5): See next page.

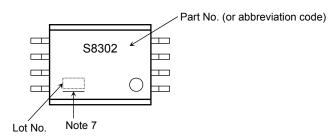
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Please handle with caution.

Thermal Characteristics

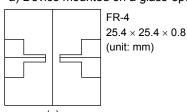
Characteristics	Symbol	Max	Unit		
Thermal resistance channel to ambient	Single-device operation (Note 3a)	R _{th (ch-a) (1)}	114		
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)		167	°C/W		
Thermal resistance, channel to ambient	Single-device operation (Note 3a)	R _{th (ch-a) (1)}	208		
(t = 10 s) (Note 2b)	Single-device value at dual operation (Note 3b)	R _{th (ch-a) (2)}	357	°C/W	

Marking (Note 6)

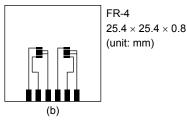


Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: a) Device mounted on a glass-epoxy board (a)



b) Device mounted on a glass-epoxy board (b)



- Note 3: a) The power dissipation and thermal resistance values are shown for a single device (During single-device operation, power is only applied to one device.)
 - b) The power dissipation and thermal resistance values are shown for a single device (During dual operation, power is evenly applied to both devices.)
- Note 4: $V_{DD} = -16 \text{ V}$, $T_{ch} = 25^{\circ}\text{C}$, L = 1.0 mH, $I_{AR} = -5 \text{ A}$, $R_G = 25 \Omega$
- Note 5: Repetitive rating: pulse width limited by maximum channel temperature
- Note 6: on the lower left of the marking indicates Pin 1.

Weekly code: (Three digits)
 Week of manufacture
 (01 for first week of year, continuing up to 52 or 53)
 Year of manufacture
 (The last digit of the calendar year)

Note 7: A line under a Lot No. identifies the indication of product Labels.

Not underlined: [[Pb]]/INCLUDES > MCV

Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. The RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.



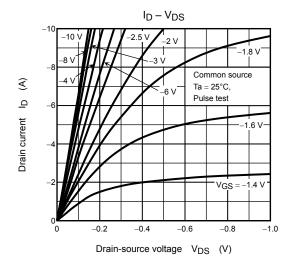
Electrical Characteristics (Ta = 25°C)

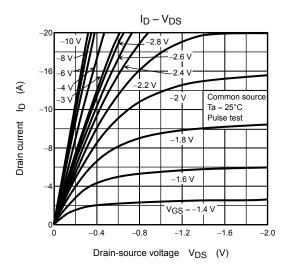
Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cur	e leakage current		$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±10	μА
Drain cut-OFF cu	ırrent	I _{DSS}	$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}$	_			μА
Drain-source bre	akdown voltago	V _{(BR) DSS}	$I_D = -10 \text{ mA}, V_{GS} = 0 \text{ V}$	-20	_	_	V
Dialii-source bre	akdowii vollage	V _{(BR) DSX}	$I_D = -10 \text{ mA}, V_{GS} = 12 \text{ V}$		V		
Gate threshold vo	oltage	V _{th}	$V_{DS} = -10 \text{ V}, I_D = -200 \mu\text{A}$	-0.5	_	-1.2	V
			$V_{GS} = -2.0 \text{ V}, I_D = -2.5 \text{ A}$	_	42	95	mΩ
Drain-source ON	resistance	R _{DS} (ON)	$V_{GS} = -2.5 \text{ V}, I_D = -2.5 \text{ A}$	_	32	60	
			$V_{GS} = -4.5 \text{ V}, I_D = -2.5 \text{ A}$	_	22	35	
Forward transfer	admittance	Y _{fs}	$V_{DS} = -10 \text{ V}, I_D = -2.5 \text{ A}$	5.5	12	_	S
Input capacitance		C _{iss}		_	1590	_	
Reverse transfer	capacitance	C _{rss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	_	380	_	pF
Output capacitance		Coss		_	430	_	
Reverse transfer cap Output capacitance F Switching time T Total gate charge	Rise time	t _r	VGS 0 V 1D = -2.5 A O VOUT C C C C C C C C C C C C C C C C C C C	_	9	_	
	Turn-ON time	t _{on}		_	16	_	- ns
	Fall time	t _f		_	45	_	
	Turn-OFF time	t _{off}	$V_{DD} \simeq 10 \text{ V}$ Duty $\leq 1\%$, $t_W = 10 \mu\text{s}$	_	113	_	
Total gate charge (gate-source plus gate-drain)		Qg	$V_{DD} \simeq 16 \text{ V}, V_{GS} = -5 \text{ V}, I_D = -5 \text{ A}$	_	28.5		
Gate-source charge 1		Q _{gs}		_	19	_	nC -
Gate-drain ("miller") charge		Q _{gd}		_	9.4	_	

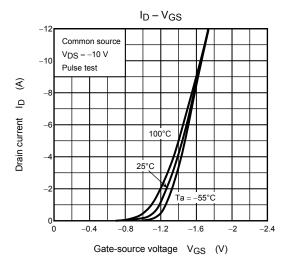
Source-Drain Ratings and Characteristics (Ta = 25°C)

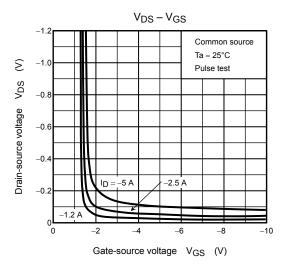
Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Drain reverse current	Pulse (Note 1)	I _{DRP}	_	_	_	-20	Α
Forward voltage (diode)		V _{DSF}	$I_{DR} = -5 \text{ A}, V_{GS} = 0 \text{ V}$	_	_	1.2	V

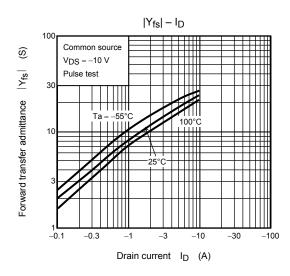
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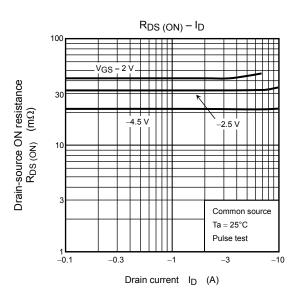


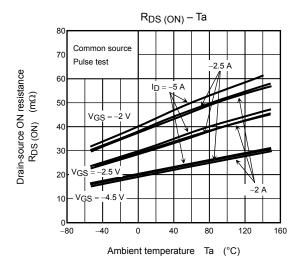


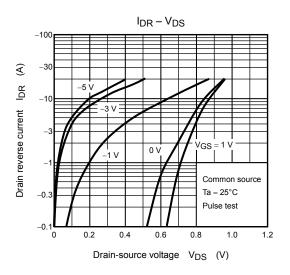


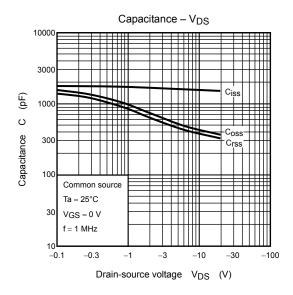


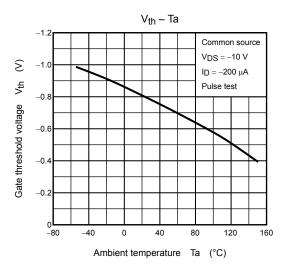


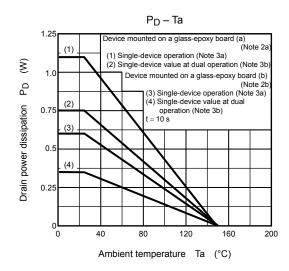


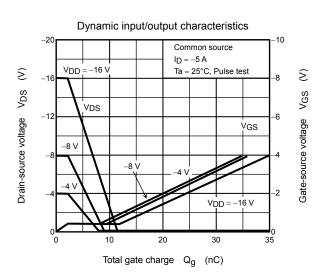


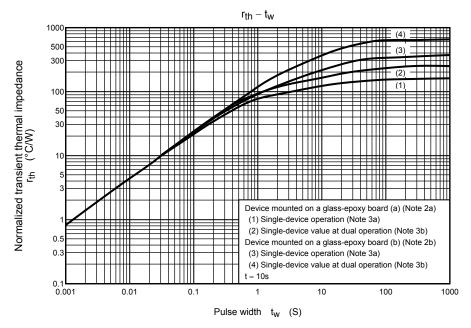




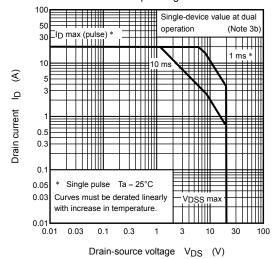












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