TEA1752T; TEA1752LT

GreenChip III SMPS control IC

Rev. 02 — 24 June 2010 Product data sheet

1. General description

The GreenChip III is the third generation of green Switched Mode Power Supply (SMPS) controller ICs. The TEA1752T and TEA1752LT combine a controller for Power Factor Correction (PFC) and a flyback controller. The high level of integration facilitates the design of a cost-effective power supply using a minimum number of external components.

The special built-in green functions provide high efficiency at all power levels. This applies to quasi-resonant operation at high power levels, quasi-resonant operation with valley skipping and reduced frequency operation at lower power levels. At low power levels, the PFC switches off to maintain high efficiency.

During low power conditions, the flyback controller switches to frequency reduction mode and limits the peak current to an adjustable minimum value. This will ensure high efficiency at low power and good standby power performance while minimizing audible noise from the transformer.

The TEA1752(L)T is a MultiChip Module (MCM), containing two chips. The proprietary high voltage BCD800 process which enables direct start-up from the rectified universal mains voltage in an effective and green way and a low voltage Silicon-On Insulator (SOI) which provides accurate, high speed protection functions and control.

The TEA1752(L)T enables highly efficient and reliable supplies with power requirements of up to 250 W to be designed easily and with a minimum number of external components.

2. Features and benefits

2.1 Distinctive features

- Integrated PFC and flyback controller
- Universal mains supply operation (70 V (AC) to 276 V (AC))
- Dual boost PFC with accurate maximum output voltage (NXP Semiconductors patented, US patent number: US7575280)
- High level of integration, resulting in a very low external component count and a cost-effective design
- Adjustable PFC switch-off delay

2.2 Green features

- On-chip start-up current source

2.3 PFC green features

- Valley/zero voltage switching for minimum switching losses (NXP Semiconductors patented, US patent number: US6256210)
- Frequency limitation to reduce switching losses
- PFC is switched off when a low load is detected at the flyback output

2.4 Flyback green features

- Valley switching for minimum switching losses (NXP Semiconductors patented, US patent number: US6256210)
- Frequency reduction with fixed minimum peak current at low power operation to maintain high-efficiency at low output power levels

2.5 Protection features

- Safe restart mode for system fault conditions
- Continuous mode protection by means of demagnetization detection for both converters (NXP Semiconductors patented, patent number: US5032967)
- UnderVoltage Protection (UVP) (foldback during overload)
- Accurate OverVoltage Protection (OVP) for PFC
- Accurate, adjustable OverVoltage Protection (OVP) for flyback converter (NXP Semiconductors patented, patent number: US6542386)
- Mains voltage independent OverPower Protection (OPP) (NXP Semiconductors patented, patent number: US6542386)
- Open control loop protection for both converters. The open-loop protection on the flyback converter is latched on the TEA1752LT and safe restart on the TEA1752T
- IC overtemperature protection
- Low and adjustable OverCurrent Protection (OCP) trip level for both converters
- General purpose input for latched protection, e.g. to be used for system OverTemperature Protection (OTP)

3. Applications

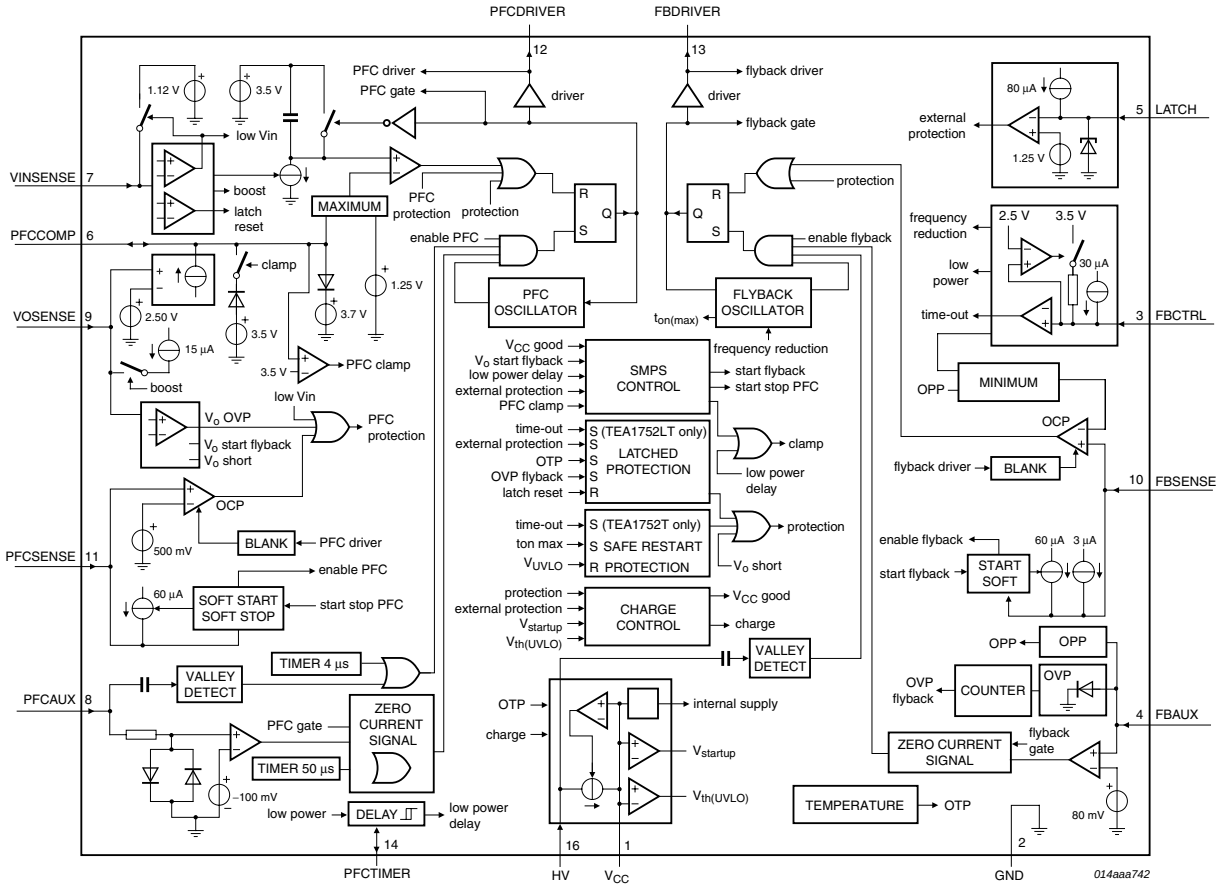
- All applications requiring efficient and cost-effective power supply solutions to 250 W. Notebook adapters in particular can benefit from the high level of integration

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1752T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TEA1752LT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Block diagram



Remark:

TEA1752LT time-out is latched.

TEA1752T time-out is safe restart.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

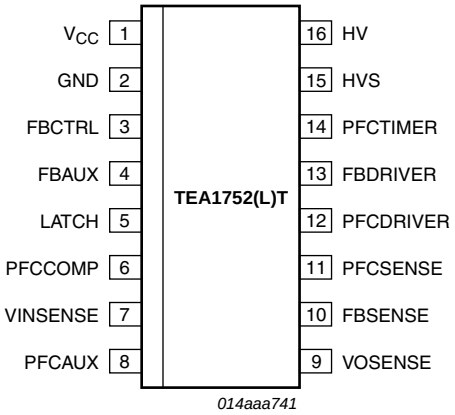


Fig 2. Pin configuration: TEA1752(L)T (SOT109-1)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{CC}	1	supply voltage
GND	2	ground
FBCTRL	3	control input for flyback
FBAUX	4	input from auxiliary winding for demagnetization timing and overvoltage protection for flyback
LATCH	5	general purpose protection input
PFCCOMP	6	frequency compensation pin for PFC
VINSENSE	7	sense input for mains voltage
PFCAUX	8	input from auxiliary winding for demagnetization timing for PFC and valley sensing of the PFC part
VOSENSE	9	sense input for PFC output voltage
FBSENSE	10	programmable current sense input for flyback
PFCSENSE	11	programmable current sense input for PFC
PFCDRIVER	12	gate driver output for PFC
FBDRIVER	13	gate driver output for flyback
PFCTIMER	14	delay timer pin for PFC on/off control
HVS	15	high voltage safety spacer, not connected
HV	16	high voltage start-up and valley sensing of flyback part

7. Functional description

7.1 General control

The TEA1752(L)T contains controllers for a power factor correction circuit and for a flyback circuit. A typical configuration is shown in Figure 3.

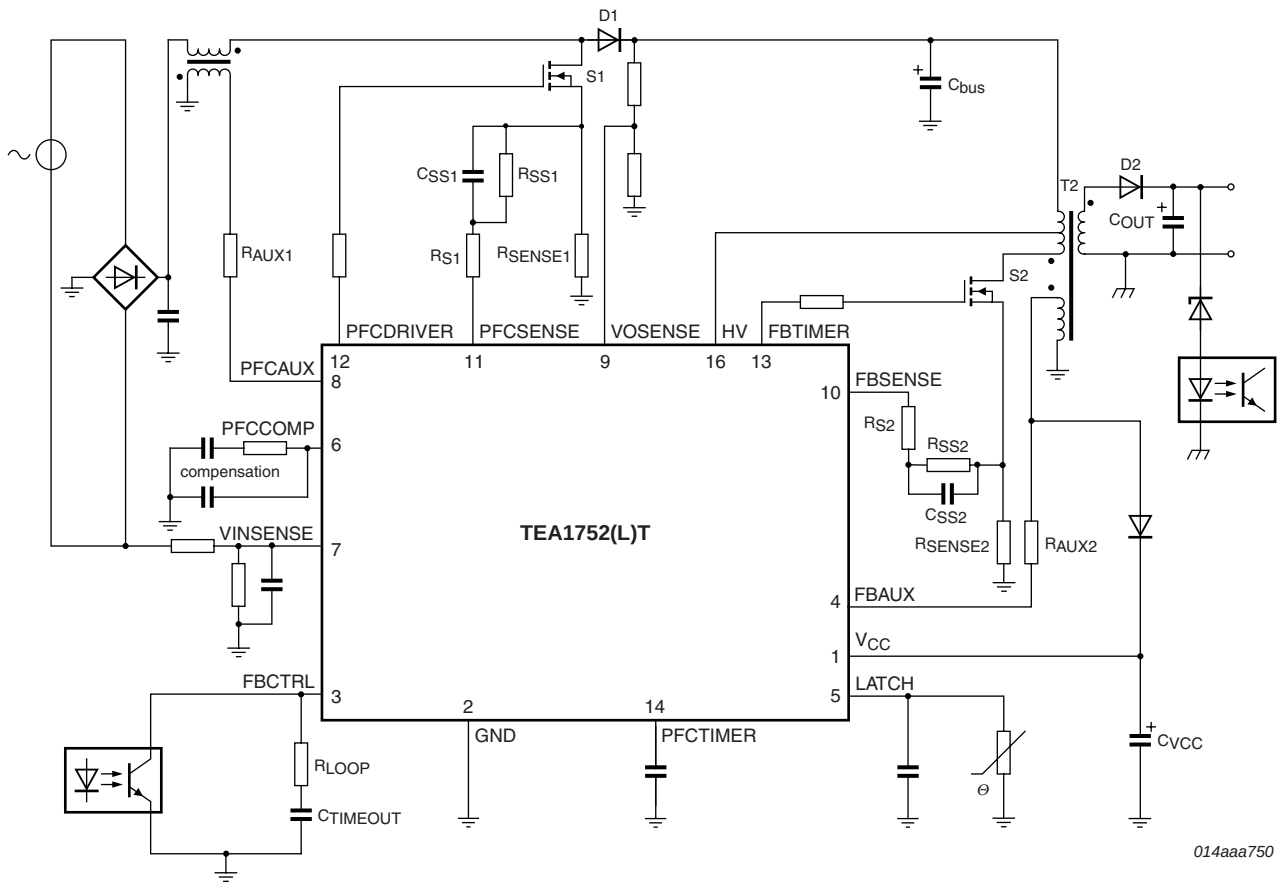


Fig 3. Typical configuration

7.1.1 Start-up and UnderVoltage LockOut (UVLO)

Initially the capacitor on the V_{CC} pin is charged from the high voltage mains via the HV pin.

If V_{CC} is lower than V_{trip}, the charge current is low. This protects the IC if the V_{CC} pin is shorted to ground. The charge current above V_{trip} is increased until V_{CC} reaches $V_{th(UVLO)}$ to achieve a short start-up time. If V_{CC} is between $V_{th(UVLO)}$ and $V_{startup}$, the charge current is low again, ensuring a low duty cycle during fault conditions.

The control logic activates the internal circuitry and switches off the HV charge current when the voltage on pin V_{CC} passes the $V_{startup}$ level. The LATCH pin current source is then activated and the soft start capacitors on pins PFCSENSE and FBSENSE are charged and the clamp circuit on pin PFCCOMP is activated. When the LATCH pin voltage exceeds $V_{en(LATCH)}$, the PFCCOMP pin voltage exceeds $V_{en(PFCCOMP)}$ and the soft start capacitor on pin PFCSENSE pin is charged, the PFC circuit is activated. The flyback

converter is also activated (providing the soft start capacitor on the FBSENSE pin is charged). The flyback converter output voltage is then regulated to its nominal value. The IC supply is taken over by the auxiliary winding of the flyback converter. See Figure 4.

If during start-up the LATCH pin does not reach the $V_{en(LATCH)}$ level before V_{CC} reaches $V_{th(UVLO)}$, the LATCH pin output is deactivated and the charge current is switched on again.

When the flyback converter is started, the voltage on pin FBCTRL is monitored. If the flyback converter output voltage does not reach its intended regulation level in a predefined time, the voltage on pin FBCTRL reaches the $V_{to(FBCTRL)}$ level and an error is assumed. The TEA1752T then initiates a safe restart, while in the TEA1752LT the protection is latched.

When one of the protection functions is activated, both converters stop switching and the V_{CC} voltage drops to $V_{th(UVLO)}$. A latched protection recharges the capacitor C_{VCC} via the HV pin, but does not restart the converters. For a safe restart protection, the capacitor is recharged via the HV pin and the device restarts. See Figure 1.

In the event of an overvoltage protection of the PFC circuit where $V_{VOSENSE} > V_{ovp(VOSENSE)}$, the PFC controller stops switching until the VOSENSE pin voltage drops back below $V_{ovp(VOSENSE)}$. If a mains undervoltage is detected where $V_{VINSENSE} < V_{stop(VINSENSE)}$, the PFC controller stops switching until $V_{VINSENSE} > V_{start(VINSENSE)}$.

When the voltage on pin V_{CC} drops below the undervoltage lockout level, both controllers stop switching and reenter the safe restart mode. In this mode the driver outputs are disabled and the V_{CC} pin voltage is recharged via the HV pin.

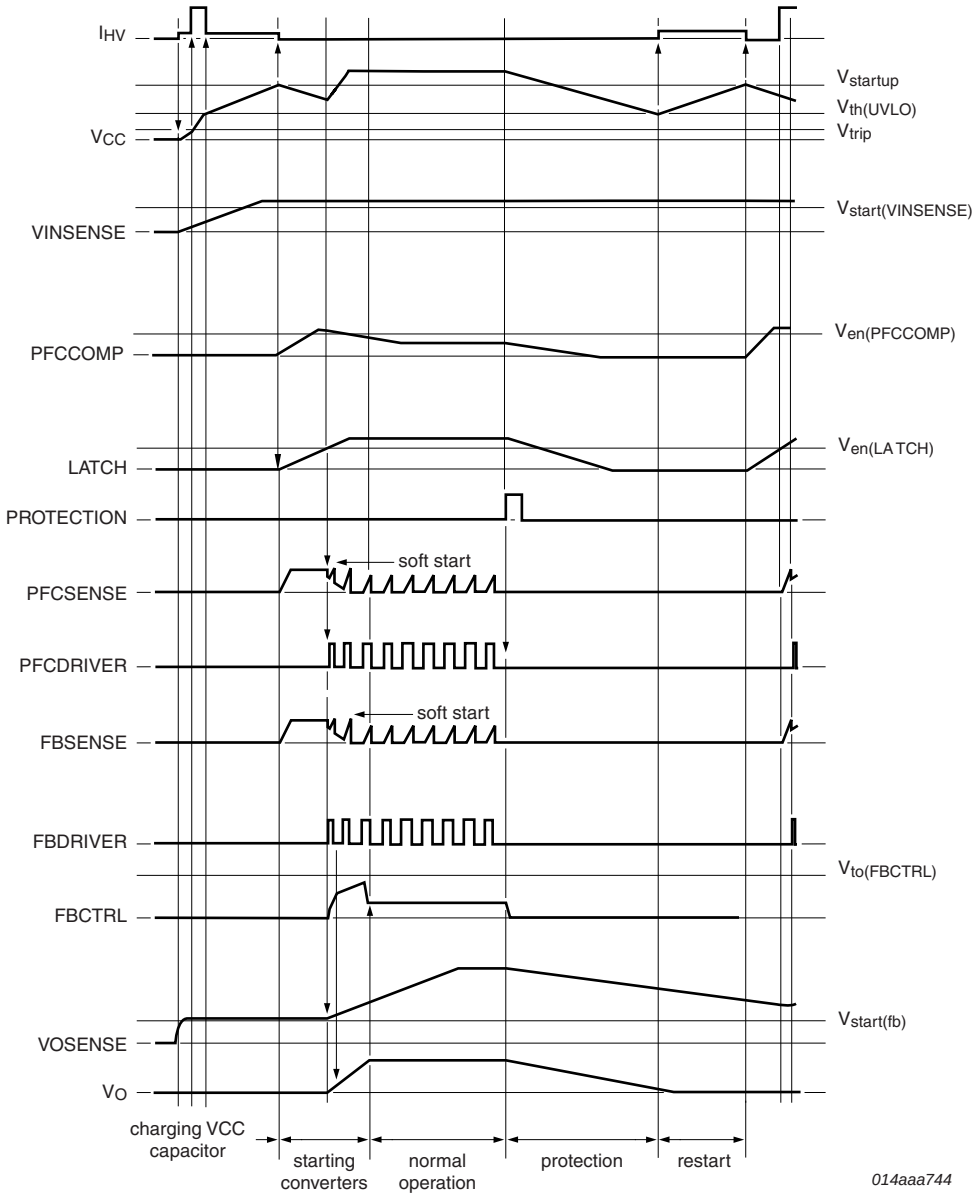


Fig 4. Start-up sequence, normal operation and restart sequence

7.1.2 Supply management

All internal control voltages are derived from a temperature compensated and trimmed on-chip band gap circuit. Internal reference currents are derived from a temperature compensated and trimmed on-chip current reference circuit.

7.1.3 Latch input

Pin LATCH is a general purpose input pin, which can be used to switch off both converters. The pin sources a current $I_{O(LATCH)}$ (80 μA typical). Switching off both converters is stopped as soon as the voltage on this pin drops below 1.25 V.

At initial start-up the switching is inhibited until the capacitor on the LATCH pin is charged above 1.35 V (typical). No internal filtering is carried out on this pin. An internal zener clamp of 2.9 V (typical) protects this pin from excessive voltages.

7.1.4 Fast latch reset

In a typical application the mains supply can be interrupted briefly to reset the latched protection. The PFC bus capacitor, C_{bus}, does not need to discharge for this latched protection to reset.

Typically the PFC bus capacitor, C_{bus}, must discharge for the V_{CC} to drop to this reset level. When the latched protection is set, the VINSENSE clamping circuit is disabled. See Section 7.2.10. When the VINSENSE voltage drops below 0.75 V (typical) then increases to 0.87 V (typical), the latched protection is reset.

The latched protection is also reset by removing the voltage on pins V_{CC} and HV.

7.1.5 OverTemperature Protection (OTP)

Integrated overtemperature protection ensures the IC stops switching if the junction temperature exceeds the thermal temperature shutdown limit.

Capacitor C_{VCC} will not recharge from the HV mains while OTP is active. The OTP circuit is supplied from the HV pin if the V_{CC} supply voltage is insufficient.

OTP is a latched protection that can be reset either by removing the voltage on pins V_{CC} and HV or by the fast latch reset function. See Section 7.1.4.

7.2 Power Factor Correction circuit (PFC)

The power factor correction circuit operates in quasi-resonant or discontinuous conduction mode with valley switching. The next primary stroke only starts when the previous secondary stroke has ended and the voltage across the PFC MOSFET has reached a minimum value. The voltage on the PFCAUX pin is used to detect transformer demagnetization and the minimum voltage across the external PFC MOSFET switch.

7.2.1 t_{on} control

The power factor correction circuit is operated in t_{on} control. The resulting mains harmonic reduction of a typical application is well within the class-D requirements.

7.2.2 Valley switching and demagnetization (PFCAUX pin)

The PFC MOSFET is switched on after the transformer has been demagnetized. Internal circuitry connected to the PFCAUX pin detects the end of the secondary stroke. It also detects the voltage across the PFC MOSFET. The next stroke is started when the voltage across the PFC MOSFET is at its minimum in order to reduce switching losses and ElectroMagnetic Interference (EMI) (valley switching).

If no demagnetization signal is detected on the PFCAUX pin, the controller generates a Zero Current Signal (ZCS), 50 μs (typical), after the last PFCGATE signal.

If no valley signal is detected on the PFCAUX pin, the controller generates a valley signal, 4 μs (typical), after demagnetization was detected.

It is advisable to add a 5 kΩ series resistor to this pin to provide surge protection for the internal circuitry against events such as lightning surge. To prevent incorrect switching due to external disturbance, this resistor should be placed as close as possible to the IC on the printed-circuit board.

7.2.3 Frequency limitation

To optimize the transformer and minimize switching losses, the switching frequency is limited to $f_{sw(PFC)max}$. If the frequency for quasi-resonant operation is above the $f_{sw(PFC)max}$ limit, the system switches over to discontinuous conduction mode. The PFC MOSFET is then only switched on at a minimum voltage across the switch (valley switching).

7.2.4 Mains voltage compensation (VINSENSE pin)

The mathematical equation for the transfer function of a power factor corrector contains the square of the mains input voltage. In a typical application this results in a low bandwidth for low mains input voltages, while at high mains input voltages the Mains Harmonic Reduction (MHR) requirements may be hard to meet.

The TEA1752(L)T incorporates a correction circuit to compensate for the mains input voltage influence. The average input voltage is measured via the VINSENSE pin and this information is fed to an internal compensation circuit. With this compensation it is possible to keep the regulation loop bandwidth constant over the full mains input range, yielding a fast transient response on load steps, while still complying with class-D MHR requirements.

In a typical application, the regulation loop bandwidth is set by a resistor and two capacitors on the PFCCOMP pin.

7.2.5 Soft start-up (pin PFCSENSE)

To prevent audible transformer noise at start-up or during hiccup, the transformer peak current is increased slowly by the soft start function. This can be achieved by inserting R_{SS1} and C_{SS1} between pin PFCSENSE and the current sense resistor, R_{SENSE1}. An internal current source charges the capacitor to $V_{PFCSENSE} = I_{start(soft)PFC} \times R_{SS1}$. The voltage is limited to $V_{start(soft)PFC}$.

The start level and time constant of the increasing primary current level can be adjusted externally by changing the values of R_{SS1} and C_{SS1}.

$$\tau softstart = 3 \times R_{SS1} \times C_{SS1}$$

The charging current $I_{start(soft)PFC}$ flows if the voltage on pin PFCSENSE is lower than 0.5 V (typical). If the voltage on pin PFCSENSE exceeds 0.5 V, the soft start current source limits current $I_{start(soft)PFC}$. When the PFC starts switching, the $I_{start(soft)PFC}$ current source is switched off (see Figure 5).

Resistor R_{SS1} and capacitor C_{SS1} are also used to prevent audible noise, when the PFC is switched off by performing a soft stop.

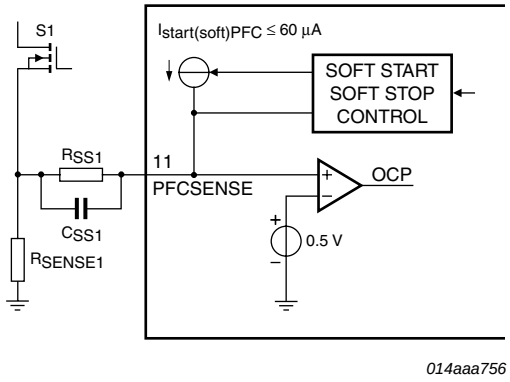


Fig 5. Soft start-up of PFC

7.2.6 Low power mode

When the output power of the flyback converter (see Section 7.3) is low, the flyback converter switches to frequency reduction mode. When the internal switching frequency limit of the flyback drops below 48 kHz (typical), the power factor correction circuit is switched off to maintain high efficiency. The switch-off can be delayed by connecting a capacitor to the PFCTIMER pin (see Section 7.2.7).

During low power mode operation the PFCCOMP pin is clamped to a minimum voltage of 3.5 V (typical) and a maximum voltage of 3.7 V (typical). The lower clamp voltage limits the maximum power delivered when the PFC is switched on again. The upper clamp voltage ensures the PFC can return to its normal regulation point in a limited amount of time when returning from low power mode.

The power factor correction circuit restores normal operation when the internal switching frequency limit of the flyback converter rises above 86 kHz (typical).

7.2.7 PFC off delay (pin PFCTIMER)

When the internal switching frequency limit of the flyback controller drops below 48 kHz (typical), the PFC is switched off. To prevent the PFC from switching off due to a fast changing load at the flyback output, the PFC switch-off can be delayed by connecting a capacitor to the PFCTIMER pin.

When the flyback controller detects a low power, it enters frequency reduction mode and the IC outputs a 10 μA (typical) current to the PFCTIMER pin. When the voltage on the PFCTIMER pin reaches 3.6 V (typical), the PFC is switched off by performing a soft stop.

When the flyback controller part leaves the frequency reduction mode, a switch discharges the PFCTIMER pin capacitor. When the voltage on the PCTIMER pin drops below 1.27 V (typical), the PFC is switched on (see Figure 6).

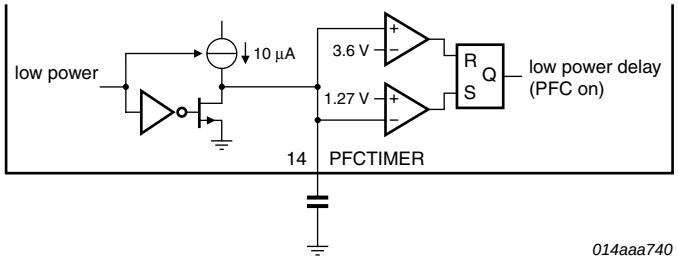


Fig 6. PFC start/stop via PFCTIMER pin

7.2.8 Dual boost PFC

The PFC output voltage depends on the mains input voltage. The mains input voltage is measured via the VINSENSE pin. Current is sourced from the VOSENSE pin if the voltage on the VINSENSE pin drops below 2.2 V (typical). To ensure a stable switch-over, a 200 mV transition region is inserted around the 2.2 V, see Figure 7.

For low VINSENSE input voltages, the output current is 15 µA (typical). This output current, in combination with the resistors on the VOSENSE pin, sets a lower PFC output voltage level at low mains voltages. At high mains input voltages the current is switched to zero. The PFC output voltage will then be at its maximum. As this current is zero in this situation, it does not effect the accuracy of the PFC output voltage.

For proper switch-off behavior, the VOSENSE current is switched to its maximum value, (15 µA (typical)), as soon as the voltage on pin VOSENSE drops below 2.1 V (typical).

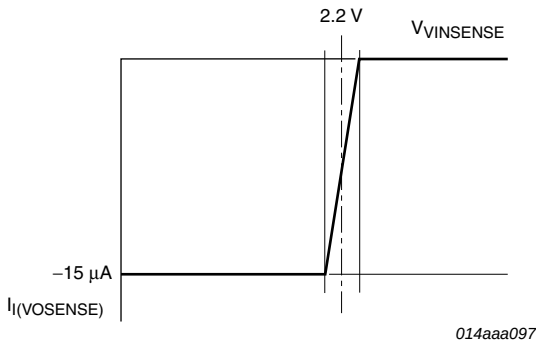


Fig 7. Voltage to current transfer function for dual boost PFC

7.2.9 Overcurrent protection (PFCSENSE pin)

The maximum peak current is limited cycle-by-cycle by sensing the voltage across an external sense resistor, R_{SENSE1}, on the source of the external MOSFET. The voltage is measured via the PFCSENSE pin.

7.2.10 Mains undervoltage lockout/brownout protection (VINSENSE pin)

To prevent the PFC from operating at very low mains input voltages, the voltage on the VINSENSE pin is continuously monitored. When the voltage on this pin drops below the $V_{stop(VINSENSE)}$ level, PFC switching is stopped.

The voltage on pin VINSENSE is clamped to a minimum value, $V_{start(VINSENSE)} + \Delta V_{pu(VINSENSE)}$, for a fast restart when mains input voltage is restored after a mains dropout.

7.2.11 Overvoltage protection (VOSENSE pin)

An overvoltage protection circuit is incorporated to prevent output overvoltage during load steps and mains transients.

When voltage on the VOSENSE pin exceeds the $V_{ovp(VOSENSE)}$ level, switching of the power factor correction circuit is inhibited. Switching of the PFC recommences when the VOSENSE pin voltage drops back below the $V_{ovp(VOSENSE)}$ level.

When the resistor between pin VOSENSE and ground is open, the overvoltage protection is also triggered.

7.2.12 PFC open-loop protection (VOSENSE pin)

The power factor correction circuit will not start switching until the voltage on the VOSENSE pin is above the $V_{th(ol)(VOSENSE)}$ level. This protects the circuit from open-loop and VOSENSE short circuit situations.

7.2.13 Driver (pin PFCDRIVER)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically −500 mA and a current sink capability of typically 1.2 A. This enables fast turn-on and turn-off of the power MOSFET for efficient operation.

7.3 Flyback controller

The TEA1752(L)T includes a controller for a flyback converter. The flyback converter operates in quasi-resonant or discontinuous conduction mode with valley switching. The auxiliary winding of the flyback transformer provides demagnetization detection and powers the IC after start-up.

7.3.1 Multimode operation

The TEA1752(L)T flyback controller can operate in several modes (see Figure 8).

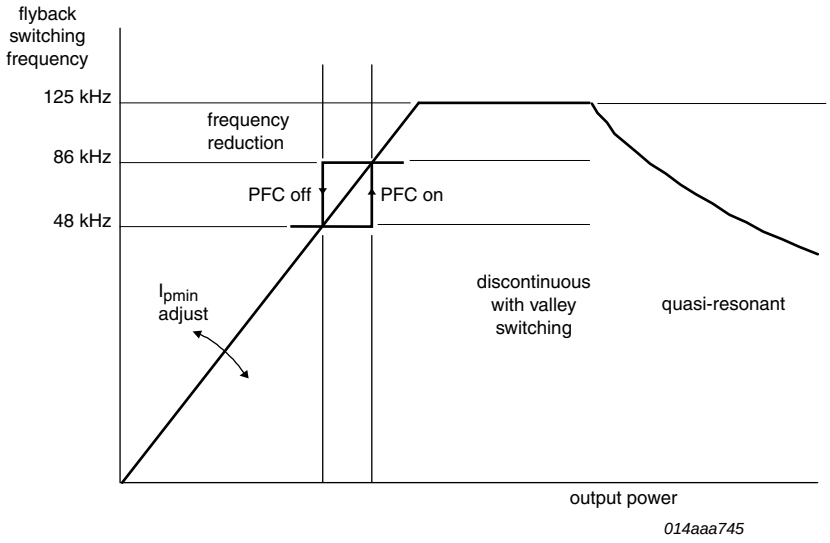


Fig 8. Multimode operation flyback

At high output power the converter switches to quasi-resonant mode. The next converter stroke is started after demagnetization of the transformer current. In quasi-resonant mode switching losses are minimized as the converter only switches on when the voltage across the external MOSFET is at its minimum (valley switching, see Section 7.3.2).

To prevent high frequency operation at lower loads, the quasi-resonant operation changes to discontinuous mode operation with valley skipping, in which the EMI switching frequency is limited to $f_{sw(fb)max}$ (125 kHz typical). Again, the external MOSFET is only switched on when the voltage across the MOSFET is at its minimum.

At very low power and standby levels the frequency is reduced by a Voltage Controlled Oscillator (VCO). The minimum frequency can be reduced to zero. During frequency reduction mode the primary peak current is kept constant at a minimum adjustable level to control the PFC on-power and off-power levels. I_{pmin} in frequency reduction mode will generally be greater than I_{pmax} / 4, so a high efficiency at low loads is guaranteed. As the primary peak current is low in frequency reduction operation, no audible noise is noticeable at switching frequencies in the audible range. Valley switching is also active in this mode.

In frequency reduction mode the PFC controller is switched off and the flyback maximum frequency changes linearly with the control voltage on the FBCTRL pin (see Figure 9). For stable on and off switching of the PFC, hysteresis has been added. At no load operation the switching frequency can be reduced to (almost) zero.

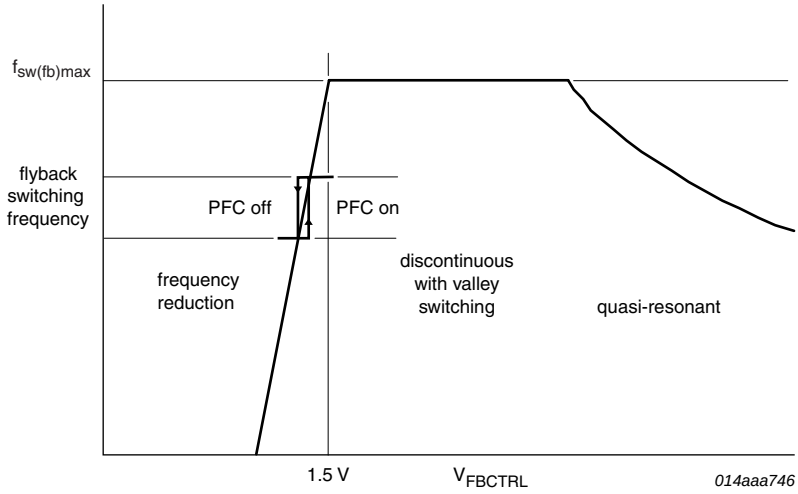


Fig 9. Frequency control of flyback part

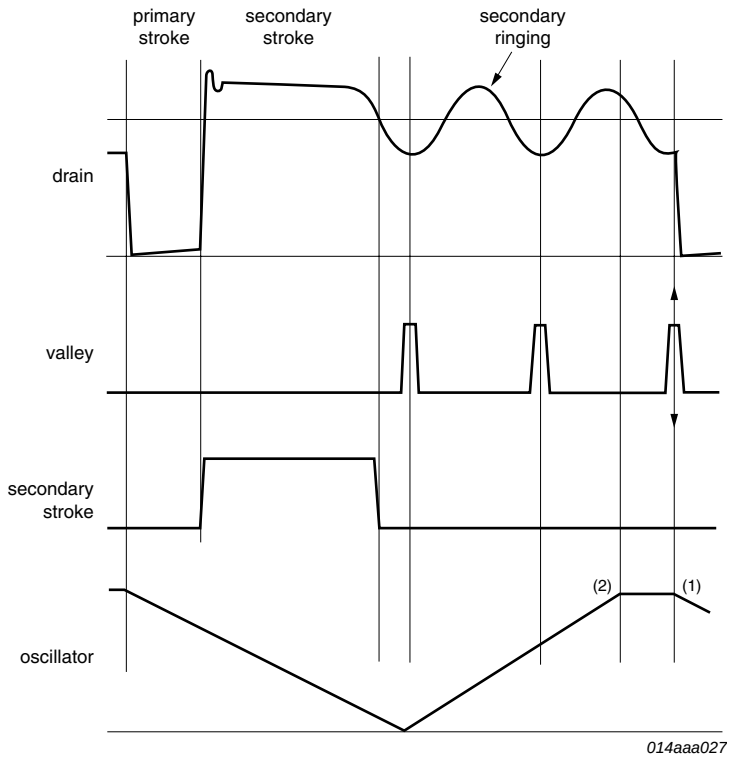
7.3.2 Valley switching (HV pin)

Figure 10 shows that a new cycle starts when the external MOSFET is activated. After the on-time (determined by the FBSENSE voltage and the FBCTRL voltage), the MOSFET is switched off and the secondary stroke starts. After the secondary stroke, the drain voltage shows an oscillation with a frequency of approximately $\frac{1}{(2 \times \pi \times \sqrt{(L_p \times C_d)})}$ where L_p is the primary self-inductance of the flyback transformer and C_d is the capacitance on the drain node.

When the internal oscillator voltage is high again and the secondary stroke has ended, the circuit waits for the lowest drain voltage before starting a new primary stroke. Figure 10 shows the drain voltage, valley signal, secondary stroke signal and the internal oscillator signal.

Valley switching allows high frequency operation as capacitive switching losses are reduced (see Equation 1). High frequency operation makes small and cost-effective magnetics possible.

$$\left(P = \frac{1}{2} \times C_d \times V^2 \times f\right) \quad (1)$$



(1) Start of new cycle at lowest drain voltage.

(2) Start of new cycle in a classical Pulse Width Modulation (PWM) system without valley detection.

Fig 10. Signals for valley switching

7.3.3 Current mode control (FBSENSE pin)

Current mode control is used for the flyback converter for its good line regulation.

The primary current is sensed by the FBSENSE pin across external resistor R_{SENSE2} (see Figure 3) and compared with an internal control voltage. The internal control voltage is proportional to the FBCTRL pin voltage (see Figure 11).

The FBSENSE pin outputs a current of 3 μA (typical). This current runs through resistors R_{S2} and R_{SS2} from the FBSENSE pin to the sense resistor, R_{SENSE2} and creates an offset voltage (See Figure 3). With this offset voltage, the minimum peak current of the flyback can be adjusted. Adjusting the minimum peak current level, will change the frequency reduction slope (See Figure 8).

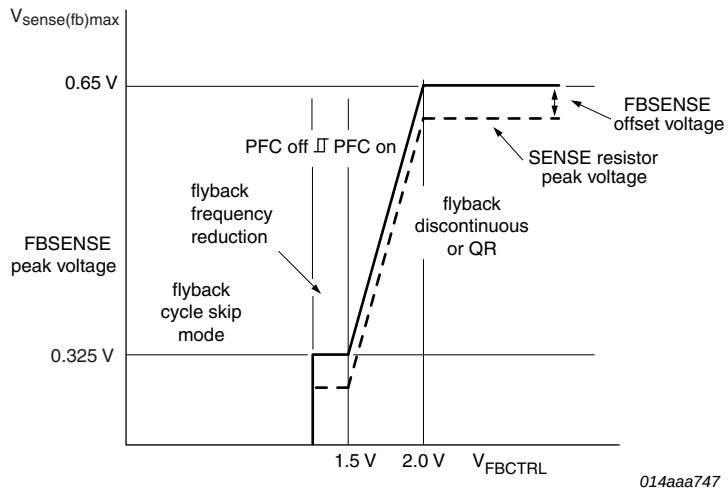


Fig 11. Peak current control of flyback part

7.3.4 Demagnetization (FBAUX pin)

The system is always in quasi-resonant or discontinuous conduction mode. The internal oscillator does not start a new primary stroke until the previous secondary stroke has ended.

Demagnetization features a cycle-by-cycle output short circuit protection by immediately lowering the frequency (longer off-time), thus reducing the power level.

Demagnetization recognition is suppressed during the first $t_{sup(xfmr\_ring)}$ time (2 μs typical). This suppression may be necessary at low output voltages and at start-up and in applications where the transformer has a large leakage inductance.

If pin FBAUX is open circuit or not connected, a fault condition is assumed and the converter stops operating immediately. Operation restarts as soon as the fault condition is removed.

7.3.5 Flyback control/time-out (FBCTRL pin)

The pin FBCTRL is connected to an internal voltage source of 3.5 V via an internal resistor (typical resistance is 3 kΩ). As soon as the voltage on this pin rises above 2.5 V (typical), this connection is disabled. Above 2.5 V the pin is biased with a small current. When the voltage on this pin rises above 4.5 V (typical), a fault is assumed and switching is inhibited. In the TEA1752T a restart will then be made, while in the TEA1752LT the protection will be latched.

When a small capacitor is connected to this pin, a time-out function can be created to protect against an open control loop situation. (see Figure 12 and Figure 13) The time-out function can be disabled by connecting a resistor (100 kΩ) to ground on the FBCTRL pin.

If the pin is shorted to ground, switching of the flyback controller is inhibited.

In normal operating conditions, when the converter is regulating the output voltage, the voltage on the FBCTRL pin is between 1.4 V (typical) and 2.0 V (typical) from minimum to maximum output power.

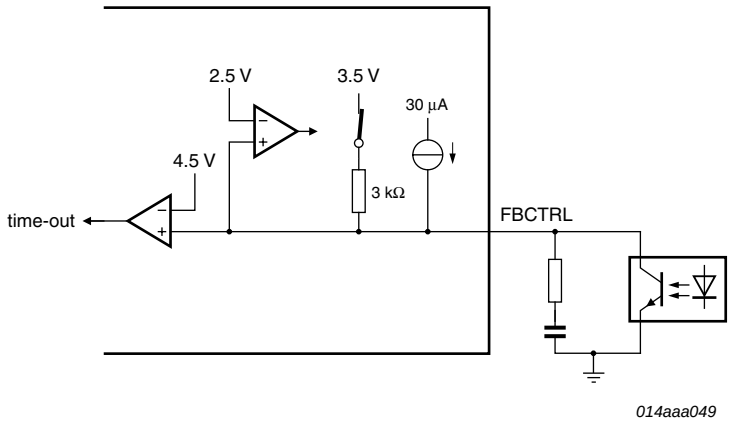


Fig 12. Time-out protection circuit

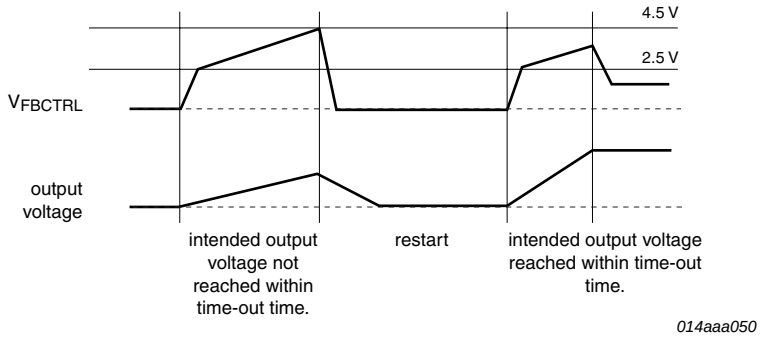


Fig 13. Time-out protection (signals), safe restart in the TEA1752T

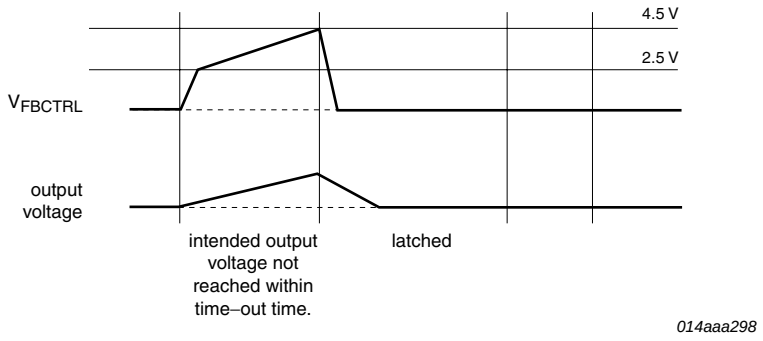


Fig 14. Time-out protection (signals), latched in the TEA1752LT

7.3.6 Soft start-up (pin FBSENSE)

To prevent audible transformer noise during start-up, the transformer peak current is slowly increased by the soft start function. This can be achieved by inserting a resistor (R_{SS2}) and a capacitor (C_{SS2}) between pin 10 (FBSENSE) and the current sense resistor.

An internal current source charges the capacitor to V = $I_{start(soft)fb} \times R_{SS2}$, with a maximum of approximately 0.63 V.

The start level and the time constant of the increasing primary current level can be externally adjusted by changing the values of R_{SS2} and C_{SS2}.

$$\tau softstart = 3 \times R_{SS2} \times C_{SS2}$$

The soft start current $I_{start(soft)fb}$ is switched on when V_{CC} reaches $V_{startup}$. When the voltage on pin FBSENSE has reached 0.63 V the flyback converter starts switching.

The charging current $I_{start(soft)PFC}$ flows if voltage on pin FBSENSE is below approximately 0.63 V. If the voltage on pin FBSENSE exceeds 0.63 V, the soft start current source limits the current. Once the flyback converter has started, the soft start current source is switched off.

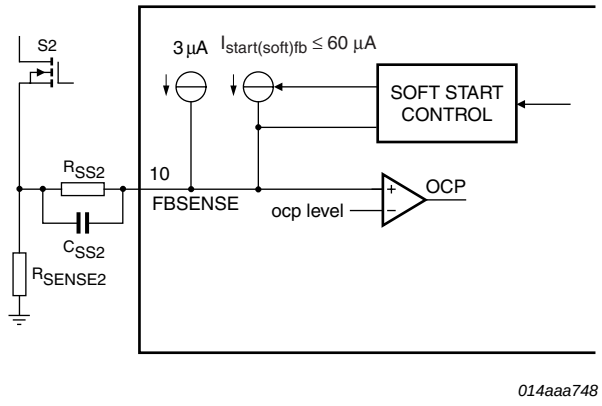


Fig 15. Soft start-up of flyback

7.3.7 Maximum on-time

The flyback controller limits the 'on-time' of the external MOSFET to 40 µs (typical). When the 'on-time' is longer than 40 µs, the IC stops switching and enters the safe restart mode.

7.3.8 Overvoltage protection (FBAUX pin)

An output overvoltage protection is implemented in the GreenChip III series. This operates for the TEA1752(L)T by sensing the auxiliary voltage via the current flowing into pin FBAUX during the secondary stroke. The auxiliary winding voltage is a well defined replica of the output voltage. Voltage spikes are averaged by an internal filter.

If the output voltage exceeds the OVP trip level, an internal counter starts counting subsequent OVP events. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. If the output voltage exceeds the OVP trip level a few times and then not again in a subsequent cycle, the internal counter counts down at twice the speed it uses when counting up. However, when typically eight cycles of subsequent OVP events are detected, the IC assumes a true OVP and the OVP circuit switches the power MOSFET off. As the protection is latched, the converter only restarts after the internal latch is reset. In a typical application the mains should be interrupted to reset the internal latch.

The output voltage $V_{o(OVP)}$ at which the OVP function trips, can be set by the demagnetization resistor, R_{FBAUX} :

$$V_{o(OVP)} = \frac{N_s}{N_{aux}}(I_{ovp(FBAUX)} \times R_{FBAUX} + V_{clamp(FBAUX)})$$

where N_s is the number of secondary turns and N_{aux} is the number of auxiliary turns of the transformer. The current $I_{ovp(FBAUX)}$ is internally trimmed.

The value of R_{FBAUX} can be adjusted to the turns ratio of the transformer, making an accurate OVP detection possible.

7.3.9 Overcurrent protection (FBSENSE pin)

The primary peak current in the transformer is accurately measured cycle-by-cycle using external sense resistor R_{SENSE2}. The OCP circuit limits the voltage on pin FBSENSE to an internal level (see Section 7.3.3). The OCP detection is suppressed during the leading edge blanking period, t_{leb}, to prevent false triggering caused by switch-on spikes.

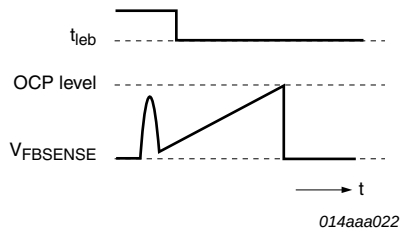


Fig 16. OCP leading edge blanking

7.3.10 Overpower protection

During the primary stroke of the flyback converter its input voltage is measured by sensing the current that is drawn from pin FBAUX.

This information is used to adjust the peak drain current of the flyback converter measured via pin FBSENSE. The internal compensation is such that an almost input voltage independent maximum output power can be realized.

The OPP curve is given in Figure 17.

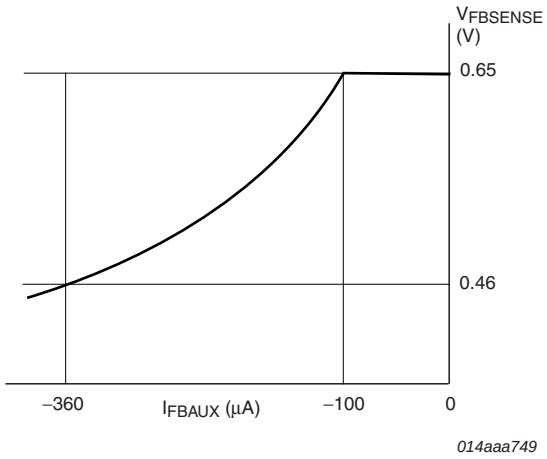


Fig 17. Overpower protection curve

7.3.11 Driver (pin FBDRIVER)

The driver circuit to the gate of the external power MOSFET has a current sourcing capability of typically −500 mA and a current sink capability of typically 1.2 A. This enables fast turn-on and turn-off of the power MOSFET for efficient operation.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{CC}	supply voltage		−0.4	+38	V
V_{LATCH}	voltage on pin LATCH	current limited	−0.4	+5	V
V_{FBCTRL}	voltage on pin FBCTRL		−0.4	+5	V
$V_{PFCCOMP}$	voltage on pin PFCCOMP		−0.4	+5	V
$V_{VINSENSE}$	voltage on pin VINSENSE		−0.4	+5	V
$V_{VOSENSE}$	voltage on pin VOSENSE		−0.4	+5	V
V_{PFCAUX}	voltage on pin PFCAUX		−25	+25	V
$V_{FBSENSE}$	voltage on pin FBSENSE	current limited	−0.4	+5	V
$V_{PFCSENSE}$	voltage on pin PFCSENSE	current limited	−0.4	+5	V
$V_{PFCTIMER}$	voltage on pin PFCTIMER		−0.4	+5	V
V_{HV}	voltage on pin HV		−0.4	+650	V
Currents					
I_{FBCTRL}	current on pin FBCTRL		−3	0	mA
I_{FBAUX}	current on pin FBAUX		−1	+1	mA
$I_{PFCSENSE}$	current on pin PFCSENSE		−1	+10	mA
$I_{FBSENSE}$	current on pin FBSENSE		−1	+10	mA
$I_{FBDRIVER}$	current on pin FBDRIVER	duty cycle < 10 %	−0.8	+2	A

Table 3. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$I_{PFCDRIVER}$	current on pin PFCDRIVER	duty cycle < 10 %		–0.8	+2	A
I_{HV}	current on pin HV			-	8	mA
General						
P_{tot}	total power dissipation	T_{amb} < 75 °C		-	0.6	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–40	+150	°C
ESD						
V_{ESD}	electrostatic discharge voltage	class 1				
		human body model				
		pins 1 to 13	[1]	-	2000	V
		pin 16 (HV)	[1]	-	1500	V
		machine model	[2]	-	200	V
		charged device model		-	500	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; JEDEC test board	124	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air; JEDEC test board	37	K/W

10. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up current source (pin HV)						
I_{HV}	current on pin HV	V_{HV} > 80 V				
		V_{CC} < V_{trip}; $V_{th(UVLO)}$ < V_{CC} < $V_{startup}$	-	1.0	-	mA
		V_{trip} < V_{CC} < $V_{th(UVLO)}$	-	5.4	-	mA
		with auxiliary supply	8	20	40	μA
V_{BR}	breakdown voltage		650	-	-	V
Supply voltage management (pin V_{CC})						
V_{trip}	trip voltage		0.55	0.65	0.75	V

Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{startup}$	start-up voltage		21	22	23	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		14	15	16	V
$V_{start(hys)}$	hysteresis of start voltage	during start-up phase	-	300	-	mV
V_{hys}	hysteresis voltage	$V_{startup} - V_{th(UVLO)}$	6.3	7	7.7	V
$I_{ch(low)}$	low charging current	V_{HV} > 80 V; $V_{CC} < V_{trip}$ or $V_{th(UVLO)} < V_{CC} < V_{startup}$	–1.2	–1.0	–0.8	mA
$I_{ch(high)}$	high charging current	V_{HV} > 80 V; $V_{trip} < V_{CC} < V_{th(UVLO)}$	–4.6	–5.4	–6.3	mA
$I_{CC(oper)}$	operating supply current	no load on pins FBDRIVER and PFCDRIVER	2.25	3	3.75	mA
Input voltage sensing PFC (pin VINSENSE)						
$V_{stop(VINSENSE)}$	stop voltage on pin VINSENSE		0.86	0.89	0.92	V
$V_{start(VINSENSE)}$	start voltage on pin VINSENSE		1.11	1.15	1.19	V
$\Delta V_{pu(VINSENSE)}$	pull-up voltage difference on pin VINSENSE	active after $V_{stop(VINSENSE)}$ is detected	-	–100	-	mV
$I_{pu(VINSENSE)}$	pull-up current on pin VINSENSE	active after $V_{stop(VINSENSE)}$ is detected	–55	–47	–40	µA
$V_{mvc(VINSENSE)max}$	maximum mains voltage compensation voltage on pin VINSENSE		4.0	-	-	V
V_{flr}	fast latch reset voltage	active after $V_{th(UVLO)}$ is detected	-	0.75	-	V
$V_{flr(hys)}$	hysteresis of fast latch reset voltage		-	0.12	-	V
$I_{I(VINSENSE)}$	input current on pin VINSENSE	$V_{VINSENSE} > V_{stop(VINSENSE)}$ after $V_{start(VINSENSE)}$ is detected	5	33	100	nA
$V_{bst(dual)}$	dual boost voltage	current switch-over point	-	2.2	-	V
		switch-over region	-	200	-	mV
Loop compensation PFC (pin PFCCOMP)						
g_m	transconductance	$V_{VOSENSE}$ to $I_{O(PFCCOMP)}$	60	80	100	µA/V
$I_{O(PFCCOMP)}$	output current on pin PFCCOMP	$V_{VOSENSE}$ = 2.0 V	33	39	45	µA
		$V_{VOSENSE}$ = 3.3 V	–45	–39	–33	µA
$V_{en(PFCCOMP)}$	enable voltage on pin PFCCOMP		-	3.5	-	V
$V_{clamp(PFCCOMP)}$	clamp voltage on pin PFCCOMP	low power mode; PFC off; lower clamp voltage [1]	-	3.5	-	V
		upper clamp voltage [1]	-	3.7	-	V
$V_{ton(PFCCOMP)zero}$	zero on-time voltage on pin PFCCOMP		3.4	3.5	3.6	V
$V_{ton(PFCCOMP)max}$	maximum on-time voltage on pin PFCCOMP		1.20	1.25	1.30	V

Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pulse width modulator PFC							
$t_{on(PFC)}$	PFC on-time	$V_{VINSENSE}$ = 3.3 V; $V_{PFCCOMP} = V_{ton(PFCCOMP)max}$		3.6	4.5	5.0	µs
		$V_{VINSENSE}$ = 0.9 V; $V_{PFCCOMP} = V_{ton(PFCCOMP)max}$		30	40	53	µs
Output voltage sensing PFC (pin VOSENSE)							
$V_{th(ol)(VOSENSE)}$	open-loop threshold voltage on pin VOSENSE			-	1.15	-	V
$V_{reg(VOSENSE)}$	regulation voltage on pin VOSENSE	for $I_{O(PFCCOMP)}$ = 0		2.475	2.500	2.525	V
$V_{ovp(VOSENSE)}$	overvoltage protection voltage on pin VOSENSE			2.60	2.63	2.67	V
$I_{bst(dual)}$	dual boost current	$V_{VINSENSE} < V_{bst(dual)}$ or $V_{VOSENSE}$ < 2.1 V		-	–15	-	µA
		$V_{VINSENSE} > V_{bst(dual)}$		-	–30	-	nA
Overcurrent protection PFC (pin PFCSENSE)							
$V_{sense(PFC)max}$	maximum PFC sense voltage	ΔV/Δt = 50 mV/µs		0.49	0.52	0.55	V
		ΔV/Δt = 200 mV/µs		0.51	0.54	0.57	V
$t_{leb(PFC)}$	PFC leading edge blanking time			250	310	370	ns
$I_{prot(PFCSENSE)}$	protection current on pin PFCSENSE			–50	-	–5	nA
Soft start PFC (pin PFCSENSE)							
$I_{start(soft)PFC}$	PFC soft start current			–75	–60	–45	µA
$V_{start(soft)PFC}$	PFC soft start voltage	enabling voltage		0.46	0.50	0.54	V
$V_{stop(soft)PFC}$	PFC soft stop voltage	disabling voltage		0.42	0.45	0.48	V
$R_{start(soft)PFC}$	PFC soft start resistance			12	-	-	kΩ
Oscillator PFC							
$f_{sw(PFC)max}$	maximum PFC switching frequency			-	250	-	kHz
$t_{off(PFC)min}$	minimum PFC off-time			0.8	1.1	1.4	µs
Valley switching PFC (pin PFCAUX)							
$(\Delta V/\Delta t)_{vrec(PFC)}$	PFC valley recognition voltage change with time			-	-	1.7	V/µs
$t_{vrec(PFC)}$	PFC valley recognition time	V_{PFCAUX} = 1 V peak-to-peak	[2]	-	-	300	ns
		demagnetization to ΔV/Δt = 0	[3]	-	-	50	ns
$t_{to(vrec)PFC}$	PFC valley recognition time-out time			3	4	6	µs
Demagnetization management PFC (pin PFCAUX)							
$V_{th(comp)PFCAUX}$	comparator threshold voltage on pin PFCAUX			–150	–100	–50	mV
$t_{to(demag)PFC}$	PFC demagnetization time-out time			40	50	60	µs

Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{prot(PFCAUX)}$	protection current on pin PFCAUX	V_{PFCAUX} = 50 mV	–75	-	–5	nA
PFC off delay (pin PFCTIMER)						
$I_{source(PFCTIMER)}$	source current on pin PFCTIMER		-	–10	-	μA
$I_{sink(PFCTIMER)}$	sink current on pin PFCTIMER		-	0.9	-	mA
$V_{start(PFCTIMER)}$	start voltage on pin PFCTIMER		-	1.27	-	V
$V_{stop(PFCTIMER)}$	stop voltage on pin PFCTIMER		-	3.6	-	V
Driver (pin PFCDRIVER)						
$I_{src(PFCDRIVER)}$	source current on pin PFCDRIVER	$V_{PFCDRIVER}$ = 2 V	-	–0.5	-	A
$I_{sink(PFCDRIVER)}$	sink current on pin PFCDRIVER	$V_{PFCDRIVER}$ = 2 V	-	0.7	-	A
		$V_{PFCDRIVER}$ = 10 V	-	1.2	-	A
$V_{O(PFCDRIVER)max}$	maximum output voltage on pin PFCDRIVER		-	11	12	V
Overvoltage protection flyback (pin FBAUX)						
$I_{ovp(FBAUX)}$	overvoltage protection current on pin FBAUX		279	300	321	μA
$N_{cy(ovp)}$	number of overvoltage protection cycles		6	8	12	
Demagnetization management flyback (pin FBAUX)						
$V_{th(comp)FBAUX}$	comparator threshold voltage on pin FBAUX		60	80	110	mV
$I_{prot(FBAUX)}$	protection current on pin FBAUX	V_{FBAUX} = 50 mV	–75	-	–5	nA
$V_{clamp(FBAUX)}$	clamp voltage on pin FBAUX	I_{FBAUX} = –100 μA	–0.85	–0.7	–0.55	V
		I_{FBAUX} = 300 μA	0.79	0.94	1.09	V
$t_{sup(xfmr\_ring)}$	transformer ringing suppression time		1.5	2	2.5	μs
Pulse width modulator flyback						
$t_{on(fb)min}$	minimum flyback on-time		-	t_{leb}	-	ns
$t_{on(fb)max}$	maximum flyback on-time		32	40	48	μs
Oscillator flyback						
$f_{sw(fb)max}$	maximum flyback switching frequency		100	125	150	kHz
$V_{start(VCO)FBCTRL}$	VCO start voltage on pin FBCTRL		1.3	1.5	1.7	V
$f_{sw(fb)swon(PFC)}$	PFC switch-on flyback switching frequency		-	86	-	kHz
$f_{sw(fb)swoff(PFC)}$	PFC switch-off flyback switching frequency		-	48	-	kHz
$\Delta V_{VCO(FBCTRL)}$	VCO voltage difference on pin FBCTRL		-	–0.2	-	V

Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Peak current control flyback (pin FBCTRL)						
V_{FBCTRL}	voltage on pin FBCTRL	for maximum flyback peak current	1.85	2.0	2.15	V
$V_{to(FBCTRL)}$	time-out voltage on pin FBCTRL	enable voltage	-	2.5	-	V
		trip voltage	4.2	4.5	4.8	V
$R_{int(FBCTRL)}$	internal resistance on pin FBCTRL		-	3	-	kΩ
$I_{O(FBCTRL)}$	output current on pin FBCTRL	V_{FBCTRL} = 0 V	–1.4	–1.19	–0.93	mA
		V_{FBCTRL} = 2 V	–0.6	–0.5	–0.4	mA
$I_{to(FBCTRL)}$	time-out current on pin FBCTRL	V_{FBCTRL} = 2.6 V	–36	–30	–24	µA
		V_{FBCTRL} = 4.1 V	–34.5	–28.5	–22.5	µA
Valley switching flyback (pin HV)						
$(\Delta V/\Delta t)_{vrec(fb)}$	flyback valley recognition voltage change with time		–75	-	+75	V/µs
$t_{d(vrec-swon)}$	valley recognition to switch-on delay time	[4]	-	150	-	ns
Soft start flyback (pin FBSENSE)						
$I_{start(soft)fb}$	flyback soft start current		–75	–60	–45	µA
$V_{start(soft)fb}$	flyback soft start voltage	enable voltage	0.55	0.63	0.70	V
$R_{start(soft)fb}$	flyback soft start resistance		16	-	-	kΩ
Overcurrent protection flyback (pin FBSENSE)						
$V_{sense(fb)max}$	maximum flyback sense voltage	$\Delta V/\Delta t$ = 50 mV/µs	0.61	0.65	0.69	V
		$\Delta V/\Delta t$ = 200 mV/µs	0.64	0.68	0.72	V
$V_{sense(fb)min}$	minimum flyback sense voltage	$\Delta V/\Delta t$ = 50 mV/µs	0.305	0.325	0.345	V
$t_{leb(fb)}$	flyback leading edge blanking time		255	305	355	ns
$I_{adj(FBSENSE)}$	adjust current on pin FBSENSE	peak current	–3.2	–3.0	–2.8	µA
Overpower protection flyback (pin FBSENSE)						
$V_{sense(fb)max}$	maximum flyback sense voltage	$\Delta V/\Delta t$ = 50 mV/µs				
		I_{FBAUX} = 80 µA	0.61	0.65	0.69	V
		I_{FBAUX} = 120 µA	0.57	0.62	0.67	V
		I_{FBAUX} = 240 µA	0.47	0.52	0.57	V
		I_{FBAUX} = 360 µA	0.41	0.46	0.51	V
Driver (pin FBDRIVER)						
$I_{src(FBDRIVER)}$	source current on pin FBDRIVER	$V_{FBDRIVER}$ = 2 V	-	–0.5	-	A
$I_{sink(FBDRIVER)}$	sink current on pin FBDRIVER	$V_{FBDRIVER}$ = 2 V	-	0.7	-	A
		$V_{FBDRIVER}$ = 10 V	-	1.2	-	A
$V_{O(FBDRIVER)(max)}$	maximum output voltage on pin FBDRIVER		-	11	12	V

Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LATCH input (pin LATCH)						
$V_{prot(LATCH)}$	protection voltage on pin LATCH		1.23	1.25	1.27	V
$I_{O(LATCH)}$	output current on pin LATCH	$V_{prot(LATCH)} < V_{LATCH} < V_{oc(LATCH)}$	−85	−80	−75	µA
$V_{en(LATCH)}$	enable voltage on pin LATCH	at start-up	1.30	1.35	1.40	V
$V_{hys(LATCH)}$	hysteresis voltage on pin LATCH	$V_{en(LATCH)} - V_{prot(LATCH)}$	80	100	140	mV
$V_{oc(LATCH)}$	open-circuit voltage on pin LATCH		2.65	2.9	3.15	V
Temperature protection						
$T_{pl(IC)}$	IC protection level temperature		130	140	150	°C
$T_{pl(IC)hys}$	hysteresis of IC protection level temperature		-	10	-	°C

[1] For a typical application with a compensation network on pin PFCCOMP (see Figure 3).

[2] Minimum required voltage change time for valley recognition on pin PFCAUX.

[3] Minimum time required between demagnetization detection and $\Delta V/\Delta t = 0$ on pin PFCAUX.

[4] Guaranteed by design.

11. Application information

A power supply with the TEA1752(L)T consists of a power factor correction circuit followed by a flyback converter (See Figure 18).

Capacitor C_{VCC} buffers the IC supply voltage, which is powered via the high voltage rectified mains supply during start-up and via the auxiliary winding of the flyback converter during operation. Sense resistors R_{SENSE1} and R_{SENSE2} convert the current through MOSFETs S1 and S2 into a voltage on pins PFCSENSE and FBSENSE. The values of R_{SENSE1} and R_{SENSE2} define the maximum primary peak current on MOSFETs S1 and S2.

In the example shown in Figure 18, the LATCH pin is connected to a Negative Temperature Coefficient (NTC) resistor. When the resistance drops below $\frac{V_{prot(LATCH)}}{I_{O(LATCH)}} = 15.6\ k\Omega\ (typical)$, the protection is activated. A capacitor $C_{TIMEOUT}$ is connected to the FBCTRL pin. Time-out protection is activated typically after 10 ms for a 120 nF capacitor. R_{LOOP} is added so the time-out capacitor does not interfere with the normal regulation loop.

R_{S1} and R_{S2} prevent the soft start capacitors from being charged during normal operation due to negative voltage spikes across the sense resistors.

Resistor R_{AUX1} protects the IC from damage during events such as lightning strikes.

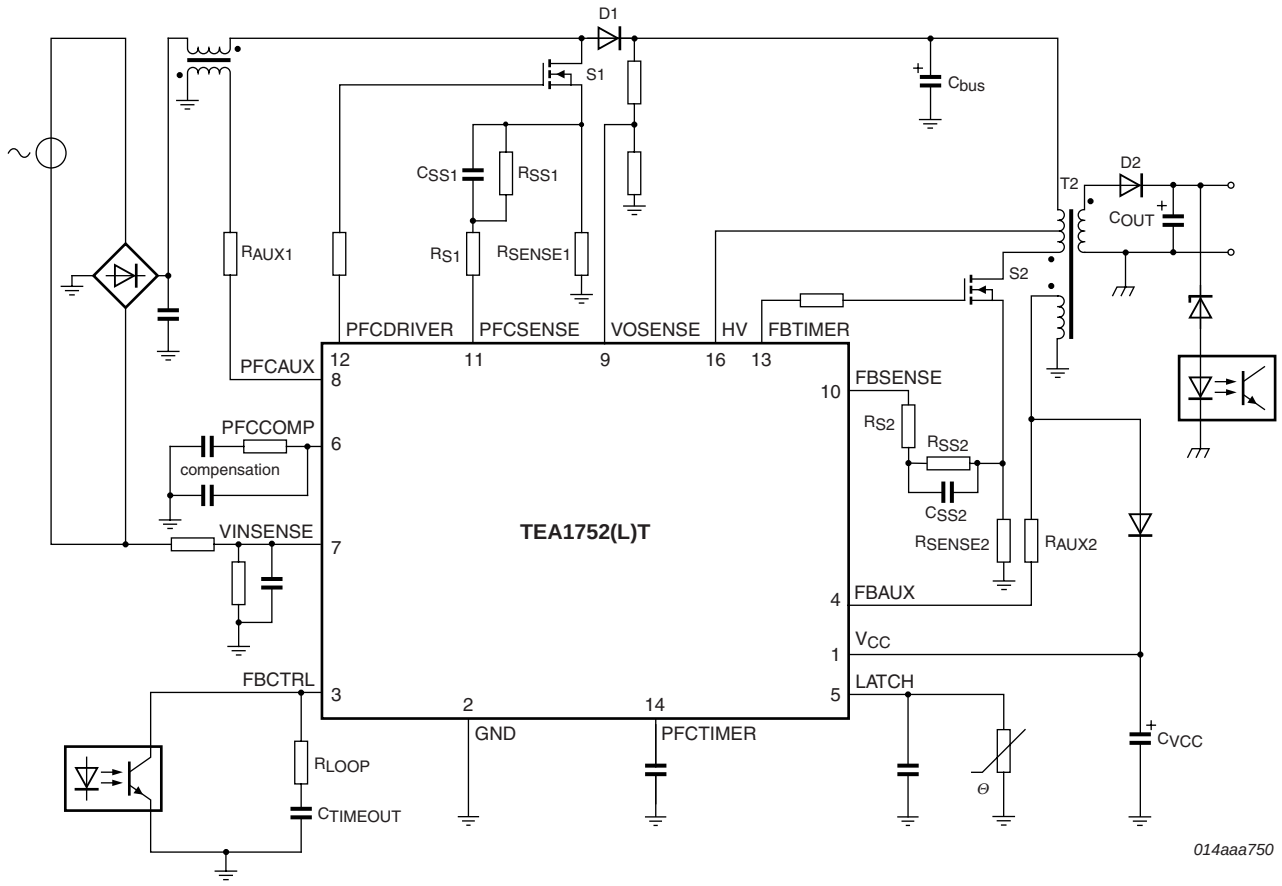
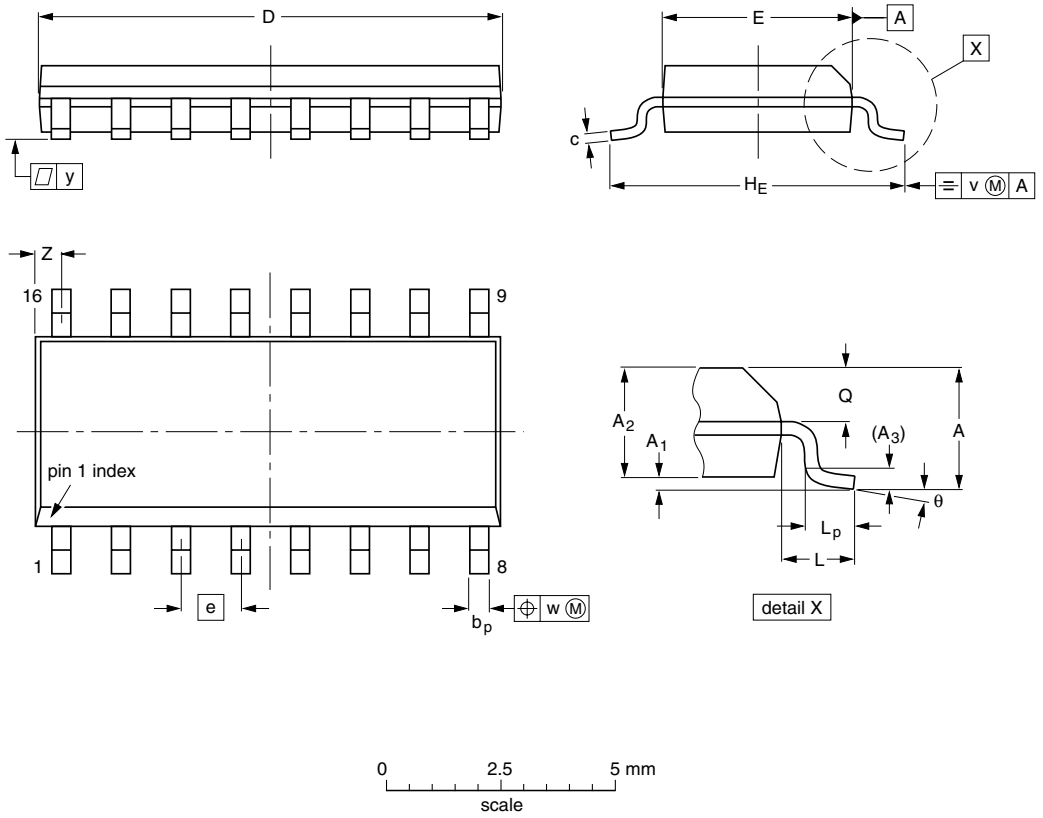


Fig 18. Typical application diagram TEA1752(L)T

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 19. Package outline SOT109-1 (SO16)

13. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1752T_LT v.2	20100624	Product data sheet	-	TEA1752T_LT_1
Modifications	• Template upgraded to Rev 2.12.0 including revised legal information. • Text and drawings updated throughout entire data sheet. • Figure 1 updated. • $V_{stop(soft)PFC}$ added in Table 5. • Minimum junction temperature changed in Table 3.			
TEA1752T_LT_1	20090213	Objective data sheet	-	-

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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16. Contents

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