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RF3164

3V 1900MHz LINEAR POWER AMPLIFIER MODULE

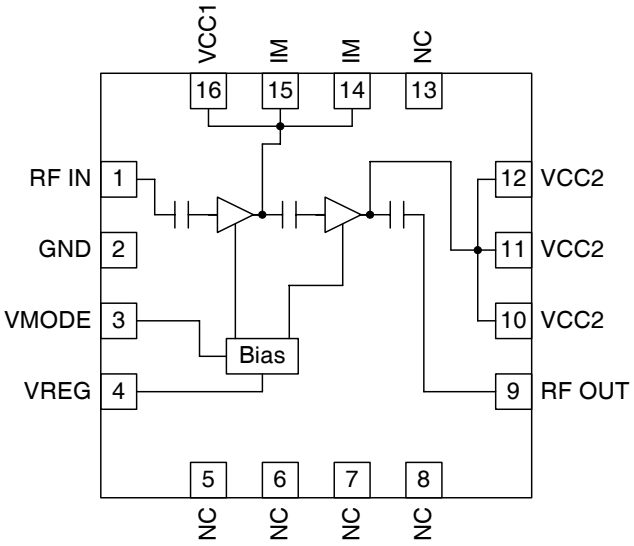
RoHS Compliant & Pb-Free Product
Package Style: QFN, 16-Pin, 3 x 3

Features

- Input Internally Matched@50Ω
- Output Internally Matched
- 28dBm Linear Output Power
- 40% Peak Linear Efficiency
- 28dB Linear Gain
- -50dBc ACPR @ 1.25MHz

Applications

- 3V CDMA US-PCS Handset
- 3V CDMA2000/1XRTT US-PCS Handset
- 3V CDMA2000/1X-EV-DO US-PCS Handset
- Spread-Spectrum System



Functional Block Diagram

Product Description

The RF3164 is a high-power, high-efficiency linear amplifier module specifically designed for 3V handheld systems. The device is manufactured on an advanced third generation GaAs HBT process, and was designed for use as the final RF amplifier in 3V IS-95/CDMA 2000 1X handheld digital cellular equipment, spread-spectrum systems, and other applications in the 1850MHz to 1910MHz band. The RF3164 has a digital control line for low power applications to lower quiescent current. The RF3164 is assembled in at 16-pin, 3mmx3mm, QFN package.

Ordering Information

RF3164	3V 1900MHz Linear Power Amplifier Module
RF3164PCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V
Supply Voltage ($P_{OUT} \leq 31$dBm)	+5.2	V
Control Voltage (V_{REG})	+3.9	V
Input RF Power	+10	dBm
Mode Voltage (V_{MODE})	+3.9	V
Operating Temperature	-30 to +110	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity Level IPC/JEDEC J-STD-20	MSL 2 @260	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Gain Mode (V_{MODE} Low)					T=25°C Ambient, V_{CC}=3.4V, V_{REG}=2.8V, V_{MODE}=0V, and P_{OUT}=28dBm for all parameters (unless otherwise specified).
Operating Frequency Range	1850		1910	MHz	
Linear Gain	26	28		dB	
Second Harmonics		-35		dBc	
Third Harmonics		-40		dBc	
Maximum Linear Output	28			dBm	
Linear Efficiency	37	40		%	
Maximum I_{CC}		460	502	mA	
ACPR @ 1.25MHz		-50.0	-46.0	dBc	
ACPR @ 1.98MHz		-55.5	-53.0	dBc	
ACPR @ 2.25MHz		-59.0	-56.0	dBc	
Input VSWR		2:1			
Output VSWR Stability			6:1		No oscillation>-70dBc
			10:1		No damage
Noise Power		-138		dBm/Hz	At 80MHz offset.

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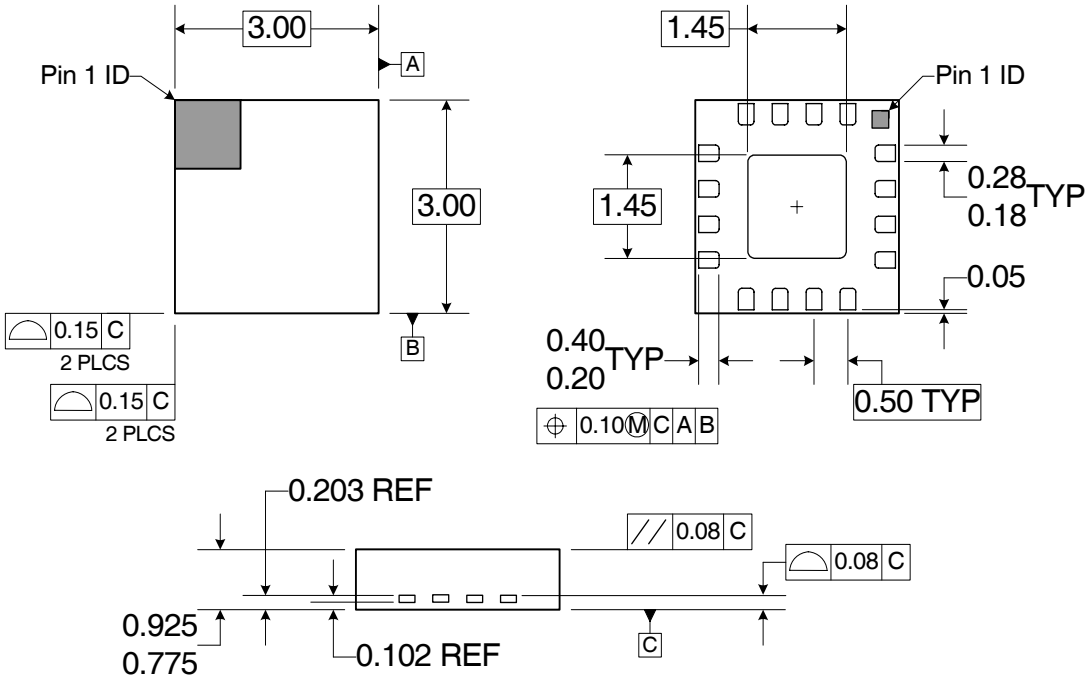
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Low Gain Mode (V_{MODE} High)					T=25°C Ambient, V_{CC}=3.4V, V_{REG}=2.8V, V_{MODE}=2.8V, and P_{OUT}=28dBm for all parameters (unless otherwise specified).
Operating Frequency Range	1850		1910	MHz	
Linear Gain	26	28		dB	
Second Harmonics		-35		dBc	
Third Harmonics		-40		dBc	
Maximum Linear Output	28			dBm	
Linear Efficiency	37	40		%	
ACPR @1.25MHz		-50	-46	dBc	
ACPR @ 1.98MHz		-55	-53	dBc	
ACPR @2.25MHz		-58	-56	dBc	
Maximum I_{CC}		130	156	mA	P_{OUT}=16dBm
Linear Gain		26		dB	P_{OUT}=16dBm
Input VSWR		2:1			
Output VSWR Stability			6:1		No oscillation>-70dBc
			10:1		No damage
Power Supply					
Supply Voltage	3.2	3.4	4.2	V	
High Gain Idle Current		65	95	mA	V_{MODE}=low and V_{REG}=2.8V
Low Gain Idle Current		55	85	mA	V_{MODE}=high and V_{REG}=2.8V
V_{REG} Current		1	2	mA	
V_{MODE} Current		250	1000	uA	
RF Turn On/Off Time		1.2	6	uS	
DC Turn On/Off Time		2	40	uS	
Total Current (Power Down)		0.2	2.0	uA	
V_{REG} Low Voltage (Power Down)	0		0.5	V	
V_{REG} High Voltage (Recommended)	2.75	2.8	2.95	V	
V_{REG} High Voltage (Operational)	2.7		3.0	V	
V_{MODE} Voltage	0		0.5	V	High Gain Mode
V_{MODE} Voltage	2.0		3.0	V	Low Gain Mode

Pin	Function	Description	Interface Schematic
1	RF IN	RF input internally matched to 50Ω. This input is internally AC-coupled.	
2	GND	Ground connection.	
3	VMODE	For nominal operation (High Power mode), V_{MODE} is set LOW. When set HIGH, devices are biased lower to improve efficiency.	
4	VREG	Regulated voltage supply for amplifier bias circuit. In power down mode, both V_{REG} and V_{MODE} need to be LOW (<0.5V).	
5	NC	No connection. Do not connect this pin to any external circuit.	
6	NC	No connection. Do not connect this pin to any external circuit.	
7	NC	No connection. Do not connect this pin to any external circuit.	
8	NC	No connection. Do not connect this pin to any external circuit.	
9	RF OUT	RF output. Internally AC-coupled.	
10	VCC2	Output stage collector supply. Please see the schematic for required external components.	
11	VCC2	Same as pin 10.	
12	VCC2	Same as pin 10.	
13	NC	No connection. Do not connect this pin to any external circuit.	
14	IM	Interstage matching. Connect to pin 15.	
15	IM	Interstage matching. Connect to pin 14.	
16	VCC1	First stage collector supply. A 4.7µF decoupling capacitor is required.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Package Drawing



Shaded areas represent pin 1. *Dimensions in mm.*

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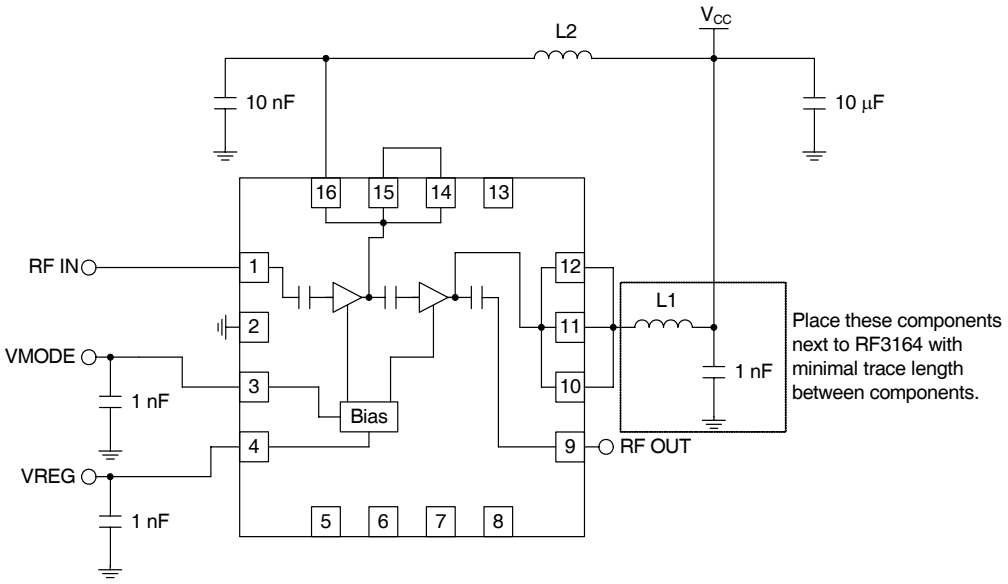
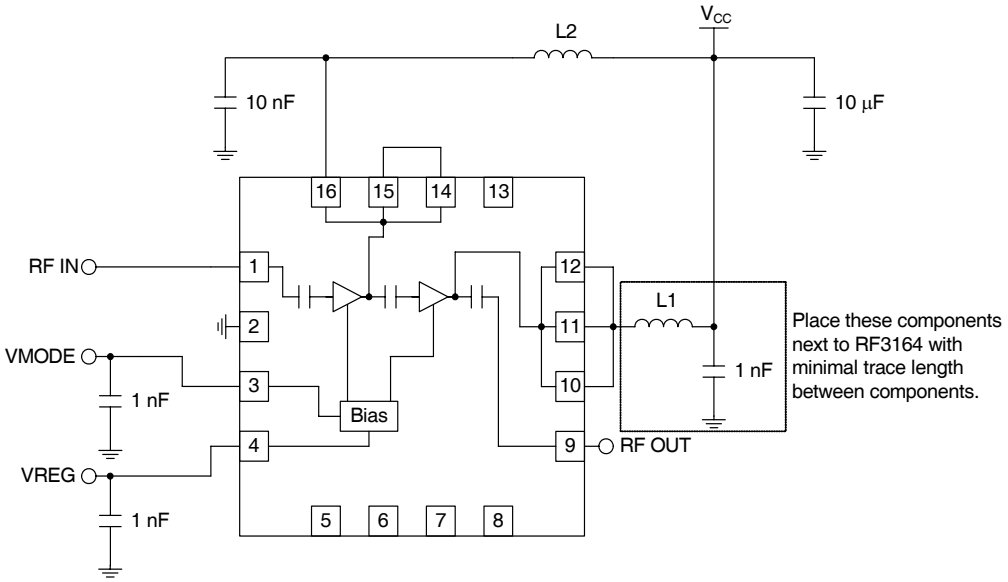
Application Schematic
Output Power Requirements of 28dBm



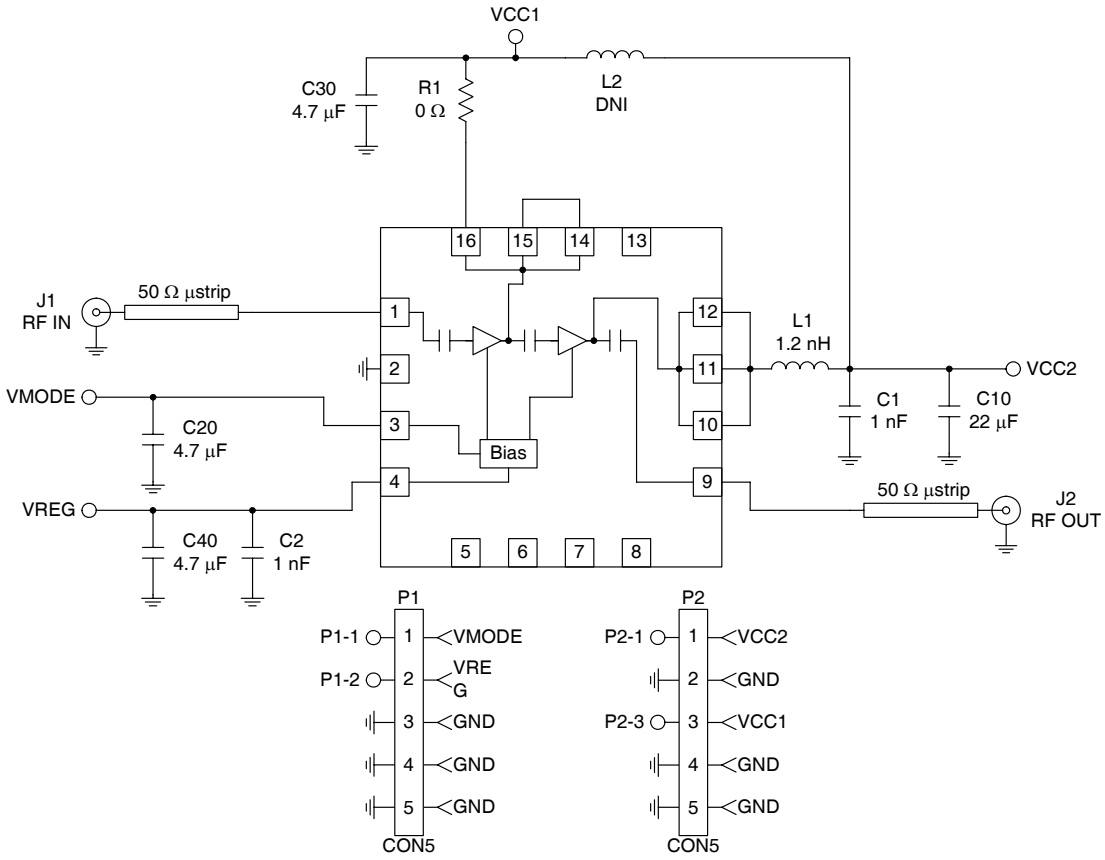
L1 = 1.5nH is recommended, but any value between 1.2nH to 2.2nH may be used.
L2 = 6.8nH is recommended, but any value between 4.7nH to 8.2nH may be used.
L2 may not be needed if Pin 16 is not routed directly to Pins 10, 11, and 12.

Application Schematic
Output Power Requirements of 28.5dBm



L1 = 3.3nH is recommended, but any value between 2.2nH to 3.9nH may be used.
L2 = 6.8nH is recommended, but any value between 4.7nH to 8.2nH may be used.
L2 may not be needed if Pin 16 is not routed directly to Pins 10, 11, and 12.

Evaluation Board Schematic



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Electrostatic Discharge Sensitivity

Human Body Model (HBM)

Figure 3 shows the HBM ESD sensitivity level for each pin to ground. The ESD test is in compliance with JESD22-A114.

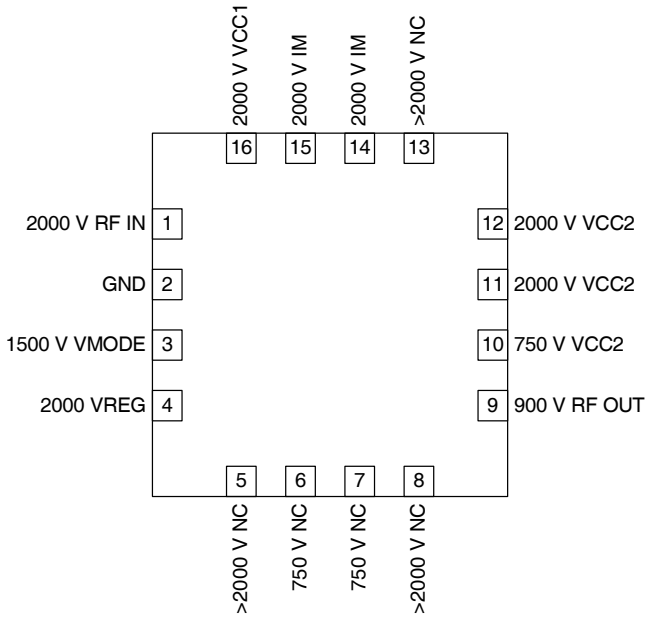

Figure 3. ESD Level - Human Body Model

Machine Model (MM)

Figure 4 shows the MM ESD sensitivity level for each pin to ground. The ESD test is in compliance with JESD22-A115.

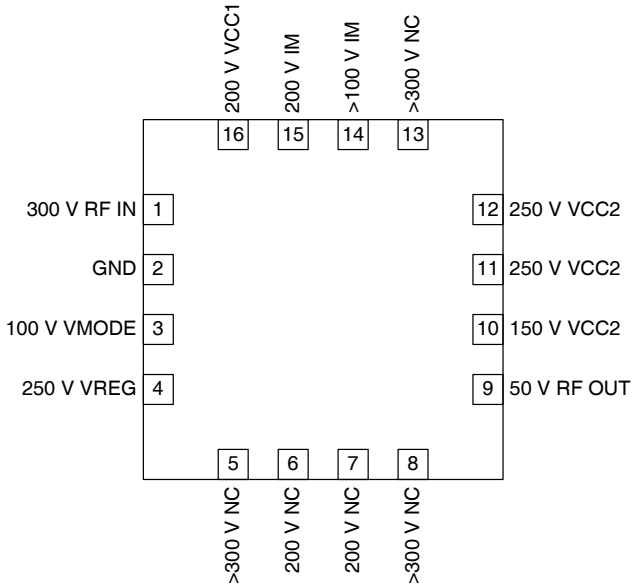

Figure 4. ESD Level - Machine Model

PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land Pattern

A = 0.64 x 0.28 (mm) Typ.
B = 0.28 x 0.64 (mm) Typ.
C = 0.78 x 0.64 (mm)
D = 0.64 x 1.28 (mm)
E = 1.50 (mm) Sq.

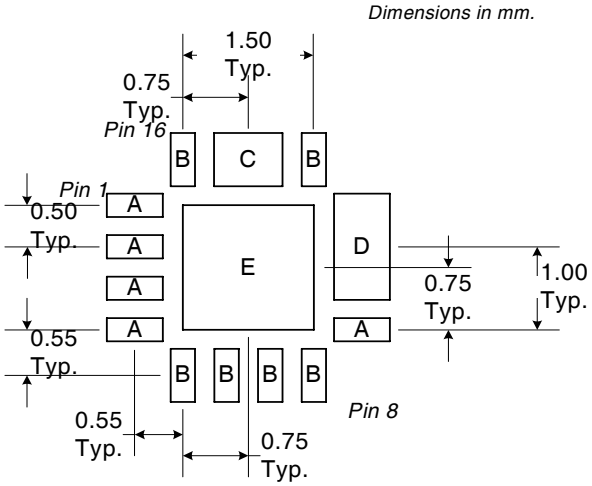

Figure 1. PCB Metal Land Pattern (Top View)

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PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

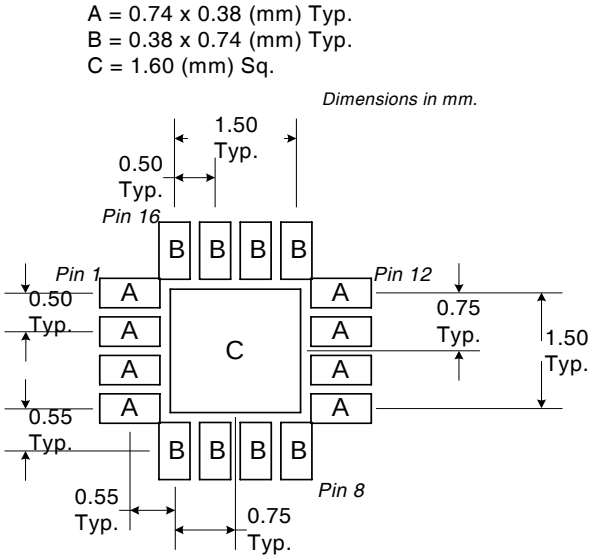

Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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Tape and Reel Information

Carrier tape basic dimensions are based on EIA481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but width and pitch will be consistent.

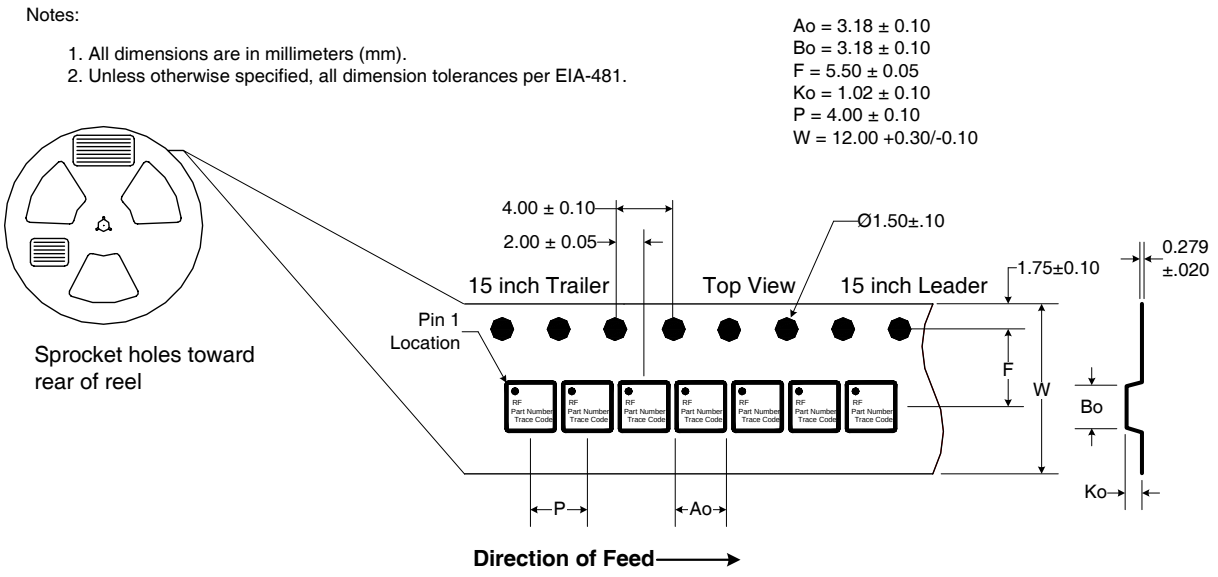
Carrier tape is wound or placed onto a shipping reel either 330 mm (13 inches) in diameter or 178 mm (7 inches) in diameter. The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, moisture sensitive parts (MSL level 2a-5a) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier, ESD bag, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, most carrier tape and shipping reels are not rated as bakeable at 125°C. If baking is required, devices may be baked according to section 4, table 4-1, column 8 of Joint Industry Standard IPC/JEDEC J-STD-033A.

The following table provides useful information for carrier tape and reels used for shipping the devices described in this document.

RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
RF3164TR7	7 (178)	2.4 (61)	12	4	Single	2500

QFN (Carrier Tape Drawing with Part Orientation)



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