32-Mbit (2M x 16) Static RAM

Features

- **High density 32-Mbit SRAM**
- **High speed**
  - **— t_{AA} = 10 ns**
- **Low active power**
  - **— I_{CC} = 450 mA**
- **Operating voltages of 3.3 ± 0.3V**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Available in standard 119-ball FBGA**

Functional Description

The CY7C1071AV33 is a 3.3V high-performance 32-Megabit static RAM organized as a 2,097,152 words by 16 bits.

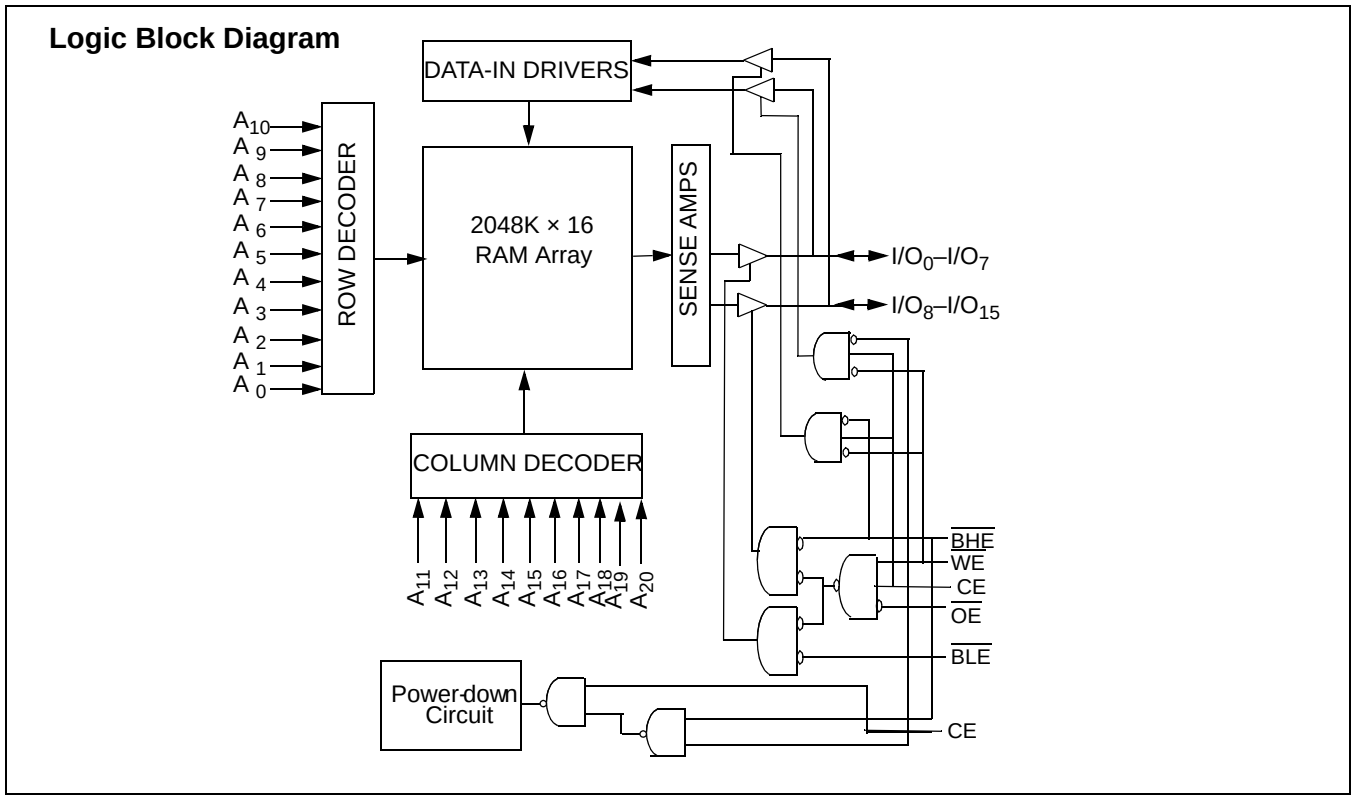
Writing to the device is accomplished by enabling the chip (CE HIGH) while forcing the Write Enable (WE) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{20}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{20}).

Reading from the device is accomplished by enabling the chip by taking CE HIGH while forcing the Output Enable ($\overline{OE}$) LOW and the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected (CE LOW), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a Write operation (CE HIGH, and $\overline{WE}$ LOW).

The CY7C1071AV33 is available in a 119-ball grid array (FBGA) package.

Logic Block Diagram



Selection Guide

		CY7C1071AV33-10	CY7C1071AV33-12	Unit
Maximum Access Time		10	12	ns
Maximum Operating Current	Com'l / Ind'l	450	400	mA
Maximum CMOS Standby Current	Com'l / Ind'l	100	100	mA

Pin Configurations

119 BGA

(Top View)

	1	2	3	4	5	6	7
A	NC	A	A	A	A	A	NC
B	NC	A	A	NC	A	A	NC
C	NC	$\overline{BHE}$	CE	A	NC	$\overline{BLE}$	NC
D	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC
E	I/O_8	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_0
F	I/O_9	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_1
G	I/O_{10}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_2
H	I/O_{11}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_3
J	NC	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	DNU
K	I/O_{12}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_4
L	I/O_{13}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_5
M	I/O_{14}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_6
N	I/O_{15}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_7
P	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC
R	NC	A	NC	A	NC	A	NC
T	NC	A	A	$\overline{WE}$	A	A	NC
U	NC	A	A	$\overline{OE}$	A	A	NC

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[1] .... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[1] .....–0.3V to V_{CC} + 0.3V

DC Input Voltage[1].....–0.3V to V_{CC} + 0.3V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-10		-12		Unit
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–2	+2	–2	+2	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–2	+2	–2	+2	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = 1/t_{RC}	Com'l / Ind'l		450		400	mA
I_{SB1}	Automatic CE Power-down Current —TTL Inputs	CE <= V_{IL}, Max. V_{CC},V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			140		140	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	CE <= 0.3V, Max. V_{CC}, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Com'l / Ind'l		100		100	mA

Capacitance[2]

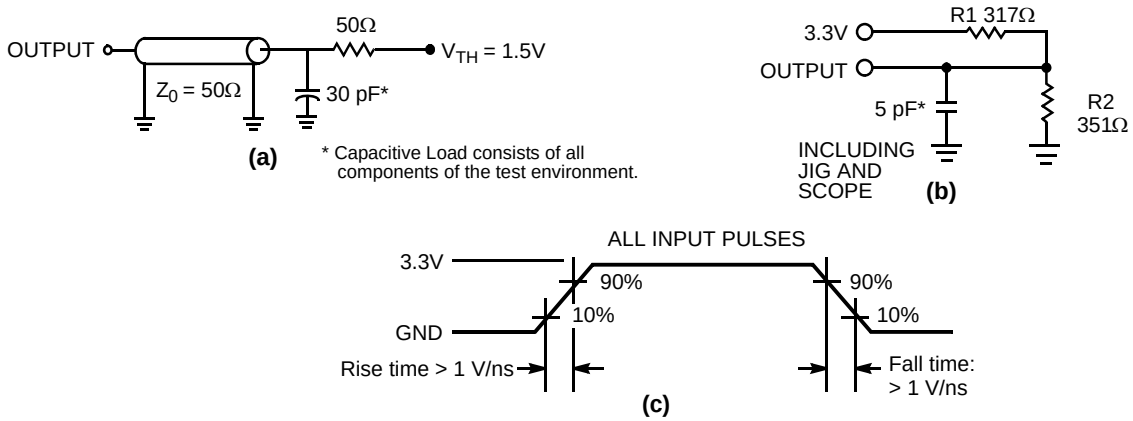
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	12	pF
C_{OUT}	I/O Capacitance		15	pF

Thermal Resistance[2]

Parameter	Description	Test Conditions	All-Packages	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)[2]	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	TBD	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)[2]		TBD	°C/W

Notes:
1. V_{IL} (min.) = –2.0V and V_{IH}(max) = V_{CC} + 0.5V for pulse durations of less than 20 ns.
2. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[3]



AC Switching Characteristics Over the Operating Range [4]

Parameter	Description	-10		-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{power}	V_{CC}(typical) to the first access[5]	1		1		ms
t_{RC}	Read Cycle Time	10		12		ns
t_{AA}	Address to Data Valid		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	CE HIGH to Data Valid		10		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z	1		1		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[6]		5		6	ns
t_{LZCE}	CE HIGH to Low-Z[6]	3		3		ns
t_{HZCE}	CE LOW to High-Z[6]		5		6	ns
t_{PU}	CE HIGH to Power-Up[7]	0		0		ns
t_{PD}	CE LOW to Power-Down[7]		10		12	ns
t_{DBE}	Byte Enable to Data Valid		10		12	ns
t_{LZBE}	Byte Enable to Low-Z	1		1		ns
t_{HZBE}	Byte Disable to High-Z		5		6	ns
Write Cycle[8, 9]						
t_{WC}	Write Cycle Time	10		12		ns
t_{SCE}	CE HIGH to Write End	7		8		ns

Notes:

3. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0V). As soon as 1 ms (T_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0V) voltage.
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and specified transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC test loads, unless specified otherwise.
5. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
6. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE} and t_{LZOE}, t_{LZCE}, t_{LZWE}, t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
7. These parameters are guaranteed by design and are not tested.
8. The internal Write time of the memory is defined by the overlap of CE HIGH and $\overline{WE}$ LOW. Chip enables must be active and $\overline{WE}$ and byte enables must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
9. The minimum Write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

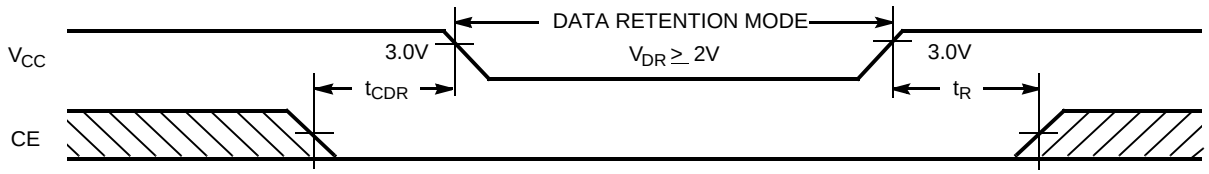
AC Switching Characteristics Over the Operating Range (continued)[4]

Parameter	Description	-10		-12		Unit
		Min.	Max.	Min.	Max.	
t_{AW}	Address Set-up to Write End	7		8		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		ns
t_{SD}	Data Set-up to Write End	5.5		6		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[6]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[6]		5		6	ns
t_{BW}	Byte Enable to End of Write	7		8		ns

Data Retention Characteristics Over the Operating Range

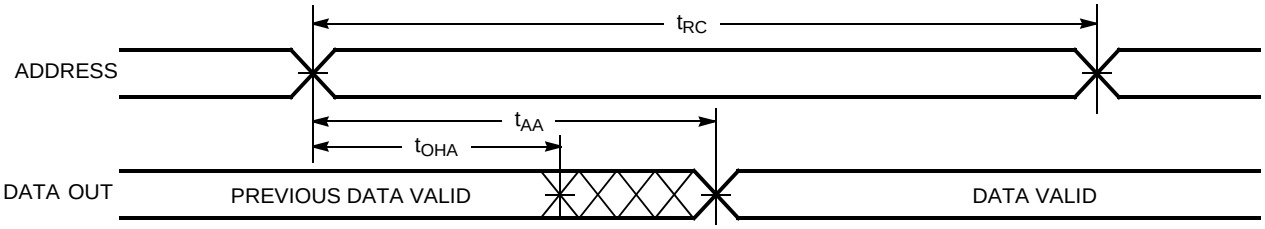
Parameter	Description		Conditions[11]	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	Com'l / Ind'l	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		100	mA
t_{CDR}[2]	Chip Deselect to Data Retention Time			0		ns
t_R[10]	Operation Recovery Time					µs

Data Retention Waveform



Switching Waveforms

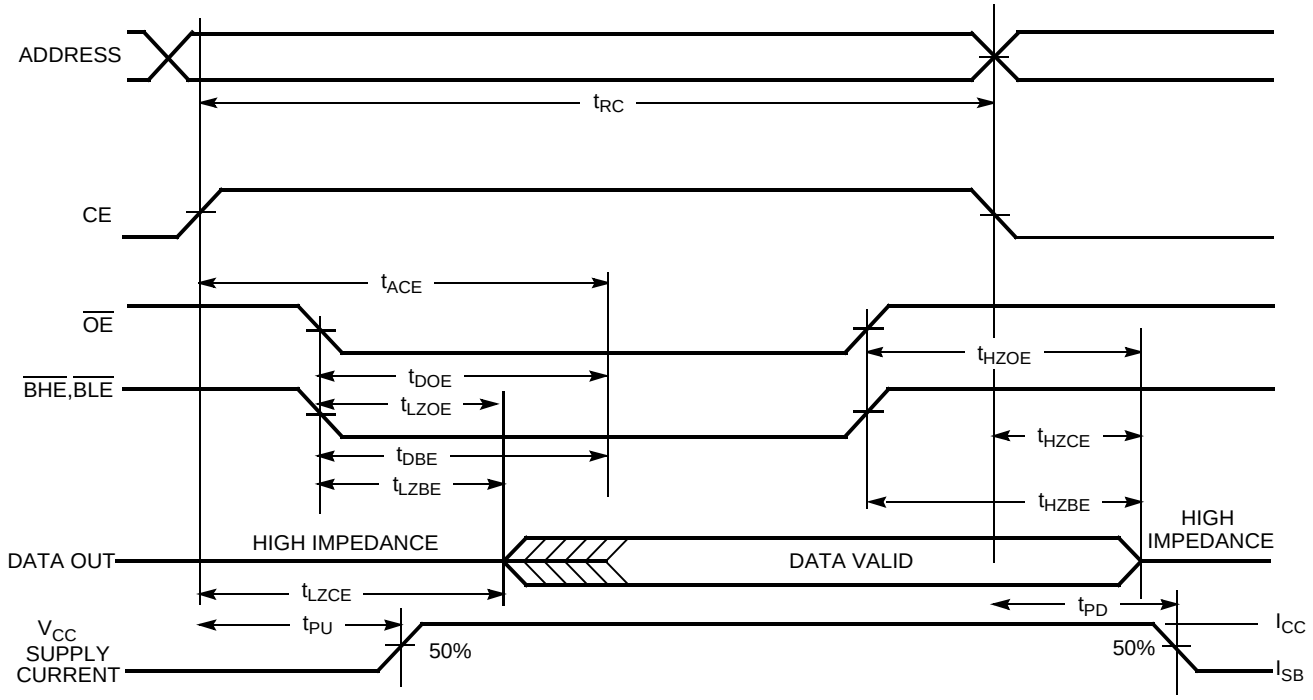
Read Cycle No. 1[11, 13]



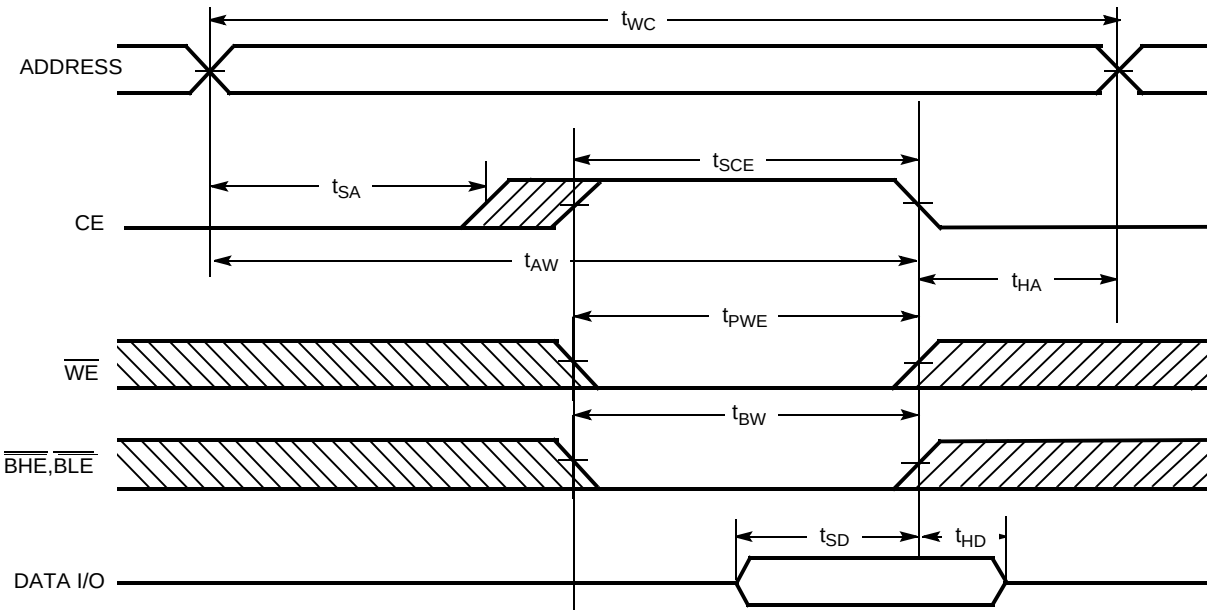
Notes:
10. Test conditions assume $t_f \leq 3$ ns.
11. No input may exceed V_{CC} + 0.3V.
12. Device is continuously selected. $\overline{OE}$, $\overline{BHE}$ and/or $\overline{BHE}$ = V_{IL}. CE = V_{IH}.
13. $\overline{WE}$ is HIGH for Read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]



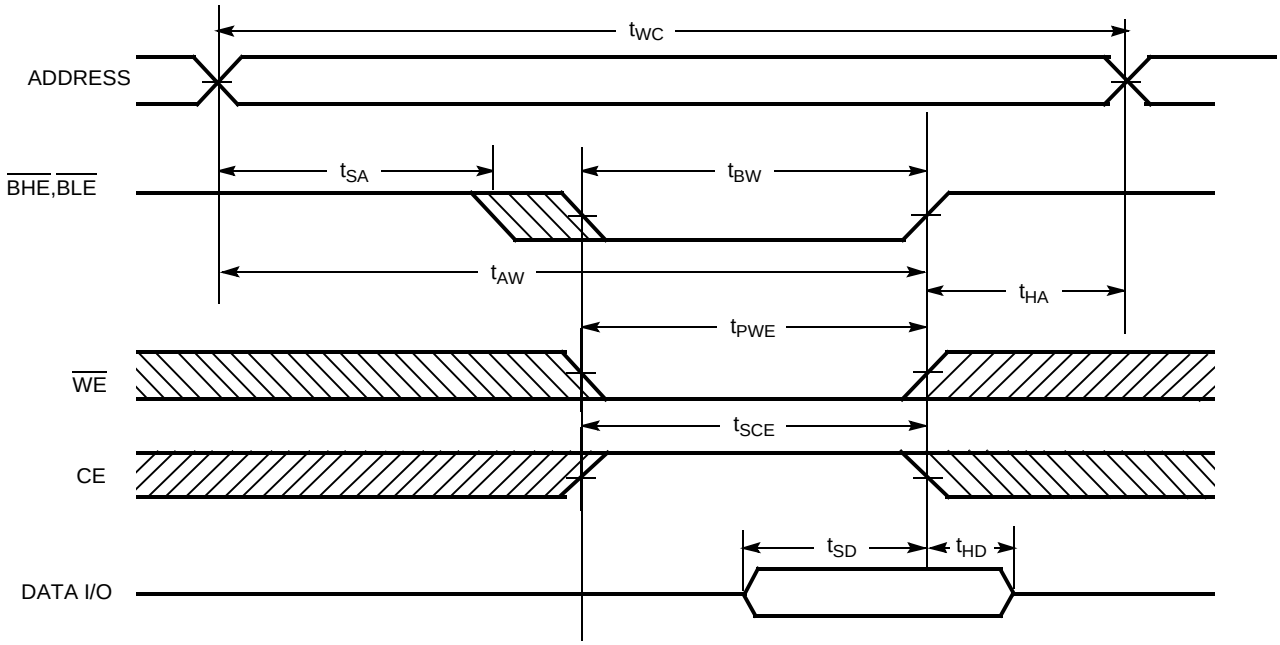
Write Cycle No. 1 (CE Controlled)[15, 16]



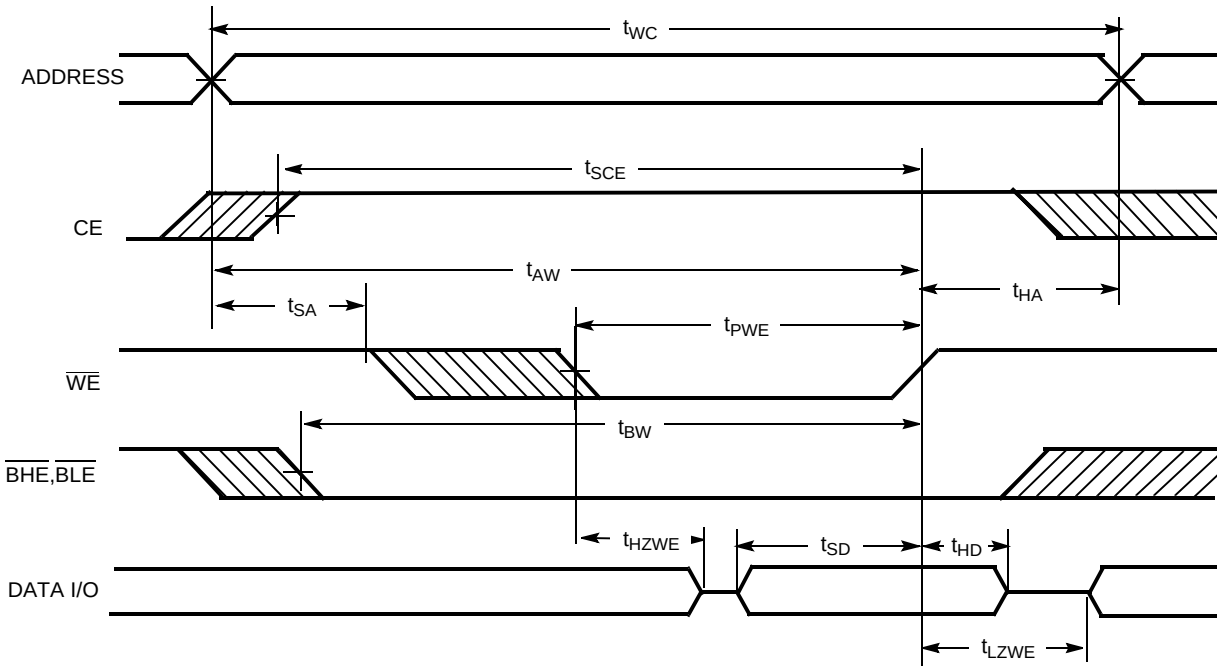
Notes:
14. Address valid prior to or coincident with CE transition HIGH.
15. Data I/O is high-impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IH}.
16. If CE goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)[15, 16]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[15, 16]



Truth Table

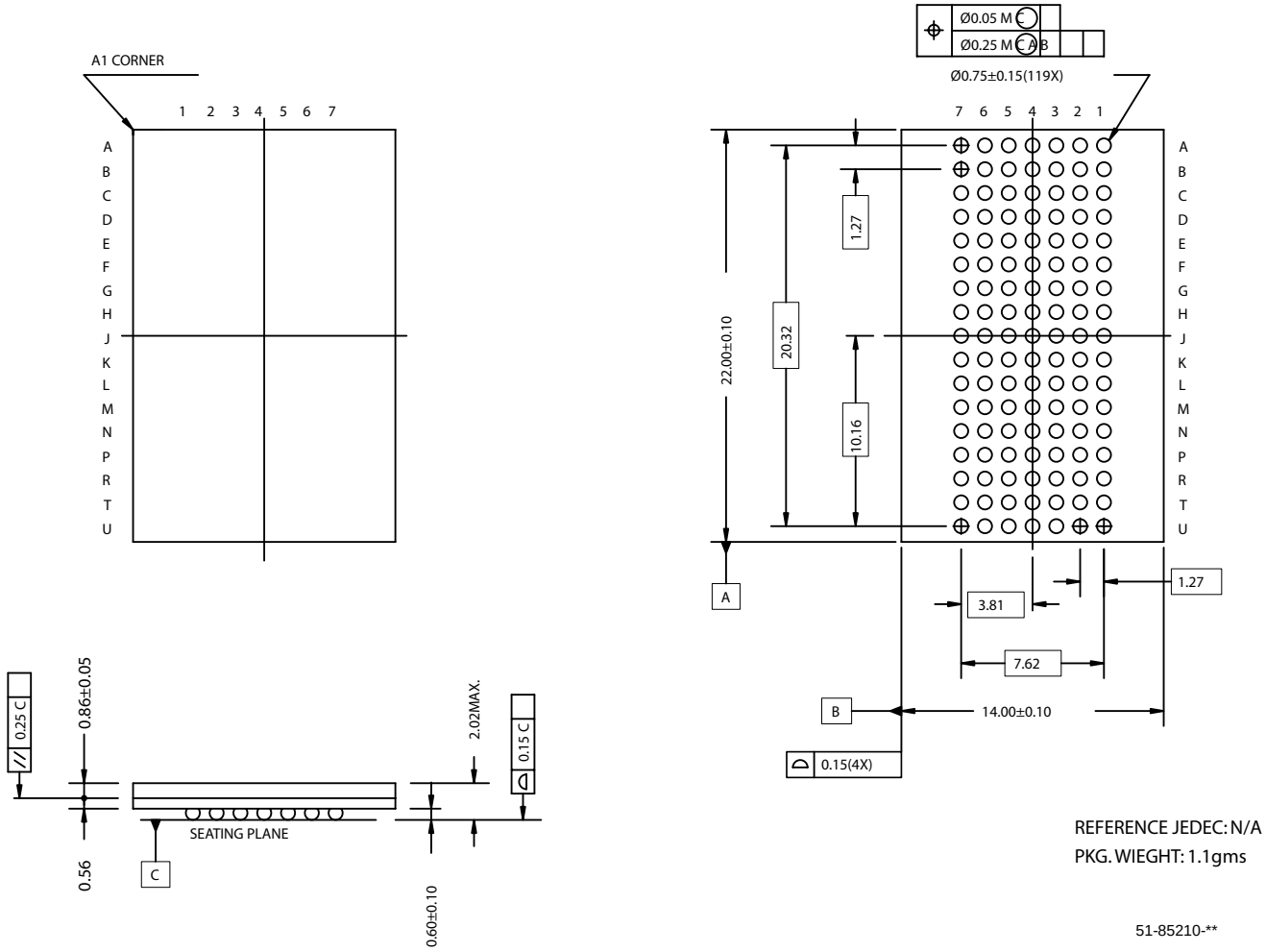
CE	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	Mode	Power
L	X	X	X	X	High-Z	High-Z	Power-down	Standby (I_{SB})
H	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I_{CC})
H	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active (I_{CC})
H	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active (I_{CC})
H	X	L	L	L	Data In	Data In	Write All Bits	Active (I_{CC})
H	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active (I_{CC})
H	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active (I_{CC})
H	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1071AV33-10 BBC	BB119	119-Ball (14 x 22 x 2.02 mm) FBGA	Commercial
	CY7C1071AV33-10 BBI			Industrial
12	CY7C1071AV33-12 BBC	BB119	119-Ball (14 x 22 x 2.02 mm) FBGA	Commercial
	CY7C1071AV33-12 BBI			Industrial

Package Diagram

119 FBGA (14 x 22 x 2.02 mm) BB119B



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Document History Page

Document Title: CY7C1071AV33 32-Mbit (2M x 16) Static RAM Document Number: 38-05634				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	278072	See ECN	RKF	New Datasheet
*A	397695	See ECN	SYT	Converted from “Advance Information” to “Preliminary” Changed the MPN from CYM1071AV33 to CY7C1071AV33 Changed Title from “CY7C1071AV33 32-Mbit (2M x 16) Static RAM Module” to “CY7C1071AV33 32-Mbit (2M x 16) Static RAM “ Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” Removed redundant information from the “Features” and “Functional Description” sections Edited typo ‘A_{19}’ to ‘A_{20}’ in the Functional Description on Page # 1 Changed Package offering from 119 PBGA (BG119) to 119 FBGA (BB119) Removed the Package Column from the Capacitance table on Page # 3 Changed the DC Voltage Applied to Outputs in High-Z State and DC Input Voltage from “-0.5V to V_{CC} + 0.5V” to “-0.3V to V_{CC} + 0.3V” in the Maximum Ratings on Page # 3 Changed t_{DBE} from 5 ns to 10 ns and 6 ns to 12 ns for -10 and -12 speed bins respectively on Page # 4 Included spec for I_{CCDR} = 100 mA in the Data Retention Characteristics table on Page# 5 Edited footnote # 11 from “V_{CC} + 0.5V” to “V_{CC} + 0.3V” Referenced footnotes # 15 and 16 on to Write Cycle No.2 Page # 7 Updated the Ordering Information to include the BB119 Package