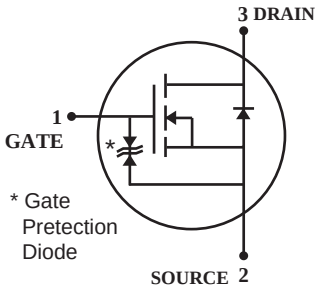
WEITRON

2N7002K

N-Channel Enhancement Mode Power MOSFET

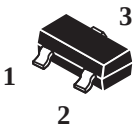
Pb Lead(Pb)-Free



DRAIN CURRENT
640m AMPERES
DRAIN SOURCE VOLTAGE
60 VOLTAGE

Description:

The 2N7002K utilized advanced processing techniques to achieve the lowest possible on-resistance, extremely efficient and cost-effectiveness device.
The 2N7002K is universally used for all commercial-industrial applications.



SOT-23

Features:

*Simple Drive Requirement
*Small Package Outline

Maximum Ratings(T_A=25℃ Unless Otherwise Specified)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	
Continuous Drain Current[3],V_{GS}@10V(T_A=25°C)	I_D	640	mA
,V_{GS}@10V(T_A=70°C)		500	
Pulsed Drain Current[1,2]	I_{DM}	950	
Total Power Dissipation(T_A=25°C)	P_D	1.38	W
Maximum Junction-ambient [3]	$R_{\theta JA}$	90	°C/W
Operating Junction Temperature Range	T_J	+150	°C
Storage Temperature Range	T_{stg}	-55~+150	°C
Gate−Source ESD Rating (HBM, Method 3015)	ESD	2500	V

Device Marking

2N7002K = RK

Electrical Characteristics (T_A = 25°C Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Static					
Drain-Source Breakdown Voltage V_{GS}=0, I_D=250μA	$V_{(BR)DSS}$	60	-	-	V
Gate-Source Threshold Voltage V_{DS}=V_{GS}, I_D=250μA	$V_{GS(Th)}$	1.0	-	3.0	
Gate-Source Leakage Current V_{GS}= ± 20 V	I_{GSS}	-	-	±10	μA
Drain-Source Leakage Current(T_j=25˚C) V_{DS}=60V,V_{GS}=0	I_{DSS}	-	-	1	μA
Drain-Source Leakage Current(T_j=70˚C) V_{DS}=48V,V_{GS}=0		-	-	100	
Drain-Source On-Resistance V_{GS}=10V,I_D=500mA V_{GS}=4.5V,I_D=200mA	$R_{DS(on)}$	- -	- -	2 4	Ω
Forward Transconductance V_{DS}=10V, I_D=600mA	g_{fs}	-	600	-	mS
Dynamic					
Input Capacitance V_{GS}=0V, V_{DS}=25V, f=1.0MHz	Ciss	-	32	50	pF
Output Capacitance V_{GS}=0V, V_{DS}=25V, f=1.0MHz	Coss	-	8	-	
Reverse Transfer Capacitance V_{GS}=0V, V_{DS}=25V, f=1.0MHz	Crss	-	6	-	

Switching

Turn-on Delay Time[2] V_{DS}=30V,V_{GS}=10V,I_D=600mA,R_D=52Ω,R_G=3.3Ω	$t_{d(on)}$	-	12	-	ns
Rise Time V_{DS}=30V,V_{GS}=10V,I_D=600mA,R_D=52Ω,R_G=3.3Ω	t_r	-	10	-	
Turn-off Delay Time V_{DS}=30V,V_{GS}=10V,I_D=600mA,R_D=52Ω,R_G=3.3Ω	$t_{d(off)}$	-	59	-	
Fall Time V_{DS}=30V,V_{GS}=10V,I_D=600mA,R_D=52Ω,R_G=3.3Ω	t_f	-	29	-	
Total Gate Charge[2] V_{DS}=50V,V_{GS}=4.5V,I_D=600mA	Q_g	-	1	1.6	nC
Gate-Source Charge V_{DS}=50V,V_{GS}=4.5V,I_D=600mA	Q_{gs}	-	0.5	-	
Gate-Drain Change V_{DS}=50V,V_{GS}=4.5V,I_D=600mA	Q_{gd}	-	0.5	-	

Source-Drain Diode Characteristics

Forward On Voltage[2] V_{GS}=0V, I_S=200mA	V_{SD}	-	-	1.2	V

Note: 1. Pulse width limited by Max, junction temperature.
2. pulse width≦300μs, duty cycle≦2%.
3. Surface mounted on 1 in^2 copper pad of FR4 board; 270℃/W when mounted on min, copper pad.

Characteristics Curve

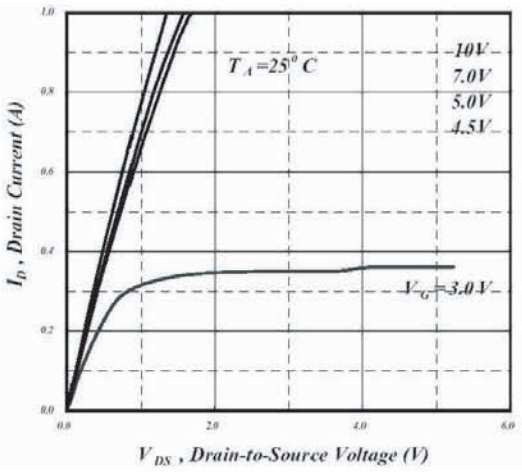


Fig 1. Typical Output Characteristics

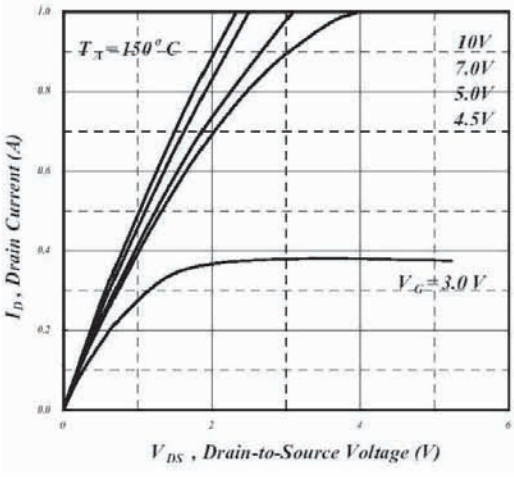


Fig 2. Typical Output Characteristics

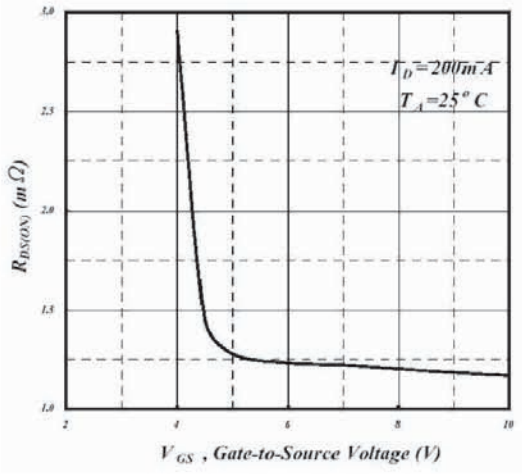


Fig 3. On-Resistance v.s. Gate Voltage

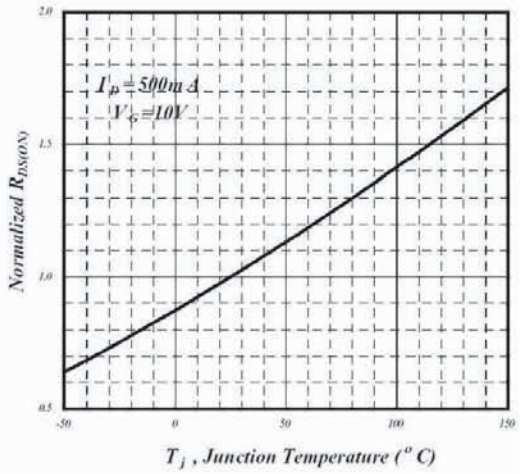


Fig 4. Normalized On-Resistance v.s. Junction Temperature

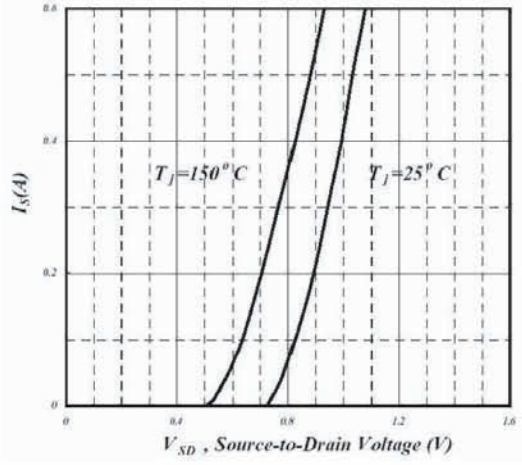


Fig 5. Forward Characteristics of Reverse Diode

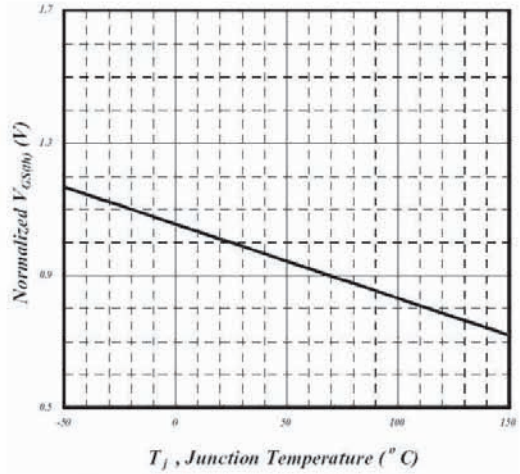


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

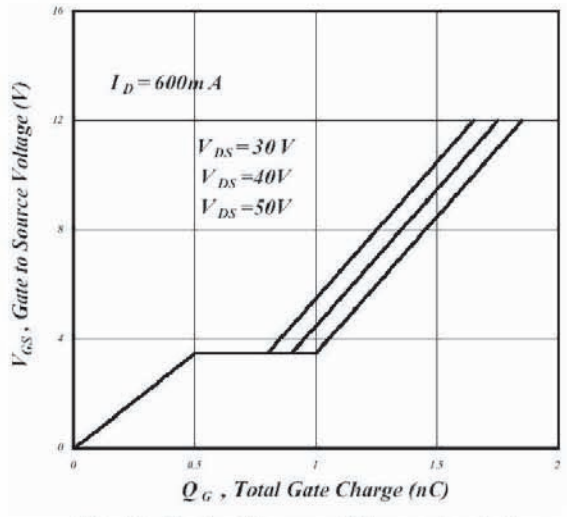


Fig 7. Gate Charge Characteristics

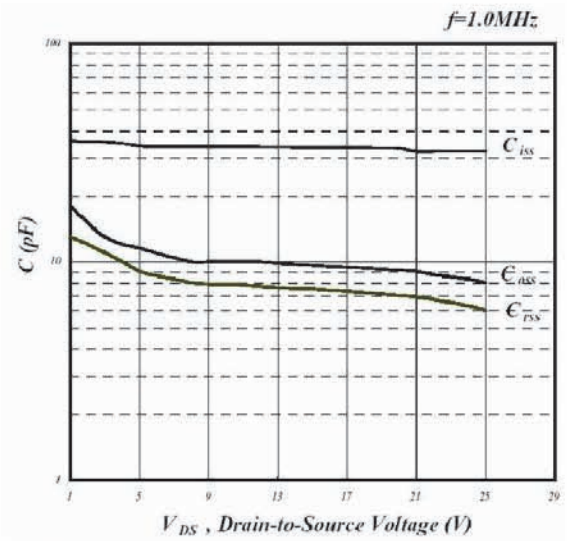


Fig 8. Typical Capacitance Characteristics

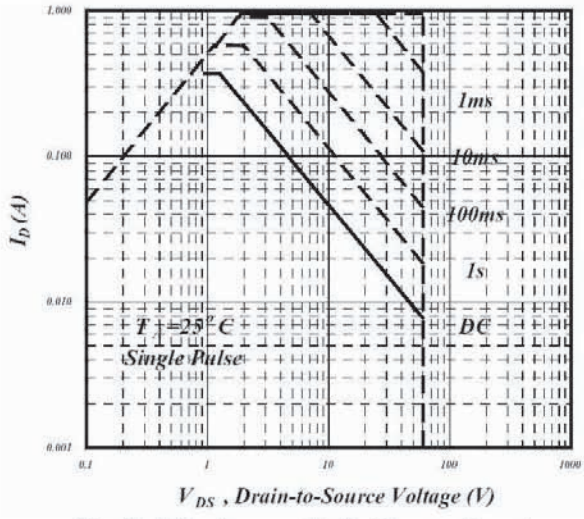


Fig 9. Maximum Safe Operating Area

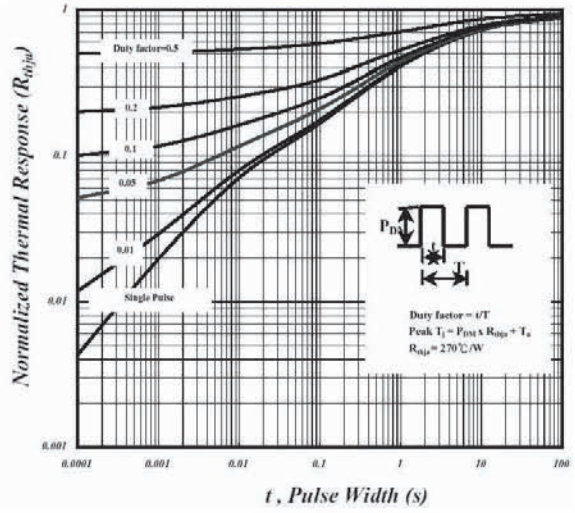


Fig 10. Effective Transient Thermal Impedance

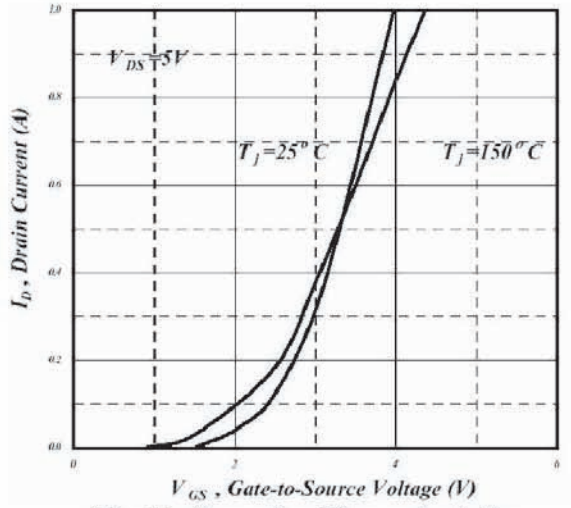


Fig 11. Transfer Characteristics

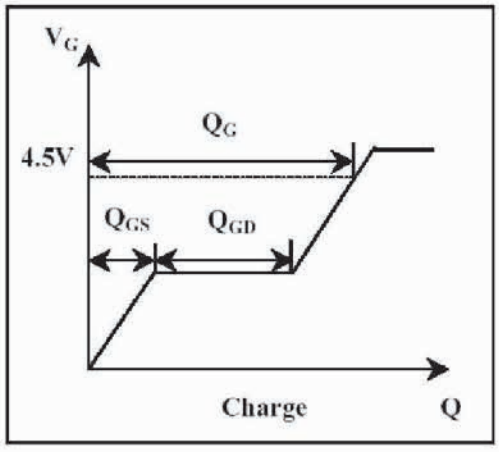
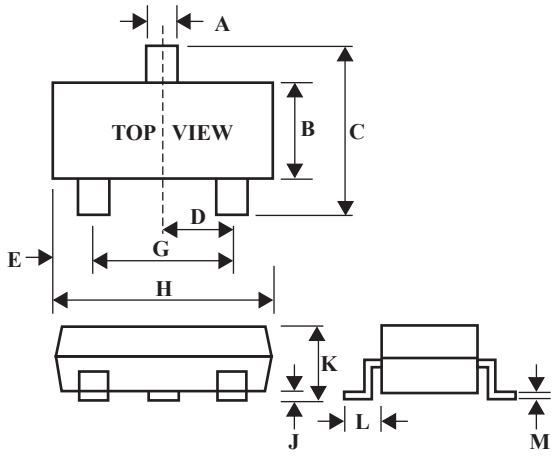


Fig 12. Gate Charge Waveform

SOT-23 Outline Dimension



SOT-23		
Dim	**Min**	**Max**
A	0.35	0.51
B	1.19	1.40
C	2.10	3.00
D	0.85	1.05
E	0.46	1.00
G	1.70	2.10
H	2.70	3.10
J	0.01	0.13
K	0.89	1.10
L	0.30	0.61
M	0.076	0.25