

# NTMFS4701N

## Power MOSFET

### 30 V, 20 A, Single N-Channel, SOIC-8 Flat Lead Package

#### Features

- Thermally and Electrically Enhanced Packaging Compatible with Standard SOIC-8
- New Package Provides Capability of Inspection and Probe After Board Mounting
- Ultra Low  $R_{DS(on)}$  (at 4.5 V<sub>GS</sub>), Low Gate Resistance and Low Q<sub>G</sub>
- Optimized for High Side Control Applications
- High Speed Switching Capability
- These are Pb-Free Devices

#### Applications

- Notebook Computer V<sub>CORE</sub> Applications
- Network Applications
- DC-DC Converters

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit	
Drain-to-Source Voltage		V <sub>DSS</sub>	30	V	
Gate-to-Source Voltage		V <sub>GS</sub>	±20	V	
Continuous Drain Current (Note 1)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	12.3	A
		T <sub>A</sub> = 70°C		9.8	
	t ≤ 10 s	T <sub>A</sub> = 25°C	I <sub>D</sub>	20	
Power Dissipation (Note 1)	Steady State	T <sub>A</sub> = 25°C	P <sub>D</sub>	2.3	W
	t ≤ 10 s	T <sub>A</sub> = 25°C	P <sub>D</sub>	6.0	
Continuous Drain Current (Note 2)	Steady State	T <sub>A</sub> = 25°C	I <sub>D</sub>	7.7	A
		T <sub>A</sub> = 70°C		6.2	
Power Dissipation (Note 2)		T <sub>A</sub> = 25°C	P <sub>D</sub>	0.9	W
Pulsed Drain Current	t <sub>p</sub> = 10 μs	I <sub>DM</sub>	60	A	
Operating and Storage Temperature		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C	
Source Current (Body Diode)		I <sub>S</sub>	6.0	A	
Single Pulse Drain-to-Source Avalanche Energy (V <sub>DD</sub> = 25 V, V <sub>GS</sub> = 10 V, I <sub>PK</sub> = 7.5 A, L = 10 mH, R <sub>G</sub> = 25 Ω)		E <sub>AS</sub>	280	mJ	
Lead Temperature for Soldering Purposes (1/8 in from case for 10 s)		T <sub>L</sub>	260	°C	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

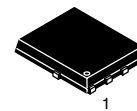
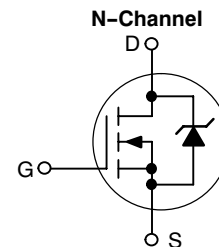
1. Surface-mounted on FR4 board using 1 in sq. pad size (Cu area 1.127 in sq. [1 oz] including traces).
2. Surface-mounted on FR4 board using minimum recommended pad size (Cu area 0.412 in sq.).



**ON Semiconductor®**

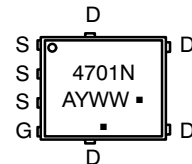
<http://onsemi.com>

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> Typ	I <sub>D</sub> Max
30 V	6.0 mΩ @ 10 V	20 A
	8.0 mΩ @ 4.5 V	



**SOIC-8 FLAT LEAD  
CASE 488AA  
STYLE 1**

#### MARKING DIAGRAM & PIN ASSIGNMENT



- 4701N = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4701NT1G	SOIC-8 FL (Pb-Free)	1500 / ȁpe & Reel
NTMFS4701NT3G	SOIC-8 FL (Pb-Free)	5000 / ȁpe & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTMFS4701N

## THERMAL RESISTANCE RATINGS

Rating	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	4.0	°C/W
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	140	
Junction-to-Ambient - $t \leq 10$ s (Note 1)	$R_{\theta JA}$	21	
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	55	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu$ A	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			7.2		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0$ V, $V_{DS} = 24$ V	$T_J = 25^\circ\text{C}$		1.0	$\mu$ A
			$T_J = 125^\circ\text{C}$		50	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			$\pm 100$	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250$ $\mu$ A	1.0		3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 17$ A		8.0	11	m $\Omega$
			$V_{GS} = 10$ V, $I_D = 20$ A		6.0	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15$ V, $I_D = 20$ A		70		S

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0$ V, $f = 1.0$ MHz, $V_{DS} = 24$ V		1280		pF
Output Capacitance	$C_{OSS}$			500		
Reverse Transfer Capacitance	$C_{RSS}$			120		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5$ V, $V_{DS} = 15$ V, $I_D = 20$ A		11	15	nC
Threshold Gate Charge	$Q_{G(TH)}$			1.1		
Gate-to-Source Charge	$Q_{GS}$			2.0		
Gate-to-Drain Charge	$Q_{GD}$			6.0		
Gate Resistance	$R_G$			1.4		

### SWITCHING CHARACTERISTICS, $V_{GS} = 4.5$ V (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10$ V, $V_{DD} = 15$ V, $I_D = 1.0$ A, $R_G = 6.0$ $\Omega$		9.0		ns
Rise Time	$t_r$			4.0		
Turn-Off Delay Time	$t_{d(OFF)}$			29		
Fall Time	$t_f$			19		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0$ V, $I_S = 6.0$ A	$T_J = 25^\circ\text{C}$		0.75	1.0	V
			$T_J = 125^\circ\text{C}$		0.55		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0$ V, $dI_S/dt = 100$ A/ $\mu$ s, $I_S = 6.0$ A			34		ns
Charge Time	$t_a$				16		
Discharge Time	$t_b$				18		
Reverse Recovery Charge	$Q_{RR}$				27		

3. Pulse Test: Pulse Width  $\leq 300$   $\mu$ s, Duty Cycle  $\leq 2\%$ .

4. Switching characteristics are independent of operating junction temperatures.

# NTMFS4701N

## TYPICAL PERFORMANCE CURVES

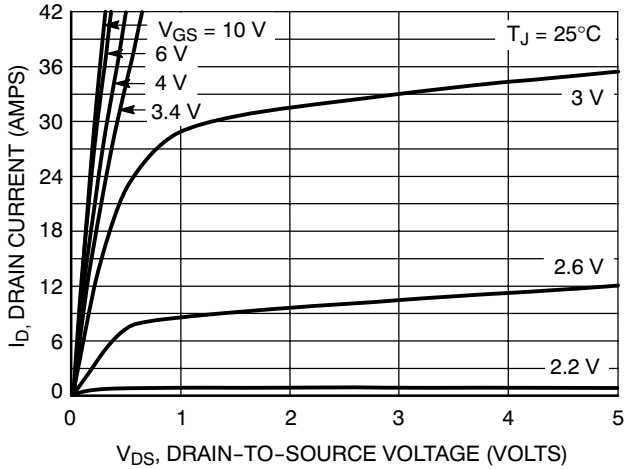


Figure 1. On-Region Characteristics

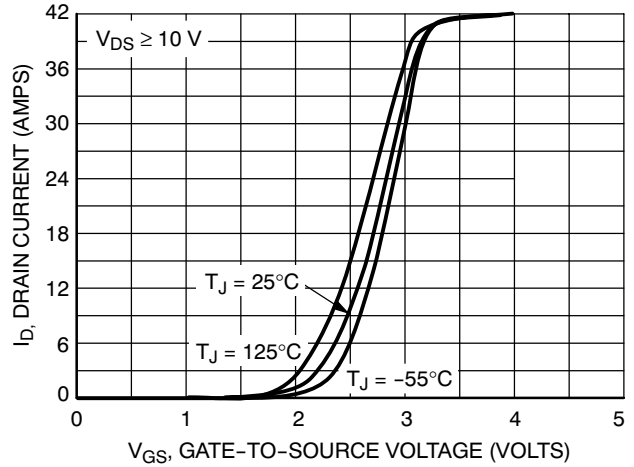


Figure 2. Transfer Characteristics

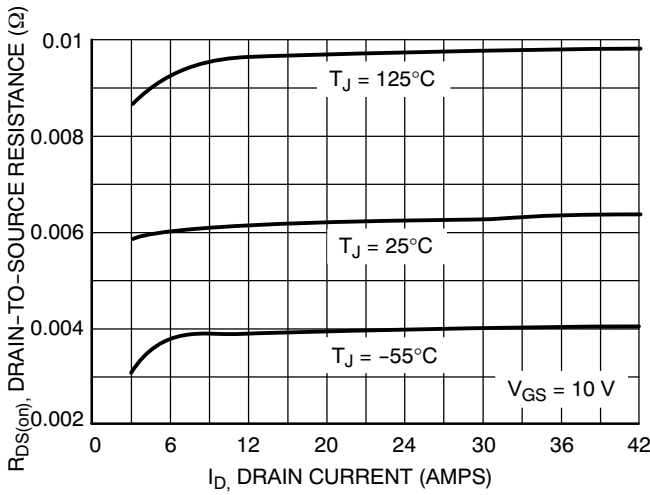


Figure 3. On-Resistance vs. Drain Current and Temperature

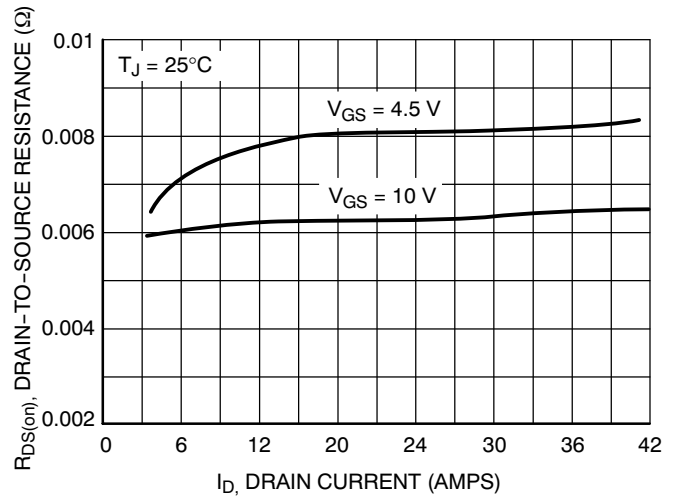


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

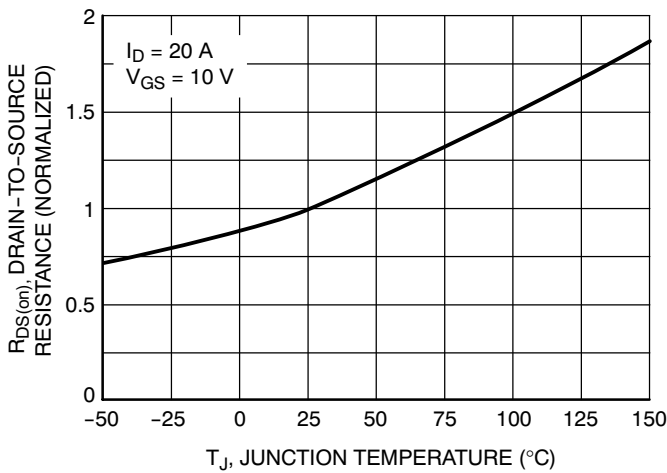


Figure 5. On-Resistance Variation with Temperature

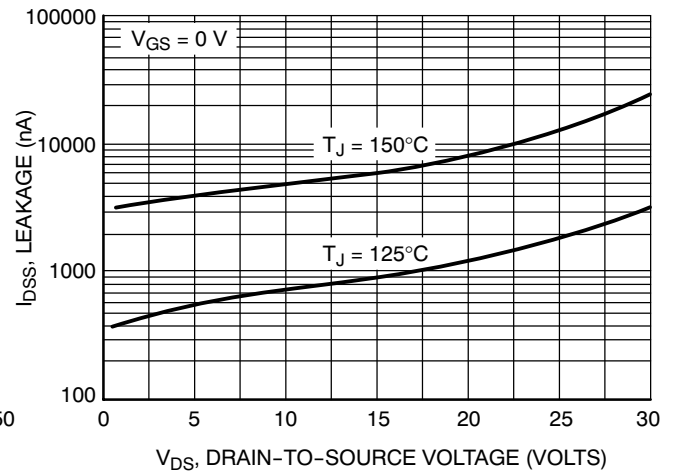


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

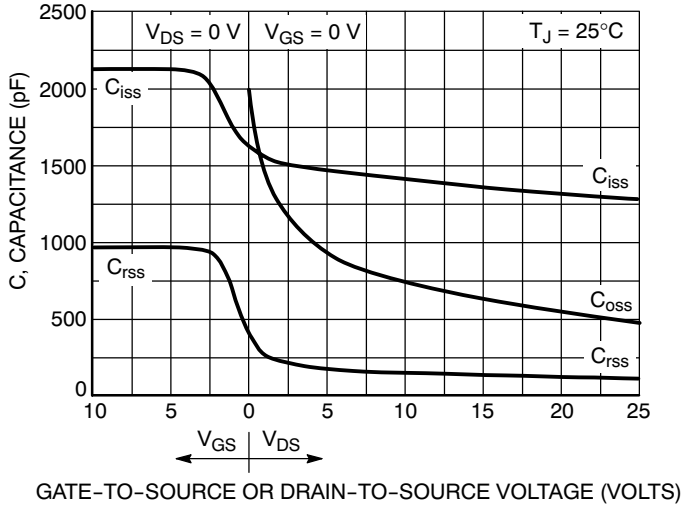


Figure 7. Capacitance Variation

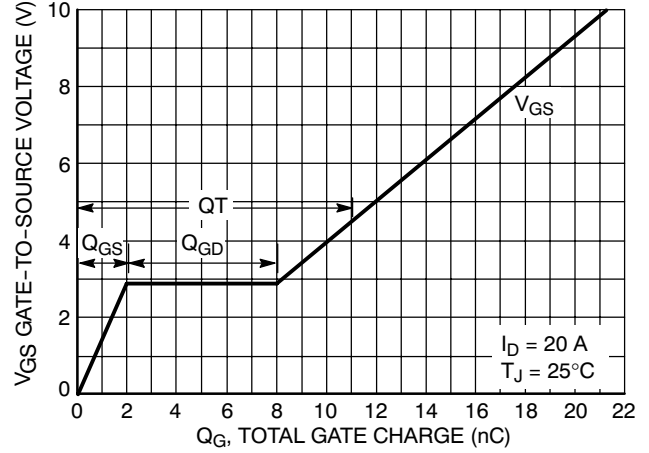


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

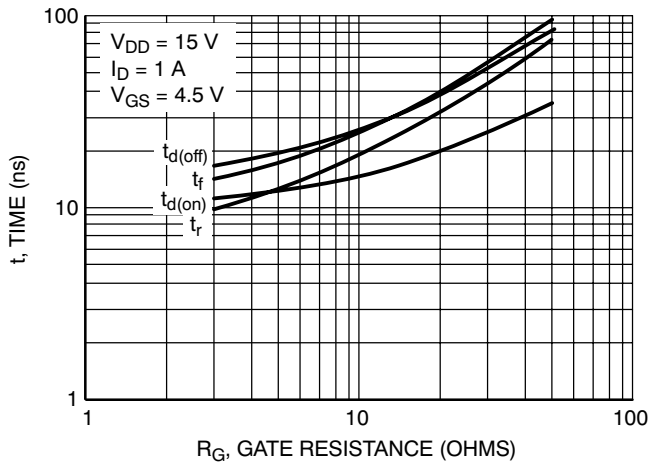


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

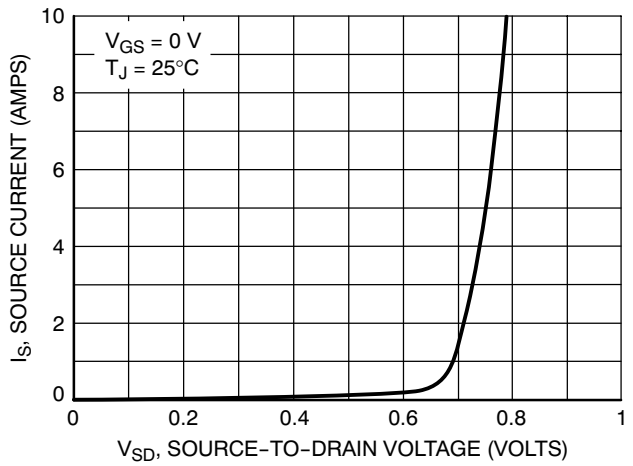


Figure 10. Diode Forward Voltage vs. Current

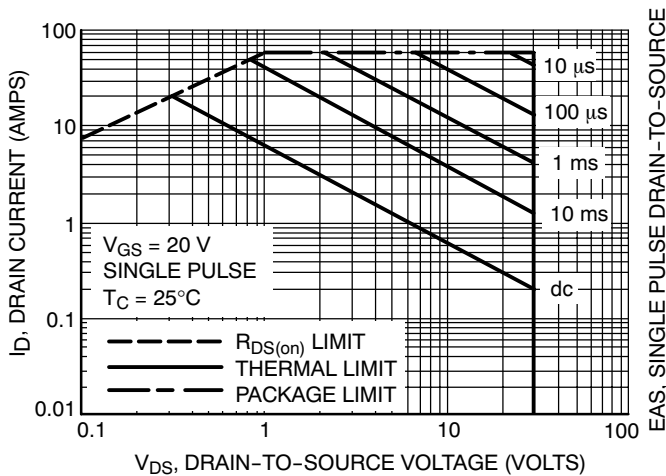


Figure 11. Maximum Rated Forward Biased Safe Operating Area

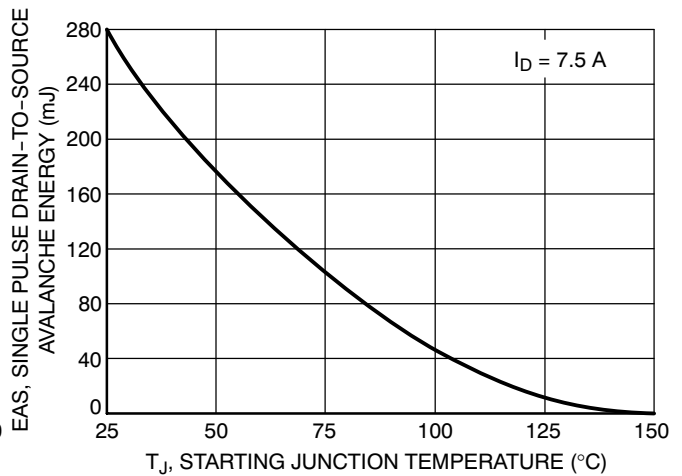
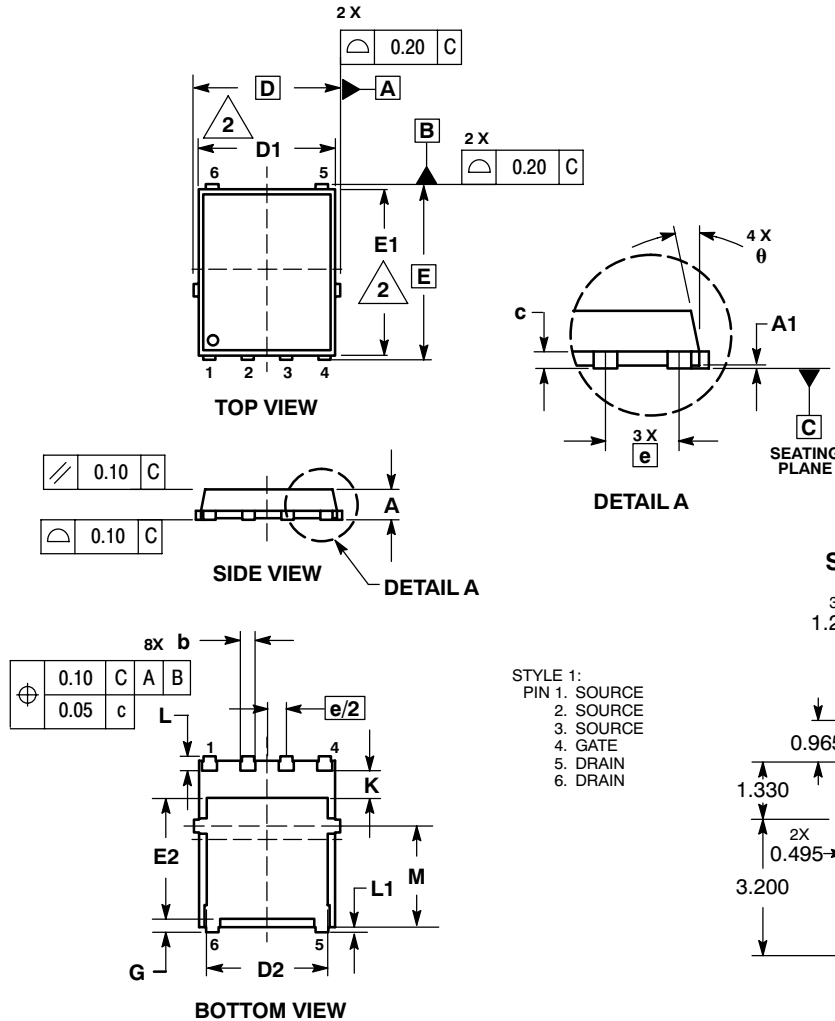


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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## PACKAGE DIMENSIONS

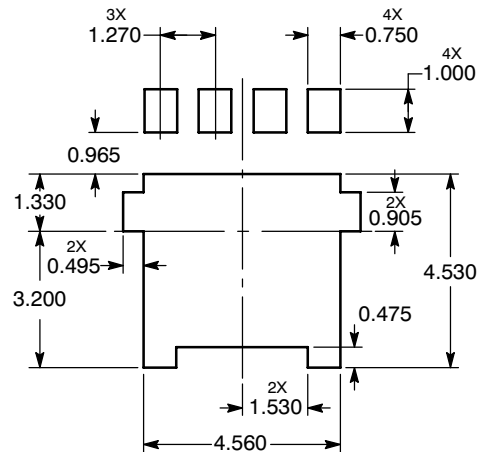
DFN6 5x6, 1.27P (SO8 FL)  
CASE 488AA-01  
ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.50	4.90	5.10
D2	3.50	---	4.22
E	6.15 BSC		
E1	5.50	5.80	6.10
E2	3.45	---	4.30
e	1.27 BSC		
G	0.51	0.61	0.71
K	0.51	---	---
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0°	---	12°

### SOLDERING FOOTPRINT\*



- STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN  
6. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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