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RoHS

Three Phase Field Effect Transistor Pre-driver

33937
33937A

THREE-PHASE PRE-DRIVER

EK SUFFIX (Pb-FREE)
98ASA99334D
54-PIN SOICW-EP

The 33937 and 33937A are Field Effect Transistor (FET) pre-drivers designed for three phase motor control and similar applications. The 33937A has been specifically enhanced to improve performance when driving very high current loads. The integrated circuit (IC) uses *SMARTMOS*™ technology.

The IC contains three High Side FET pre-drivers and three Low Side FET pre-drivers.Three external bootstrap capacitors provide gate charge to the High Side FETs.

The IC interfaces to a MCU via six direct input control signals, an SPI port for device setup and asynchronous reset, enable and interrupt signals. Both 5.0 and 3.0 V logic level inputs are accepted and 5.0 V logic level outputs are provided.

Features

- Fully specified from 8.0 to 40 V covers 12 and 24 V automotive systems
- Extended operating range from 6.0 to 58 V covers 12 and 42 V systems
- Greater than 1.0 A gate drive capability with protection
- Protection against reverse charge injection from CGD and CGS of external FETs
- Includes a charge pump to support full FET drive at low battery voltages
- Deadtime is programmable via the SPI port
- Simultaneous output capability enabled via safe SPI command
- Pb-free packaging designated by suffix code EK

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MCZ33937EK/R2	-40°C to 135°C	54 SOICW-EP
MCZ33937AEK/R2		

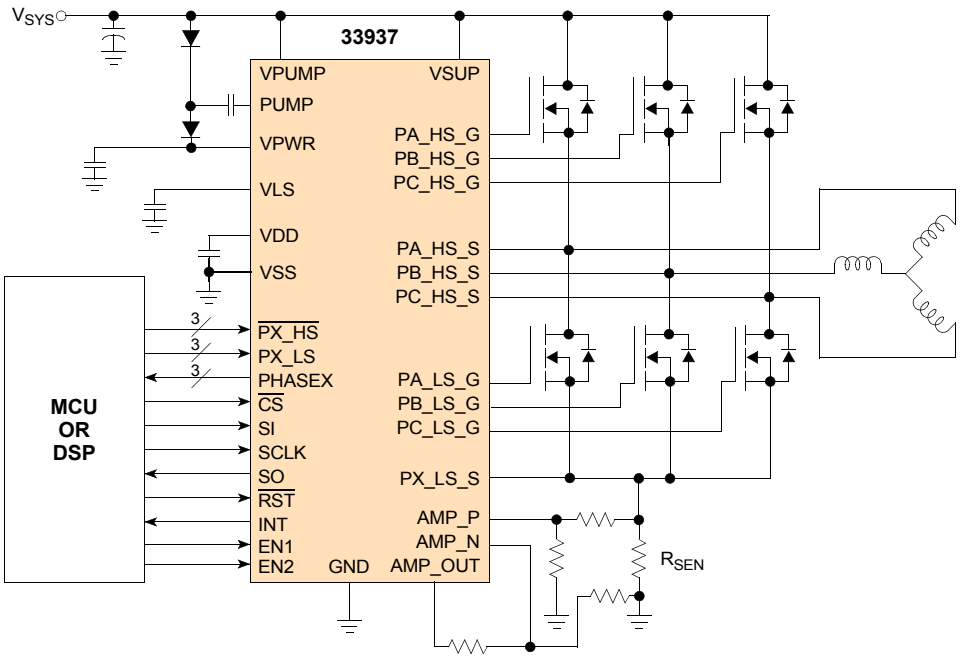

Figure 1. 33937 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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DEVICE VARIATIONS

Table 1. Device Variations

Freescale Part No.	Significant Device Variations	Reference Location
MCZ33937	Loss of regulation during indeterminate RESET level High Bootstrap initialization current causes reset	Note 2 on page 7 Caution on page 28
MCZ33937A	Invalid zero length SPI commands cause Framing Errors	Framing Error on page 37

INTERNAL BLOCK DIAGRAM

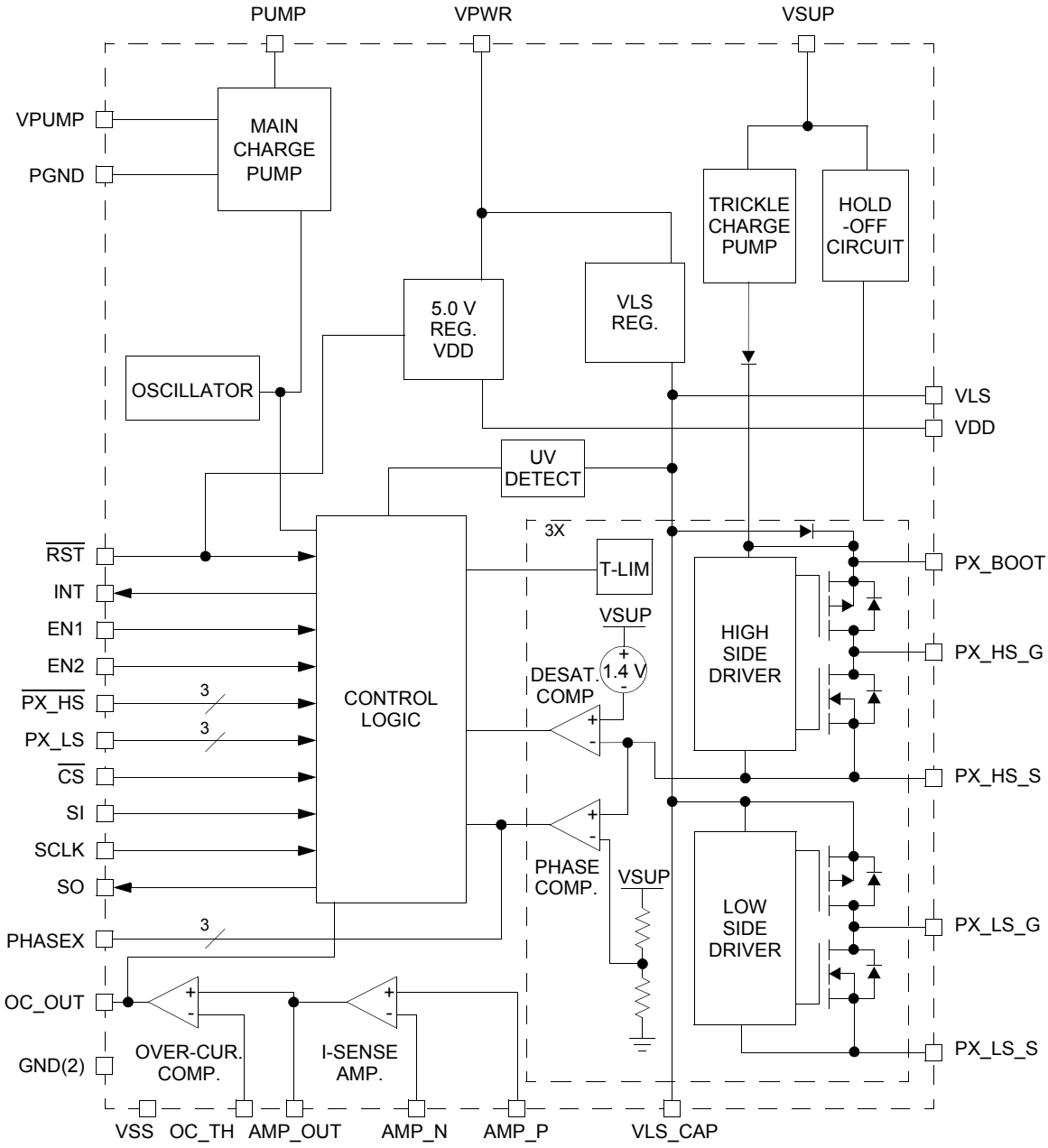


Figure 2. 33937 Simplified Internal Block Diagram

PIN CONNECTIONS

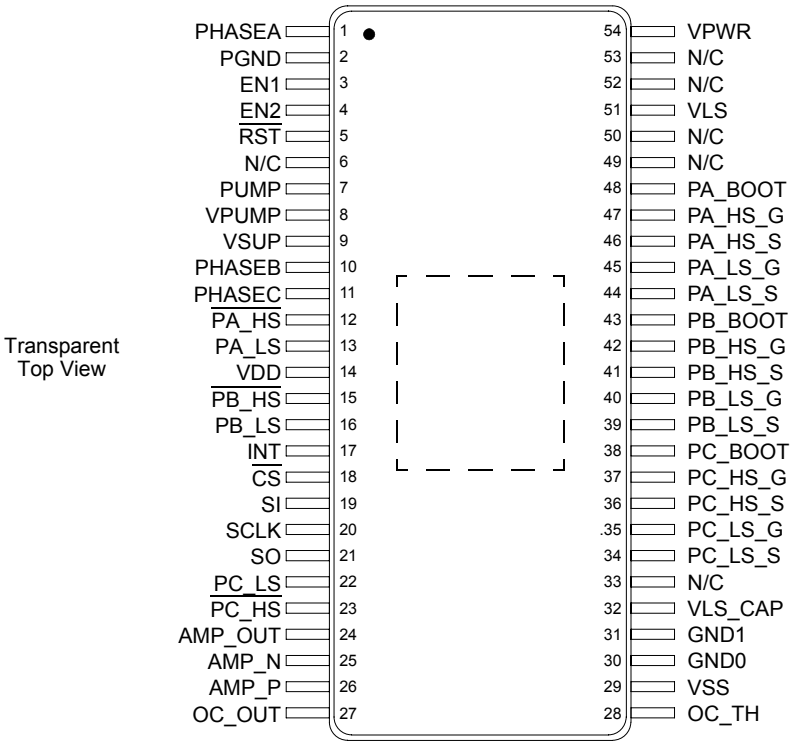


Figure 3. 33937 Pin Connections

Table 2. 33937 Pin Definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 23.

Pin	Pin Name	Pin Function	Formal Name	Definition
1	PHASEA	Digital Output	Phase A	Totem Pole output of Phase A comparator. This output is low when the voltage on PA_HS_S (Source of High Side FET) is less than 50% of V_{SUP}
2	PGND	Ground	Power Ground	Power ground for charge pump
3	EN1	Digital Input	Enable 1	Logic signal input must be high (ANDed with EN2) to enable any gate drive output.
4	EN2	Digital Input	Enable 2	Logic signal input must be high (ANDed with EN1) to enable any gate drive output
5	$\overline{RST}$	Digital Input	Reset	Reset input
6, 33, 49, 50, 52, 53	N/C	–	No Connect	Do not connect these pins
7	PUMP	Power Drive Out	Pump	Charge pump output
8	VPUMP	Power Input	Voltage Pump	Charge pump supply
9	VSUP	Analog Input	Supply Voltage	Supply voltage to the load. This pin is to be connected to the common Drains of the external High Side FETs
10	PHASEB	Digital Output	Phase B	Totem Pole output of Phase B comparator. This output is low when the voltage on PB_HS_S (Source of High Side FET) is less than 50% of V_{SUP}
11	PHASEC	Digital Output	Phase C	Totem Pole output of Phase C comparator. This output is low when the voltage on PC_HS_S (Source of High Side FET) is less than 50% of V_{SUP}

Table 2. 33937 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 23.

Pin	Pin Name	Pin Function	Formal Name	Definition
12	$\overline{\text{PA\_HS}}$	Digital Input	Phase A High Side	Active low input logic signal enables the High Side Driver for Phase A
13	PA_LS	Digital Input	Phase A Low Side	Active high input logic signal enables the Low Side Driver for Phase A
14	VDD	Analog Output	VDD Regulator	VDD regulator output capacitor connection.
15	$\overline{\text{PB\_HS}}$	Digital Input	Phase B High Side	Active low input logic signal enables the High Side Driver for Phase B
16	PB_LS	Digital Input	Phase B Low Side	Active high input logic signal enables the Low Side Driver for Phase B
17	INT	Digital Output	Interrupt	Interrupt pin output
18	$\overline{\text{CS}}$	Digital Input	Chip Select	Chip Select input. It frames SPI commands and enables SPI port
19	SI	Digital Input	Serial In	Input data for SPI port. Clocked on the falling edge of SCLK, MSB first
20	SCLK	Digital Input	Serial Clock	Clock for SPI port and typically is 3.0 MHz
21	SO	Digital Output	Serial Out	Output data for SPI port. Tri-state until $\overline{\text{CS}}$ becomes low
22	PC_LS	Digital Input	Phase C Low Side	Active high input logic signal enables the Low Side Driver for Phase C
23	$\overline{\text{PC\_HS}}$	Digital Input	Phase C High Side	Active low input logic signal enables the High Side Driver for Phase C
24	AMP_OUT	Analog Output	Amplifier Output	Output of the current-sensing amplifier
25	AMP_N	Analog Input	Amplifier Invert	Inverting input of the current-sensing amplifier
26	AMP_P	Analog Input	Amplifier Non-Invert	Non-inverting input of the current-sensing amplifier
27	OC_OUT	Digital Output	Over-current Out	Totem pole digital output of the Over-current Comparator
28	OC_TH	Analog Input	Over-current Threshold	Threshold of the over-current detector
29	VSS	Ground	Voltage Source Supply	Ground reference for logic interface and power supplies
30, 31	GND	Ground	Ground	Substrate and ESD reference, connect to VSS
32	VLS_CAP	Analog Output	VLS Regulator Output Capacitor	VLS Regulator connection for additional output capacitor, providing low impedance supply source for Low Side Gate Drive
34	PC_LS_S	Power Input	Phase C Low Side Source	Source connection for Phase C Low Side FET
35	PC_LS_G	Power Output	Phase C Low Side Gate Drive	Gate drive output for Phase C Low Side
36	PC_HS_S	Power Input	Phase C High Side Source	Source connection for Phase C High Side FET
37	PC_HS_G	Power Output	Phase C High Side Gate Drive	Gate Drive for output Phase C High Side FET
38	PC_BOOT	Analog Input	Phase C Bootstrap	Bootstrap capacitor for Phase C
39	PB_LS_S	Power Input	Phase B Low Side Source	Source connection for Phase B Low Side FET
40	PB_LS_G	Power Output	Phase B Low Side Gate Drive	Gate Drive for output Phase B Low Side
41	PB_HS_S	Power Input	Phase B High Side Source	Source connection for Phase B High Side FET
42	PB_HS_G	Power Output	Phase B High Side Gate Drive	Gate Drive for output Phase B High Side
43	PB_BOOT	Analog Input	Phase B Bootstrap	Bootstrap capacitor for Phase B
44	PA_LS_S	Power Input	Phase A Low Side Source	Source connection for Phase A Low Side FET

Table 2. 33937 Pin Definitions (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 23.

Pin	Pin Name	Pin Function	Formal Name	Definition
45	PA_LS_G	Power Output	Phase A Low Side Gate Drive	Gate Drive for output Phase A Low Side
46	PA_HS_S	Power Input	Phase A High Side Source	Source connection for Phase A High Side FET
47	PA_HS_G	Power Output	Phase A High Side Gate Drive	Gate Drive for output Phase A High Side
48	PA_BOOT	Analog Input	Phase A Bootstrap	Bootstrap capacitor for Phase A
51	VLS	Analog Output	VLS Regulator	VLS regulator output. Power supply for the gate drives
54	VPWR	Power Input	Voltage Power	Power supply input for gate drives
	EP	Ground	Exposed Pad	Device will perform as specified with the Exposed Pad un-terminated (floating) however, it is recommended that the Exposed Pad be terminated to pin 29 (VSS) and system ground

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to V_{SS} unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
VSUP Supply Voltage	V_{SUP}		V
Normal Operation (Steady-state)		58	
Transient Survival[1]		-1.5 to 80	
VPWR Supply Voltage	V_{PWR}		V
Normal Operation (Steady-state)		58	
Transient Survival[1]		-1.5 to 80	
Charge Pump (PUMP, VPUMP)	V_{PUMP}	-0.3 to 40	V
VLS Regulator Outputs (VLS, VLS_CAP)[2]	V_{LS}	-0.3 to 18	V
Logic Supply Voltage	V_{DD}	-0.3 to 7.0	V
Logic Output (INT, SO, PHASEA, PHASEB, PHASEC, OC_OUT)[3]	V_{OUT}	-0.3 to 7.0	V
Logic Input Pin Voltage (EN1, EN2, $\overline{\text{Px\_HS}}$, Px_LS, SI, SCLK, $\overline{\text{CS}}$, $\overline{\text{RST}}$) 10 mA	V_{IN}	-0.3 to 7.0	V
Amplifier Input Voltage	V_{IN_A}		V
(Both Inputs-GND), (AMP_P - GND) or (AMP_N - GND) 6.0 mA source or sink		-7.0 to 7.0	
Over-current comparator threshold 10 mA	V_{OC}	-0.3 to 7.0	V
Driver Output Voltage[4]			V
High Side bootstrap (PA_BOOT, PB_BOOT, PC_BOOT)	V_{BOOT}	75	
High Side (PA_HS_G, PB_HS_G, PC_HS_G)	V_{HS_G}	75	
Low Side (PA_LS_G, PB_LS_G, PC_LS_G)	V_{LS_G}	16	
Driver Voltage Transient Survival[5]			V
High Side (PA_HS_G, PB_HS_G, PC_HS_G, PA_HS_S, PB_HS_S, PC_HS_S)	V_{HS_G}	-7.0 to 75.0	
	V_{HS_S}	-7.0 to 75.0	
Low Side (PA_LS_G, PB_LS_G, PC_LS_G, PA_LS_S, PB_LS_S, PC_LS_S)	V_{LS_G}	-7.0 to 18.0	
	V_{LS_S}	-7.0 to 7.0	

Notes

1. The device will withstand load dump transient as defined by ISO7637 with peak voltage of 80 V.
2. Normal operation of the 33937 at VPWR voltages greater than 28V can result in degradation or failure of the VLS regulator due to transients induced during a RESET. A 20 V transient suppressor is recommended on the VLS pin (pin 51) to prevent excessive stress under these conditions. Using the 33937A will avoid this limitation.
3. Short-circuit proof, the device will not be damaged or induce unexpected behavior due to shorts to external sources within this range.
4. This voltage should not be applied without also taking voltage at HS_S and voltage at PX_LS_S into account.
5. Actual operational limitations may differ from survivability limits. The V_{LS} - V_{LS_S} differential and the V_{BOOT} - V_{HS_S} differential must be greater than 3.0 V to insure the output gate drive will maintain a commanded OFF condition on the output.

Table 3. Maximum Ratings (continued)

All voltages are with respect to V_{SS} unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ESD Voltage[6]	V_{ESD}		V
Human Body Model - HBM (All pins except for the pins listed below)		±2000	
Pins: PA_Boot, PA_HS_S, PA_HS_G, PB_Boot, PB_HS_S, PB_HS_G, PC_Boot, PC_HS_S, PC_HS_G, VPWR		±1000	
Charge Device Model - CDM			
Corner pins		±750	
All other pins		±300	
THERMAL RATINGS			
Storage Temperature	T_{STG}	-55 to +150	°C
Operating Junction Temperature	T_J	-40 to +150	°C
Thermal Resistance[7]			°C/W
Junction-to-Case	$R_{\theta JC}$	3.0	
Soldering Temperature[8]	T_{SOLDER}	Note 9	°C

Notes

6. ESD testing is performed in accordance with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
7. Case is considered EP - pin 55 under the body of the device. The actual power dissipation of the device is dependent on the operating mode, the heat transfer characteristics of the board and layout and the operating voltage. See Figure 24 and Figure 25 for examples of power dissipation profiles of two common configurations. Operation above the maximum operating junction temperature will result in a reduction in reliability leading to malfunction or permanent damage to the device.
8. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
9. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC ELECTRICAL CHARACTERISTICS

Table 4. Static Electrical Characteristics

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40°C ≤ T_A ≤ 135°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUTS					
VPWR Supply Voltage Startup Threshold[10]	V_{PWR_ST}	–	6.0	8.0	V
VSUP Supply Current, V_{PWR} = V_{SUP} = 40 V $\overline{RST}$ and ENABLE = 5.0 V No output loads on Gate Drive Pins, No PWM No output loads on Gate Drive Pins, 20 kHz, 50% Duty Cycle	I_{SUP}	 – –	 1.0 –	 – 10	mA
VPWR Supply Current, V_{PWR} = V_{SUP} = 40 V $\overline{RST}$ and ENABLE = 5.0 V No output loads on Gate Drive Pins, No PWM, Outputs initialized Output Loads = 620 nC per FET, 20 kHz PWM[11]	I_{PWR_ON}	 – –	 11 –	 20 95	mA
Sleep State Supply Current, $\overline{RST}$ = 0 V V_{SUP} = 40 V V_{PWR} = 40 V	 I_{SUP} I_{PWR}	 – –	 14 56	 30 100	µA
Sleep State Output Gate Voltage IG < 100 µA	V_{GATESS}	 –	 –	 1.3	V
Trickle Charge Pump (Bootstrap Voltage) V_{SUP} = 14 V	V_{Boot}	 22	 28	 32	V
Bootstrap Diode Forward Voltage at 10 mA	V_F	–	–	1.2	V
VDD INTERNAL REGULATOR					
V_{DD} Output Voltage, V_{PWR} = 8 to 40 V, C = 0.47 µF[12] External Load I_{DD_EXT} = 0 to 1.0 mA	V_{DD}	 4.5	 –	 5.5	V
Internal V_{DD} Supply Current, V_{DD} = 5.5 V, No External Load	I_{DD}	–	–	12	mA
VLS REGULATOR					
Peak Output Current, V_{PWR} = 16 V, V_{LS} = 10 V	I_{PEAK}	350	600	800	mA
Linear Regulator Output Voltage, I_{VLS} = 0 to 60 mA[13]	V_{LS}	13.5	15	17	V
VLS Disable Threshold[14]	V_{THVLS}	7.5	8.0	8.5	V

Notes

10. Operation with the Charge Pump is recommended when minimum system voltage could be less than 14 V. V_{PWR} must exceed this threshold in order for the Charge Pump and V_{DD} regulator to startup and drive V_{PWR} to > 8.0 V. Once V_{PWR} exceeds 8.0 V, the circuits will continue to operate even if system voltage drops below 6.0 V.
11. This parameter is guaranteed by design. It is not production tested.
12. Minimum external capacitor for stable V_{DD} operation is 0.47 µF.
13. Recommended external capacitor for the V_{LS} regulator is 2.2 µF low ESR at each pin VLS and VLS_CAP.
14. When V_{LS} is less than this value, the outputs are disabled and HOLDOFF circuits are active. Recovery is automatic when V_{LS} rises above this threshold again. A filter delay of approximately 700 ns on the comparator output eliminates responses to spurious transients on V_{LS}.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40°C ≤ T_A ≤ 135°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CHARGE PUMP					
Charge Pump					
High Side Switch On Resistance	$R_{DS(on)\_HS}$	–	6.0	10	Ω
Low Side Switch On Resistance	$R_{DS(on)\_LS}$	–	5.0	9.4	Ω
Regulation Threshold Difference(15), (17)	V_{THREG}	250	500	900	mV
Charge Pump Output Voltage(16), (17)	V_{CP}				V
I_{OUT} = 40 mA, 6.0 V < V_{SYS} < 8.0 V		8.5	9.5	–	
I_{OUT} = 40 mA, V_{SYS} > = 8.0 V		12	–	–	
GATE DRIVE					
High Side Driver On Resistance (Sourcing)	$R_{DS(ON)\_H\_SRC}$				Ω
V_{PWR} = V_{SUP} = 16 V, -40°C ≤ T_A ≤ 25°C		–	–	6.0	
V_{PWR} = V_{SUP} = 16 V, 25°C < T_A ≤ 135°C		–	–	8.5	
High Side Driver On Resistance (Sinking)	$R_{DS(ON)\_H\_SINK}$				Ω
V_{PWR} = V_{SUP} = 16 V		–	–	3.0	
High Side Current Injection Allowed Without Malfunction(17), (18)	I_{HS_INJ}	–	–	0.5	A
Low Side Driver On Resistance (Sourcing)	$R_{DS(ON)\_L\_SRC}$				Ω
V_{PWR} = V_{SUP} = 16 V, -40°C ≤ T_A ≤ 25°C		–	–	6.0	
V_{PWR} = V_{SUP} = 16 V, 25°C < T_A ≤ 135°C		–	–	8.5	
Low Side Driver On-Resistance (Sinking)	$R_{DS(ON)\_L\_SINK}$				Ω
V_{PWR} = V_{SUP} = 16 V		–	–	3.0	
Low Side Current Injection Allowed Without Malfunction(17), (18)	I_{LS_INJ}	–	–	0.5	A
Gate Source Voltage, V_{PWR} = V_{SUP} = 40 V					V
High Side, I_{GATE} = 0(19)	V_{GS_H}	13	14.8	16.5	
Low Side, I_{GATE} = 0	V_{GS_L}	13	15.4	17	
High Side Gate Drive Output Leakage Current, Per Output(20)	I_{HS_LEAK}	–	–	18	µA

Notes

15. When VLS is this amount below the normal VLS linear regulation threshold, the charge pump is enabled.
16. V_{SYS} is the system voltage on the input to the charge pump. With recommended external components (1.0 µF, MUR 120 diode). The Charge Pump is designed to supply the gate currents of a system with 100 A FETs in a 12 V application.
17. This parameter is a design characteristic, not production tested.
18. Current injection only occurs during output switch transitions. The IC is immune to specified injected currents for a duration of approximately 1.0µs after an output switch transition. 1.0 µs is sufficient for all intended applications of this IC.
19. If a slightly higher gate voltage is required, larger bootstrap capacitors are required. At high duty cycles, the bootstrap voltage may not recover completely, leading to a higher output on-resistance. This effect can be minimized by using low ESR capacitors for the bootstrap and the VLS capacitors.
20. A small internal charge pump will supply up to 30 µA nominal to compensate for leakage on the High Side FET gate output and maintain voltages after bootstrap events. It is not intended for external components to be connected to the High Side FET gate, but small amounts of additional leakage can be accommodated. See Figures 11 through 14 for typical load margins.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40°C ≤ T_A ≤ 135°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
OVER-CURRENT COMPARATOR					
Common Mode Input Range[22]	V_{CM}	2.0	–	V_{DD}-0.02	V
Input Offset Voltage	V_{OS_OC}	-50	–	50	mV
Over-current Comparator Threshold Hysteresis[21]	V_{OC_HYST}	50		300	mV
Output Voltage High Level at I_{OH} = -500 µA Low Level at I_{OL} = 500 µA	 V_{OH} V_{OL}	 0.85 V_{DD} –	 – –	 V_{DD} 0.5	V
HOLD OFF CIRCUIT					
Hold Off Current (At Each GATE Pin) 3.0 V < V_{SUP} < 40 V[23]	I_{HOLD}	10	–	300	µA
PHASE COMPARATOR					
High Level Input Voltage Threshold	V_{IH_TH}	0.5 V_{SUP}	–	0.65 V_{SUP}	V
Low Level Input Voltage Threshold	V_{IL_TH}	0.3 V_{SUP}	–	0.45 V_{SUP}	V
High Level Output Voltage at I_{OH} = -500 µA	V_{OH}	0.85 V_{DD}	–	V_{DD}	V
Low Level Output Voltage at I_{OL} = 500 µA	V_{OL}	–	–	0.5	V
High Side Source Input Resistance[21, 26]	R_{IN}	–	40	–	kΩ
DESATURATION DETECTOR					
Desaturation Detector Threshold[24]	V_{DES_TH}	1.2	1.4	1.6	V
CURRENT SENSE AMPLIFIER					
Recommended External Series Resistor (See Figure 9)	R_S	–	1.0	–	kΩ
Recommended External Feedback Resistor (See Figure 9)[27] Limited by the Output Voltage Dynamic Range	R_{FB} 	 5.0	 –	 15	kΩ
Maximum Input Differential Voltage (See Figure 9) V_{ID} = V_{AMP_P} - V_{AMP_N}	V_{ID} 	 -800	 –	 +800	mV
Input Common Mode Range[21, 25]	V_{CM}	-0.5	–	3.0	V
Input Offset Voltage R_S = 1.0 kΩ, V_{CM} = 0.0 V	V_{OS} 	 -15	 –	 +15	mV
Input Offset Voltage Drift[21]	$\delta V_{OS}/\delta T$	–	-10	–	µV/°C
Input Bias Current V_{CM} = 2.0 V	I_b 	 -200	 –	 +200	nA

Notes

21. This parameter is a design characteristic, not production tested.
22. As long as one input is in the common mode range there is no phase inversion on the output.
23. The hold off circuit is designed to operate over the full operating range of V_{SUP}. The specification indicates the conditions used in production test. Hold off is activated at V_{THRST} or V_{THVLS}.
24. Desaturation is measured as the voltage drop below V_{SUP}, thus the threshold is compared to the drain-source voltage of the external High Side FET. See Figure 5.
25. As long as one input is within V_{CM} the output is guaranteed to have the correct phase. Exceeding the common mode rails on one input will not cause a phase inversion on the output.
26. Input resistance is impedance from High Side source and is referenced to V_{SS}. Approximate tolerance is ±20%.
27. The current sense amplifier is unity gain stable with a phase margin of approximately 45°. See Figure 10.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40°C ≤ T_A ≤ 135°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE AMPLIFIER (CONTINUED)					
Input Offset Current I_{OS} = I_{AMP_P} - I_{AMP_N}	I_{OS}	-80	–	+80	nA
Input Offset Current Drift (28)	$\delta I_{OS}/\delta T$	–	40	–	pA/°C
Output Voltage High Level with R_{LOAD} = 10 kΩ to V_{SS} Low Level with R_{LOAD} = 10 kΩ to V_{DD}	 V_{OH} V_{OL}	 V_{DD}-0.2 –	 – –	 V_{DD} 0.2	V
Differential Input Resistance	R_I	1.0	–	–	MΩ
Output Short-circuit Current	I_{SC}	5.0	–	–	mA
Common Mode Input Capacitance at 10 kHz (28), (29)	C_I	–	–	10	pF
Common Mode Rejection Ratio at DC CMRR = 20*Log ((V_{OUT_diff}/V_{IN_diff}) * (V_{IN_CM}/V_{OUT_CM}))	CMRR	60	80	–	dB
Large Signal Open Loop Voltage Gain (DC) (28), (29)	A_{OL}	–	78	–	dB
Nonlinearity (28), (29) RL = 1.0 kΩ, C_L = 500 pF, 0.3 < V_O < 4.8 V, Gain = 5.0 to 15	NL	-1.0	–	+1.0	%

Notes

28. This parameter is a design characteristic, not production tested.
29. Without considering any offsets such as input offset voltage, internal mismatch and assuming no tolerance error in external resistors.

Table 4. Static Electrical Characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40°C ≤ T_A ≤ 135°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPERVISORY AND CONTROL CIRCUITS					
Logic Inputs (Px_LS, $\overline{Px\_HS}$, EN1, EN2) (31)					V
High Level Input Voltage Threshold	V_{IH}	–	–	2.1	
Low Level Input Voltage Threshold	V_{IL}	0.9	–	–	
Logic Inputs (SI, SCLK, $\overline{CS}$) (30), (31)					V
High Level Input Voltage Threshold	V_{IH}	–	–	2.1	
Low Level Input Voltage Threshold	V_{IL}	0.9	–	–	
Input Logic Threshold Hysteresis (30)	V_{IHYS}				mV
Inputs Px_LS, SI, SCLK, $\overline{CS}$, $\overline{Px\_HS}$, EN1, EN2		100	250	450	
Input Pull-down Current, (Px_LS, SI, SCLK, EN1, EN2)	I_{INPD}				µA
0.3 V_{DD} ≤ V_{IN} ≤ V_{DD}		8.0	–	18	
Input Pull-up Current, ($\overline{CS}$, $\overline{Px\_HS}$) (32)	I_{INPU}				
0 ≤ V_{IN} ≤ 0.7 V_{DD}		10	–	25	µA
Input Capacitance (30)	C_{IN}				pF
0.0 V ≤ V_{IN} ≤ 5.5 V		–	15	–	
$\overline{RST}$ Threshold (33)	$V_{TH\_\overline{RST}}$	1.0	–	2.1	V
$\overline{RST}$ Pull-down Resistance	$R_{\overline{RST}}$				kΩ
0.3 V_{DD} ≤ V_{IN} ≤ V_{DD}		40	60	85	
Power-ON $\overline{RST}$ Threshold, (V_{DD} Falling)	$V_{TH\overline{RST}}$	3.4	4.0	4.5	V
SO High Level Output Voltage	V_{SOH}				V
I_{OH} = 1.0 mA		0.9 V_{DD}	–	–	
SO Low Level Output Voltage	V_{SOL}				V
I_{OL} = 1.0 mA		–	–	0.1 V_{DD}	
SO Tri-state Leakage Current	$I_{SO\_LEAK\_T}$				µA
$\overline{CS}$ = 0.7 V_{DD}, 0.3 V_{DD} = V_{SO} = 0.7 V_{DD}		-1.0	–	1.0	
SO Tri-state Capacitance (30), (34)	C_{SO_T}				pF
0.0 V ≤ V_{IN} ≤ 5.5 V		–	15	–	
INT High Level Output Voltage	V_{OH}				V
I_{OH} = -500 µA		0.85 V_{DD}	–	V_{DD}	
INT Low Level Output Voltage	V_{OL}				V
I_{OL} = 500 µA		–	–	0.5	
THERMAL WARNING					
Thermal Warning Temperature (30), (35)	T_{WARN}	150	170	185	°C
Thermal Hysteresis (30)	T_{HYST}	8.0	10	12	°C

Notes

30. This parameter is guaranteed by design, not production tested.
31. Logic threshold voltages derived relative to a 3.3 V 10% system.
32. Pull-up circuits will not allow back biasing of V_{DD}.
33. There are two elements in the $\overline{RST}$ circuit: 1) one generally lower threshold enables the internal regulator; 2) the second removes the reset from the internal logic.
34. This parameter applies to the OFF state (tri-stated) condition of SO is guaranteed by design but is not production tested.
35. The Thermal Warning circuit does not force IC shutdown above this temperature. It is possible to set a bit in the MASK register to generate an interrupt when overtemperature is detected, and the status bit will always indicate if any of the three individual Thermal Warning circuits in the IC sense a fault.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 5. Dynamic Electrical Characteristics

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40°C ≤ T_A ≤ 135°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
INTERNAL REGULATORS					
V_{DD} Power-Up Time (Until INT High) 8.0 V ≤ V_{PWR} (36)	t_{PU_VDD}	–	–	2.0	ms
VLS Power-Up Time 16 V ≤ V_{PWR} (37)	t_{PU_VDD}	–	–	2.0	ms
CHARGE PUMP					
Charge Pump Oscillator Frequency	F_{OSC}	90	125	190	kHz
Charge Pump Slew Rate(38)	SR_{CP}	–	100	–	V/µs
GATE DRIVE					
High Side Turn On Time(39) Transition Time from 1.0 to 10 V, Load: C = 500 pF, Rg = 0, (Figure 7)	t_{ONH}	–	20	35	ns
High Side Turn On Delay(40) Delay from Command to 1.0 V, (Figure 7)	t_{D_ONH}	130	265	386	ns
High Side Turn Off Time(39) Transition Time from 10 to 1.0 V, Load: C = 500 pF, Rg = 0, (Figure 8)	t_{OFFH}	–	20	35	ns
High Side Turn Off Delay(40) Delay from Command to 10 V, (Figure 8)	t_{D_OFFH}	130	265	386	ns
Low Side Turn On Time(39) Transition Time from 1.0 to 10 V, Load: C = 500 pF, Rg = 0, (Figure 7)	t_{ONL}	–	20	35	ns
Low Side Turn On Delay(40) Delay from Command to 1.0 V, (Figure 7)	t_{D_ONL}	130	265	386	ns
Low Side Turn Off Time(39) Transition Time from 10 to 1.0 V, Load: C = 500 pF, Rg = 0, (Figure 8)	t_{OFFL}	–	20	35	ns
Low Side Turn Off Delay(40) Delay from Command to 10 V, (Figure 8)	t_{D_OFFL}	130	265	386	ns
Same Phase Command Delay Match(41)	t_{D_DIFF}	-20	0	+20	ns
Thermal Filter Duration (42)	t_{DUR}	8.0	–	30	µs

Notes

36. The power-up time of the IC depends in part on the time required for this regulator to charge up the external filter capacitor on V_{DD}.
37. The power-up time of the IC depends in part on the time required for this regulator to charge up the external filter capacitors on VLS and VLS_CAP. This delay includes the expected time for V_{DD} to rise.
38. The charge pump operating at 12 V V_{SYS}, 1.0µF pump capacitor, MUR120 diodes and 47 µF filter capacitor.
39. This parameter is guaranteed by characterization, not production tested.
40. These delays include all logic delays except deadtime. All internal logic is synchronous with the internal clock. The total delay includes one clock period for state machine decision block, an additional clock period for FULLON mux logic, input synchronization time and output driver propagation delay. Subtract one clock period for operation in FULLON mode which bypasses the state machine decision block. Synchronization time accounts for up to one clock period of variation. See Figure 6.
41. The maximum separation or overlap of the High and Low Side gate drives, due to propagation delays when commanding one ON and the other OFF simultaneously, is guaranteed by design.
42. The output of the overtemperature comparator goes through a digital filter before generating a warning or interrupt.

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40°C ≤ T_A ≤ 135°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
GATE DRIVE (CONTINUED)					
Duty Cycle (43), (44)	t_{DC}	0.0	–	96	%
100% Duty Cycle Duration (43), (44)	t_{DC}	–	–	Unlimited	s
Maximum Programmable Deadtime (45)	t_{MAX}	10.2	15	19.6	µs
OVER-CURRENT COMPARATOR					
Over-current Protection Filter Time	t_{OC}	0.9	–	3.5	µs
Rise Time (OC_OUT) 10% - 90% C_L = 100 pF	t_{ROC}	10	–	240	ns
Fall Time (OC_OUT) 90% - 10% C_L = 100 pF	t_{FOC}	10	–	200	ns
DESATURATION DETECTOR AND PHASE COMPARATOR					
Phase Comparator Propagation Delay Time to 50% of V_{DD}; C_L ≤ 100 pF Rising Edge Delay Falling Edge Delay	 t_R t_F	 – –	 – –	 200 350	ns
Phase Comparator Match (Prop Delay Mismatch of Three Phases) C_L = 100 pF (43)	t_{MATCH}	–	–	100	ns
Desaturation and Phase Error Blanking Time(46)	t_{BLANK}	4.7	7.1	9.1	µs
Desaturation Filter Time (Filter Time is digital) (43) Fault Must be Present for This Time to Trigger	t_{FILT}	 640	 937	 1231	ns
CURRENT SENSE AMPLIFIER					
Output Settle Time to 99% (43), (47) RL = 1.0 kΩ, C_L = 500 pF, 0.3 V < V_O < 4.8 V, Gain = 5 to 15	t_{SETTLE}	 –	 1.0	 2.0	µs

Notes

43. This parameter is guaranteed by design, not production tested.
44. Maximum duty cycle is actually 100% because there is an internal charge pump to maintain the gate voltage in the 100% on condition. However, in high duty cycle cases, there may not be sufficient time to recharge the bootstrap capacitors during the off time. Large bootstrap capacitors will allow high duty cycles to be obtained for a short time. For applications needing closer to 100% duty cycle, external diodes may optionally be used to provide high peak current charging capability to the bootstrap capacitors. These diodes would be connected between VLS and the Px_BOOTSTRAP pins. In applications with lower gate charge requirements, the maximum duty cycle can also be increased.
45. A Minimum Deadtime of 0.0 can be set via an SPI command. When Deadtime is set via a DEADTIME command, a minimum of 1 clock cycle duration and a maximum of 255 clock cycles is set using the internal time base clock as a reference. Commands exceeding this value limits at this value.
46. Blanking time, t_{BLANK}, is applied to all phases simultaneously when switching ON any output FET. This precludes false errors due to system noise during the switching event.
47. Without considering any offsets such as input offset voltage, internal mismatch and assuming no tolerance error in external resistors.

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40°C ≤ T_A ≤ 135°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE AMPLIFIER (CONTINUED)					
Output Rise Time to 90% (49) RL = 1.0 kΩ, C_L = 500 pF, 0.3 V < V_O < 4.8 V, Gain = 5.0 to 15	t_{IS_RISE}	–	–	1.0	µs
Output Fall Time to 10% (49) RL = 1.0 kΩ, C_L = 500 pF, 0.3 V < V_O < 4.8 V, Gain = 5.0 to 15	t_{IS_FALL}	–	–	1.0	µs
Slew Rate at Gain = 5.0(48) RL = 1.0 kΩ, C_L = 20 pF	SR(5)	5.0	–	–	V/µs
Phase Margin at Gain = 5.0(48)	f_M	–	30	–	°
Unity Gain Bandwidth (48) RL = 1.0 kΩ, C_L = 100 pF	G_{BW}	–	20	–	MHz
Bandwidth at Gain = 15 (48) R_L = 1.0 kΩ, C_L = 50 pF	BW_G	2.0	–	–	MHz
Common Mode Rejection (CMR) (48) with V_{IN} V_{IN_CM} = 400 mV*sin(2*π*freq*t) V_{IN_DIF} = 0.0 V, RS = 1.0 kΩ R_{FB} = 15 kΩ, V_{REFIN} = 0.0 V CMR = 20*Log(V_{OUT}/V_{IN_CM}) Freq = 100 kHz Freq = 1.0 MHz Freq = 10 MHz	CMR	 50 40 30	 – – –	 – – –	dB
SUPERVISORY AND CONTROL CIRCUITS					
EN1 and EN2 Propagation Delay	t_{PROP}	–	–	280	ns
INT Rise Time CL = 100 pF	t_{RINT}	10	–	250	ns
INT Fall Time CL = 100 pF	t_{FINT}	10	–	200	ns
INT Propagation Time	$t_{PROPINT}$	–	–	250	ns

Notes
48. This parameter is guaranteed by design, not production tested.
49. Rise and fall times are measured from the transition of a step function on the input to 90% of the change in output voltage.

Table 5. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 8.0 V ≤ V_{PWR} = V_{SUP} ≤ 40 V, -40°C ≤ T_A ≤ 135°C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SPI INTERFACE TIMING					
Maximum Frequency of SPI Operation	f_{OP}	–		4.0	MHz
Internal Time Base	f_{TB}	13	17	25	MHz
Internal Time Base drift from value at 25°C (50)	TC_{TB}	-5.0	–	5.0	%
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time) (50)	t_{LEAD}	100	–	–	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time) (50)	t_{LAG}	100	–	–	ns
SI to Falling Edge of SCLK (Required Setup Time) (50)	t_{SISU}	25	–	–	ns
Falling Edge of SCLK to SI (Required Setup Time) (50)	t_{SIHOLD}	25	–	–	ns
SI, $\overline{CS}$, SCLK Signal Rise Time (50), (51)	t_{RSI}	–	5.0	–	ns
SI, $\overline{CS}$, SCLK Signal Fall Time (50), (51)	t_{FSI}	–	5.0	–	ns
Time from Falling Edge of $\overline{CS}$ to SO Low-impedance (50), (52)	t_{SOEN}	–	55	100	ns
Time from Rising Edge of $\overline{CS}$ to SO High-impedance (50), (53)	t_{SODIS}	–	100	125	ns
Time from Rising Edge of SCLK to SO Data Valid (50), (54)	t_{VALID}	–	80	125	ns
Time from Rising Edge of $\overline{CS}$ to Falling Edge of the next $\overline{CS}$ (50)	t_{DT}	200	–	–	ns

Notes
50. This parameter is guaranteed by design, not production tested.
51. Rise and Fall time of incoming SI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
52. Time required for valid output status data to be available on SO pin.
53. Time required for output states data to be terminated at SO pin.
54. Time required to obtain valid data out from SO following the rise of SCLK with 200 pF load.

TIMING DIAGRAMS

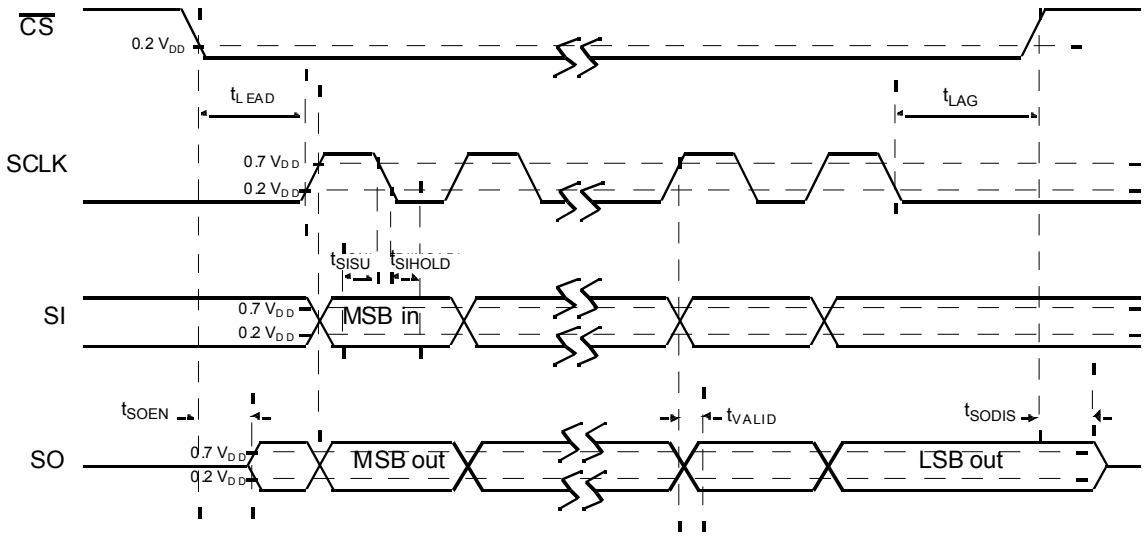


Figure 4. SPI Interface Timing

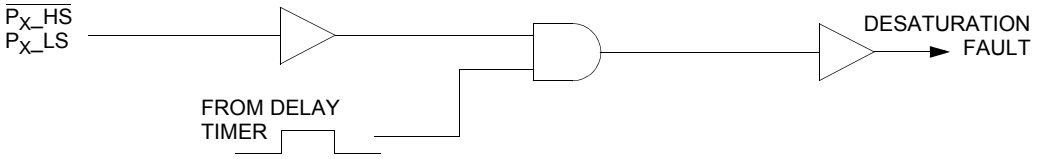


Figure 5. Desaturation Blanking and Filtering Detail

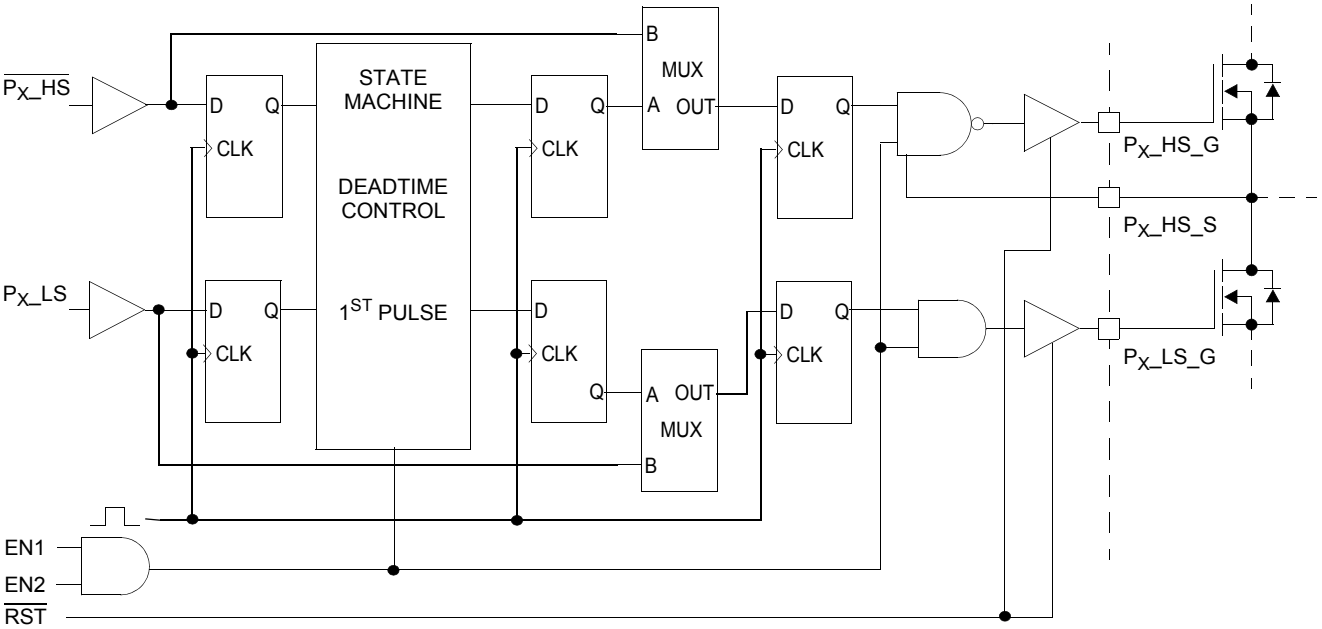


Figure 6. Deadtime Control Delays

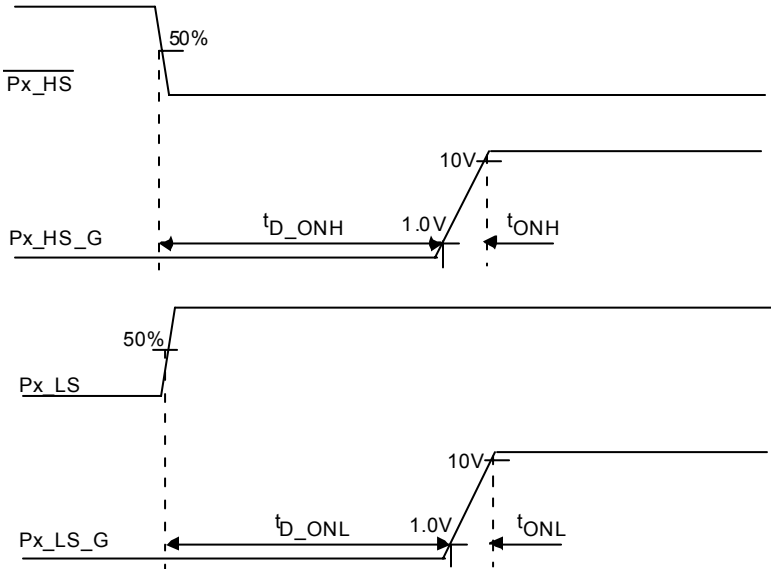


Figure 7. Driver Turn-On Time and Turn-On Delay

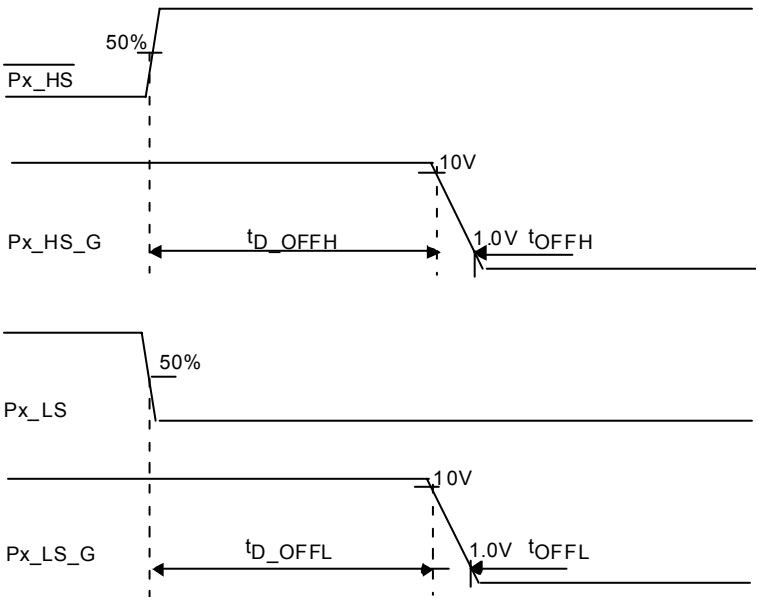


Figure 8. Driver Turn-off Time and Turn-off Delay

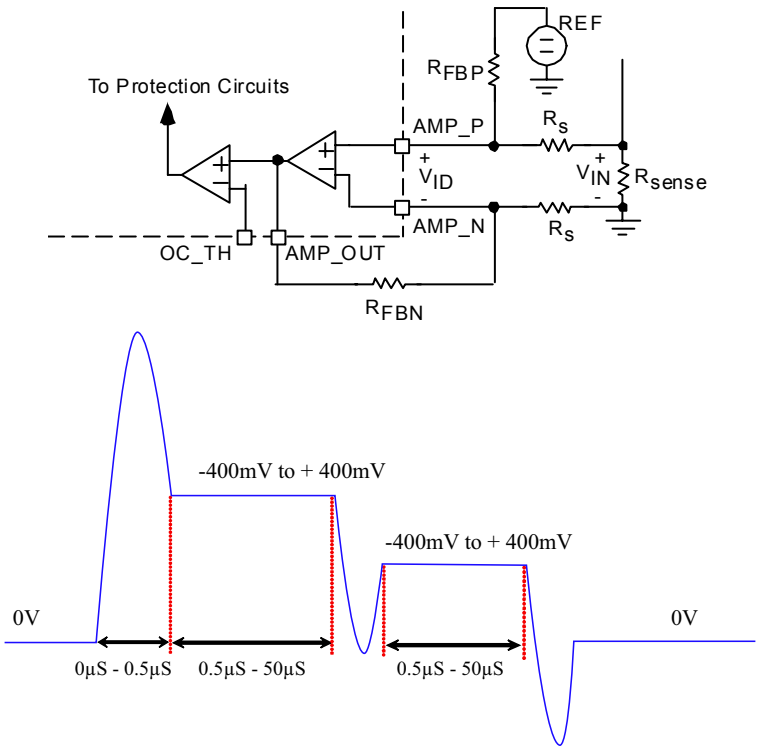


Figure 9. Current Amplifier and Input Waveform (V_{IN} Voltage Across R_{SENSE})

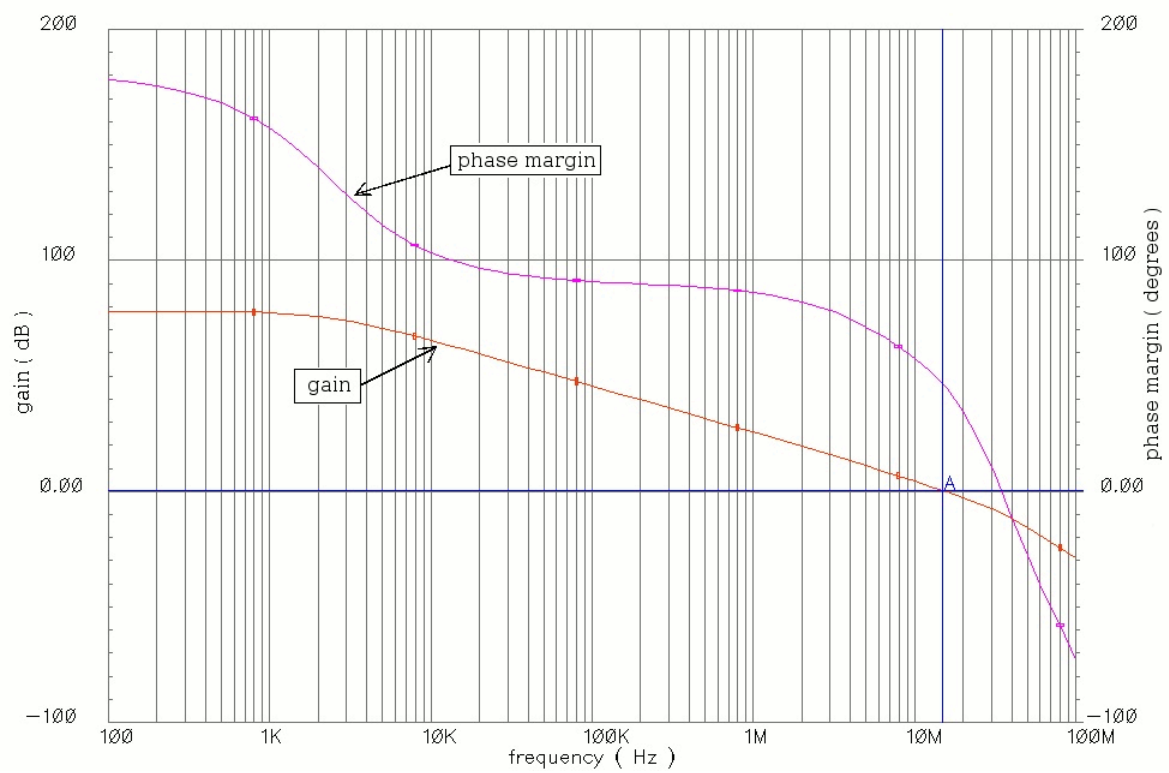


Figure 10. Typical Amplifier Open-loop Gain and Phase Margin vs Frequency

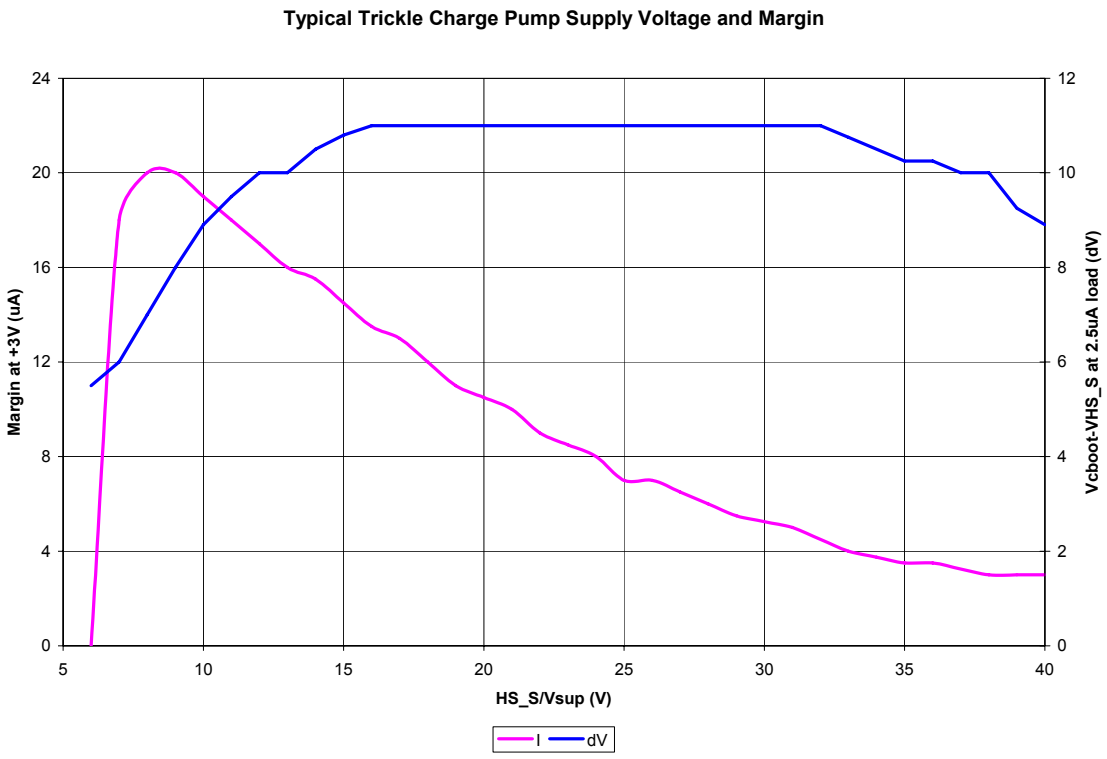


Figure 11. Typical Trickle Charge Pump Supply Voltage and Current Margin vs Supply Voltage

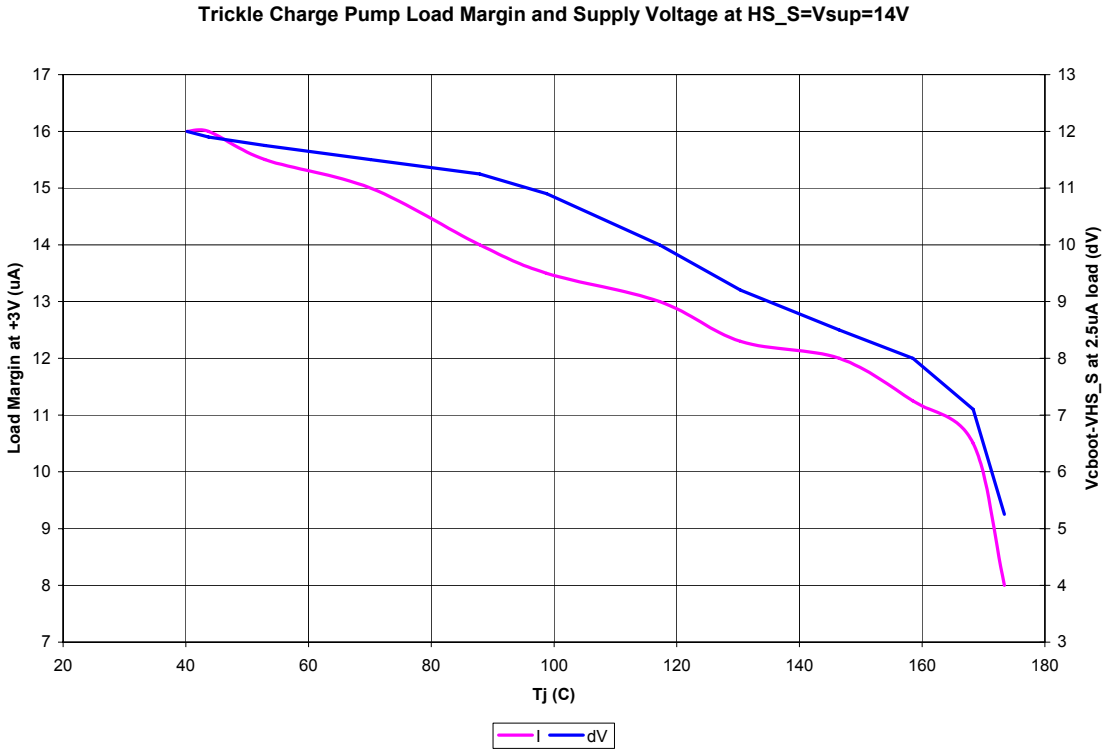


Figure 12. Typical Voltage and Load Margin For Increasing Junction Temperature at 14 V on HS_S

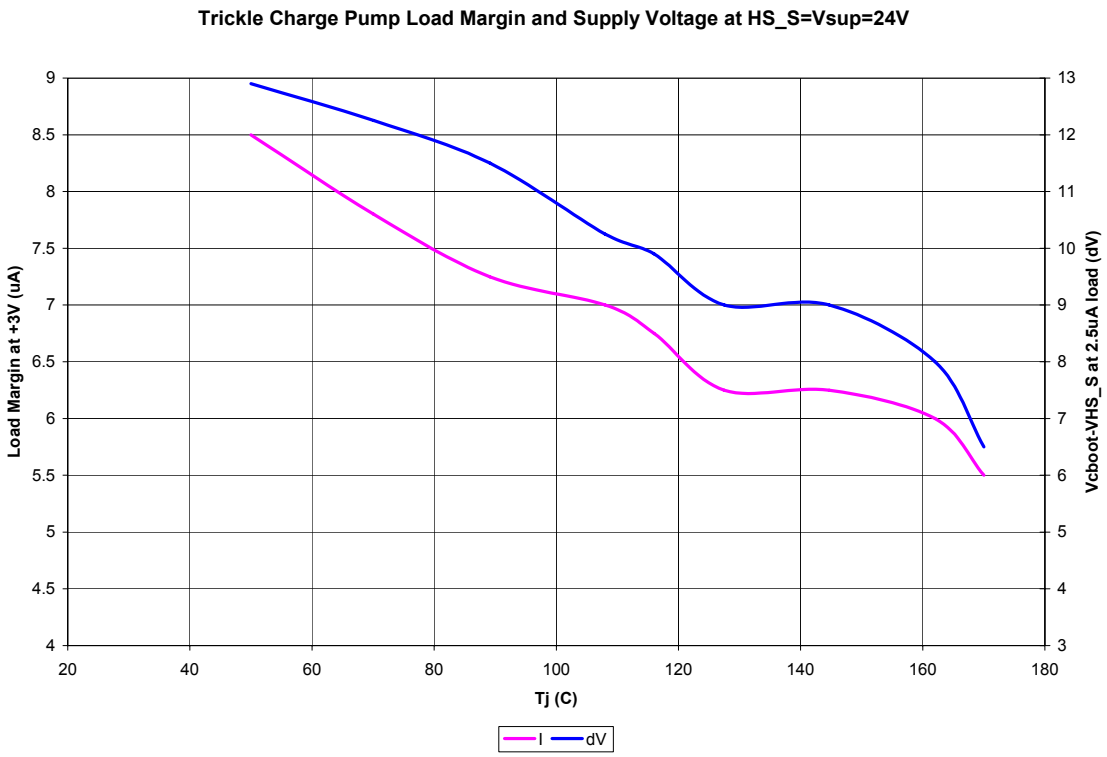


Figure 13. Typical Voltage and Load Margin For Increasing Junction Temperature at 24 V on HS_S

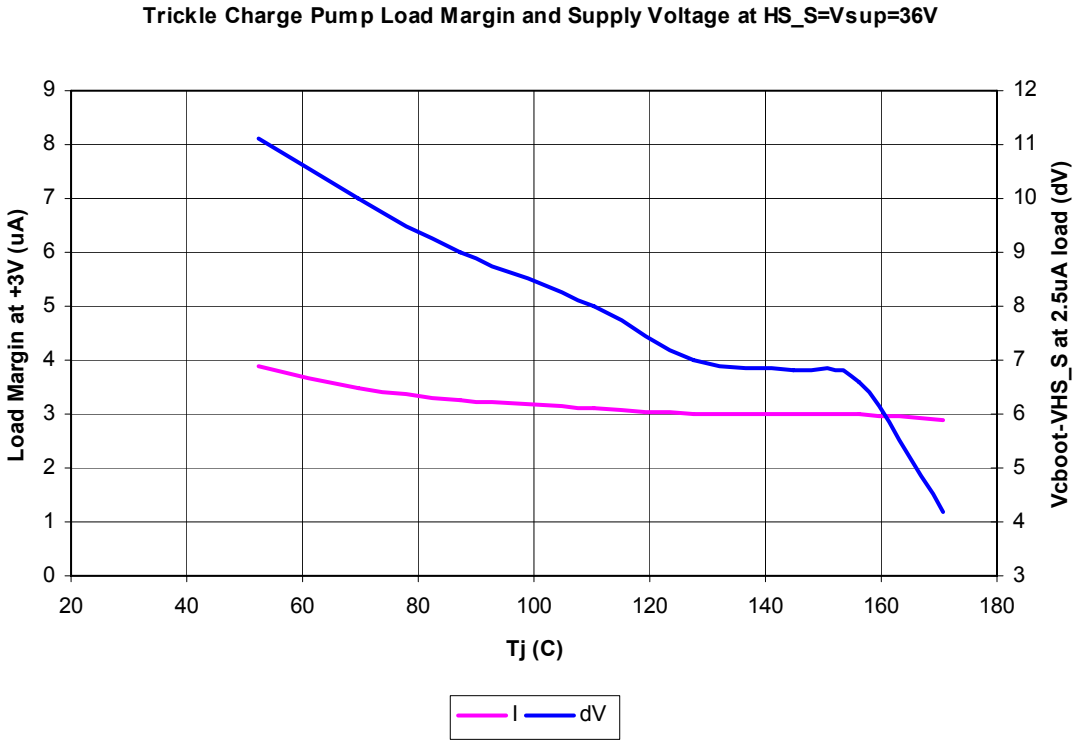


Figure 14. Typical Voltage and Load Margin For Increasing Junction Temperature at 36 V on HS_S

FUNCTIONAL DESCRIPTIONS

INTRODUCTION

The 33937 provides an interface between an MCU and the large FETs used to drive three phase loads. A typical load FET may have an on resistance of 4.0 mΩ or less and could require a gate charge of over 400 nC to fully turn on. The IC can operate in automotive 12 to 42 V environments.

Because there are so many methods of controlling three phase systems, the IC enforces few constraints on driving the FETs. It does provide deadtime (cross-over) blanking and logic, both of which can be overridden, ensuring both FETs in a phase are not simultaneously enabled.

An SPI port is used to configure the IC modes.

FUNCTIONAL PIN DESCRIPTION

PHASE A (PHASEA)

This pin is the totem pole output of the Phase A comparator. This output is low when the voltage on Phase A High Side source (source of the High Side load FET) is less than 50 percent of VSUP.

POWER GROUND (PGND)

This pin is power ground for the charge pump. It should be connected to VSS, however routing to a single point ground on the PCB may help to isolate charge pump noise.

ENABLE 1 AND ENABLE 2 (EN1, EN2)

Both of these logic signal inputs must be high to enable any gate drive output. When either or both are low, the internal logic (SPI port, etc.) still functions normally, but all gate drives are forced off (external power FET gates pulled low). The signal is asynchronous.

When EN1 and EN2 return high to enable the outputs, each LS driver must be pulsed on before the corresponding HS driver can be commanded on. This ensures that the bootstrap capacitors are charged.

RESET ($\overline{\text{RST}}$)

When the reset pin is low the integrated circuit (IC) is in a low power state. In this mode all outputs are disabled, internal bias circuits are turned off, and a small pull-down current is applied to the output gate drives. The internal logic will be reset within 77 ns of RESET going low. When $\overline{\text{RST}}$ is low, the IC will consume minimal current.

CHARGE PUMP OUT (PUMP)

This pin is the switching node of the charge pump circuit. The output of the internal charge pump support circuit. When the charge pump is used, it is connected to the external pumping capacitor. This pin may be left floating if the charge pump is not required.

CHARGE PUMP INPUT (VPUMP)

This pin is the input supply for the charge pump circuit. When the charge pump is required, this pin should be connected to a polarity protected supply. This input should never be connected to a supply greater than 40 V.

If the charge pump is not required this pin may be left floating.

VSUP INPUT (VSUP)

The supply voltage pin should be connected to the common connection of the High Side FETs. It is the reference bias for the Phase Comparators and Desaturation Comparator. It is also used to provide power to the internal steady state trickle charge pump and to energize the hold off circuit.

PHASE B (PHASEB)

This pin is the totem pole output of the Phase B comparator. This output is low when the voltage on Phase B High Side source (source of the High Side load FET) is less than 50 percent of V_{SUP}.

PHASE C (PHASEC)

This pin is the totem pole output of the Phase C comparator. This output is low when the voltage on Phase C High Side source (source of the High Side load FET) is less than 50 percent of V_{SUP}.

PHASE A HIGH SIDE INPUT ($\overline{\text{PA\_HS}}$)

This input logic signal pin enables the High Side Driver for Phase A. The signal is active low, and is pulled up by an internal current source.

PHASE A LOW SIDE INPUT (PA_LS)

This input logic signal pin enables the Low Side Driver for Phase A. The signal is active high, and is pulled down by an internal current sink.

VDD VOLTAGE REGULATOR (VDD)

VDD is an internally generated 5.0 V supply. The internal regulator provides continuous power to the IC and is a supply reference for the SPI port. A 0.47 µF (min) decoupling capacitor must be connected to this pin.

This regulator is intended for internal IC use and can supply only a small (1.0 mA) external load current.

A power-on-reset (POR) circuit monitors this pin and until the voltage rises above the threshold, the internal logic will be reset; driver outputs will be tri-stated and SPI communication disabled.

The VDD regulator can be disabled by asserting the $\overline{RST}$ signal low. The VDD regulator is powered from the VPWR pin.

PHASE B HIGH SIDE CONTROL INPUT ($\overline{PB\_HS}$)

This pin is the input logic signal, enabling the High Side driver for Phase B. The signal is active low, and is pulled up by an internal current source.

PHASE B LOW SIDE INPUT (PB_LS)

This pin is the input logic signal, enabling the Low Side driver for Phase B. The signal is active high, and is pulled down by an internal current sink.

INTERRUPT (INT)

The Interrupt pin is a totem pole logic output. When a fault is detected, this pin will pull high until it is cleared by executing the Clear Interrupt command via the SPI port. The faults capable of causing an interrupt can be masked via the MASK0 and MASK1 SPI registers to customize the response.

CHIP SELECT ($\overline{CS}$)

Chip select is a logic input that frames the SPI commands and enables the SPI port. This signal is active low, and is pulled up by an internal current source.

SERIAL IN (SI)

The Serial In pin is used to input data to the SPI port. Clocked on the falling edge of SCLK, it is the most significant bit (MSB) first. This pin is pulled down by an internal current sink.

SERIAL CLOCK (SCLK)

This logic input is the clock is used for the SPI port. The SCLK typically runs at 3.0 MHz (up to 5.0 MHz) and is pulled down by an internal current sink.

SERIAL OUT (SO)

Output data for the SPI port streams from this pin. It is tri-stated until $\overline{CS}$ is low. New data appears on rising edges of SCLK in preparation for latching by the falling edge of SCLK on the master.

PHASE C LOW SIDE INPUT (PC_LS)

This input logic pin enables the Low Side Driver for Phase C. This pin is an active high, and is pulled down by an internal current sink.

PHASE C HIGH SIDE INPUT ($\overline{PC\_HS}$)

This input logic pin enables the High Side Driver for Phase C. This signal is active low, and is pulled up by an internal current source.

AMPLIFIER OUTPUT (AMP_OUT)

This pin is the output for the current sensing amplifier. It is also the sense input to the over-current comparator.

AMPLIFIER INVERTING INPUT (AMP_N)

The inverting input to the current sensing amplifier.

AMPLIFIER NON-INVERTING INPUT (AMP_P)

The non-inverting input to the current sensing amplifier.

OVER-CURRENT COMPARATOR OUTPUT (OC_OUT)

The over-current comparator output is a totem pole logic level output. A logic high indicates an over-current condition.

OVER-CURRENT COMPARATOR THRESHOLD (OC_TH)

This input sets the threshold level of the over-current comparator.

VOLTAGE SOURCE SUPPLY (VSS)

VSS is the ground reference for the logic interface and power supplies.

GROUND (GND0,GND1)

These two pins are connected internally to VSS by a 1.0 Ω resistor. They provide device substrate connections and also the primary return path for ESD protection.

VLS REGULATOR CAPACITOR (VLS_CAP)

This connection is for a capacitor which will provide a low-impedance for switching currents on the gate drive. A low ESR decoupling capacitor, capable of sourcing the pulsed drive currents must be connected between this pin and VSS. Use the 33937A to avoid the CAUTION on page 28 for capacitances greater than 3.5 µF.

This is the same DC node as VLS, but it is physically placed on the opposite end of the IC to minimize the source impedance to the gate drive circuits.

PHASE C LOW SIDE SOURCE (PC_LS_S)

The phase C Low Side source is the pin used to return the gate currents from the Low Side FET. Best performance is realized by connecting this node directly to the source of the Low Side FET for phase C.

PHASE C LOW SIDE GATE (PC_LS_G)

This is the gate drive for the phase C Low Side output FET. It provides high current through a low impedance to turn on

and off the Low Side FET.. A low-impedance drive ensures transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FET. This output has also been designed to resist the influence of negative currents.

PHASE C HIGH SIDE SOURCE (PC_HS_S)

The source connection for the phase C High Side output FET is the reference voltage for the gate drive on the High Side FET and also the low voltage end of the bootstrap capacitor.

PHASE C HIGH SIDE GATE (PC_HS_G)

This is the gate drive for the phase C High Side output FET. This pin provides the gate bias to turn the external FET on or off. The gate voltage is limited to about 15 V above the FET source voltage. A low-impedance drive is used, ensuring transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FETs. This output has also been designed to resist the influence of negative currents.

PHASE C BOOTSTRAP (PC_BOOT)

This is the bootstrap capacitor connection for phase C. A capacitor connected between PC_HS_S and this pin provides the gate voltage and current to drive the external FET gate. Typically, the boostrap capacitor selection is 10 to 20 times the gate capacitance. The voltage across this capacitor is limited to about 15 V. Use the 33937A to avoid the CAUTION on page 28 for bootstrap capacitances greater than 100 nF.

PHASE B LOW SIDE SOURCE (PB_LS_S)

The phase B Low Side source is the pin used to return the gate currents from the Low Side FET. Best performance is realized by connecting this node directly to the source of the Low Side FET for phase B.

PHASE B LOW SIDE GATE (PC_LS_G)

This is the gate drive for the phase B Low Side output FET. It provides high current through a low impedance to turn on and off the Low Side FET. A low-impedance drive ensures transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FET. This output has also been designed to resist the influence of negative currents.

PHASE B HIGH SIDE SOURCE (PB_HS_S)

The source connection for the phase B High Side output FET is the reference voltage for the gate drive on the High Side FET and also the low voltage end of the bootstrap capacitor.

PHASE B HIGH SIDE GATE (PB_HS_G)

This is the gate drive for the phase B High Side output FET. This pin provides the gate bias to turn the external FET on or off. The gate voltage is limited to about 15 V above the FET source voltage. A low-impedance drive is used, ensuring transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FETs. This output has also been designed to resist the influence of negative currents.

PHASE B BOOTSTRAP (PB_BOOT)

This is the bootstrap capacitor connection for phase B. A capacitor connected between PC_HS_S and this pin provides the gate voltage and current to drive the external FET gate. Typically, the boostrap capacitor selection is 10 to 20 times the gate capacitance. The voltage across this capacitor is limited to about 15 V. Use the 33937A to avoid the CAUTION on page 28 for bootstrap capacitances greater than 100 nF.

PHASE A LOW SIDE SOURCE (PA_LS_S)

The phase A Low Side source is the pin used to return the gate currents from the Low Side FET. Best performance is realized by connecting this node directly to the source of the Low Side FET for phase A.

PHASE A LOW SIDE GATE (PA_LS_G)

This is the gate drive for the phase A Low Side output FET. It provides high current through a low impedance to turn on and off the Low Side FET. A low-impedance drive ensures transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FET. This output has also been designed to resist the influence of negative currents.

PHASE A HIGH SIDE SOURCE (PA_HS_S)

The source connection for the phase A High Side output FET is the reference voltage for the gate drive on the High Side FET and also the low voltage end of the bootstrap capacitor.

PHASE A HIGH SIDE GATE (PA_HS_G)

This is the gate drive for the phase A High Side output FET. This pin provides the gate bias to turn the external FET on or off. The gate voltage is limited to about 15 V above the FET source voltage. A low-impedance drive is used, ensuring transient currents do not overcome an off-state driver and allow pulses of current to flow in the external FETs. This output has also been designed to resist the influence of negative currents.

PHASE A BOOTSTRAP (PA_BOOT)

This is the bootstrap capacitor connection for phase A. A capacitor connected between PC_HS_S and this pin provides the gate voltage and current to drive the external FET gate. Typically, the boostrap capacitor selection is 10 to 20 times the gate capacitance. The voltage across this capacitor is limited to about 15 V. Use the 33937A to avoid

the CAUTION on page 28 for bootstrap capacitances greater than 100 nF.

VLS REGULATOR (VLS)

VLS is the gate drive power supply regulated at approximately 15 V. This is an internally generated supply from VPWR. It is the source for the Low Side gate drive voltage, and also the High Side bootstrap source. A low ESR decoupling capacitor, capable of sourcing the pulsed drive currents, must be connected between this pin and VSS. Use the 33937A to avoid the CAUTION on page 28 for capacitances greater than 3.5 µF.

VPWR INPUT (VPWR)

VPWR is the power supply input for VLS and VDD. Current flowing into this input recharges the bootstrap capacitors as well as supplying power to the Low Side gate drivers and the VDD regulator. An internal regulator regulates the actual gate voltages. This pin can be connected to system battery voltage if power dissipation is not a concern.

EXPOSED PAD (EP)

The primary function of the Exposed Pad is to conduct heat out of the device. This pad may be connected electrically to the substrate of the device.The device will perform as specified with the Exposed Pad un-terminated (floating). However, it is recommended that the Exposed Pad be terminated to pin 29 (VSS) and the system ground.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

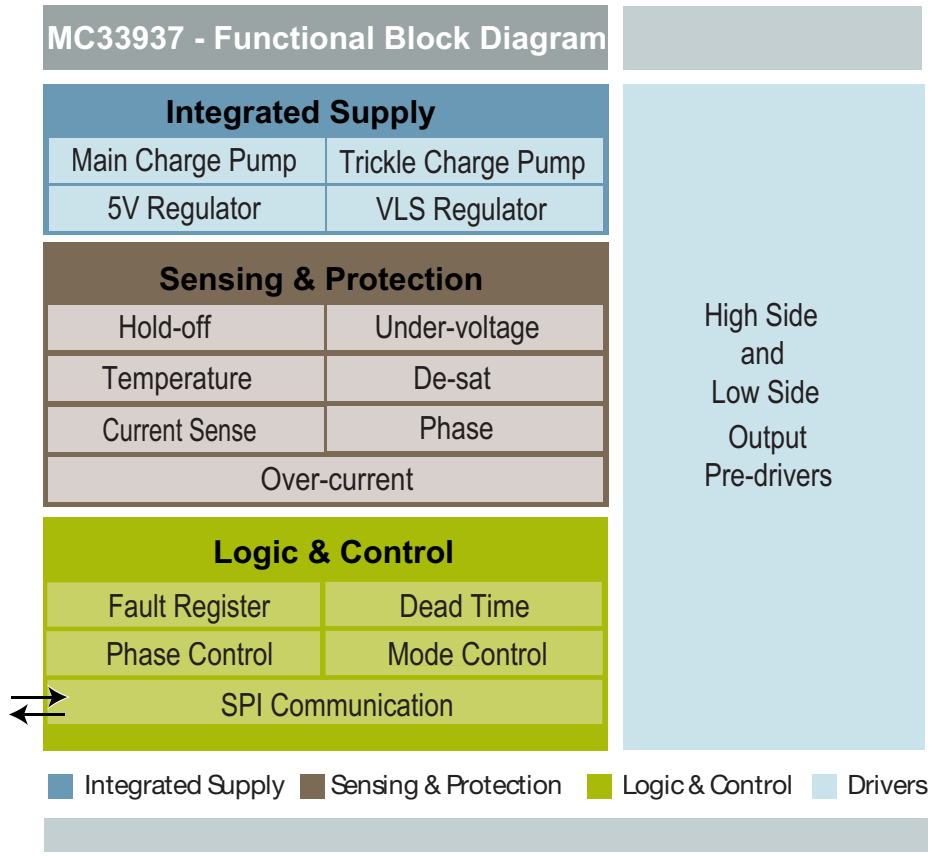


Figure 15. Functional Internal Block Description

All functions of the IC can be described as the following five major functional blocks:

- Logic Inputs and Interface
- Bootstrap Supply
- Low Side Drivers
- High Side Drivers
- Charge Pump

LOGIC INPUTS AND INTERFACE

This section contains the SPI port, control logic, and shoot-through timers.

The IC logic inputs have Schmitt trigger inputs with hysteresis. Logic inputs are 3.0 V compatible. The logic outputs are driven from the internal supply of approximately 5.0 V.

The SPI registers and functionality is described completely in the LOGIC COMMANDS AND REGISTERS section of this document. SPI functionality includes the following:

- **Programming of deadtime delay**—This delay is adjustable in approximately 50 ns steps from 0 ns to 12 µs. Calibration of the delay, because of internal IC variations, is performed via the SPI.
- **Enabling of simultaneous operation of High Side and Low Side FETs**—Normally, both FETs would not be enabled simultaneously. However, for certain applications where the load is connected between the High Side and Low Side FETs, this could be advantageous. If this mode is enabled, the blanking time delay will be disabled. A sequence of commands may be required to enable this function to prevent inadvertent enabling. In addition, this command can only be executed once after reset to enable or disable simultaneous turn-on.
- **Setting of various operating modes** of the IC and enabling of interrupt sources.
  The 33937 allows different operating modes to be set and locked by an SPI command (FULLON, Desaturation Fault, Zero Deadtime). SPI commands can also determine how the various faults are (or are not) reported.
- **Read back of internal registers**.
  The status of the 33937 Status Registers can be read back by the Master (DSP or MCU).

The $\overline{\text{Px\_HS}}$ and Px_LS logic inputs are edge sensitive. This means the leading edge on an input will cause the

complementary output to immediately turn off and the selected one to turn on after the deadtime delay as illustrated in Figure 16. The deadtime delay timer starts when the corresponding FET was commanded off (see Figure 6 and Figure 16).

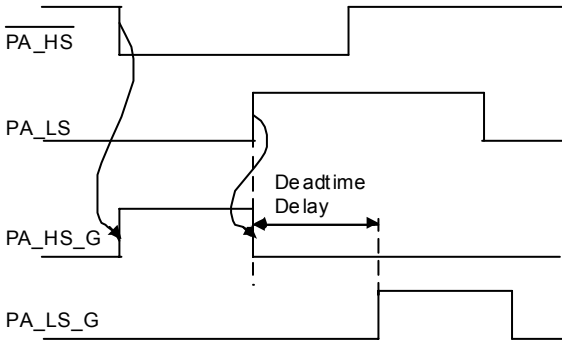


Figure 16. Edge Sensitive Logic Inputs (Phase A)

BOOTSTRAP SUPPLY (VLS)

This is the portion of the IC providing current to recharge the bootstrap capacitors. It also supplies the peak currents required for the Low Side gate drivers.

The power for the gate drive circuits is provided by VLS which is supplied from the VPWR pin. This pin can be connected to system battery voltage and is capable of withstanding up to the full load dump voltage of the system. However, the IC only requires a low-voltage supply on this pin, typically 13 to 16 V. Higher voltages on this pin will increase the IC power dissipation.

In 12 V systems the supply voltage can fall as low as 6.0 V. This limits the gate voltage capable of being applied to the FETs and reduces system performance due to the higher FET on-resistance. To allow a higher gate voltage to be supplied, the IC also incorporates a charge pump. The switches and control circuitry are internal; the capacitors and diodes are external (see Figure 22).

LOW SIDE DRIVERS

These three drivers turn on and off the external Low Side FETs. The circuits provide a low-impedance drive to the gate, ensuring the FETs remain off in the presence of high dV/dt transients on their drains. Additionally, these output drivers isolate the other portions of the IC from currents capable of being injected into the substrate due to rapid dV/dt transients on the FET drains.

Low Side drivers switch power from VLS to the gates of the Low Side FETs. The Low Side drivers are capable of providing a typical peak current of 2.0 A. This gate drive current may be limited by external resistors in order to achieve a good trade-off between the efficiency and EMC (Electro-Magnetic Compatibility) compliance of the application. the Low Side driver uses High Side PMOS for turn on and Low Side isolated LDMOS for turn off. The circuit ensures the impedance of the driver remains low, even during periods of reduced current. Current limit is blanked immediately after subsequent input state change in order to ensure device stays off during dV/dt transients.

HIGH SIDE DRIVERS

These three drivers switch the voltage across the bootstrap capacitor to the external High Side FETs. The circuits provide a low-impedance drive to the gate, ensuring the FETs remain off in the presence of high dV/dt transients on their sources. Further, these output drivers isolate the other portions of the IC from currents capable of being injected into the substrate due to rapid dV/dt transients on the FETs.

The High Side drivers deliver power from their bootstrap capacitor to the gate of the external High Side FET, thus turning the High Side FET on. The High Side driver uses a level shifter, which allows the gate of the external High Side FET to be turned off by switching to the High Side FET source.

The gate supply voltage for the High Side drivers is obtained from the bootstrap supply, so, a short time is required after the application of power to the IC to charge the bootstrap capacitors. To ensure this occurrence, the internal control logic will not allow a High Side switch to be turned on after entering the ENABLE state until the corresponding Low Side switch is enabled at least once. Caution must be exercised after a long period of inactivity of the Low Side switches to verify the bootstrap capacitor is not discharged. It will be charged by activating the Low Side switches for a brief period, or by attaching external bleed resistors from the HS_S pins to GND.

CAUTION for 33937 only (Use the 33937A to avoid this CAUTION)

Using the 33937 in applications which use large value bootstrap capacitors requires extra care to insure the transient induced when charging fully depleted capacitors does not cause an unintended power on reset. The 33937A has been modified to eliminate the need for these special considerations. Factors which affect the sensitivity to this effect are, bootstrap capacitor size, VLS filter capacitor size, VLS voltage and the junction temperature. The effect is more pronounced for greater values of these parameters. It is also more pronounced if all phases charge depleted capacitors simultaneously. For balanced capacitance on VLS and VLS_CAP of greater than 3.5 µF (total of 7.0 µF VLS filtering), 1.2 µF bootstrap capacitance on each phase could cause a POR at room temperature with VLS at 13 V. At the worst case conditions of 15.4 V VLS voltage and 150°C junction temperature, with the same total VLS capacitance of 7.0 µF, approximately 0.3 µF total (0.1µF each) on Px_BOOT could cause the same effect. Since this characteristic is intrinsic to the bootstrap diode integrated on the device, a valid solution to prevent an undesired reset during initialization would be to use external diodes between VLS and the Px_BOOT pin.

In order to achieve a 100% duty cycle operation of the High Side external FETs, a fully integrated trickle charge pump provides the charge necessary to maintain the external FET gates at fully enhanced levels. The trickle charge pump has limited ability to supply external leakage paths while performing it's primary function. The graphs in Figures 11 through 14 beginning on page 21 show the typical margin for supplying external current loads. These limits are based on maintaining the voltage at CBOOT at least 3.0 V greater than the voltage on the HS_S for that phase. If this voltage differential becomes less than 3.0 V, the corresponding high side FET will most likely not remain fully enhanced and the high side driver may malfunction due to insufficient bias voltage between CBOOT and HS_S.

The slew rate of the external output FET is limited by the driver output impedance, overall (external and internal) gate resistance and the load capacitance. To ensure the Low Side FET is not turned on by a large positive dV/dt on the drain of the Low Side FET, the turn-on slew rate of the High Side should be limited. If the slew rate of the High Side is limited by the gate-drain capacitance of the High Side FET, then the displacement current injected into the Low Side gate drive output will be approximately the same value. Therefore, to ensure the Low Side drivers can be held off, the voltage drop across the Low Side gate driver must be lower than the threshold voltage of the Low Side FET (see Figure 17).

Similarly, during large negative dV/dt, the High Side FET will be able to remain off if its gate drive Low Side switch, develops a voltage drop less than the threshold voltage of the High Side FET. The gate drive Low Side switch discharges the gate to the source.

Additionally, during negative dV/dt the Low Side gate drive could be forced below ground. The Low Side FETs must not inject detrimental substrate currents in this condition.

The occurrence of these cases depends on the polarity of the load current during switching.

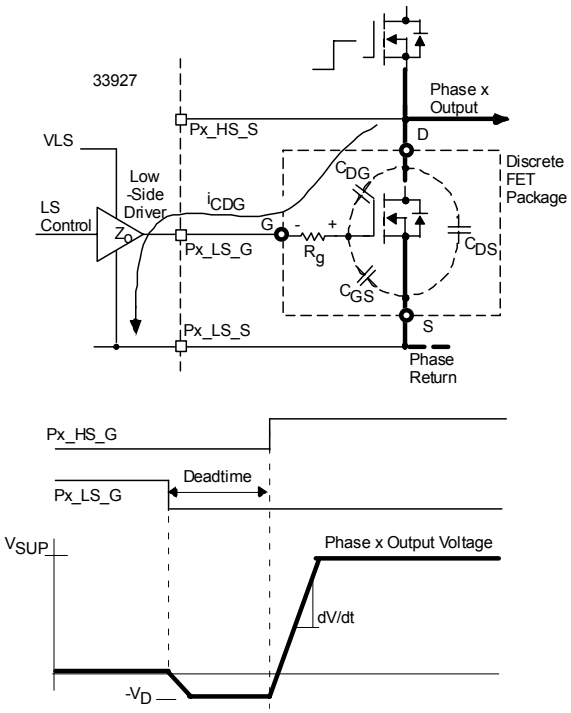


Figure 17. Positive DV/dt Transient

DRIVER FAULT PROTECTION

The 33937 IC integrates several protection mechanisms against various faults. The first of them is the Current Sense Amplifier with the Over-current Comparator. These two blocks are common for all three driver phases.

Current Sense Amplifier

This amplifier is usually connected as a differential amplifier (see Figure 9). It senses a current flowing through the external FETs as a voltage across the current sense resistor R_{SENSE}. Since the amplifier common mode range does not extend below ground, it is necessary to use an external reference to permit measuring both positive and negative currents.

The amplifier output can be monitored directly (e.g. by the microcontroller's ADC) at the AMP_OUT pin, providing the means for closed loop control with the 33937.

The output voltage is internally compared with the Over-current Comparator threshold voltage (see Figure 22).

Over-current Comparator

The amplified voltage across R_{SENSE} is compared with the pre-set threshold value by the over-current comparator input. If the Current Sense Amplifier output voltage exceeds the threshold of the Over-current Comparator it would change the status of its output (OC_OUT pin) and the fault condition would be latched (see Figure 20).

The occurrence of this fault would be signalled by the return value of the Status Register 0. If the proper Interrupt Mask has been set, this fault condition will generate an

interrupt - the INT pin will be asserted High. The INT will be held in the High state until the fault is removed, and the appropriate bit in the Status Register 0 is cleared by the CLINT0 command. This fault reporting technique is described in detail in the Logic Commands and Registers section.

Desaturation Detector

The Desaturation Detector is a comparator integrated into the output driver of each phase channel. It provides an additional means to protect against “Short-to-Ground” fault condition when the output node gets shorted to the supply voltage (short across the High Side FET).

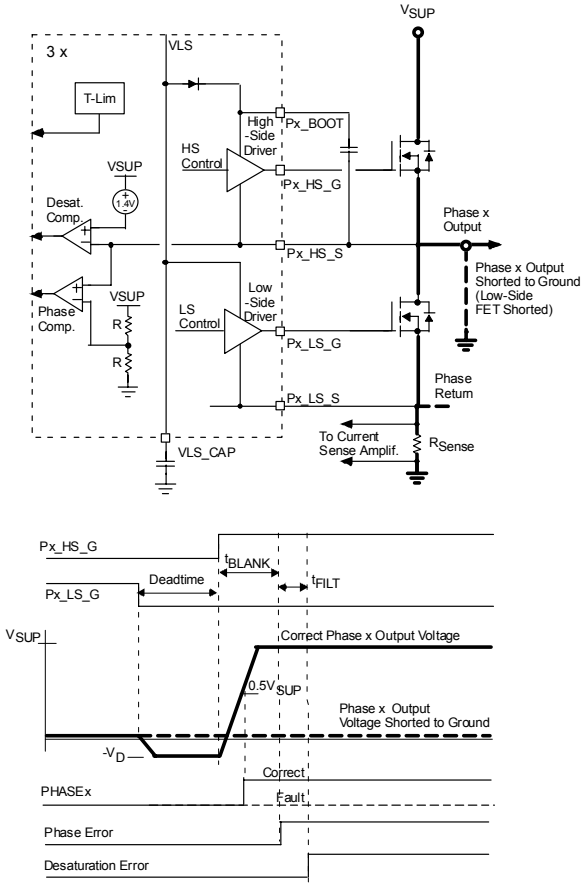


Figure 18. Short to Ground Detection

When switching from Low Side to High Side, the High Side will be commanded ON after the end of the deadtime. The deadtime period starts when the Low Side is commanded OFF. If the voltage at Px_HS_S is less than 1.4V below V_{SUP} after the blanking time (t_{BLANK}) a desaturation fault is initiated. An additional 1.0 µs digital filter is applied from the initiation of the desaturation fault before it is registered, and all phase drivers are turned OFF (Px_HS_G clamped to Px_HS_S and Px_LS_G clamped to Px_LS_S). If the desaturation fault condition clears before the filter time expires, the fault is ignored and the filter timer resets.

Valid faults are registered in the fault status register, which can be retrieved by way of the SPI. Additional SPI commands will mask the INT flag and disable output stage shutdown, due to desaturation and phase errors. See the Logic Commands and Registers section for details on masking INT behavior and disabling the protective function.

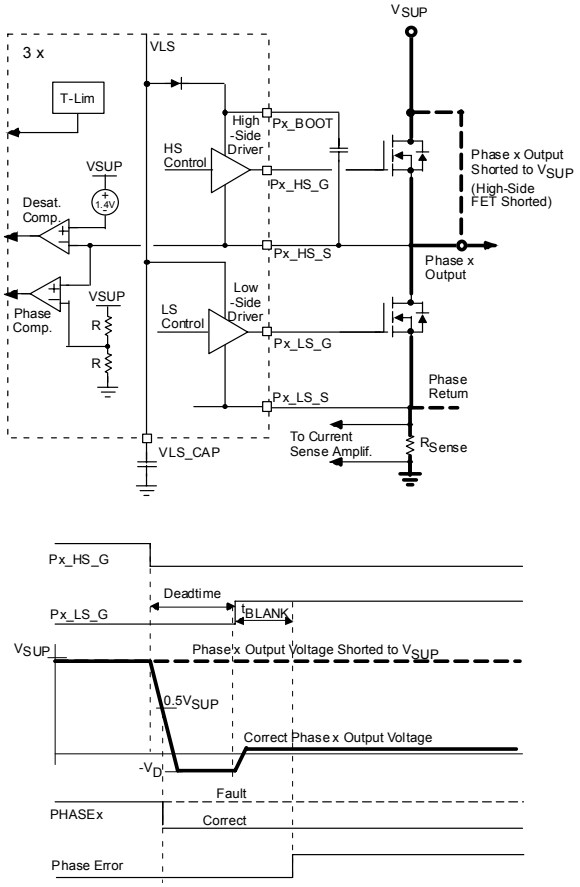


Figure 19. Short to Supply Detection

Phase Comparator

Faults could also be detected as Phase Errors. A phase error is generated if the output signal (at Px_HS_S) does not properly reflect the drive conditions.

A phase error is detected by a Phase Comparator. The Phase Comparator compares the voltage at the Px_HS_S node with a reference of one half the voltage at the VSUP pin. A High Side phase error (which will also trigger the Desaturation Detector) occurs when the High Side FET is commanded on, and Px_HS_S is still *low* at the end of the deadtime and blanking time duration. Similarly, a LS phase error occurs when the Low Side FET is commanded on, and the Px_HS_S is still *high* at the end of the deadtime and blanking time duration.

The Phase Error Flag is the triple OR of phase errors from each phase. Each phase error is the OR of the High Side and Low Side phase errors. This flag can generate an interrupt if

the appropriate mask bit is set. The INT will be held in the High state until the fault is removed, and the appropriate bit in the Status Register 0 is cleared by the CLINT1 command. This fault reporting mechanism is described in detail in the Logic Commands and Registers section.

HOLD OFF CIRCUIT

The IC guarantees the output FETs are turned off in the absence of V_{DD} or V_{PWR} by means of the Hold off circuit. A small current source, generated from VSUP, typically 100 µA, is mirrored and pulls all the output gate drive pins low when V_{DD} is less than about 3.0 V, $\overline{RST}$ is active (low), or when VLS is lower than the VLS_Disable threshold. A minimum of approximately 3.0 V is required on VSUP to energize the Hold off circuit.

CHARGE PUMP

The Charge Pump circuit provides the basic switching elements required to implement a charge pump, when combined with external capacitors and diodes for enhanced low voltage operation.

When the 33937 is connected per the typical application using the charge pump (see Figure 22), the regulation path for VLS includes the charge pump and a linear regulator. The regulation set point for the linear regulator is nominally at 15.34 V. As long as VLS output voltage (VLS_{OUT}) is greater than the VLS analog regulator threshold (VLS_{ATH}) minus V_{THREG}, the charge pump is not active.

If $VLS_{OUT} < VLS_{ATH} – V_{THREG}$ the charge pump turns ON until $VLS_{OUT} > VLS_{ATH} – V_{THREG} + V_{HYST}$

V_{HYST} is approximately 200 mV. VLS_{ATH} will not interfere with this cycle even when there is overlap in the thresholds, due to the design of the regulator system.

The maximum current the charge pump can supply is dependent on the pump capacitor value and quality, the pump frequency (nominally 130 kHz), and the Rdson of the pump FETs. The effective charge voltage for the pump capacitor would be $V_{SYS} – 2 * V_{DIODE}$. The total charge transfer would then be $C_{PUMP} * (V_{SYS} – 2*V_{DIODE})$. Multiplying by the switch frequency gives the theoretical current the pump can transfer: $F_{PUMP} * C_{PUMP} * (V_{SYS} – 2*V_{DIODE})$.

NOTE: There is also another smaller, fully integrated charge pump (Trickle Charge Pump - see Figure 2), which is used to maintain the High Side drivers' gate V_{GS} in 100 percent duty cycle modes.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

RESET AND ENABLE

The 33937 has three power modes of operation described in Table 6. There are three global control inputs ($\overline{RST}$, EN1, EN2), which together with the status of the VDD and VLS, control the behavior of the IC.

The operating status of the IC can be described by the following three modes:

Sleep Mode - When $\overline{RST}$ is low, the IC is in Sleep mode. The current consumption of the IC is at minimum.

- **Standby Mode** - The $\overline{RST}$ input is high while one of the Enable inputs is low. The IC is fully biased up and operating, all the external FETs are actively turned off by both High Side and Low Side gate drives. The IC is ready to enter the Enable mode.
- **Enable Mode** - In order to enter the Enable mode (normal mode of operation), and to operate the outputs, the $\overline{RST}$ input must be high, and both Enable inputs EN1 and EN2 must also be high.

Table 6. Functions of $\overline{RST}$, EN1 and EN2 Pins

RST	EN1, EN2	Mode of Operation (Driver Condition)
0	xx	**Sleep Mode** - in this mode (low quiescent current) the driver output stage is switched-off with a weak pull-down. All error and SPI registers are cleared. The internal 5.0 V regulator is turned off and VDD is pulled low. All logic outputs except SO are clamped to VSS.
1	0x x0	**Standby Mode** - IC fully biased up and all functions are operating, the output drivers actively turn off all of the external FETs (after initialization). The SPI port is functional. Logic level outputs are driven with low impedance. SO is high impedance unless $\overline{CS}$ is low. V_{DD}, Charge Pump and V_{LS} regulators are all operating. The IC is ready to move to Enable Mode.
1	11	**Enable Mode** - (normal operation). Drivers are enabled; output stages follow the input command. After Enable, outputs require a pulse on Px_LS before corresponding HS outputs will turn on in order to charge the bootstrap capacitor. All error pin and register bits are active if detected.

- After entry to Enable Mode, the IC requires a pulse on Px_LS in order to charge the bootstrap capacitor before allowing the $\overline{Px\_HS}$ to turn on. This pulse should be long enough to guarantee the bootstrap capacitor is charged (typically less than 50 µs), but the IC does not enforce this condition. If there is an alternate means of pre-charging the bootstrap capacitor, i.e. an external resistor from Px_HS_S to GND, then a very brief pulse of 100 ns is sufficient to reset the logic.

Table 7. Functional Ratings

(T_J = -40°C to 150°C and supply voltage range V_{SUP} = V_{PWR} = 5.0 to 45 V, C = 0.47 µF)

Characteristic	Value
Default State of input pin Px_LS, EN1, EN2, $\overline{RST}$, SI, SCLK, if left open (55) (Driver output is switched off, high-impedance mode)	Low (<1.0 V)
Default State of input pin $\overline{Px\_HS}$, $\overline{CS}$ if left open (55) (Driver output is switched off, high-impedance mode)	High (>2.0 V)

Notes

55. To assure a defined status for all inputs, these pins are internally biased by pull-up/down current sources.

LOGIC COMMANDS AND REGISTERS

COMMAND DESCRIPTIONS

The IC contains internal registers to control the various operating parameters, modes, and interrupt characteristics. These commands are sent and status is read via 8-bit SPI commands. The IC will use the last eight bits in an SPI transfer, so devices can be daisy-chained. The first three bits in an SPI word can be considered to be the Command with the trailing five bits being the data.

The SPI logic will generate a framing error and ignore the SPI message if the number of received bits is not eight or if it is not a multiple of eight.

After $\overline{RST}$, the first SPI result returned is Status Register 0.

Table 8. Command List

Command	Name	Description
000x xxxx	NULL	These commands are used to read IC status. These commands do not change any internal IC status. Returns Status Register 0-3, depending on sub command.
0010 xxxx	MASK0	Sets a portion of the interrupt mask using lower four bits of command. A “1” bit enables interrupt generation for that flag. INT remains asserted if uncleared faults are still present. Returns Status Register 0.
0011 xxxx	MASK1	Sets a portion of the interrupt mask using lower four bits of command. A “1” bit enables interrupt generation for that flag. INT remains asserted if uncleared faults are still present. Returns Status Register 0.
010x xxxx	MODE	Enables Desat/Phase Error Mode. Enables FULLON Mode. Locks further Mode changes. Returns Status Register 0.
0110 xxxx	CLINT0	Clears a portion of the fault latch corresponding to MASK0 using lower four bits of command. A 1 bit clears the interrupt latch for that flag. INT remains asserted if other unmasked faults are still present. Returns Status Register 0.
0111 xxxx	CLINT1	Clears a portion of the fault latch corresponding to MASK1 using lower four bits of command. A 1 bit clears the interrupt latch for that flag. INT remains asserted if other unmasked faults are still present. Returns Status Register 0.
100x xxxx	DEADTIME	Set deadtime with calibration technique. Returns Status Register 0.

FAULT REPORTING AND INTERRUPT GENERATION

Different fault conditions described in the previous chapters can generate an interrupt - INT pin output signal asserted high. When an interrupt occurs, the source can be read from Status Register 0, which is also the return word of most SPI messages.

Faults are latched on occurrence, and the interrupt and faults are only cleared by sending the corresponding CLINTx command. A fault that still exists will continue to assert an interrupt.

Note: If there are multiple pending interrupts, the INT line will not toggle when one of the faults is cleared. Interrupt processing circuitry on the host must be level sensitive to correctly detect multiple simultaneous interrupt.

Thus, when an interrupt occurs, the host can query the IC by sending a NULL command; the return word contains flags indicating any faults not cleared since the CLINTx command was last written (rising edge of $\overline{CS}$) and the beginning of the current SPI command (falling edge of $\overline{CS}$). The NULL command causes no changes to the state of any of the fault or mask bits.

The logic clearing the fault latches occurs only when:

1. A valid command had been received(i.e. no framing error);
2. A state change did not occur during the SPI message (if the bit is being returned as a 0 and a fault change occurs during the middle of the SPI message, the latch will remain set). The latch is cleared on the trailing (rising) edge of the $\overline{CS}$ pulse. Note, to prevent missing any faults the CLINTx command should not generally clear any faults without being observed; i.e. it should only clear faults returned in the prior NULL response.

NULL COMMANDS

This command is sent by sending binary 000x xxxx data. This can be used to read IC status in the SPI return word. Message 000x xx00 reads Status Register 0. Message 000x xx01 through 000x xx11 read additional internal registers.

Table 9. NULL Commands

SPI Data Bits	7	6	5	4	3	2	1	0
Write	0	0	0	x	x	x	0	0
Reset								

NULL Commands are described in detail in the STATUS REGISTERS section of this document.

MASK Command

This is the mask for interrupts. A bit set to “1” enables the corresponding interrupt. Because of the number of MASK bits, this register is in two portions:

1. MASK0
2. MASK1

Both are accessed with 0010 xxxx and 0011 xxxx patterns respectively. Figure 20 illustrates how interrupts are enabled and faults cleared.

CLINT0 and CLINT1 have the same format as MASK0 and MASK1 respectively, but the action is to clear the interrupt latch and status register 0 bit corresponding to the lower nibble of the command.

Table 10. MASK0 Register

SPI Data Bits	7	6	5	4	3	2	1	0
Write	0	0	1	0	x	x	x	x
Reset					1	1	1	1

INTERRUPT HANDLING

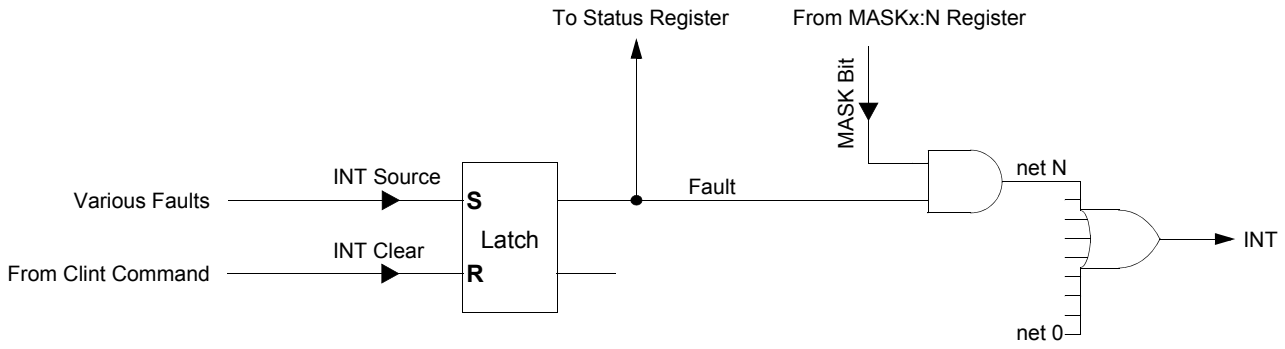


Figure 20. Interrupt Handling

Table 11. MASK1 Register

SPI Data Bits	7	6	5	4	3	2	1	0
Write	0	0	1	1	x	x	x	x
Reset					1	1	1	1

Table 12. Setting Interrupt Masks

Mask:bit	Description
MASK0:0	**Over-temperature** on any gate drive output generates an interrupt if this bit is set.
MASK0:1	**Desaturation** event on any output generates an interrupt if this bit is set.
MASK0:2	**VLS under-voltage** generates an interrupt if this bit is set.
MASK0:3	**Over-current Error**–if the over-current comparator threshold is exceeded, an interrupt is generated.
MASK1:0	**Phase Error**–if any Phase comparator output is not at the expected value when an output is command on, an interrupt is generated. This signal is the XOR of the phase comparator output with the output drive state, and blacked for the duration of the desaturation blanking interval. In FULLON mode, this signal is blanked and cannot generate an error.
MASK1:1	**Framing Error**–if a framing error occurs, an interrupt is generated.
MASK1:2	**Write Error** after locking.
MASK1:3	**Reset Event**–If the IC is reset or disabled, an interrupt occurs. Since the IC will always start from a reset condition, this can be used to test the interrupt mechanism because when the IC comes out of RESET, an interrupt will immediately occur.

MODE COMMAND

This command is sent by sending binary 010x xxxx data.

Table 13. MODE Command

SPI Data Bits	7	6	5	4	3	2	1	0
Write	0	1	0	0	Desaturation Fault Mode	0	FULLON Mode	Mode Lock
Reset					0	0	0	0

- **Bit 0**–**Mode Lock** is used to enable or disable Mode Lock. If Bit 0 is set, changes to the internal registers are disallowed to prevent inadvertent changes. This bit cannot be cleared once set. Since the mode Lock mode can only be set, this bit prevents any subsequent, and likely erroneous, mode, deadtime, or mask register changes from being received. The only way to clear this bit is to RESET the IC. If an attempt is made to write to a register when Mode Lock is enabled, a Write Error fault is generated.
- **Bit 1**–**FULLON Mode.** If this bit is set, programmed deadtime control is disabled, making it is possible to have both high and Low Side drivers in a phase on simultaneously. This could be useful in special applications such as alternator regulators, or switched-reluctance motor drive applications. There is no deadtime control in FULLON mode. Input signals directly control the output stages, synchronized with the internal clock.
  This bit is a “0”, after RESET. Until overwritten, the IC operates normally; deadtime control and logic prevents both outputs from being turned on simultaneously.
- **Bit 3**– **Desaturation Fault Mode** controls what happen when a desaturation event is detected. When set to “0”, any desaturation on any channel causes all six output drivers to shutoff. The drivers can only be re-enabled by executing the CLINT command. When 1, desaturation faults are completely ignored.
  Bit 3 controls behavior if a Desaturation, or Phase Error event is detected. The possibilities are:
  — 0: Default: When a Desaturation, or Phase Error event is detected on *any* channel, *all* channels turn off and generates an Interrupt, if interrupts are enabled.
  — 1: Disable: Desaturation /Phase Error channel shutdown is disabled, but interrupts are still possible if unmasked.

Sending a MODE command and setting the Mode Lock simultaneously are allowed. This sets the requested mode and locks out any further changes.

DEADTIME COMMAND

Deadtime prevents the turn-on of both transistors in the same phase until the deadtime has expired. The deadtime timer starts when a FET is commanded off (see Figure 6 and Figure 16). The deadtime control is disabled by enabling the FULLON mode.

The deadtime is set by sending the DEADTIME command (100x xxx1), and then sending a calibration pulse of $\overline{CS}$. This pulse must be 16 times longer than the required deadtime (see Figure 21). Deadtime is measured in cycle times of the internal time base, f_{TB}. This measurement is divided by 16 and stored in an internal register to provide the reference for timing the deadtime between high and low gate transactions in the same phase.

For example: the internal time base is running at 20 MHz and a 1.5 µs deadtime is required. First a DEADTIME command is sent (using the SPI), then a $\overline{CS}$ is sent. The $\overline{CS}$ pulse is 16*1.5 = 24 µs wide. The IC measures this pulse as 24000 ns/50 ns = 480 clock cycles and stores 480/16 = 30 in the deadtime register. Until the next deadtime calibration is performed, 30 clock cycles will separate the turn off and turn on gate signals in the same phase. The worst case error immediately after calibration will be +0/-1 time base cycle, for this example +0 ns/-50 ns. Note that if the internal time base drifts, the effect on dead time will scale directly.

Sending a ZERO DEADTIME command (100x xxx0) sets the deadtime timer to 0. However, simultaneous turn-on of High Side and Low Side FETs in the same phase is still prevented unless the FULLON command has been transmitted. There is no calibration pulse expected after receiving the ZERO DEADTIME command.

After RESET, deadtime is set to the maximum value of 255 time base cycles (typically 15 µs).

The IC ignores any SPI data that is sent during the calibration pulse. If there are any transitions on SI or SCLK while the Deadtime $\overline{CS}$ pulse is low, a Framing Error will be generated, however, the $\overline{CS}$ pulse will be used to calibrate the deadtime

Table 14. .DEADTIME Command

SPI Data Bits	7	6	5	4	3	2	1	0
Write	1	0	0	x	x	x	x	ZERO/ CALIBRATE
Reset					x	x	x	x

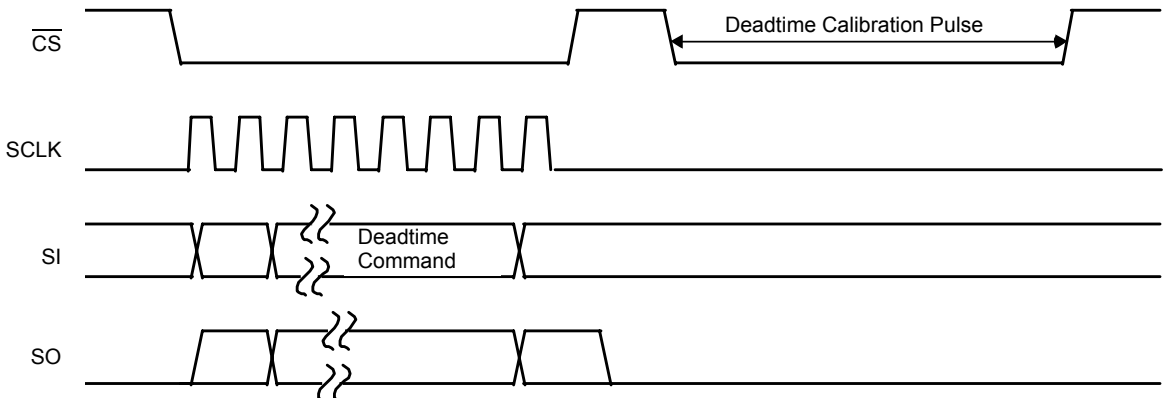


Figure 21. Deadtime Calibration

STATUS REGISTERS

After any SPI command, the status of the IC is reported in the return value from the SPI port. There are four variants of the NULL command used to read various status in the IC.

Other commands return a general status word in the Status Register 0.

There are four Status Registers in the IC. Status Register 0 is most commonly used for general status. Registers one through three are used to read or confirm internal IC settings.

Status Register 0 (Status Latch Bits)

This register is read by sending the NULL0 command (000x xx00). It is also returned after any other command. This command returns the following data:

Table 15. Status Register 0

SPI Data Bits	7	6	5	4	3	2	1	0
Results Register 0 Read	RESET Event	Write Error	Framing Error	Phase Error	Over-current	Low VLS	DESAT Detected on any Channel	TLIM Detected on any Channel
Reset	1	0	0	0	0	0	0	0

All status bits are latched. The latches are cleared only by sending a CLINT0 or CLINT1 command with the appropriate bits set. If the status is still present, that bit will not clear. CLINT0 and CLINT1 have the same format as MASK0 and MASK1 respectively.

- **Bit 0**–is a flag for **Over-temperature** on any channel. This bit is the OR of the latched three internal TLIM detectors.This flag can generate an interrupt if the appropriate mask bit is set.
- **Bit 1**–is a flag for **Desaturation Detection** on any channel. This bit is the OR of the latched three internal High Side desaturation detectors and phase error logic. Faults are also detected on the Low Side as *phase errors.* A phase error is generated if the output signal (at Px_HS_S) does not properly reflect the drive conditions. The phase error is the triple OR of phase errors from each phase. Each phase error is the OR of the HS and LS phase errors. An HS phase error (which will also trigger the desaturation detector) occurs when the HS FET is commanded on, and the Px_HS_S is still *low* in the deadtime duration after it is driven ON. Similarly, a LS phase error occurs when the LS FET is commanded on, and the Px_HS_S is still *high* in the deadtime duration after the FET is driven ON. This flag can generate an interrupt if the appropriate mask bit is set.
- **Bit 2**– is a flag for **Low Supply Voltage**. This bit is latched, thus a prior low voltage event is returned once before being cleared on read. This flag can generate an interrupt if the appropriate mask bit is set.
- **Bit 3**–is a flag for the output of the **Over-current Comparator**. This flag can generate an interrupt if the appropriate mask bit is set.
- **Bit 4**–is a flag for a **Phase Error**. If any Phase comparator output is not at the expected value when just one of the individual high or Low Side outputs is enabled, the fault flag is set. This signal is the XOR of the phase comparator output with the output driver state, and blanked for the duration of the desaturation blanking interval. This flag can generate an interrupt if the appropriate mask bit is set.
- **Bit 5**–is a flag for a **Framing Error**. A framing error is an SPI message not containing a multiple of eight bits (a 0-length message is also a framing error on 33937A). SCLK toggling while measuring the Deadtime calibration pulse is also a framing error. This would typically be a transient or permanent hardware error, perhaps due to noise on the SPI lines. This flag can generate an interrupt if the appropriate mask bit is set.
- **Bit 6**–indicates a **Write Error After the Lock** bit is set. A write error is any attempted write to the MASKn, Mode, or a Deadtime command after the Mode Lock bit is set. A write error is any attempt to write any other command than the one defined in the Table 8. This would typically be a software error. This flag can generate an interrupt if the appropriate mask bit is set.
- **Bit 7**–is set upon **exiting $\overline{\text{RST}}$**. It can be used to test the interrupt mechanism or to flag for a condition where the IC gets reset without the host being otherwise aware. This flag can generate an interrupt if the appropriate mask bit is set.

Status Register 1 (MODE Bits)

This register is read by sending the NULL1 command (000x xx01). This is guaranteed to not affect IC operation and returns the following data:

Table 16. Status Register 1

SPI Data Bits	7	6	5	4	3	2	1	0
Results Register 1 Read	0	Desaturation Mode	Zero Deadtime Set	Calibration Overflow	Deadtime Calibration	0	FULLON Mode	Lock Bit
Reset	0	0	0	0	0	0	0	0

- **Bit 0**–**Lock Bit** indicates the IC registers (Deadtime, MASKn, CLINTn, and Mode) are locked. Any subsequent write to these registers is ignored and will set the Write Error flag.
- **Bit 1**– is the present status of **FULLON Mode**. If this bit is set to “0”, the FULLON mode is not allowed. A “1” indicates the IC can operate in FULLON Mode (both High Side and Low Side FETs of one phase can be simultaneously turned on).
- **Bit 3**–indicates **Deadtime Calibration** occurred. It will be “0” until a successful Deadtime command is executed. This includes the Zero Deadtime setting, as well as a Calibration Overflow.
- **Bit 4**–is a flag for a Deadtime **Calibration Overflow**.
- **Bit 5**–is set if **Zero Deadtime** is commanded.
- **Bit 6**–reflects the current state of the **Desaturation/Phase Error turn-off** mode.

Status Register 2 (MASK bits)

This register is read by sending the NULL2 command (000x xx10). This is guaranteed to not affect IC operation and returns the following data:

Table 17. Status Register 2

SPI Data Bits	7	6	5	4	3	2	1	0
Results Register 2 Read	Mask1:3	Mask1:2	Mask1:1	Mask1:0	Mask0:3	Mask0:2	Mask0:1	Mask0:0
Reset	1	1	1	1	1	1	1	1

Status Register 3 (Deadtime)

This register is read by sending the NULL3 command (000x xx11). This is guaranteed to not affect IC operation and returns the following data:

Table 18. Status Register 3

SPI Data Bits	7	6	5	4	3	2	1	0
Results Register 3 Read	Dead7	Dead6	Dead5	Dead4	Dead3	Dead2	Dead1	Dead0
Reset	0	0	0	0	0	0	0	0

These bits represent the calibration applied to the internal oscillator to generate the requested deadtime. If calibration is not yet performed, all these bits return 0 even though the actual dead time is the maximum.

IC Initialization

Here is a possible flow to initialize the IC and its software environment.

1. Apply power (V_{SYS}) to module
   1.1. With $\overline{RST}$ still low, V_{SUP} and V_{SYS} current will be low because it will only be leakage and the small hold off bias current.
2. Remove $\overline{RST}$ (EN1 and EN2 are still low)
   2.1. When $\overline{RST}$ rises above the threshold, the IC will power-up. The charge pump (if configured) will start, and V_{PWR} and V_{LS} will stabilize.
   2.2. V_{DD} will rise as the internal regulator charges the external reservoir capacitor and the IC will come out of reset.
   2.3. Initialize interrupt handler for MCU
   2.4. Interrupt will occur because of the RESET (Interrupt processing will occur here)
3. Initialize registers
   3.1. Initialize MASK register by sending 0010 xxxx or 0011 xxxx to mask out unwanted interrupts.
   3.2. Set desired dead time either by commanding zero dead time or calibrating the dead time.
   3.3. Send MODE command with desired bits, and also the Lock bit. e.g. 01000001. This prevents further mode changes.
4. Bring EN1 & EN2 high
5. Initialize the outputs
   5.1. Command all Px_LS and $\overline{Px\_HS}$ to logic 1 simultaneously (command ON Low Side, sequentially switching the phases will reduce the transient with very large bootstrap capacitors and may prevent an unintended reset)
   5.2. Command all Px_LS and $\overline{Px\_HS}$ to logic 0 simultaneously (command ON High Side)
   5.3. Command all Px_LS and $\overline{Px\_HS}$ to logic 1 simultaneously (command ON Low Side)
   5.4. The device is now ready for operation.

MAIN LOOP

1. While (forever)
   1.1. Send SPI messages (except NULL1-3), read results
   1.2. If sending NULL1-3 messages, use a semaphore to detect interrupts
      1.2.1. Set Semaphore flag in RAM
      1.2.2. Send NULL1-3
      1.2.3. Send NULL0, read SR1-3
      1.2.4. If Semaphore is still set, then result is good, else go to 1.2.1 (because an interrupt has gotten in the way)
      1.2.5. Clear semaphore
2. END

Interrupt Handler

When an interrupt occurs, the general procedure is to send NULL0 and NULL1 commands to determine what happened, take corrective action (if needed), clear the fault and return.

Because the return value from an SPI command is actually returned in the subsequent message, main-loop software that tries to read SR1, SR2 or SR3, may experience an interrupt between sending the SPI command and the subsequent read. Thus if these registers are to be read, special care must be taken in the software to ensure that the correct results are being interpreted.

1. Interrupt Service Routine:
   1.1. Disable further interrupts from the 33937
   1.2. Clear semaphore set in 1.2.1 of Main loop. This indicates to the main loop that an interrupt occurred and that the return value it gets may not be as expected.
   1.3. Send NULL0 Command. Ignore return value (the previous command is unknown)
   1.4. Send NULL0 Command. The return value will be SR0 from the previous NULL0 command
2. Process Bits in SR0 and correct any faults
3. Send CLINT0 command to clear known (i.e. processed faults from SR0) faults 0:3
4. Send CLINT1 command to clear processed faults 4:7. Note, the return SR0 register from this command is actually read in the main routine.
5. Re-enable interrupts from the 33937

6. Return

PROTECTION AND DIAGNOSIS FEATURES

Table 19. 33937 Fault Protection

No.	Fault	Cause	Detection	33937 Protective Action
1	Phase Output Shorted to VSUP (High Side FET Shorted)	Wire harness shorted to battery Drain-to-Source short on the High Side FET	• Directly sensed by ADC as voltage across R_{SENSE} • Over-current Comparator output OC_OUT monitoring (Over-current Error) • Low Side Phase Error • Direct PHASEx output monitoring	• All external FETs turned off • Fault bit set in Status Register • INT pin set high • OC_OUT pin set high
2	Phase Output Shorted to Ground (R_{SENSE} Bypassed)	Wire harness shorted to battery	• Desaturation Error • High Side Phase Error • Direct PHASEx output monitoring	• All external FETs turned off • Fault bit set in Status Register • INT pin set high
3	Low Side FET Shorted	Drain-to-Source short on the Low Side FET	• Directly sensed by the ADC as voltage across R_{SENSE} • Over-current Comparator output OC_OUT high (Over-current error) • Desaturation Error • High Side Phase Error • Direct PHASEx output monitoring	• All external FETs turned off • Fault bit set in Status Register • INT pin set high • OC_OUT pin set high
4	High Side FET Opened	Module board assembly issue	• Desaturation Error • High Side Phase Error	• All external FETs turned off • Fault bit set in Status Register • INT pin set high
5	Low Side FET Opened	Module board assembly issue	• Directly sensed by ADC as voltage across R_{SENSE} • Low Side Phase Error	• All external FETs turned off • Fault bit set in Status Register • INT pin set high
6	Phase Output Opened (No Load)	Wire harness open	• Directly sensed by ADC as voltage across R_{SENSE}	

NOTE: Other protective actions should be taken at the system level by the controlling microcontroller or DSP. It is possible to disable all automatic shutdowns except for VLS undervoltage. Even when masked, faults will be registered by the status registers.

TYPICAL APPLICATIONS

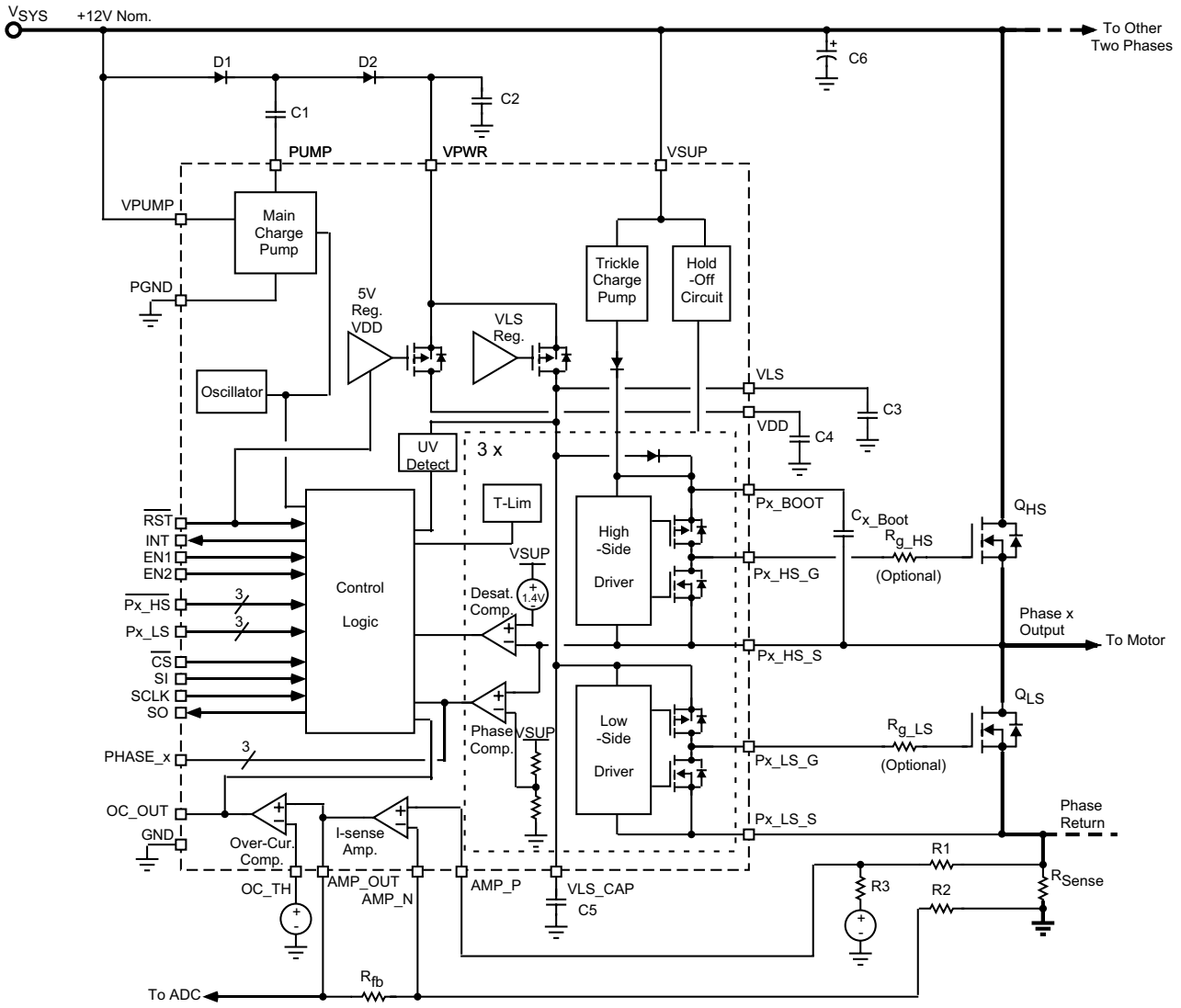


Figure 22. Typical Application Diagram Using Charge Pump (+12 V Battery System)

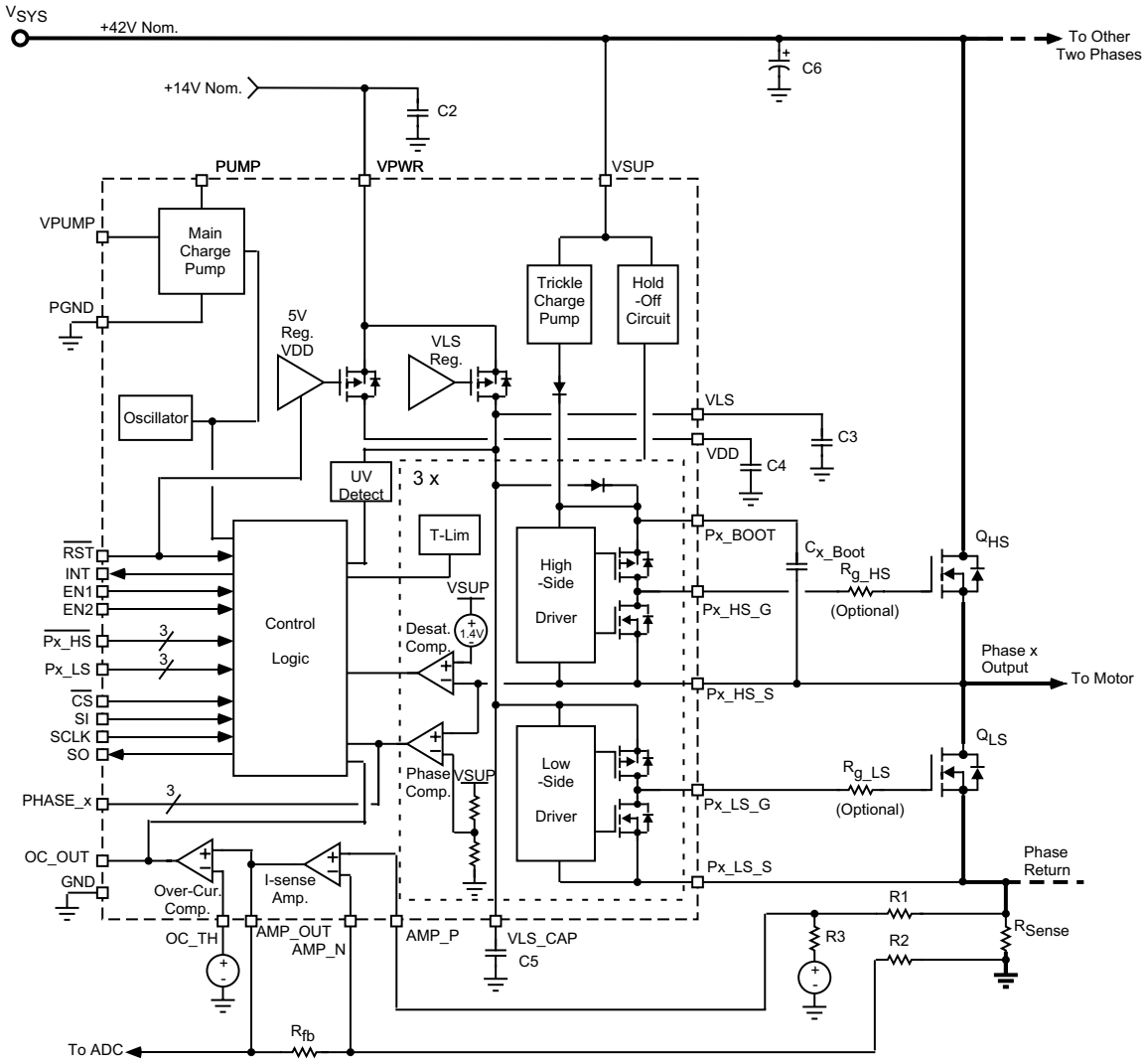


Figure 23. High Voltage Application Diagram (+42 V Battery System)

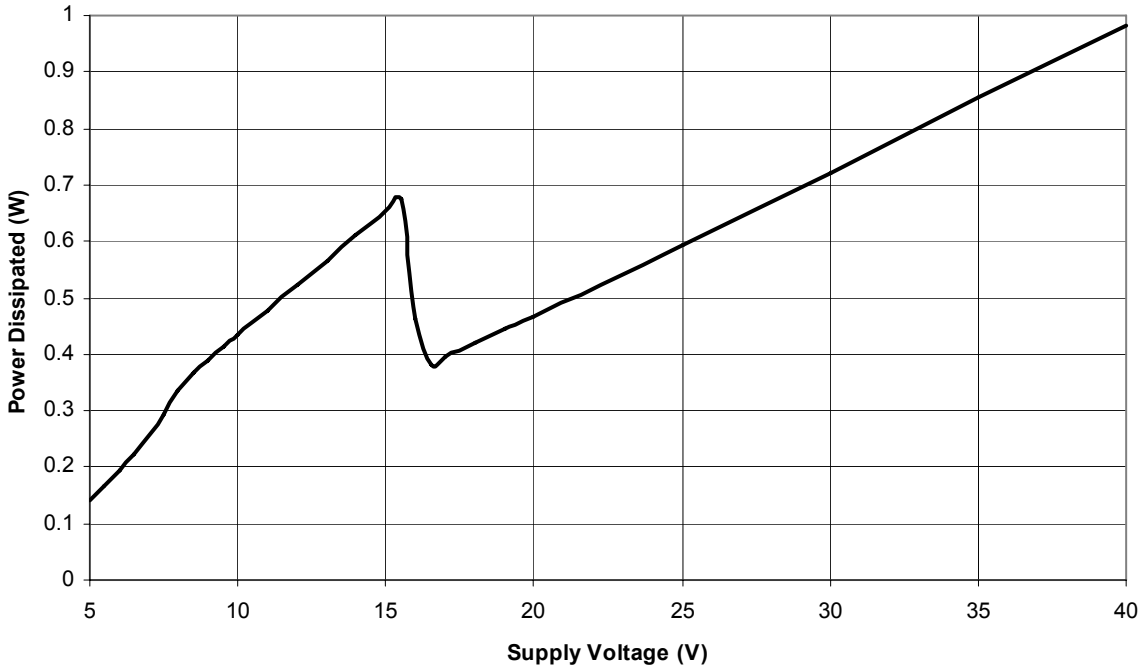


Figure 24. Power Dissipation Profile of Application Using Charge Pump

Reference application with:

- Pump capacitor: 1.0 µF MLC
- Pump filter capacitor: 47 µF low ESR aluminum electrolytic
- Pump diodes: MUR120
- Output FET gate charge: 240 nC @ 10 V
- PWM Frequency: 20 kHz
- Switching Single Phase

Below approximately 17 V the charge pump is actively regulating V_{PWR}. The increased power dissipation is due to the charge pump losses. Above this voltage the charge pump oscillator shuts down and V_{SYS} is passed through the pump diodes directly to V_{PWR}.

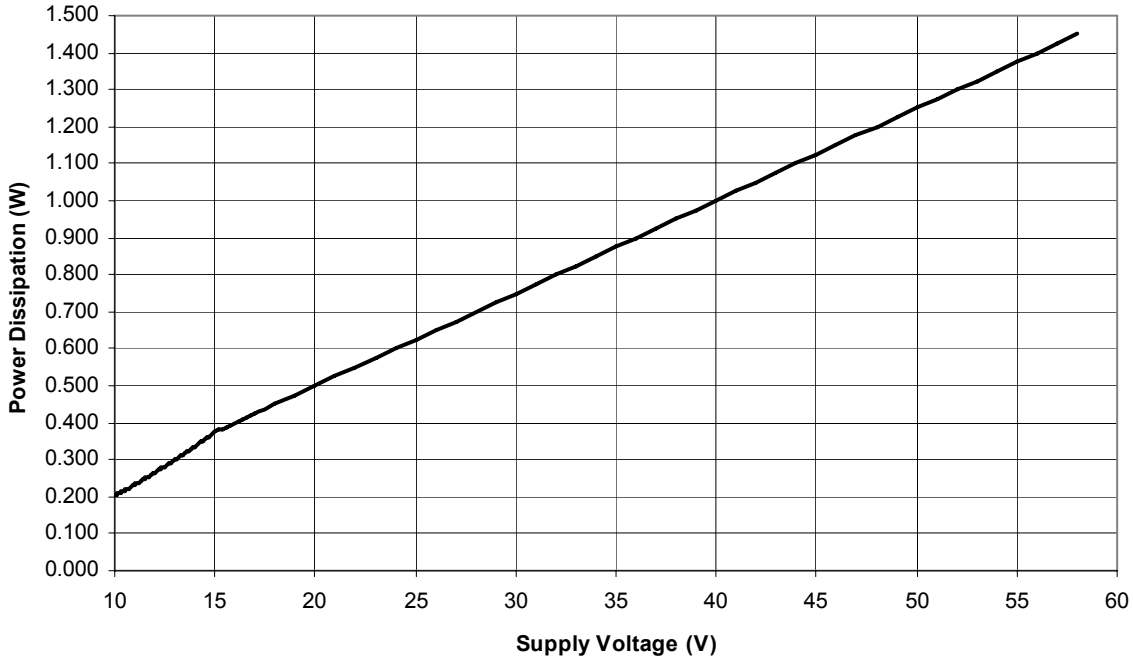


Figure 25. Power Dissipation Profile of Application Not Using Charge Pump

Reference application with:

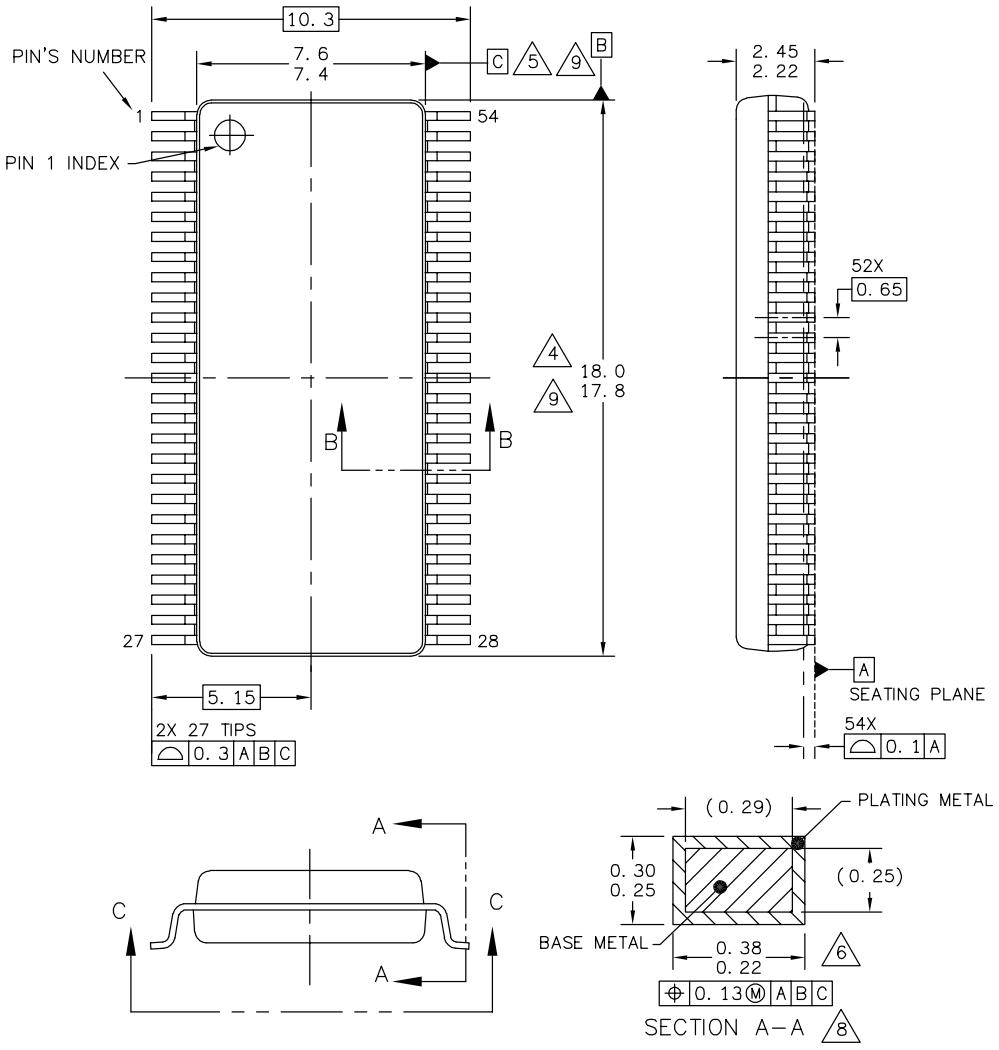
- Output FET gate charge: 240 nC @ 10 V
- PWM Frequency: 20 kHz
- Switching Single Phase
- No connections to PUMP or VPUMP
- VPWR connected to V_{SYS}

If VPWR is supplied by a separate pre-regulator, the power dissipation profile will be nearly flat at the value of the pre-regulator voltage for all V_{SYS} voltages.

PACKAGING

PACKAGING DIMENSION

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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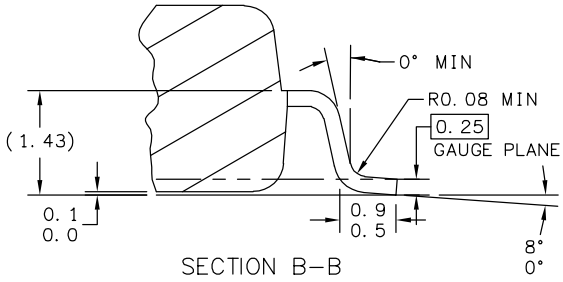
33937

PACKAGING DIMENSION (CONTINUED)



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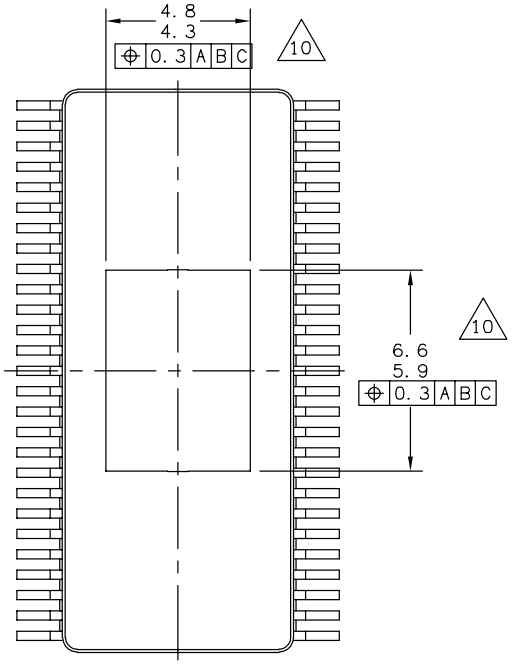

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REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	6/2008	• Initial Release
2.0	7/2008	• Updated specifications for current sense amplifier and overcurrent comparator • Added Gain/Phase curves for current sense amplifier • Added typical curves for load margin on Px_CBOOT • Added discussion about bootstrap capacitors and requirements for external bootstrap diodes • Updated application drawings • Added VSUP requirement for hold-off
3.0	11/2008	• Updated Freescale form and style • Added note to VLS Regulator Outputs (VLS, VLS_CAP)(2) • Changed Charge Device Model - CDM • Corrected title to No output loads on Gate Drive Pins, No PWM, Outputs initialized • Changed CAUTION for 33937 only (Use the 33937A to avoid this CAUTION) and associated paragraphs
4.0	12/2008	• Added PCZ33937AEK/R2 Part number throughout. • Added Note and changed parameters for Desaturation Detector and Phase Comparator to Dynamic Electrical Characteristics Table. • Replaced Typical Application Diagrams (Pages 40 and 41). • Page 10 remove V_{DD} Threshold (V_{DD} Falling) change note 23
5.0	4/2009	• Note 41 clarification.
6.0	9/2009	• Changed part number from PCZ33937A to MCZ33937A on page 1. Added Device Variation table on page 2.

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