

## OC-192/STM-64 SFF Transponder

(1310nm, 7km and 20km transmission)

### Members of Softac Family



### Features

- ◆ Compliant with the 300 pin MSA in a compact size
- ◆ Support transmission distance of 7km and 20km
- ◆ Support multi-rate operation from 9.953Gb/s to 11.318 Gb/s
- ◆ 1310nm externally EA modulated laser
- ◆ Wide dynamic range InGaAs PIN receiver
- ◆ 1:16 MUX/DEMUX integrated
- ◆ 16-bit parallel 622.08Mbps LVDS data interface
- ◆ Selectable dual fixed-rate jitter clean-up which can be bypassed for multi-rate operation
- ◆ Compliant I2C MSA (Edition 4.0) interface for monitoring/control
- ◆ Supply voltage: +1.8V, +3.3V, +5.0V, -5.2V
- ◆ Operating case temperature: -5°C to +70°C

### Applications

- ◆ Metro network SDH / SONET system
- ◆ 10 Gigabit Ethernet system
- ◆ Forward Error Correction (FEC) system
- ◆ Optical Transport Network (OTN) System

### Standard

Compliant with 300-PIN MSA  
 Compliant with ITU-T G.691  
 Compliant with ITU-T G.959.1  
 Compliant with Telcordia GR-253  
 Compliant with IEEE 802.3ae  
 Compliant with OIF SFI-4 interface  
 Compliant with Telcordia GR-468-Core  
 Compliant with IEC-60825-1 Class I

### Description

Fiberxon 1310nm transponders are intended for 1310nm system applications with reaches of up to 7km and 20km, which is designed to provide high optical performance for SONET OC-192 / SDH STM-64.

The transmitter converts the electrical data into 10Gbit/s optical signal, which uses 1310nm externally EA modulated laser with specified driving circuit.

At the receiving side, the incoming data stream is received at 10Gb/s PIN receiver, which converts it into a 10Gb/s electrical data stream.

The MUX section multiplexes 16 parallel 622Mb/s electrical channels into a 10Gb/s series data stream and sent it to the transmitter. And the DEMUX section demultiplexes the 10Gb/s electrical data stream into 16 parallel 622Mb/s electrical channels. The parallel data is sent out to and get from the 300-pin MSA (Multi Source Agreement) compliant connector.

The transmitter and receiver reference clock rates are selectable for divide by 16 or 64.

### Block Diagram

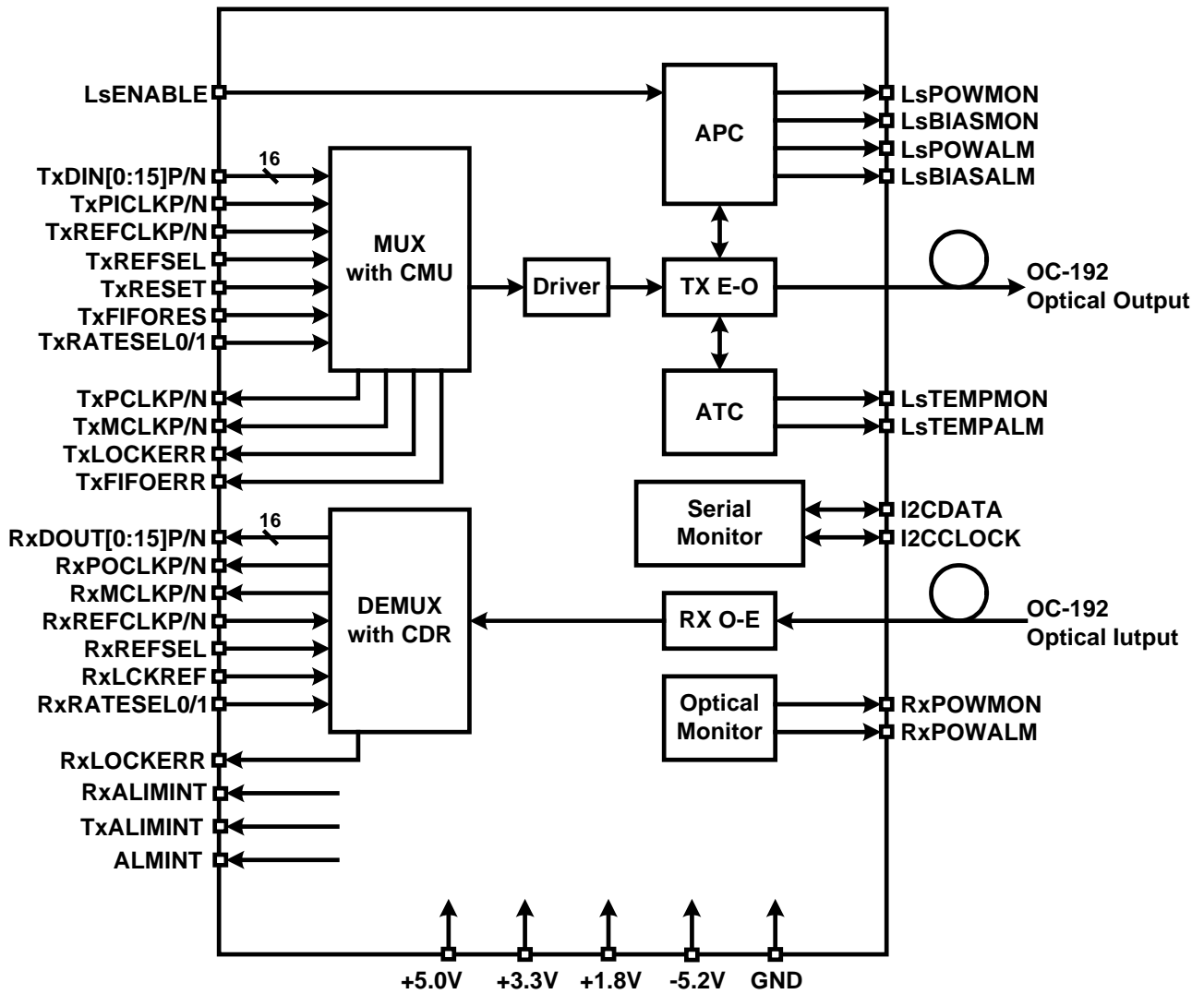


Figure 1, Block Diagram of Transponder

## Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device.

**Table 1- Absolute Maximum Ratings**

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	$T_S$	-40	+85	°C
Operating Case Temperature	$T_{cm}$	-10	+75	°C
Supply Voltage	$V_{cc}$	-0.5	+6.0	V
	$V_{dd1}$	-0.5	+4.2	V
	$V_{dd2}$	-0.5	+3.3	V
	$V_{ee}$	-7.0	+0.5	V
Operating Relative Humidity (non-condensing)	RH		85	%
Electro-Static Discharge	ESD		2000	V
Input Optical Power	Pin		+3	dBm

## Recommended Operating Conditions

Specified performance is maintained over all conditions in the table below, and damage to the device may occur over an extended period of time.

**Table 2 - Recommended Operating Conditions**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	$T_C$	-5		+70	°C
Supply Voltage	$V_{cc}$	4.75	5.0	5.25	V
	$V_{dd1}$	3.13	3.3	3.46	V
	$V_{dd2}$	1.62	1.8	1.98	V
	$V_{ee}$	-5.46	-5.2	-4.94	V
Supply Current	$I_{cc}$		100	150	mA
	$I_{dd1}$		300	750	mA
	$I_{dd2}$		700	850	mA
	$I_{ee}$		450	600	mA
Power consumption	$P_d$		5.00	7.00	W
Power supply noise rejection				50	mVp-p

## Optical Interface Characteristics

**Table 3 - Optical Characteristics**

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
<b>Transmitter</b>						
Centre Wavelength	$\lambda_C$	1290		1330	nm	
Output Power (BOL) – 7km	$P_{Out}$	-5		-1	dBm	1
Output Power (EOL) – 7km	$P_{Out}$	-6		-1	dBm	1
Output Power (BOL) – 20km	$P_{Out}$	+2		+5	dBm	1
Output Power (EOL) – 20km	$P_{Out}$	+1		+5	dBm	1
Output Power Stability		-0.5		+0.5	dBm	
Output Power at laser disable	$P_{Out}$			-45	dBm	
Spectral Width (-20dB)	$\Delta_{20}$			0.3	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Extinction Ratio (BOL)	ER	7			dB	
Extinction Ratio (EOL)	ER	6			dB	
Output Optical Eye	Compliant with Telcordia GR-253-CORE and ITU-T G.691					2
Jitter Generation	B1			0.3	UI	3
	B2			0.1	UI	3
<b>Receiver</b>						
Centre Wavelength	$\lambda_C$	1290		1600	nm	
Receiver Sensitivity (BOL)	$P_{in}$			-15	dBm	4
Receiver Sensitivity (EOL)	$P_{in}$			-13	dBm	4
Receiver Overload	$P_{in}$	-1.0			dBm	4
Optical Path Penalty				1	dB	
Reflection of Receiver				-27	dB	
Jitter Tolerance	Compliant with Telcordia GR-253 and ITU-T G.825					
Jitter Transfer	Compliant with Telcordia GR-253 and ITU-T G.825					

**Notes:**

1. The optical power is launched into SMF.
2. The mask margin is 10%.
3. Measured with a NRZ PRBS  $2^{31}-1$  test pattern @ 9.95328Gbps.
4. Measured with a NRZ PRBS  $2^{31}-1$  test pattern @ 9.95328Gbps, BER  $\leq 1 \times 10^{-12}$ .

## Electrical Interface Characteristics

**Table 4 - LVDS Input/Output Specification**

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
<b>LVDS interface</b>						
Input Differential Voltage	$V_{ID}$	200			mV	
Input Differential impedance	$R_{ID}$	80	100	120	$\Omega$	
Output Differential Voltage	$V_{OD}$	500		1000	mV	
Output Differential impedance	$R_{OD}$	80	100	120	$\Omega$	
Rise Time/Fall time	$T_{rise/fall}$			250	ps	
Clock Signal Duty Cycle		45	50	55	%	

**Definition of Differential Voltage Levels**

**Table 5 - Input Reference Clocks**

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Input Differential Voltage	$V_{ID}$	400		1800	mV	
Differential Input Impedance	$R_{ID}$	80	100	120	$\Omega$	
Clock signal Duty Cycle	$T_w/T_o$	45		55	%	

**Table 6 - LVTTTL Input/Output Pin Characteristics**

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Input High Voltage		2.0		Vdd	V	
Input Low Voltage		GND		0.8	V	
Output High Voltage		2.4		Vdd	V	
Output Low Voltage		GND		0.4	V	

## Transponder Clock Interfaces and Control

There are seven clock interfaces to the transponder. This section details the specific functions, capabilities, and limitations of each. Note that all clock rates shown are at STM-64/OC-192 rate, but should be scaled appropriately for other data rates.

The LVPECL TxREFCLK, provided via the 300-pin interface, may be at 1/16 or 1/64 of the transmitted serial data rate. The TxREFCLK must be synchronous with the TxPICKL. There are several approaches to ensure this synchronous relationship. The two most common are

- 1) Locking the TxPICKL to the TxPCLK out of the transponder

2) Generating TxPICK and TxREFCLK from the same clock on the line-card.  
 The LVPECL RxREFCLK may be at 1/16 or 1/64 of the incoming data rate also.

**Table 7 - Reference Clock characteristics**

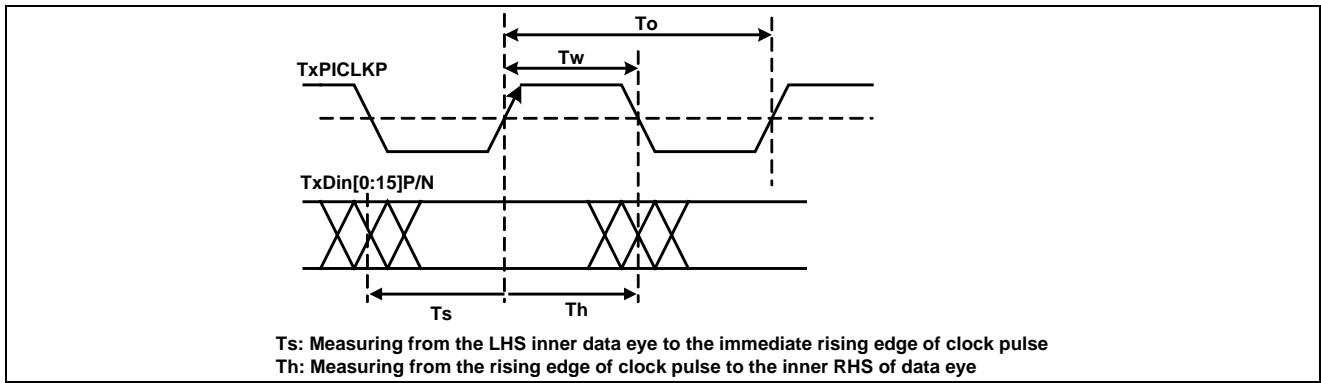
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
<b>Transmitter</b>						
Frequency	TxREFCLKP TxREFCLKN	155.52/622.08			MHz	Serial data-rate is 9.953Gbps
Frequency tolerance		-100		+100	ppm	
Rise/Fall time	Tr/Tf			300	ps	
Duty Cycle		40	50	60	%	
<b>Receiver</b>						
Frequency	RxREFCLKP RxREFCLKN	155.52/622.08			MHz	Serial data-rate is 9.953Gbps
Frequency tolerance		-100		+100	ppm	
Rise/Fall time	Tr/Tf			300	ps	
Duty Cycle		40	50	60	%	

**Table 8 - Transmitter/Receiver Parallel Data/Clock Interface**

Parameter	Symbol	Level	Notes
Transmitter 16-bit parallel Data Input	TxDin[0:15]P/N	LVDS	TxDin0: LSB, TxDin15: MSB
Transmitter Source synchronous Parallel Input Clock	TxPICKP/N	LVDS	
Transmitter Counter Clock	TxPCLKP/N	LVDS	
Receiver 16-bit parallel Data Output	RxDout[0:15]P/N	LVDS	RxDout0: LSB, RxDout15: MSB
Receiver Source synchronous Parallel Output Clock	RxPOCLKP/N	LVDS	

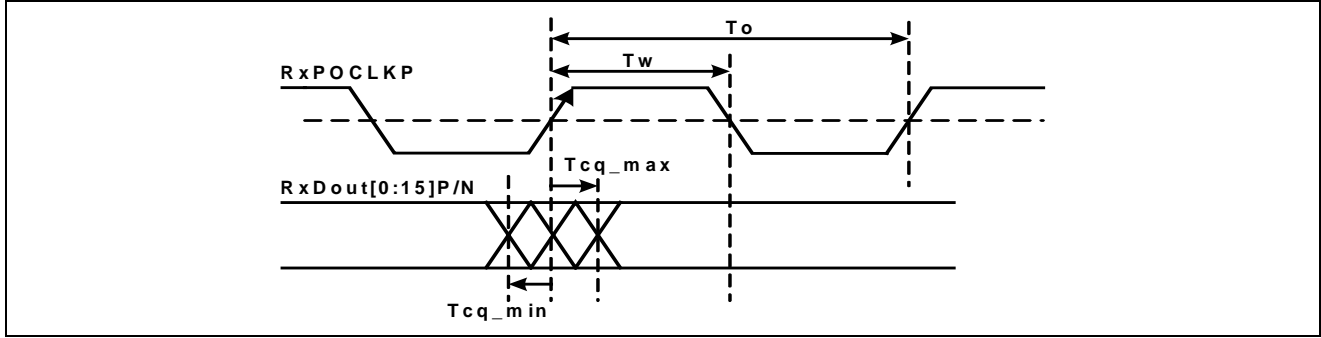
**Table 9 - Transmitter/Receiver Parallel Data/Clock Timing**

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
<b>Transmitter Data/Clock Timing: SERDES Input Timing at SERDES pin</b>						
TxPICK	Duty Cycle	Tw/To	40		60	%
	Rise and Fall time	Tr/Tf			300	ps
TxDin	Setup time	Ts	300			ps
	Hold time	Th	300			ps



**Receiver Data/Clock Timing: SERDES Output Timing at SERDES pin**

RxPOCLK	Duty cycle	Tw/To	40		60	%	
	Rise and Fall time	Tr/Tf			300	ps	20 – 80%
RxDout	Data/Clock skew	Tcq_min,			250	ps	
		Tcq_max			250	ps	



**Table 10 - Monitor Clock**

Parameter	Symbol	Level	Notes
Transmitter monitor clock	TxMCLKP/N	LVDS	The LVDS TxMCLK is either a 1/16 or 1/64 replica of the clock used to time the serial data output. The rate of the TxMCLK is always the same as that of the TxREFCLK
Receiver monitor clock	RxMCLKP/N	LVDS	The LVDS RxMCLK is a 1/16 or 1/64 replica of the clock recovered from the incoming data

**Table 11 - Serial Data Rate selection**

(LVTTTL with pull-up resistor)

TxRATESEL1/ RxRATESEL1	TxRATESEL0/ RxRATESEL0	Function		
		Tx/Rx Serial Data Rate	Parallel Data Rate TxDIN[0:15]/RxOUT[0:15]	TxPICLK/RxPOCLK
L	L	10.3125Gbps	644.54Mbps	644.54Mbps
L	H	11.049/11.095/ 11.318Gbps	690.56/693.43/ 707.37Mbps	690.56/693.43/ 707.37Mbps
H	L	10.519/10.664/ 10.709Gbps	657.43/666.51/ 669.32Mbps	657.43/666.51/ 669.32Mbps
H	H	9.95328Gbps	622.08Mbps	622.08Mbps

## Digital Control Signal

**Table 12 - Input Digital signals**

Function	Symbol	Level	Description	Note	
Module RESET	MOD_RESET	LVTTTL	L	Module reset	Reset both Tx and Rx section (LVTTTL with pull-up resistor)
			H	Normal operation	
Diagnostic Loop-back	DLOOPENB	LVTTTL	L	Enable	(LVTTTL with pull-up resistor)
			H	Normal operation	
Line Loop-back	LLOOPENB	LVTTTL	L	Enable	(LVTTTL with pull-up resistor)
			H	Normal operation	
<b>Transmitter</b>					
Select serial data rate	TxRATESEL0,1	LVTTTL	0,0	10.3125Gbps	(LVTTTL with pull-up resistor)
			0,1	11.049/11.095/ 11.318Gbps	
			1,0	10.519/10.664/ 10.709Gbps	
			1,1	9.95328Gbps	
Select the frequency of TxREFCLK	TxREFSEL	LVTTTL	L	1/64 data-rate	(LVTTTL with pull-up resistor)
			H	1/16 data-rate	
Select the frequency of TxPICKL	TxPICKLSEL	LVTTTL	L	1/16 data-rate	(LVTTTL with pull-down resistor)
			H	1/32 data-rate	
Enable internal Line Timing	TxLINETIMSEL	LVTTTL	L	Enable	On multi-rate units without jitter clean up, this pin is ignored. (LVTTTL with pull-up resistor)
			H	Normal operation	
Select delay of TxPICKL	TxSKEWSEL0,1	LVTTTL	0,0	Delays 915ps	(LVTTTL with pull-up resistor)
			0,1	Delays 1015ps	
			1,0	Delays 715ps	
			1,1	Delays 815ps	
Enable/Disable Laser	LsENABLE	LVTTTL	L	Normal operation	(LVTTTL with pull-down resistor)
			H	Laser disabled	
Asynchronous system reset	TxRESET	LVTTTL	L	MUX reset	(LVTTTL with pull-up resistor)
			H	Normal operation	
MUX FIFO reset	TxFIFOES	LVTTTL	L	MUX FIFO reset	Internally the FIFO reset is connected to TxRESET and TxFIFOES, as well as TxFIFOERR. TxFIFOERR will initiate a FIFO reset (LVTTTL with pull-up resistor)
			H	Normal operation	



Receiver					
Select data rate	TxRATESEL0,1	LVTTTL	0,0	10.3125Gbps	(LVTTTL with pull-up resistor)
			0,1	11.049/11.095/ 11.318Gbps	
			1,0	10.519/10.664/ 10.709Gbps	
			1,1	9.95328Gbps	
Select the frequency of RxREFCLK	RxREFSEL	LVTTTL	L	1/64 data-rate	(LVTTTL with pull-down resistor)
			H	1/16 data-rate	
Select the frequency of RxMCLK	RxMCLKSEL	LVTTTL	L	1/64 data-rate	(LVTTTL with pull-up resistor)
			H	1/16 data-rate	
Lock RxPOCLK to RxREFCLK	RxLCKREF	LVTTTL	L	Lock to RxREFCLK	(LVTTTL with pull-up resistor)
			H	Normal operation	
Mutes the RxDOOUT[0:15]	RxMUTEDOUT	LVTTTL	L	Mutes the RxDOOUT[0:15]	(LVTTTL with pull-up resistor)
			H	Normal operation	
Mutes the receiver output monitor clock	RxMUTEMCLK	LVTTTL	L	Mutes the RxMCLK	(LVTTTL with pull-up resistor)
			H	Normal operation	
Mutes receiver parallel output clock RxPOCLK	RxMUTEPOCLK	LVTTTL	L	Mutes the RxPOCLK	(LVTTTL with pull-up resistor)
			H	Normal operation	
Rx synchronous system reset	RxRESET	LVTTTL	L	Asynchronous reset	(LVTTTL with pull-up resistor)
			H	Normal operation	

## Digital Alarm Signal

**Table 13 - Alarms Digital signals**

Function	Symbol	Level	Description		Note
<b>Common Digital Signal</b>					
Indicates all alarm active	ALMINT	LVTTTL	L	Any alarm from both transmitter and receiver	Activation Time: 10ms Deactivation Time: 10ms
			H	Normal operation	
<b>Transmitter</b>					
Loss of Tx PLL lock	TxLOCKERR	LVTTTL	L	Alarm active	Loss of transmitter PLL lock Activation Time: 1ms Deactivation Time: 1ms
			H	Normal operation	
MUX FIFO error	TxFIFOERR	LVTTTL	L	Alarm active (FIFO overflow)	TxError is internally connected to TxFIFO RES. (Default) Customer may have control of TXFIFO RES without internal loopback (Optional)
			H	Normal operation	
Laser bias out of range	LsBIASALM	LVTTTL	L	Alarm active (laser bias current alarm)	Alarm when laser bias changes by a factor of 2 from beginning of life or if monitor reaches maximum level corresponding to approximate 150mA. Activation Time: 10 ms Deactivation Time: 10 ms
			H	Normal operation	
Laser temperature out of range	LsTEMPALM	LVTTTL	L	Alarm active	Laser temperature 5°C from nominal, Activation Time : 10ms Deactivation Time : 10ms
			H	Normal operation	
Laser output power out of range	LsPOWALM	LVTTTL	L	Alarm active	Output power degrades 3dB below the BOL Activation Time : 10ms Deactivation Time : 10ms
			H	Normal operation	
Tx alarms	TxALMINT	LVTTTL	L	Alarm from transmitter	Activation Time: 10 ms; Deactivation Time: 10 ms
			H	Normal operation	
<b>Receiver</b>					
Loss of Rx PLL lock	RxLOCKERR	LVTTTL	L	Alarm active	Activation Time: 1ms Deactivation Time: 1ms
			H	Normal operation	
Loss of receiver average power alarm	RxPOWALM	LVTTTL	L	Alarm active	Activation Time: <60us Deactivation Time: <60us
			H	Normal operation	
Rx alarms	RxALMINT	LVTTTL	L	Alarm from transmitter	Activation Time: 10 ms; Deactivation Time: 10 ms
			H	Normal operation	

## Analog Monitoring Signal

**Table 14 - Monitor Signals**

Function	Symbol	Min.	Typ.	Max.	Unit
<b>Transmitter</b>					
Normalized laser power monitor voltage BOL	LsPOWMON	0.47	0.5	0.53	V
Laser power monitor voltage slope		0.25 V change for 50% power variation (mW)			
Laser bias monitor voltage offset	LsBIASMON	0.2	0	2	V
Laser bias monitor voltage slope		18	20	22	mV/mA
Normalized laser temperature Monitor voltage	LsTEMPMON	2.4	2.5	2.6	V
Laser temperature Monitor voltage slop		23	25	27	mV/°C
<b>Receiver</b>					
Input optical power monitor voltage offset @-10dBm	RxPOWMON	0.09		0.11	mV
Input optical power monitor voltage slope		0.8	1.0	1.26	V/mW
Input optical power monitor error		-1.0		+1.0	dBm

## I2C Serial Interface

**Table 14 – I2C Interface**

Function	Symbol	Level	Description	Note
I2C Address	I2CAD0	LVTTL	I2C address input for module addressing (LSB)	(LVTTL with pull-down resistor)
	I2CAD1	LVTTL	I2C address input for module addressing	(LVTTL with pull-down resistor)
	I2CAD2	LVTTL	I2C address input for module addressing (MSB)	(LVTTL with pull-down resistor)
I2C Clock	I2CCLOCK	Open collector	I2C clock input/output for remote access	N/A
I2C Data	I2CDATA	Open collector	I2C data input/output for remote access	N/A

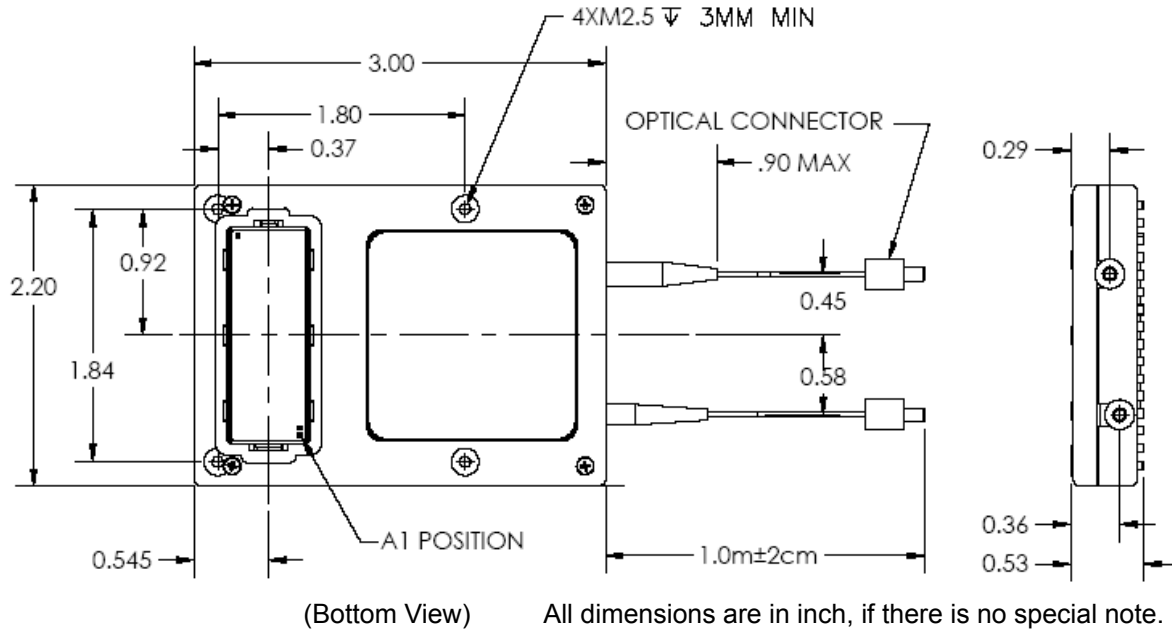
## Pin Definitions

**Table 15 - Pin Function Definitions**

	K	J	H	G	F	E	D	C	B	A	
1	+5V	FFU	GND	RxDout12P	+1.8V	RxDout8P	GND	RxDout4P	GND	RxDout0P	
2	+5V	FFU	GND	RxDout12N	+1.8V	RxDout8N	GND	RxDout4N	GND	RxDout0N	
3	RxRATESEL0	RxRATESEL1	FFU	GND	RxPOWMON	GND	I2CAD0	GND	FFU	GND	
4	+3.3V	NUC	GND	RxDout13P	+3.3V	RxDout9P	GND	RxDout5P	GND	RxDout1P	
5	+3.3V	NUC	GND	RxDout13N	+3.3V	RxDout9N	GND	RxDout5N	GND	RxDout1N	
6	Rx_Reset	NUC	DLOOPENB	GND	RxPOWALM	GND	I2CAD1	GND	RxMUTE Dout	GND	
7	+3.3V	FFU	GND	RxDout14P	+3.3V	RxDout10P	GND	RxDout6P	GND	RxDout2P	
8	+3.3V	FFU	GND	RxDout14N	+3.3V	RxDout10N	GND	RxDout6N	GND	RxDout2N	
9	RxMUTEPOCLK	NUC	FFU	GND	FFU	GND	I2CAD2	GND	RxLCKREF	GND	
10	-5.2V	NUC	GND	RxDout15P	-5.2V	RxDout11P	GND	RxDout7P	GND	RxDout3P	
11	-5.2V	NUC	GND	RxDout15N	-5.2V	RxDout11N	GND	RxDout7N	GND	RxDout3N	
12	RxMUTEMCLK	NUC	FFU	GND	FFU	GND	MOD RESET	GND	RxMCLKSEL	GND	
13	-5.2V	FFU	GND	FFU	-5.2V	RxPOCLKP	GND	RxMCLKP	GND	RxREFCLKP	
14	-5.2V	RxALMINT	GND	FFU	-5.2V	RxPOCLKN	GND	RxMCLKN	GND	RxREFCLKN	
15	I2CCLOCK	NUC	FFU	GND	RxREFSEL	GND	FFU	GND	RxLOCKERR	GND	
16	+5V	TxALMINT	GND	TxDin12P	+1.8V	TxDin8P	GND	TxDin4P	GND	TxDin0P	
17	+5V	FFU	GND	TxDin12N	+1.8V	TxDin8N	GND	TxDin4N	GND	TxDin0N	
18	I2CDATA	NUC	FFU	GND	LsBIASMON	GND	LsPOWMON	GND	TxSKEWSEL0	GND	
19	+3.3V	FFU	GND	TxDin13P	+3.3V	TxDin9P	GND	TxDin5P	GND	TxDin1P	
20	+3.3V	FFU	GND	TxDin13N	+3.3V	TxDin9N	GND	TxDin5N	GND	TxDin1N	
21	TxRATESEL0	TxRATESEL1	FFU	GND	LsENABLE	GND	LsTEMPMON	GND	TxSKEWSEL1	GND	
22	+3.3V	FFU	GND	TxDin14P	+3.3V	TxDin10P	GND	TxDin6P	GND	TxDin2P	
23	+3.3V	FFU	GND	TxDin14N	+3.3V	TxDin10N	GND	TxDin6N	GND	TxDin2N	
24	TxRESET	NUC	FFU	GND	LsBIASALM	GND	FFU	GND	FFU	GND	
25	-5.2V	NUC	GND	TxDin15P	-5.2V	TxDin11P	GND	TxDin7P	GND	TxDin3P	
26	-5.2V	NUC	GND	TxDin15N	-5.2V	TxDin11N	GND	TxDin7N	GND	TxDin3N	
27	TxFIFORES	NUC	LLOOPENB	GND	LsTEMPALM	GND	FFU	GND	TxPICKSEL	GND	
28	-5.2V	FFU	GND	TxPICKP	-5.2V	TxPCLKP	GND	TxMCLKP	GND	TxREFCLKP	
29	-5.2V	TxTRACE	GND	TxPICKN	-5.2V	TxPCLKN	GND	TxMCLKN	GND	TxREFCLKN	
30	TxFIFOERR	NUC	LINETIMESEL	GND	TxREFSEL	GND	LsPOWALM	GND	TxLOCKERR	GND	
FFU: Reserved for Future Use				NUC: No Use Connection							

## Mechanical Design Diagram

The mechanical design diagram is shown in Figure 2.



**Figure 2, Mechanical Diagram**

## Ordering Information

Part No.	Product Description
<b>FAM-30X1S-T7</b>	1310nm, 10Gbps, 7km, 300-Pin, SC connector, -5°C~+70°C,
<b>FAM-30X1S-T20</b>	1310nm, 10Gbps, 20km, 300-Pin, SC connector, -5°C~+70°C,

## Related Documents

For further information, please refer to the following documents:

- Application Note for Fiberxon 10G Transponder I2C Serial Interface Specifications
- Reference Document for 300 pin Multi Source Agreement for 10 Gigabit Transponders (SERDES Transceivers), Edition 4, August 14, 2002
- I2C Reference Document for 300-PIN MSA 10G and 40G Transponders, Edition 4, July 24, 2002.

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