**Flash-ROM Module 4MByte (1Mx32Bit), 100Pin-MMC, 5.5V Design**
**Part No. HMF1M32F8**

## GENERAL DESCRIPTION

The HMF1M32F8 is a high-speed flash read only memory (FROM) module containing 1,048,576 words organized in a x32bit configuration. The module consists of eight 512K x 8 FROM mounted on a 100-pin stackable type, double -sided, FR4-printed circuit board.
Commands are written to the command register using standard microprocessor write timings.
Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.
Eight chip enable inputs, (/CE_UU1, /CE_UM1, /CE_LM1, /CE_LL1, /CE_UU2, /CE_UM2, /CE_LM2 , /CE_LL2) are used to enable the module's 4 bytes independently. Output enable (/OE) and write enable (/WE) can set the memory input and output.
When FROM module is disable condition the module is becoming power standby mode, system designer can get low -power design. All module components may be powered from a single +5V DC power supply and all inputs and outputs are TTL -compatible.

## FEATURES

- Access time: 55, 70, 90, 120ns
- High-density 4MByte design
- High-reliability, low-power design
- Single + 5V ± 0.5V power supply
- Easy memory expansion
- All in/outputs are TTL-compatible
- FR4-PCB design
- 100-pin Designed by
  50-pin Fine Pitch Connector
- Minimum 1,000,000 write/erase cycle
- Sector erases architecture
- Sector group protection
- Temporary sector group unprotection

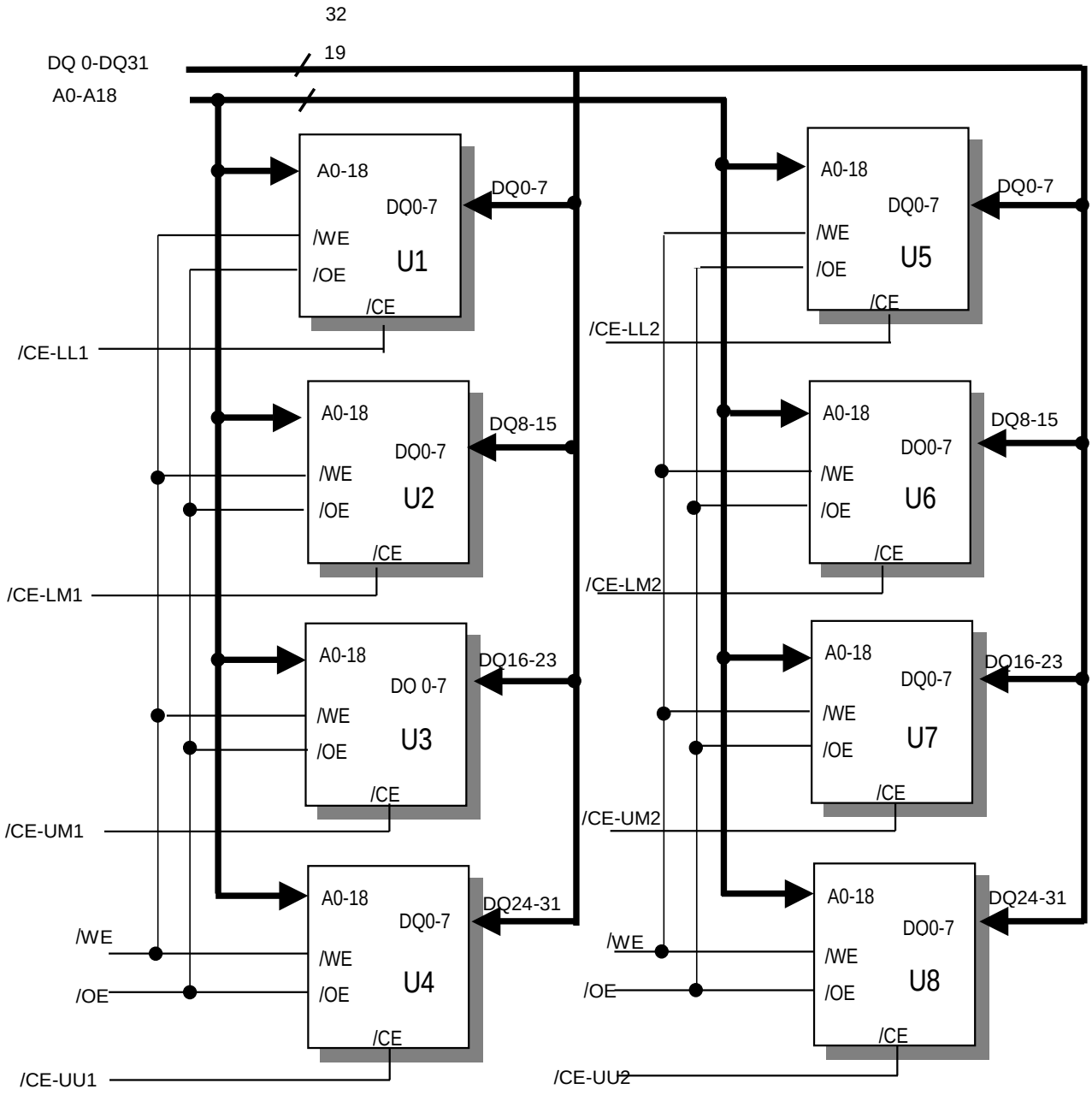
## OPTIONS MARKING

- Timing
  - 55ns access -55
  - 70ns access -70
  - 90ns access -90
  - 120ns access -120
- Packages
  - 100-pin SMM F

## PIN ASSIGNMENT

| P1 | | | | P2 | | | |
|---|---|---|---|---|---|---|---|
| PIN | Symbol | PIN | Symbol | PIN | Symbol | PIN | Symbol |
| 1 | Vcc | 26 | Vcc | 51 | Vcc | 76 | Vcc |
| 2 | NC | 27 | /CE_LL2 | 52 | NC | 77 | /CE_UM2 |
| 3 | /CE_LL1 | 28 | /CE_LM2 | 53 | /CE_UM1 | 78 | /CE_UU2 |
| 4 | /CE_LM1 | 29 | A18 | 54 | /CE_UU1 | 79 | DQ22 |
| 5 | DQ15 | 30 | A17 | 55 | DQ31 | 80 | DQ21 |
| 6 | DQ14 | 31 | A16 | 56 | DQ30 | 81 | DQ20 |
| 7 | DQ13 | 32 | A15 | 57 | DQ29 | 82 | DQ19 |
| 8 | Vss | 33 | Vss | 58 | Vss | 83 | Vss |
| 9 | DQ12 | 34 | A14 | 59 | /OE | 84 | DQ18 |
| 10 | DQ11 | 35 | A13 | 60 | /WE | 85 | DQ17 |
| 11 | DQ10 | 36 | DQ9 | 61 | NC | 86 | DQ16 |
| 12 | DQ8 | 37 | DQ7 | 62 | NC | 87 | NC |
| 13 | Vss | 38 | Vss | 63 | Vss | 88 | Vss |
| 14 | DQ6 | 39 | DQ5 | 64 | NC | 89 | NC |
| 15 | DQ4 | 40 | A12 | 65 | NC | 90 | NC |
| 16 | DQ3 | 41 | A11 | 66 | DQ28 | 91 | NC |
| 17 | DQ2 | 42 | A10 | 67 | DQ27 | 92 | NC |
| 18 | Vss | 43 | Vss | 68 | Vss | 93 | Vss |
| 19 | DQ1 | 44 | A9 | 69 | DQ26 | 94 | NC |
| 20 | DQ0 | 45 | A8 | 70 | DQ25 | 95 | NC |
| 21 | A0 | 46 | A7 | 71 | DQ24 | 96 | NC |
| 22 | A1 | 47 | A6 | 72 | DQ23 | 97 | NC |
| 23 | A2 | 48 | A5 | 73 | Vss | 98 | Vss |
| 24 | A3 | 49 | A4 | 74 | NC | 99 | NC |
| 25 | Vcc | 50 | Vcc | 75 | Vcc | 100 | Vcc |

## FUNCTIONAL BLOCK DIAGRAM



## TRUTH TABLE

| MODE | /OE | /CE | /WE | DQ | POWER |
|---|---|---|---|---|---|
| STANDBY | X | H | X | HIGH-Z | STANDBY |
| NOT SELECTED | H | L | H | HIGH-Z | ACTIVE |
| READ | L | L | H | Q | ACTIVE |
| WRITE or ERASE | X | L | L | D | ACTIVE |

NOTE: X means don't care

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING |
|---|---|---|
| Voltage with respect to ground all other pins | $V_{IN,OUT}$ | -2.0V to +7.0V |
| Voltage with respect to ground Vcc | $V_{CC}$ | -2.0V to +7.0V |
| Power Dissipation | $P_D$ | 8W |
| Storage Temperature | $T_{STG}$ | -65°C to +125°C |
| Operating Temperature | $T_A$ | -55°C to +125°C |

**w** Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device.

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN | TYP. | MAX |
|---|---|---|---|---|
| Vcc for ±5% device Supply Voltages | $V_{CC}$ | 4.75V | | 5.25V |
| Vcc for ± 10% device Supply Voltages | Vcc | 4.5V | | 5.5V |
| Ground | $V_{SS}$ | 0 | 0 | 0 |

## DC AND OPERATING CHARACTERISTICS ($0^oC \le T_A \le 70\ ^oC$ ; Vcc = 5V ± 0.5V )

| PARAMETER | TEST CONDITIONS | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| Input Load Current | Vcc=Vcc max, $V_{IN}$= Vss to Vcc | $I_{L1}$ | | ±1.0 | µA |
| Output Leakage Current | Vcc=Vcc max, $V_{OUT}$= Vss to Vcc | $I_{L0}$ | | ±1.0 | µA |
| Output High Voltage | $I_{OH}$ = -2.5mA, Vcc = Vcc min | $V_{OH}$ | 2.4 | | V |
| Output Low Voltage | $I_{OL}$ = 12mA, Vcc =Vcc min | $V_{OL}$ | | 0.45 | V |
| Vcc Active Current for Read(1) | /CE = $V_{IL}$, /OE=$V_{IH}$, | $I_{CC1}$ | | 30 | mA |
| Vcc Active Current for Program or Erase(2) | /CE = $V_{IL}$, /OE=$V_{IH}$ | $I_{CC2}$ | | 40 | mA |
| Vcc Standby Current | /CE= $V_{IH}$ | $I_{CC3}$ | | 1.0 | mA |
| Low Vcc Lock-Out Voltage | | $V_{LKO}$ | 3.2 | 4.2 | V |

**Notes:** 1. The Icc current listed is typically less than 2mA/MHz, with /OE at $V_{IH}$.

2. Icc active while embedded algorithm (program or erase) is in progress

3. Maximum Icc current specifications are tested with Vcc=Vcc max

## ERASE AND PROGRAMMING PERFORMANCE

| PARAMETER | LIMITS | | | UNIT | COMMENTS |
|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | | |
| Sector Erase Time | - | 1 | 8 | sec | Excludes 00H programming prior to erasure |
| Byte Programming Time | - | 7 | 300 | μs | Excludes system-level overhead |
| Chip Programming Time | - | 3.6 | 10.8 | sec | Excludes system-level overhead |

## CAPACITANCE

| PARAMETER SYMBOL | PARAMETER DESCRIPTION | TEST SETUP | TYP. | MAX | UNIT |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | 6 | 7.5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | 8.5 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | 7.5 | 9 | pF |

**Notes** : Test conditions $T_A$ = 25° C, f=1.0 MHz.

## AC CHARACTERISTICS

### u Read Only Operations Characteristics

| PARAMETER SYMBOLS | | DESCRIPTION | TEST SETUP | | Speed Options | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| JEDEC | STANDARD | | | | -55 | -70 | -90 | -120 | |
| $T_{AVAV}$ | $t_{RC}$ | Read Cycle Time | | Min | 55 | 70 | 90 | 120 | ns |
| $T_{AVQV}$ | $t_{ACC}$ | Address to Output Delay | /CE = $V_{IL}$ /OE = $V_{IL}$ | Max | 55 | 70 | 90 | 120 | ns |
| $T_{ELQV}$ | $t_{CE}$ | Chip Enable to Output Delay | /OE = $V_{IL}$ | Max | 55 | 70 | 90 | 120 | ns |
| $T_{GLQV}$ | $t_{OE}$ | Output Enable to Output Delay | | Max | 30 | 30 | 35 | 50 | ns |
| $T_{EHQZ}$ | $t_{DF}$ | Chip Enable to Output High-Z | | Max | 18 | 20 | 20 | 30 | ns |
| $T_{GHQZ}$ | $t_{DF}$ | Output Enable to Output High-Z | | | 18 | 20 | 20 | 30 | ns |
| $T_{AXQX}$ | $t_{QH}$ | Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First | | Min | 0 | 0 | 0 | 0 | ns |

**Notes** : Test Conditions

Output Load : 1TTL gate and Output Load Capacitance 100 pF, in case of 55ns-30pF

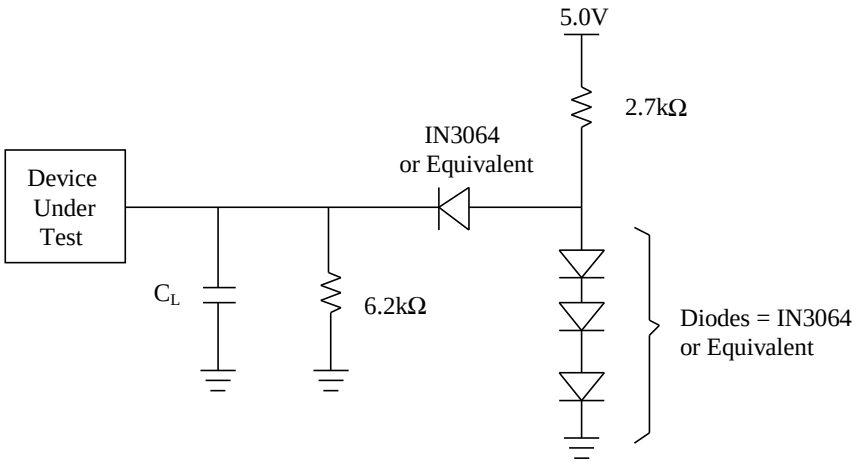
Input rise and fall times : 5 ns, In case of 55ns-5ns

Input pulse levels : 0.45V to 2.4V, In case of 55ns- 0.0V-3.0V

Timing measurement reference level

Input : 0.8V, Incase of 55ns-1.5V

Output : 2.0V, In case of 55ns-1.5V




**Note** : $C_L$ = 100pF including jig capacitance

## u Erase/Program Operations

| PARAMETER SYMBOLS | | DESCRIPTION | | Speed Options | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| JEDEC | STANDARD | | | -55 | -70 | -90 | -120 | |
| $T_{AVAV}$ | $t_{WC}$ | Write Cycle Time | Min | 55 | 70 | 90 | 120 | ns |
| $T_{AVWL}$ | $t_{AS}$ | Address Setup Time | Min | 0 | | | | ns |
| $T_{WLAX}$ | $t_{AH}$ | Address Hold Time | Min | 40 | 45 | 45 | 50 | ns |
| $T_{DVWH}$ | $t_{DS}$ | Data Setup Time | Min | 25 | 30 | 45 | 50 | ns |
| $T_{WHDX}$ | $t_{DH}$ | Data Hold Time | Min | 0 | | | | ns |
| | $t_{OES}$ | Output Enable Setup Time | Min | 0 | | | | ns |
| $T_{GHWL}$ | $t_{GHWL}$ | Read Recover Time Before Write | Min | 0 | | | | ns |
| $T_{ELWL}$ | $t_{CS}$ | /CE Setup Time | Min | 0 | | | | ns |
| $T_{WHEH}$ | $t_{CH}$ | /CE Hold Time | Min | 0 | | | | ns |
| $T_{WLWH}$ | $t_{WP}$ | Write Pulse Width | Min | 30 | 35 | 45 | 50 | ns |
| $t_{WHWL}$ | $t_{WPH}$ | Write Pulse Width High | Min | 20 | | | | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Byte Programming Operation | Typ | 7 | | | | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note1) | Typ | 1 | | | | sec |
| | $t_{VCS}$ | Vcc set up time | Min | 50 | | | | µs |

**Notes**： 1. Not 100% tested.

2. See the “Erase And Programming Performance” section for more information.

## u Erase/Program Operations

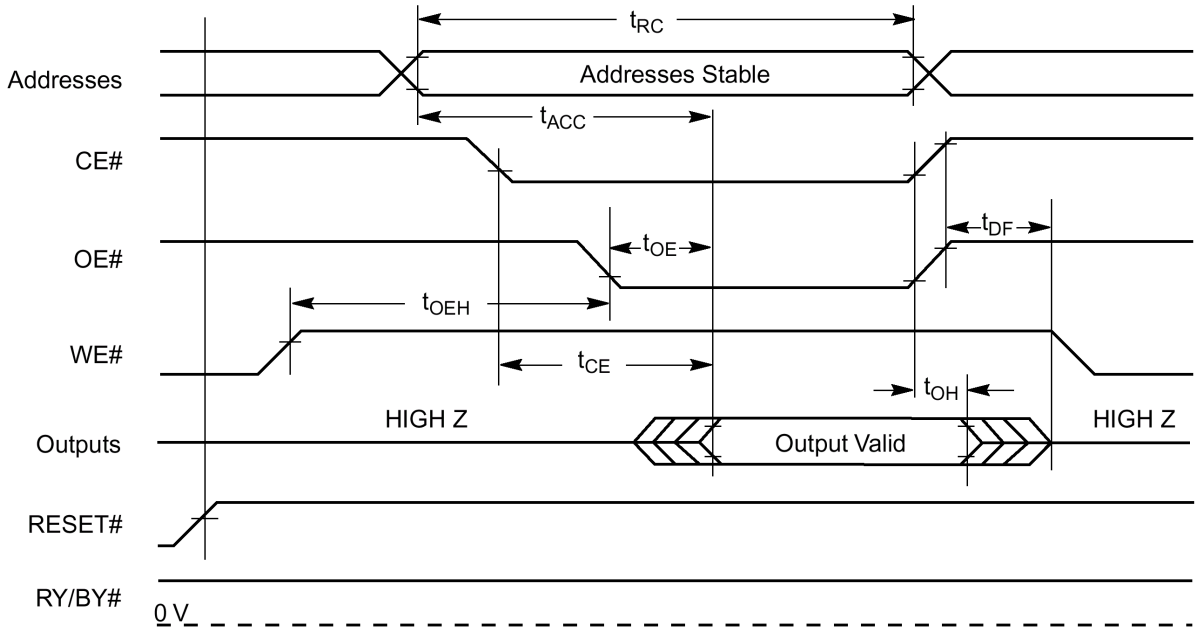
### Alternate /CE Controlled Writes

| PARAMETER SYMBOLS | | DESCRIPTION | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| JEDEC | STANDARD | | | -55 | -70 | -90 | -120 | ns |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time | Min | 55 | 70 | 90 | 120 | ns |
| $t_{AVEL}$ | $t_{AS}$ | Address Setup Time | Min | 0 | | | | ns |
| $t_{ELAX}$ | $t_{AH}$ | Address Hold Time | Min | 40 | 45 | 45 | 50 | ns |
| $t_{DVEH}$ | $t_{DS}$ | Data Setup Time | Min | 25 | 30 | 45 | 50 | ns |
| $t_{EHDX}$ | $t_{DH}$ | Data Hold Time | Min | 0 | | | | ns |
| $t_{GHEL}$ | $t_{GHEL}$ | Read Recover Time Before Write | Min | 0 | | | | ns |
| $t_{WLEL}$ | $t_{WS}$ | /CE Setup Time | Min | 0 | | | | ns |
| $t_{EHWH}$ | $t_{WH}$ | /CE Hold Time | Min | 0 | | | | ns |
| $t_{ELEH}$ | $t_{CP}$ | Write Pulse Width | Min | 30 | 35 | 45 | 50 | ns |
| $t_{EHEL}$ | $t_{CPH}$ | Write Pulse Width High | Min | 20 | 20 | 20 | 20 | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Byte Programming Operation | Typ | 7 | | | | μs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note) | Typ | 1 | | | | sec |

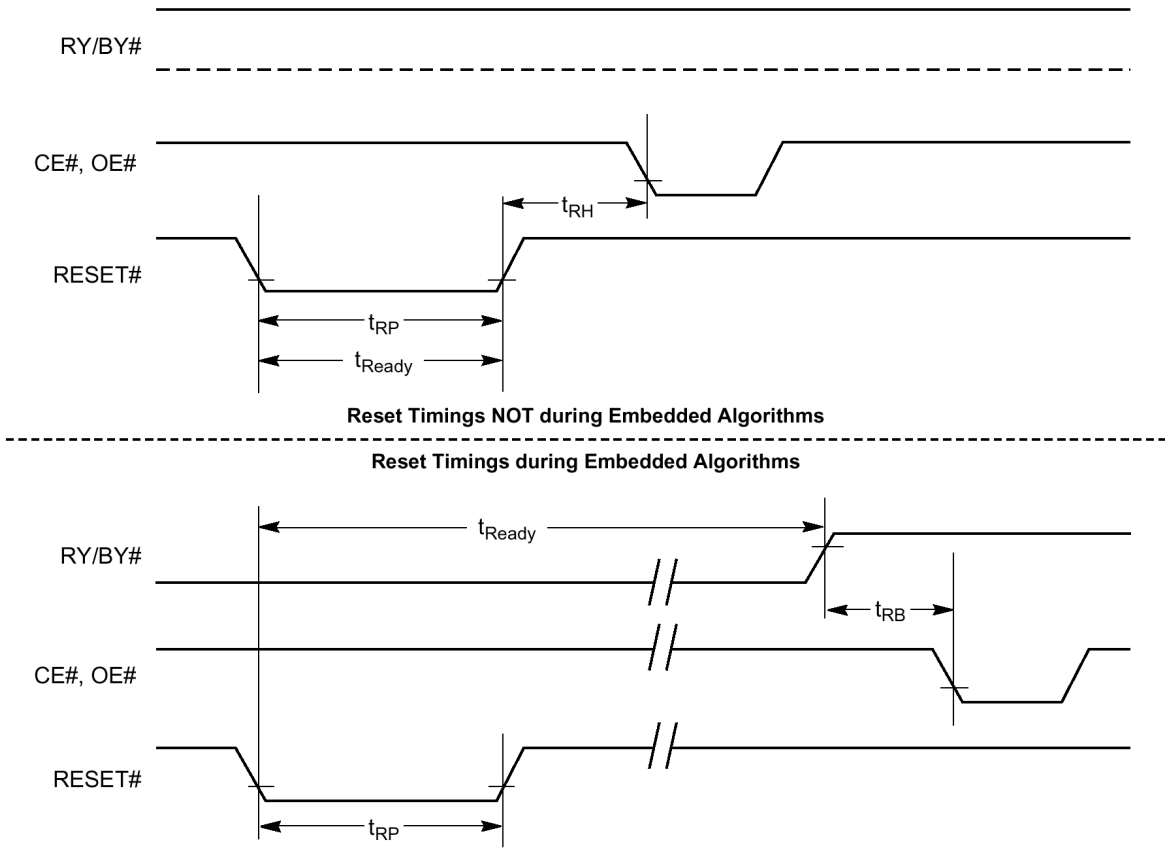
**Notes** : 1. Not 100% tested.

2. See the “Erase And Programming Performance” section for more information.

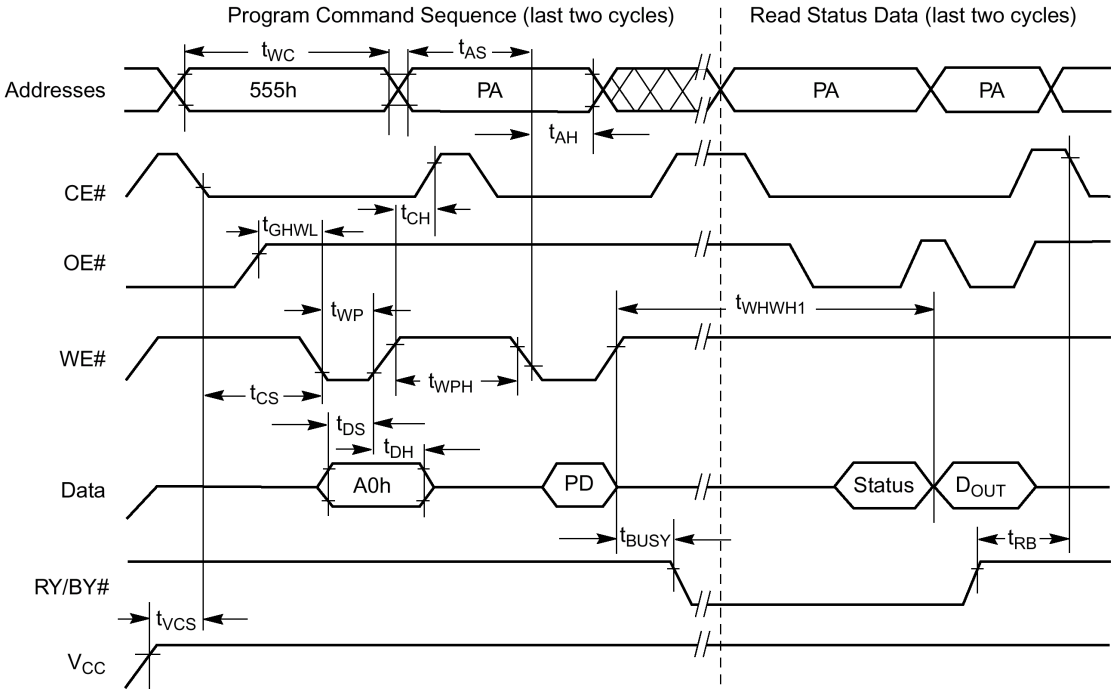
## u READ OPERATIONS TIMING



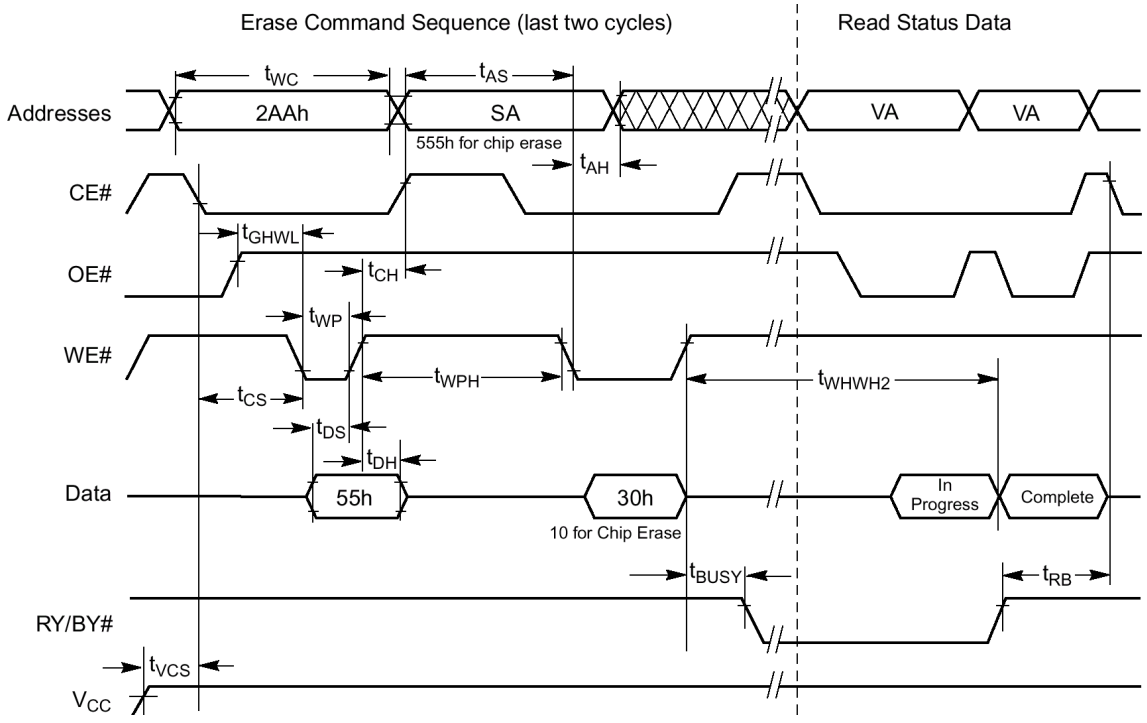

## u RESET TIMING



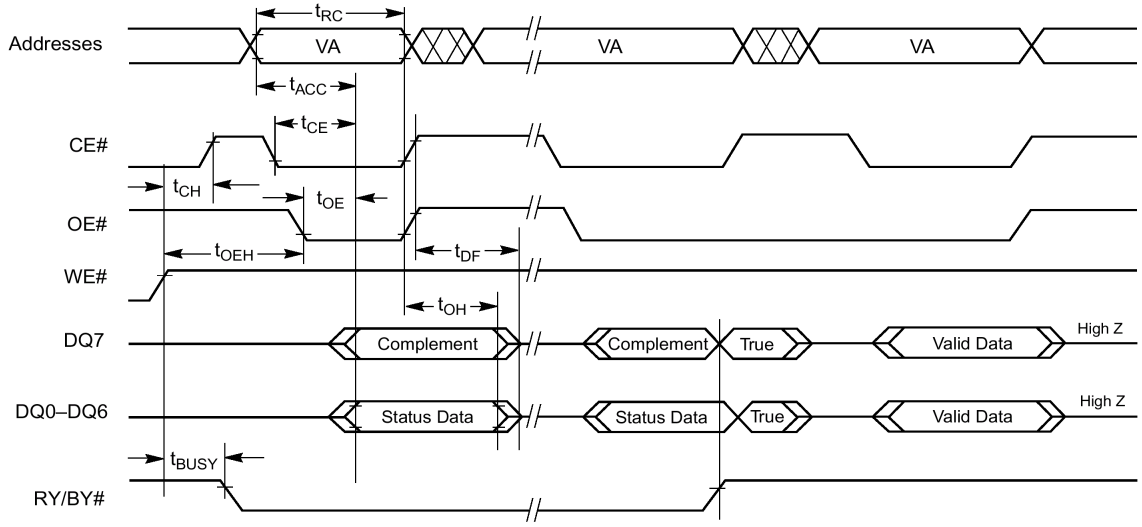
## u PROGRAM OPERATIONS TIMING



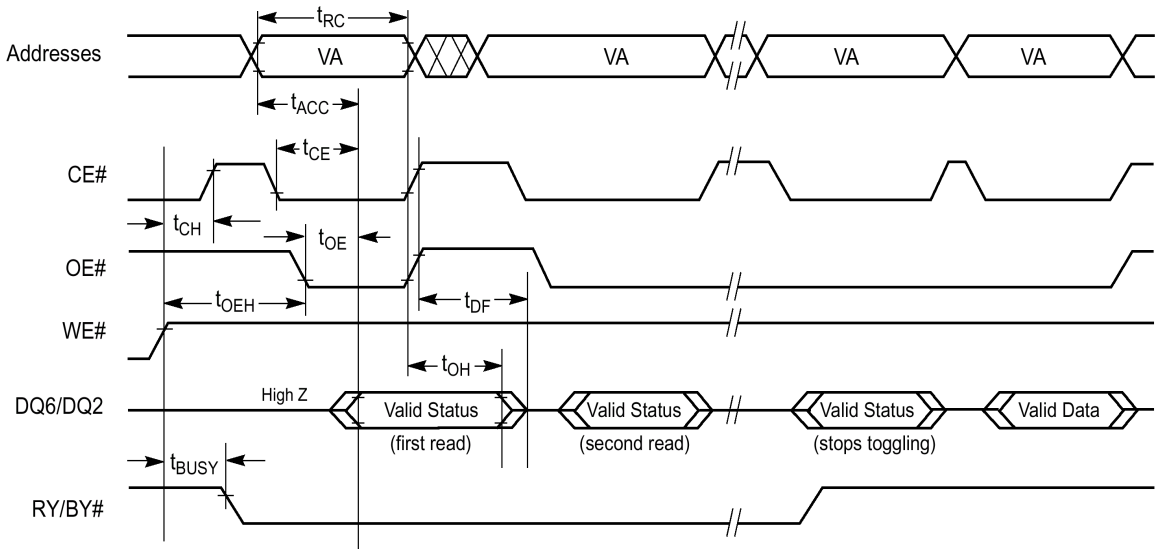

## u CHIP/SECTOR ERASE OPERATION TIMINGS



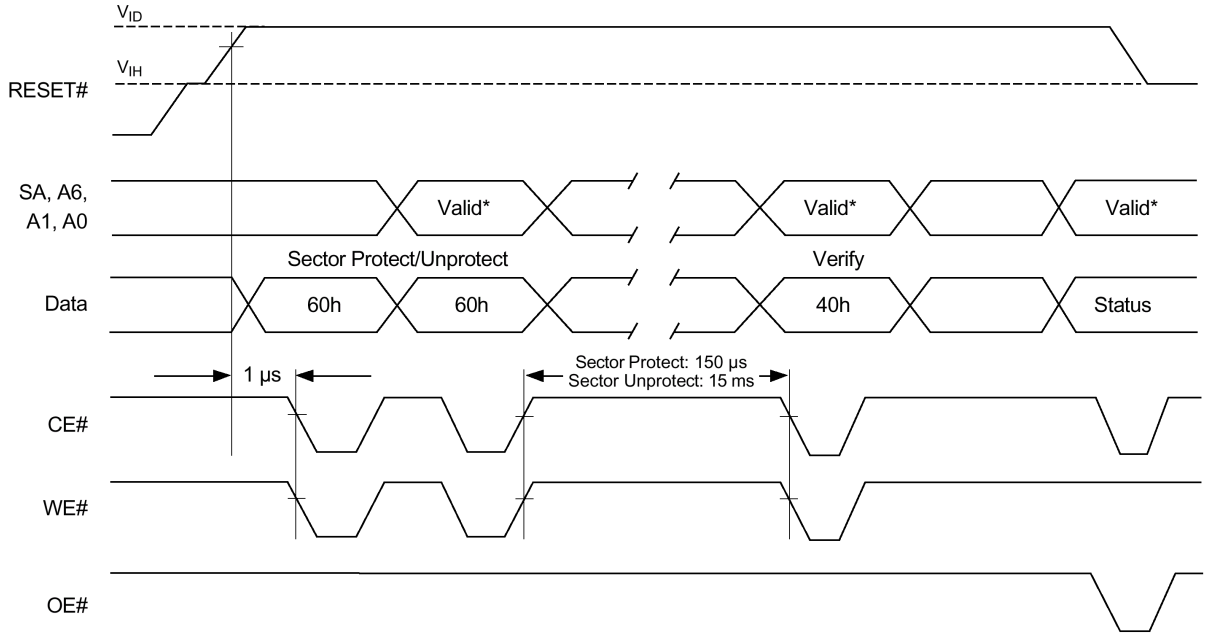
## u DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)



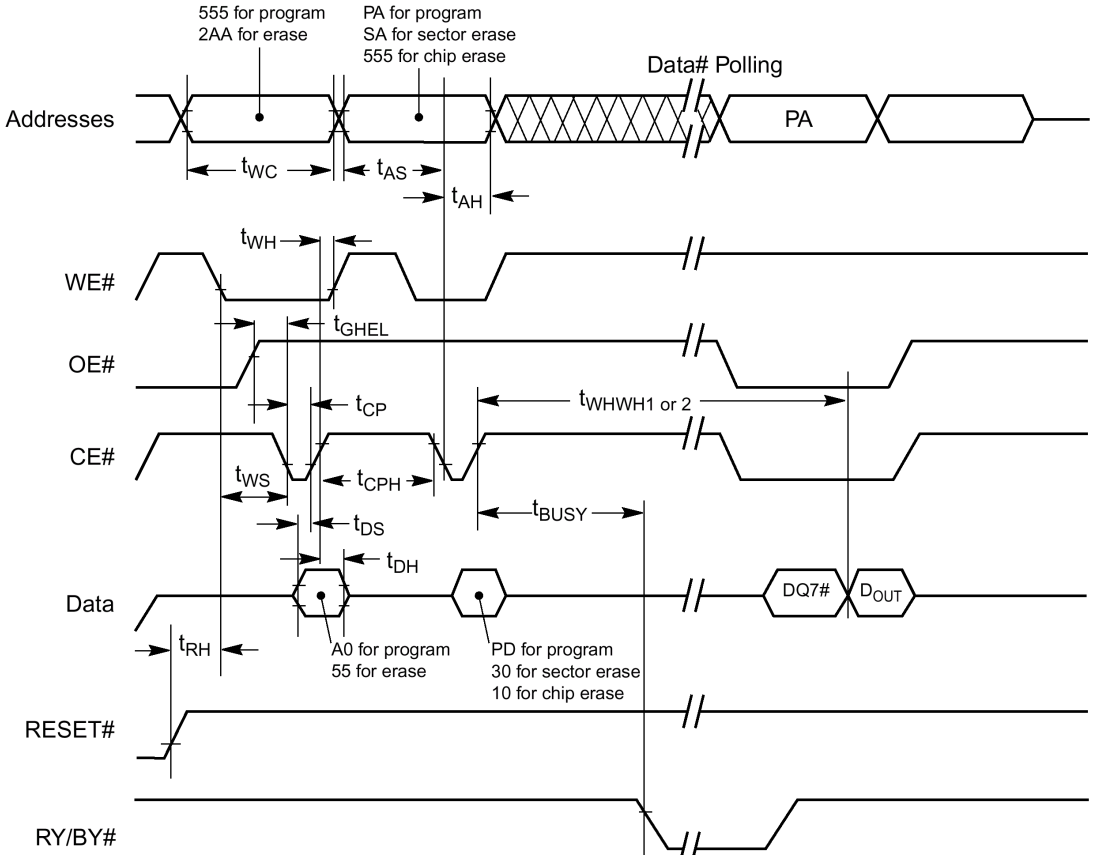

## u TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



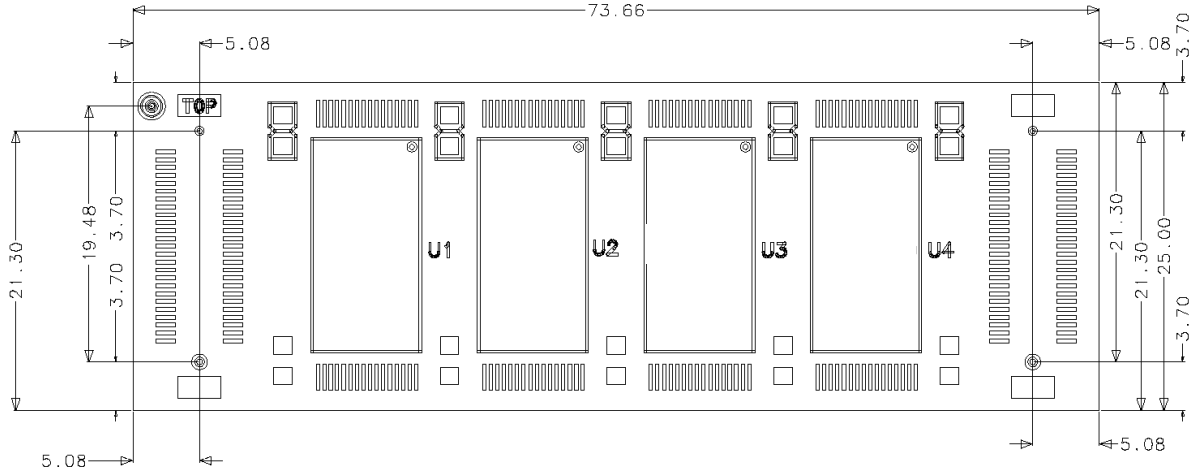
## u SECTOR PROTECT UNPROTECT TIMEING DIAGRAM




## u ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS



## PACKAGE DIMENSIONS




# ORDERING INFORMATION

| Part Number | Density | Org. | Package | Component Number | Vcc | SPEED |
|---|---|---|---|---|---|---|
| **HMF1M32F8-55** | 4MByte | 1Mx 32 | 100 Pin-SMM | 8EA | 5.0V | 55ns |
| **HMF1M32F8-70** | 4MByte | 1Mx 32 | 100 Pin-SMM | 8EA | 5.0V | 70ns |
| **HMF1M32F8-90** | 4MByte | 1Mx 32 | 100 Pin-SMM | 8EA | 5.0V | 90ns |
| **HMF1M32F8-120** | 4MByte | 1Mx 32 | 100 Pin-SMM | 8EA | 5.0V | 120ns |