ELPIDA

PRELIMINARY DATA SHEET

256MB Direct Rambus DRAM SO-RIMM™ Module

EBR25EC8ABSA (128M words × 18 bits)

Description

The Direct Rambus SO-RIMM module is a general-purpose high-performance memory module subsystem suitable for use in a broad range of applications including computer memory, mobile personal computers, networking systems and other applications where high bandwidth and low latency are required.

The EBR25EC8ABSA consists of 8 pieces of 288M Direct Rambus DRAM (Direct RDRAM) devices. These are extremely high-speed CMOS DRAMs organized as 16M words by 18 bits. The use of Rambus Signaling Level (RSL) technology permits 1066MHz or 800MHz transfer rates while using conventional system and board design technologies.

The architecture of the Direct RDRAM enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed memory transactions.

The separate control and data buses with independent row and column control yield over 95% bus efficiency. The Direct RDRAM's 32 banks support up to four simultaneous transactions per device.

Features

- 256MB Direct RDRAM storage and 256 banks total on module
- High speed 1066MHz/800MHz Direct RDRAM devices
- 160 edge connector pads with 0.65mm pad spacing
  - Module PCB size: 67.60mm × 31.25mm × 1.00mm
  - Gold plated edge connector pads contacts
- Serial Presence Detect (SPD) support
- Operates from a 2.5V supply
- Low power and power down self refresh modes
- Separate Row and Column buses for higher efficiency
- RDRAM®s uses Chip Scale Package (CSP)
  - FBGA package

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Ordering Information

Part number	Organization	I/O Freq. (MHz)	RAS access time (ns)	Package	Mounted devices
EBR25EC8ABSA-AD	128M x 18	1066	35	160 edge connector pads SO-RIMM with heat spreader	EDR2518ABSE
EBR25EC8ABSA-8C		800	40	Edge connector: Gold plated	

Module Pad Names

Pad	Signal Name	Pad	Signal Name	Pad	Signal Name	Pad	Signal Name
A1	GND	B1	GND	A41	NC	B41	NC
A2	LDQA8	B2	LDQA7	A42	VREF	B42	VREF
A3	GND	B3	GND	A43	SCL	B43	SA0
A4	LDQA6	B4	LDQA5	A44	VDD	B44	VDD
A5	GND	B5	GND	A45	SDA	B45	SA1
A6	LDQA4	B6	LDQA3	A46	VDD	B46	VDD
A7	GND	B7	GND	A47	SVDD	B47	SWP
A8	LDQA2	B8	LDQA1	A48	GND	B48	GND
A9	GND	B9	GND	A49	RSCK	B49	RCMD
A10	LDQA0	B10	LCFM	A50	GND	B50	GND
A11	GND	B11	GND	A51	RDQB8	B51	RDQB6
A12	LCTM	B12	LCFMN	A52	GND	B52	GND
A13	GND	B13	GND	A53	RDQB7	B53	RDQB4
A14	LCTMN	B14	LROW2	A54	GND	B54	GND
A15	GND	B15	GND	A55	RDQB5	B55	RDQB2
A16	LROW1	B16	LROW0	A56	GND	B56	GND
A17	GND	B17	GND	A57	RDQB3	B57	RDQB0
A18	LCOL4	B18	LCOL3	A58	GND	B58	GND
A19	GND	B19	GND	A59	RDQB1	B59	RCOL0
A20	LCOL2	B20	LCOL1	A60	GND	B60	GND
A21	GND	B21	GND	A61	RCOL1	B61	RCOL2
A22	LCOL0	B22	LDQB1	A62	GND	B62	GND
A23	GND	B23	GND	A63	RCOL3	B63	RCOL4
A24	LDQB0	B24	LDQB3	A64	GND	B64	GND
A25	GND	B25	GND	A65	RROW0	B65	RROW1
A26	LDQB2	B26	LDQB5	A66	GND	B66	GND
A27	GND	B27	GND	A67	RROW2	B67	RCTMN
A28	LDQB4	B28	LDQB7	A68	GND	B68	GND
A29	GND	B29	GND	A69	RCFMN	B69	RCTM
A30	LDQB6	B30	LDQB8	A70	GND	B70	GND
A31	GND	B31	GND	A71	RCFM	B71	RDQA0
A32	LSCK	B32	LCMD	A72	GND	B72	GND
A33	GND	B33	GND	A73	RDQA1	B73	RDQA2
A34	SOUT	B34	SIN	A74	GND	B74	GND
A35	VDD	B35	VDD	A75	RDQA3	B75	RDQA4
A36	NC	B36	NC	A76	GND	B76	GND

Pad	Signal Name	Pad	Signal Name
A37	GND	B37	GND
A38	NC	B38	NC
A39	VCMOS	B39	VCMOS
A40	NC	B40	NC

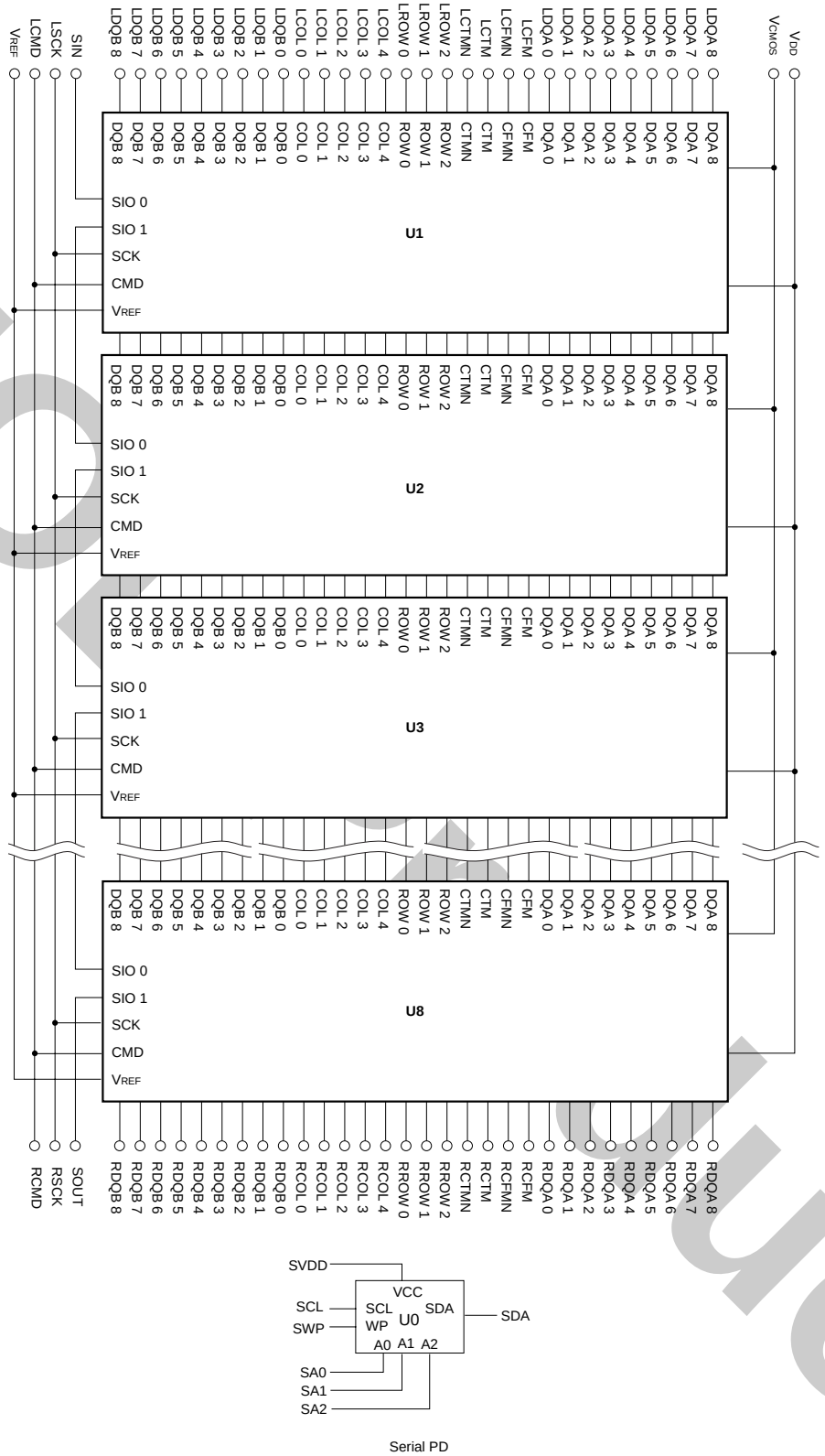
Pad	Signal Name	Pad	Signal Name
A77	RDQA5	B77	RDQA6
A78	GND	B78	GND
A79	RDQA7	B79	RDQA8
A80	GND	B80	GND

Module Connector Pad Description

Signal	Module Connector Pads	I/O	Type	Description
GND	A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29,A31, A33, A37, A48, A50, A52, A54,A56, A58, A60, A62, A64, A66, A68,A70, A72, A74, A76, A78, A80, B1,B3, B5, B7, B9, B11, B13, B15, B17,B19, B21, B23, B25, B27, B29, B31,B33, B37, B48, B50, B52, B54, B56, B58, B60, B62, B64, B66, B68, B70, B72, B74, B76, B78, B80	–	–	Ground reference for RDRAM core and interface.
LCFM	B10	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
LCFMN	B12	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
LCMD	B32	I	VCMOS	Serial Command used to read from and write to the control registers. Also used for power management.
LCOL4..LCOL0	A18, B18, A20, B20, A22	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
LCTM	A12	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
LCTMN	A14	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
LDQA8..LDQA0	A2, B2, A4, B4, A6, B6, A8, B8, A10	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM..
LDQB8..LDQB0	B30, B28, A30, B26, A28, B24, A26, B22, A24	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM.
LROW2..LROW0	B14, A16, B16	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.
LSCK	A32	I	VCMOS	Serial clock input. Clock source used to read from and write to the RDRAM control registers.
NC	A36, B36, A38, B38, A40, B40, A41, B41	–	–	These pads are not connected. These 8 connector pads are reserved for future use.
RCFM	A71	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
RCFMN	A69	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
RCMD	B49	I	VCMOS	Serial Command Input used to read from and write to the control registers. Also used for power management.
RCOL4..RCOL0	B63, A63, B61, A61, B59	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
RCTM	B69	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RCTMN	B67	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.

Signal	Module Connector Pads	I/O	Type	Description
RDQA8..RDQA0	B79, A79, B77, A77, B75, A75, B73, A73, B71	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM.
RDQB8..RDQB0	A51, A53, B51, A55, B53, A57, B55, A59, B57	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM.
RROW2..RROW0	A67, B65, A65	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.
RSCK	A49	I	VCMOS	Serial clock input. Clock source used to read from and write to the RDRAM control registers.
SA0	B43	I	SVDD	Serial Presence Detect Address 0.
SA1	A43	I	SVDD	Serial Presence Detect Address 1.
SCL	B45	I	SVDD	Serial Presence Detect Clock.
SDA	A45	I/O	SVDD	Serial Presence Detect Data (Open Collector I/O).
SIN	B34	I/O	VCMOS	Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module.
SOUT	A34	I/O	VCMOS	Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module.
SVDD	A47	—	—	SPD Voltage. Used for signals SCL, SDA, SWP, SA0, SA1 and SA2.
SWP	B47	I	SVDD	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
VCMOS	A39, B39	—	—	CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.
VDD	A35, B35, A44, B44, A46, B46	—	—	Supply voltage for the RDRAM core and interface logic.
VREF	A42, B42	—	—	Logic threshold reference voltage for RSL signals.

Block Diagram



Serial PD

Note: 1. Rambus Channel signals form a loop through the SO-RIMM module, with the exception of the SIO chain.
2. See Serial Presence Detection Specification for information on the SPD device and its contents.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	min.	max.	Unit
VI,ABS	Voltage applied to any RSL or CMOS signal pad with respect to GND	–0.3	VDD + 0.3	V
VDD,ABS	Voltage on VDD with respect to GND	–0.5	VDD + 1.0	V
TSTORE	Storage temperature	–50	+100	°C

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC Recommended Electrical Conditions

Symbol	Parameter and conditions	min.	max.	Unit
VDD	Supply voltage*[1]	2.50 – 0.13	2.50 + 0.13	V
VCMOS	CMOS I/O power supply at pad 2.5V controllers	2.50 – 0.13	2.50 + 0.25	V
	1.8V controllers	1.8 – 0.1	1.8 + 0.2	V
VREF	Reference voltage*[1]	1.4 – 0.2	1.4 + 0.2	V
VSPD	Serial Presence Detector- positive power supply	2.2	3.6	V

Note: 1. See Direct RDRAM datasheet for more details.

AC Electrical Specifications

Symbol	Parameter and Conditions	Grade	min.	typ.	max.	Unit
Z	Module Impedance of RSL signals		25.2	28.0	30.8	Ω
	Module Impedance of SCK and CMD signals		23.8	28.0	32.2	Ω
TPD	Average clock delay from finger to finger of all RSL clock nets (CTM, CTMN,CFM, and CFMN)		—	—	TBD	ns
ΔTPD	Propagation delay variation of RSL signals with respect to TPD *1, 2		TBD	—	TBD	ps
ΔTPD-CMOS	Propagation delay variation of SCK signal with respect to an average clock delay *1		TBD	—	TBD	ps
ΔTPD- SCK,CMD	Propagation delay variation of CMD signal with respect to SCK signal		TBD	—	TBD	ps
Vα/VIN	Attenuation Limit	-AD -8C	—	—	TBD	%
VXF/VIN	Forward crosstalk coefficient (300ps input rise time 20% - 80%)	-AD -8C	—	—	TBD	%
VXB/VIN	Backward crosstalk coefficient (300ps input rise time 20% - 80%)	-AD -8C	—	—	TBD	%
RDC	DC Resistance Limit	-AD -8C	—	—	TBD	Ω

Notes 1. TPD or Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).

2. If the SO-RIMM module meets the following specification, then it is compliant to the specification. If the SO-RIMM module does not meet these specifications, then the specification can be adjusted by the "Adjusted ΔTPD Specification" table.

Adjusted ΔTPD Specification

Symbol	Parameter and conditions	Adjusted min./max.	Absolute min.	Absolute max.	Unit
ΔTPD	Propagation delay variation of RSL signals with respect to TPD	+/– [17+(18*N*ΔZ0)] *1	TBD	TBD	ps

Note: 1 N = Number of RDRAM devices installed on the SO-RIMM module.

ΔZ0 = delta Z0% = (max. Z0 - min. Z0) / (min. Z0)

(max. Z0 and min. Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the module.)

SO-RIMM Module Current Profile

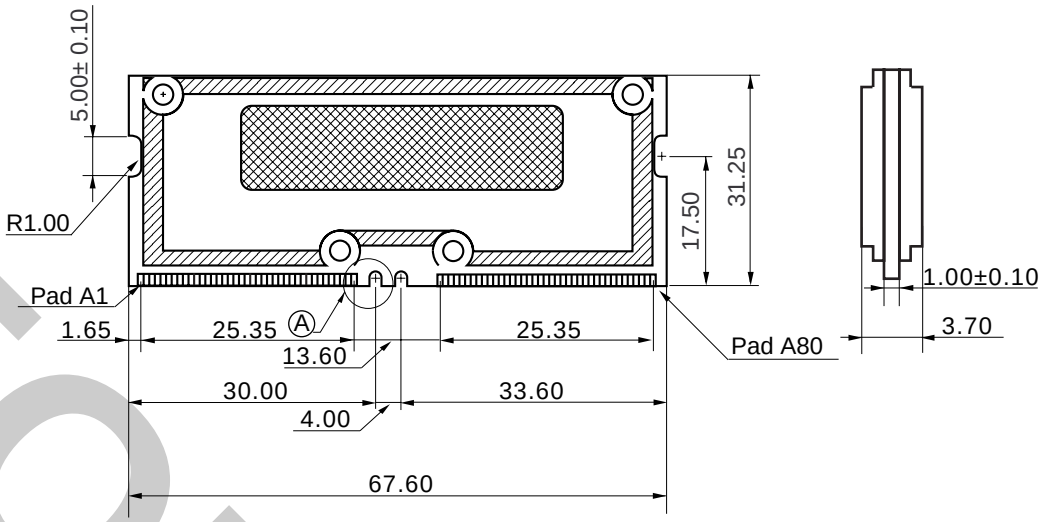
IDD	SO-RIMM module power conditions *1	Grade	max.	Unit
IDD1	One RDRAM device in Read *2, balance in NAP mode	-AD -8C	TBD	mA
IDD2	One RDRAM device in Read *2, balance in Standby mode	-AD -8C	TBD	mA
IDD3	One RDRAM device in Read *2, balance in Active mode	-AD -8C	TBD	mA
IDD4	One RDRAM device in Write, balance in NAP mode	-AD -8C	TBD	mA
IDD5	One RDRAM device in Write, balance in Standby mode	-AD -8C	TBD	mA
IDD6	One RDRAM device in Write, balance in Active mode	-AD -8C	TBD	mA

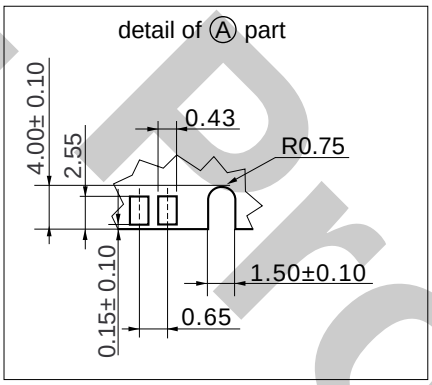
Notes: 1. Actual power will depend on individual RDRAM component specifications, memory controller and usage patterns. Power does not include Refresh Current.

2. I/O current is a function of the % of 1's, to add I/O power for 50 % 1's for a x18 need to add 276mA for the following: VDD = 2.5V, VTERM = 1.8V, VREF = 1.4V and VDIL = VREF – 0.5V.

Physical Outline

Unit: mm





Note: The dimensions without tolerance specification use the default tolerance of ± 0.13.

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CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.
In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.
Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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