ON Semiconductor®

6 and 8-Channel Low Capacitance ESD Protection Arrays

CM1213

Features

- 6 or 8 channels of ESD protection

  Note: For 1, 2, and 4 channel devices, see the CM1213A datasheet.
- Provides ESD protection to IEC61000-4-2 Level 4
  - ±8kV contact discharge
- Low channel input capacitance of 1.0pF typical
- Minimal capacitance change with temperature and voltage
- Channel input capacitance matching of 0.02pF typical is ideal for differential signals
- Mutual capacitance between signal pin and adjacent signal pin -0.11pF typical
- Zener diode protects supply rail and eliminates the need for external by-pass capacitors
- Each I/O pin can withstand over 1000 ESD strikes*
- Available in SOIC and MSOP, lead-free packaging

Applications

- USB2.0 ports at 480Mbps in desktop PCs, notebooks and peripherals
- IEEE1394 Firewire® ports at 400Mbps / 800Mbps
- DVI ports, HDMI ports in notebooks, set top boxes, digital TVs, LCD displays
- Serial ATA ports in desktop PCs and hard disk drives
- PCI Express ports
- General purpose high-speed data line ESD protection

Product Description

The CM1213 family of diode arrays has been designed to provide ESD protection for electronic components or sub-systems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the positive (V_P) or negative (V_N) supply rail. A Zener diode is embedded between V_P and V_N, offering two advantages. First, it protects the V_{CC} rail against ESD strikes, and second, it eliminates the need for a bypass capacitor that would otherwise be needed for absorbing positive ESD strikes to ground. The CM1213 will protect against ESD pulses up to ±8kV per the IEC 61000-4-2 standard.

These devices are particularly well-suited for protecting systems using high-speed ports such as USB2.0, IEEE1394 (Firewire®, iLink™), Serial ATA, DVI, HDMI and corresponding ports in removable storage, digital camcorders, DVD-RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

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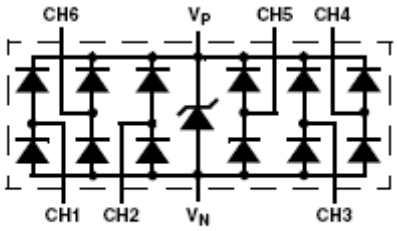
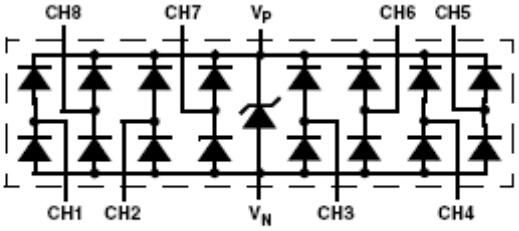
Publication Order Number:
CM1213/D

Block Diagram



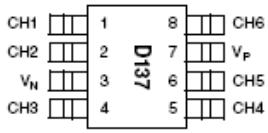
CM1213-06MR
CM1213-06SM



CM1213-08MR

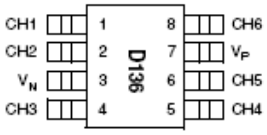
PACKAGE / PINOUT DIAGRAMS

Top View



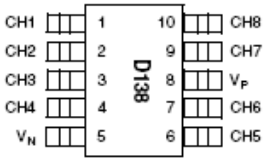
8-Lead MSOP-8

Top View



8-Lead SOIC-8

Top View



10-Lead MSOP-10

Note: These drawings are not to scale.

Pin Descriptions

PIN DESCRIPTIONS			
6-CHANNEL, 8-LEAD MSOP-8/SOIC-8 PACKAGES			
PIN	**NAME**	**TYPE**	**DESCRIPTION**
1	CH1	I/O	ESD Channel
2	CH2	I/O	ESD Channel
3	V_N	GND	Negative voltage supply rail
4	CH3	I/O	ESD Channel
5	CH4	I/O	ESD Channel
6	CH5	I/O	ESD Channel
7	V_P	PWR	Positive voltage supply rail
8	CH6	I/O	ESD Channel

PIN DESCRIPTIONS			
8-CHANNEL, 10-LEAD MSOP-10 PACKAGE			
PIN	**NAME**	**TYPE**	**DESCRIPTION**
1	CH1	I/O	ESD Channel
2	CH2	I/O	ESD Channel
3	CH3	I/O	ESD Channel
4	CH4	I/O	ESD Channel
5	V_N	GND	Negative voltage supply rail
6	CH5	I/O	ESD Channel
7	CH6	I/O	ESD Channel
8	V_P	PWR	Positive voltage supply rail
9	CH7	I/O	ESD Channel
10	CH8	I/O	ESD Channel

Ordering Information

PART NUMBERING INFORMATION				
			Lead-free Finish	
# of Channels	Leads	Package	Ordering Part Number[1]	Part Marking
6	8	SOIC-8	CM1213-06SM	D136
6	8	MSOP-8	CM1213-06MR	D137
8	10	MSOP-10	CM1213-08MR	D138

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
Operating Supply Voltage (V_P - V_N)	6.0	V
Operating Temperature Range	-40 to +85	℃
Storage Temperature Range	-65 to +150	℃
DC Voltage at any channel input	(V_N - 0.5) to (V_P + 0.5)	V

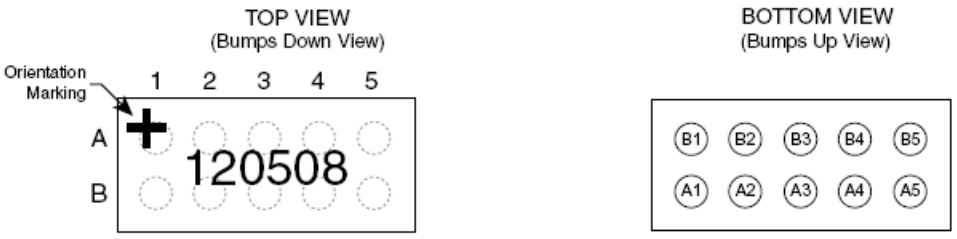
STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
Operating Temperature Range	-40 to +85	℃
Package Power Rating		
MSOP-8 Package (CM1213-06MR)	400	mW
MSOP-10 Package (CM1213-08MR)	400	mW
SOIC-8 Package (CM1213-06SM)	600	mW

ELECTRICAL OPERATING CHARACTERISTICS(SEE NOTE 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_P	Operating Supply Voltage (V_P-V_N)			3.3	5.5	V
I_P	Operating Supply Current	(V_P-V_N)=3.3V			8.0	µA
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 8mA; T_A=25°C	 0.60 0.60	 0.80 0.80	 0.95 0.95	 V V
I_{LEAK}	Channel Leakage Current	T_A=25°C; V_P=5V, V_N=0V		±0.1	±1.0	µA
C_{IN}	Channel Input Capacitance	At 1 MHz, V_P=3.3V, V_N=0V, V_{IN}=1.65V;		1.0	1.5	pF
ΔC_{IN}	Channel Input Capacitance Matching	At 1 MHz, V_P=3.3V, V_N=0V, V_{IN}=1.65V;		0.02		pF
C_{MUTUAL}	Mutual Capacitance between signal pin and adjacent signal pin	At 1 MHz, V_P=3.3V, V_N=0V, V_{IN}=1.65V;		0.11		pF
V_{ESD}	ESD Protection Peak Discharge Voltage at any channel input, in system Contact discharge per IEC 61000-4-2 standard	Notes 3 and 4; T_A=25°C	±8			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	T_A=25°C, I_{PP} = 1A, t_P = 8/20uS; Note 4		 +8.8 -1.4		 V V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	I_{PP} = 1A, t_P = 8/20uS Any I/O pin to Ground; Note 4		 0.7 0.4		 Ω Ω

Note 1: All parameters specified at T_A = -40°C to +85°C unless otherwise noted.
Note 2: Human Body Model per MIL-STD-883, Method 3015, $C_{Discharge}$ = 100pF, $R_{Discharge}$ = 1.5KΩ, V_P = 3.3V, V_N grounded.
Note 3: Standard IEC 61000-4-2 with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330Ω, V_P = 3.3V, V_N grounded.
Note 4: These measurements performed with no external capacitor on V_P (V_P floating).

PACKAGE / PINOUT DIAGRAMS



CM1205-08
10-bump CSP Package

Notes:
1) These drawings are not to scale.

Ordering Information

PART NUMBERING INFORMATION			
Bumps	**Package**	**Ordering Part Number[1]**	**Part Marking**
10	CSP	CM1205-08CP	120508

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
Storage Temperature Range	-65 to +150	℃

STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
Operating Temperature Range	-40 to +85	℃

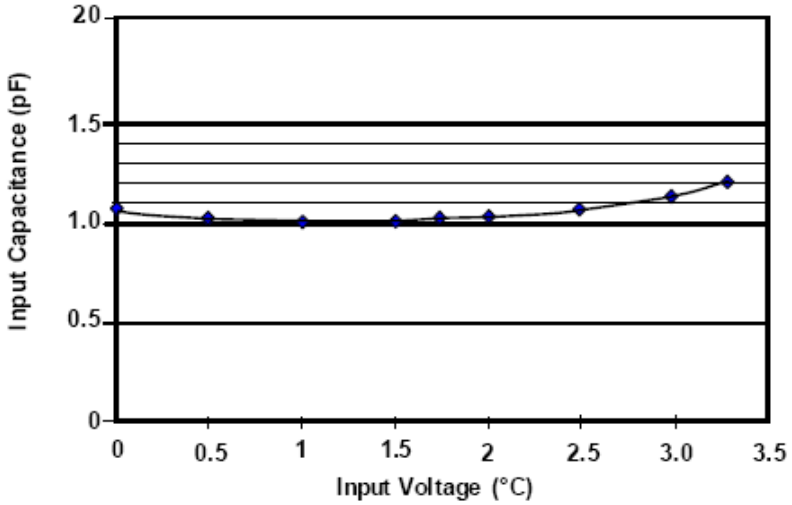
Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS[1]						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{REV}	Reverse Standoff Voltage	I_{DIODE}=10µA		6.0		V
I_{LEAK}	Leakage Current	V_{IN}=3.3V DC			100	nA
V_{SIG}	Signal Clamp Voltage Positive Clamp Negative Clamp	I_{LOAD} = 10mA	 5.6 -1.2	 6.8 -0.8	 8.0 -0.4	 V V
V_{ESD}	In-system ESD Withstand Voltage a) Human Body Model, MIL-STD-883, Method 3015 b) Contact Discharge per IEC 61000-4-2 Level 4	Notes 2 & 3	 ±30 ±25			 kV kV
V_{CL}	Clamping Voltage during ESD Discharge MIL-STD-883 (Method 3015), 8kV Positive Transients Negative Transients	Notes 2 & 3		 +12 -8		 V V
C	Channel Capacitance	At 2.5V DC, *f* = 1MHz, Note 3		39	47	pF

Note 1: T_A=25°C unless otherwise specified. GND in this document refers to the lower supply voltage.
Note 2: ESD applied to channel pins with respect to GND, one at a time. All other channels are open. All GND pins tied to ground.
Note 3: These parameters are guaranteed by design and characterization.

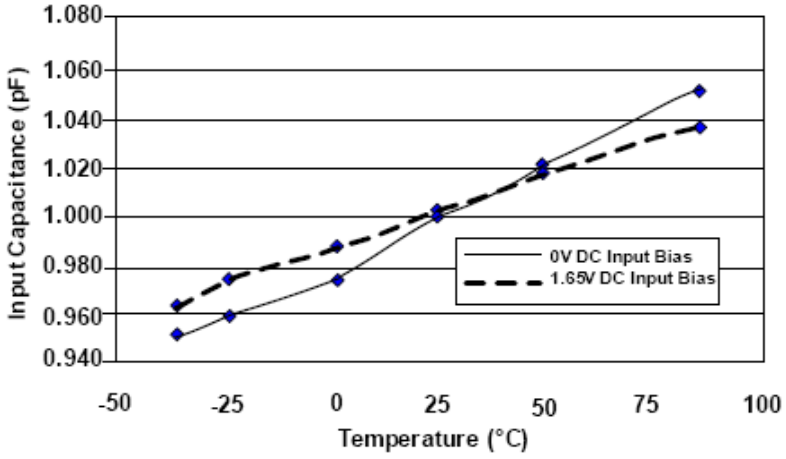
Performance Information

Input Channel Capacitance Performance Curves



Typical Variation of C_{IN} vs. V_{IN}

(f=1MHz, V_P = 3.3V, V_N = 0V, 0.1 µF chip capacitor between V_P and V_N, 25°C)



Typical Variation of C_{IN} vs. Temp

(f=1MHz, V_{IN}=30mV, V_P = 3.3V, V_N = 0V,
0.1 µF chip capacitor between V_P and V_N)

Performance Information (Cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)

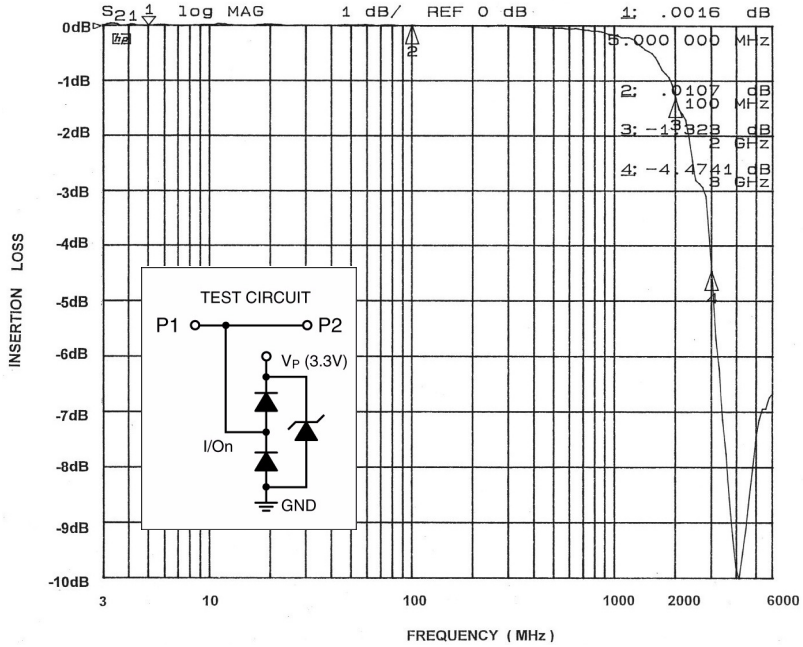


Figure 1. Insertion Loss (S21) VS. Frequency (0V DC Bias, V_P=3.3V)

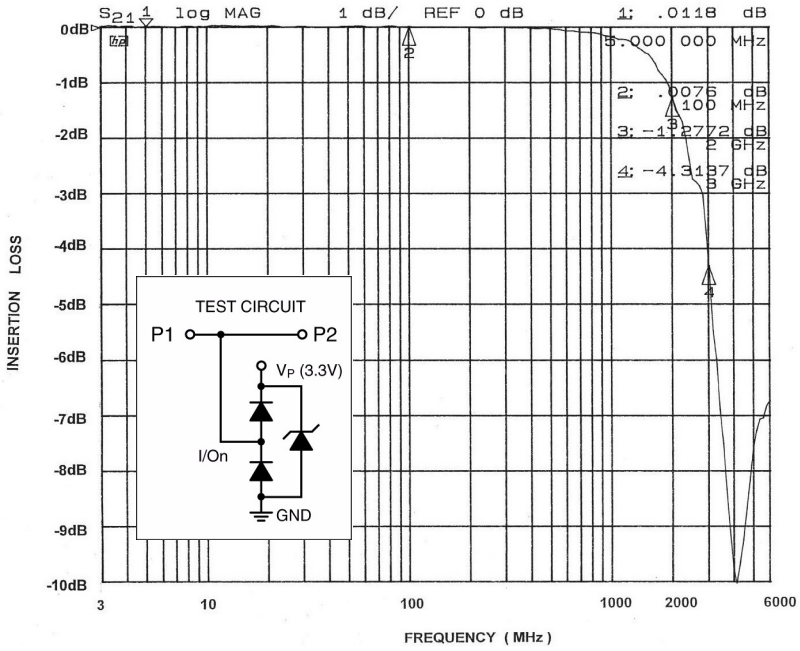


Figure 2. Insertion Loss (S21) VS. Frequency (2.5V DC Bias, V_P=3.3V)

Application Information

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Application of Positive ESD Pulse between Input Channel and Ground, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L_1 and L_2. The voltage V_{CL} on the line being protected is:

$$V_{CL} = \text{Fwd voltage drop of } D_1 + V_{SUPPLY} + L_1 \times d(I_{ESD}) / dt + L_2 \times d(I_{ESD}) / dt$$

where I_{ESD} is the ESD current pulse, and V_{SUPPLY} is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1ns. Here $d(I_{ESD})/dt$ can be approximated by $\Delta I_{ESD}/\Delta t$, or $30/(1x10^{-9})$. So just 10nH of series inductance (L_1 and L_2 combined) will lead to a 300V increment in V_{CL}!

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

The CM1213 has an integrated Zener diode between V_P and V_N. This greatly reduces the effect of supply rail inductance L_2 on V_{CL} by clamping V_P at the breakdown voltage of the Zener diode. However, for the lowest possible V_{CL}, especially when V_P is biased at a voltage significantly below the Zener breakdown voltage, it is recommended that a 0.22µF ceramic chip capacitor be connected between V_P and the ground plane.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

Additional Information

See also California Micro Devices Application Note AP209, “Design Considerations for ESD Protection”, in the Applications section at www.calmicro.com.

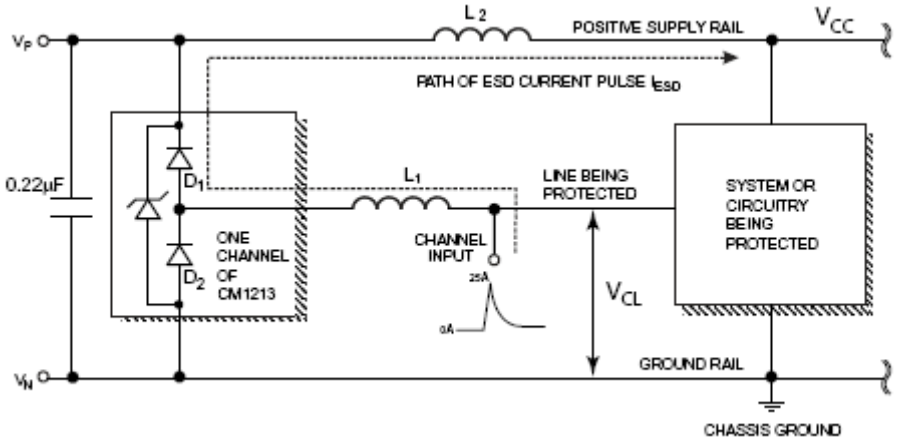


Figure 3. Application of Positive ESD Pulse between Input Channel and Ground

Mechanical Details

The CM1213 is available in MSOP-8, SOIC-8, and MSOP-10 packages with a lead-free finishing.

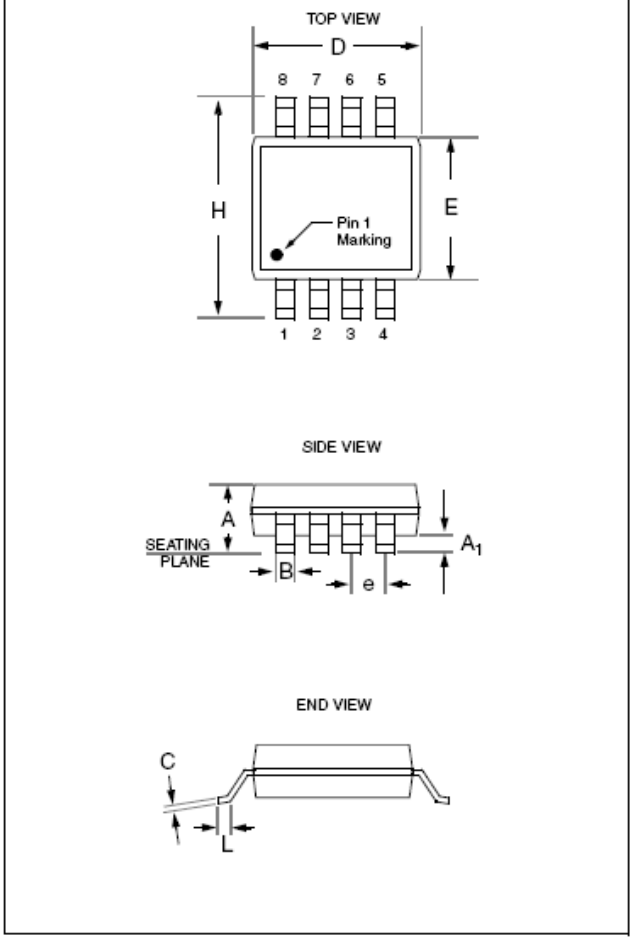
SOIC-8 Mechanical Specifications

The CM1213-06SM is supplied in an 8-pin SOIC package. Dimensions are presented below.

PACKAGE DIMENSIONS				
Package	SOIC			
Pins	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.19	0.150	0.165
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tape and reel	2500 pieces			
Controlling dimension: inches				

*

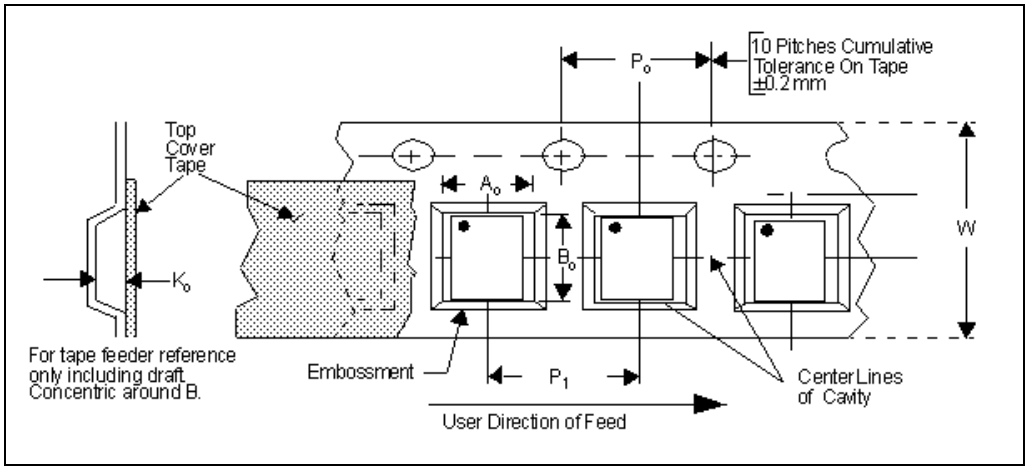
Mechanical Package Diagrams



Package Dimensions for SOIC-8

Tape and Reel Specifications

PART NUMBER	PACKAGE SIZE (mm)	POCKET SIZE (mm) B_0 X A_0 X K_0	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	P_0	P_1
CM1213-06SM	4.90 X 6.00 X 1.55	5.30 X 6.50 X 2.10	12mm	330mm (13")	2500	4mm	8mm

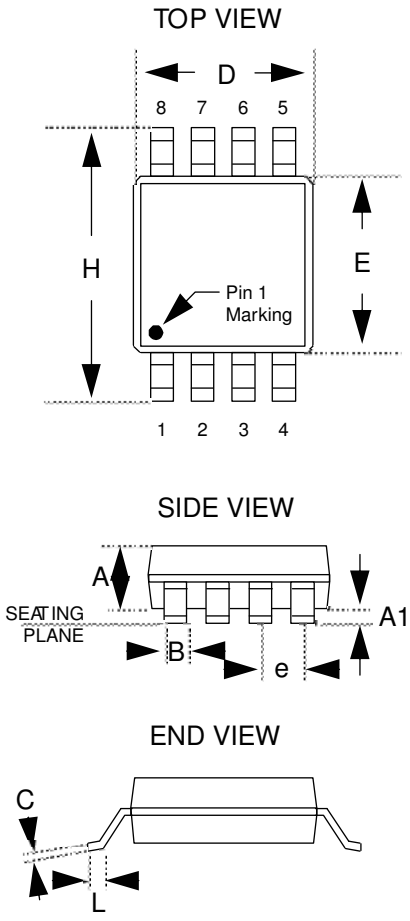


Mechanical Details (Cont'd)

MSOP-8 Mechanical Specifications:

The CM1213-06MR is supplied in an 8-pin MSOP package. Dimensions are presented below.

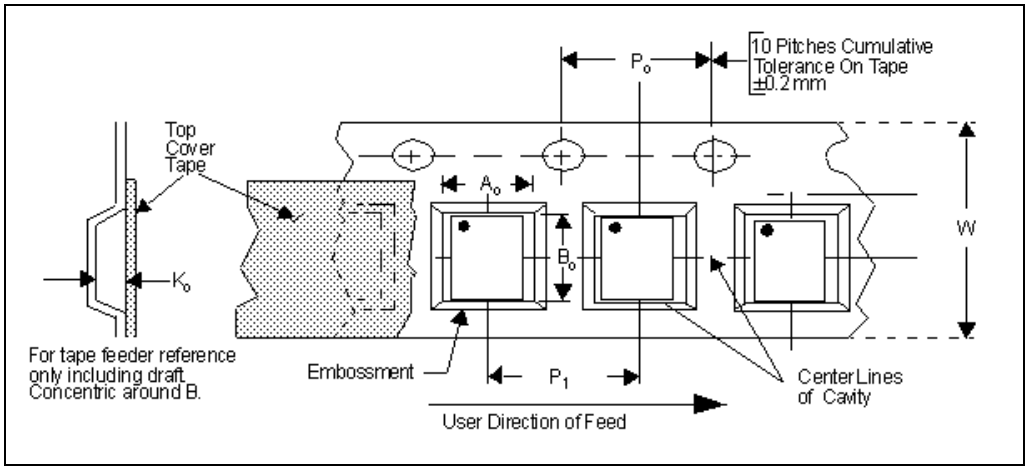
PACKAGE DIMENSIONS				
Package	MSOP			
Pins	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	0.75	0.95	0.030	0.037
A1	0.05	0.15	0.002	0.006
B	0.28	0.38	0.011	0.015
C	0.13	0.23	0.005	0.009
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.65 BSC		0.026 BSC	
H	4.90 BSC		0.193 BSC	
L	0.40	0.70	0.016	0.028
# per tape and reel	4000 pieces			
Controlling dimension: millimeters				



Package Dimensions for MSOP-8

Tape and Reel Specifications

PART NUMBER	PACKAGE SIZE (mm)	POCKET SIZE (mm) B_0 X A_0 X K_0	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	P_0	P_1
CM1213-06MR	3.00 X 3.00 X 0.85	3.3 X 5.3 X1.3	12mm	330mm (13")	4000	4mm	8mm



Mechanical Details (cont'd)

MSOP-10 Mechanical Specifications

The CM1213-08MR is supplied in a 10-pin MSOP package. Dimensions are presented below.

PACKAGE DIMENSIONS				
Package	MSOP			
Pins	10			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	0.75	0.95	0.028	0.038
A1	0.05	0.15	0.002	0.006
B	0.17	0.33	0.007	0.013
C	0.13	0.23	0.005	0.009
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.50 BSC		0.0196 BSC	
H	4.90 BSC		0.193 BSC	
L	0.40	0.70	0.0137	0.029
# per tape and reel	4000			
Controlling dimension: inches				

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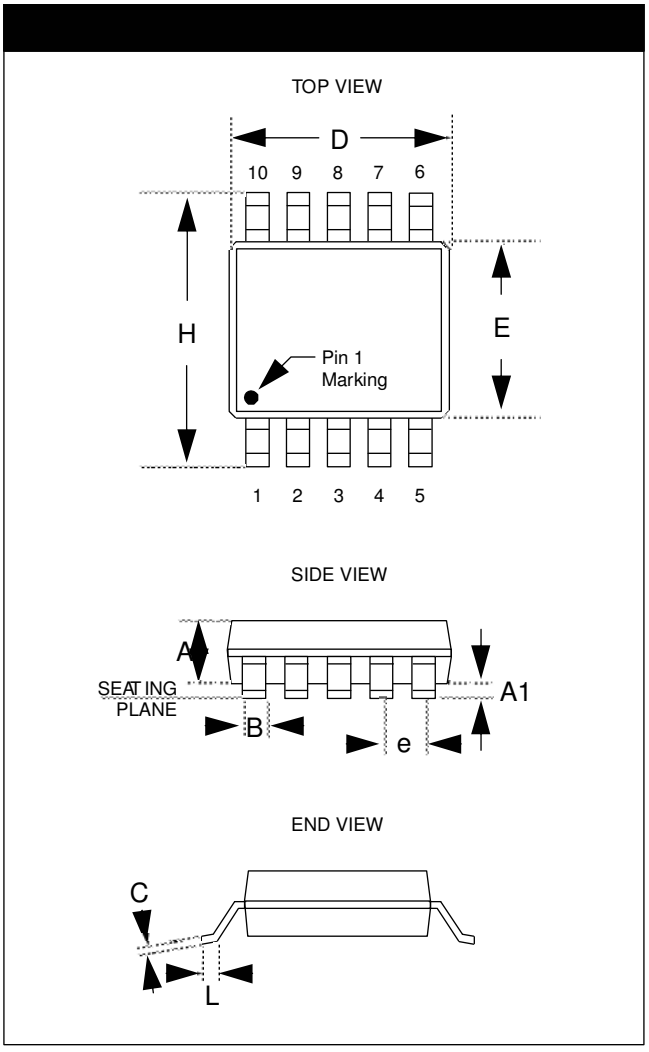
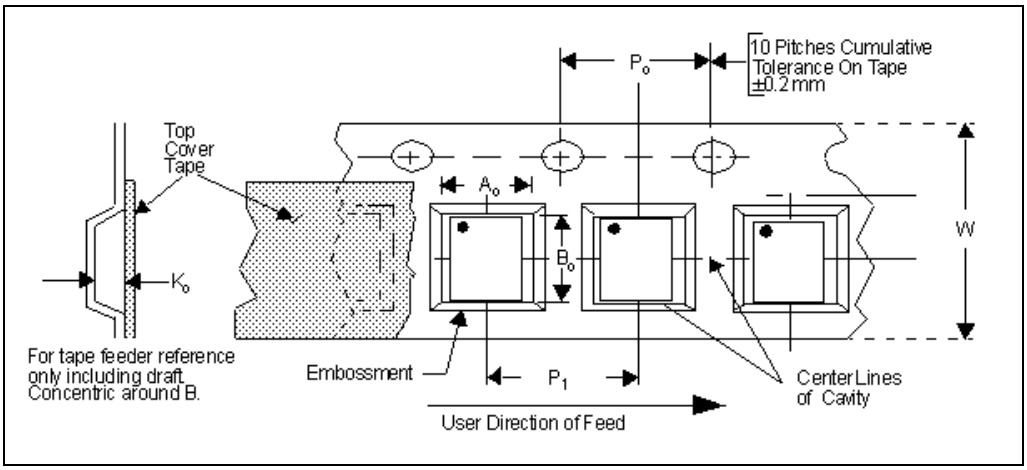


Package Dimensions for MSOP-10

Tape and Reel Specifications

PART NUMBER	PACKAGE SIZE (mm)	POCKET SIZE (mm) B_0 X A_0 X K_0	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	P_0	P_1
CM1213-08MR	3.00 X 3.00 X 0.85	3.3 X 5.3 X1.3	12mm	330mm (13")	4000	4mm	8mm



PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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Email: **orderlit@onsemi.com**

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Japan Customer Focus Center
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