

High-performance Clock Generator Series

3ch Clock Generator for Digital Cameras

BU2394KN, BU2396KN



●Description

These clock generators are an IC generating three types of clocks – CCD, USB, and VIDEO clocks – necessary for digital still camera systems and digital video camera systems, with a single chip through making use of the PLL technology. Generating these clocks with a single chip allows for the simplification of clock system, little space occupancy, reduction in the number of components used for mobile camera equipment, which is becoming increasingly downsized and less costly.

●Features

- 1) Connecting a crystal oscillator generates multiple clock signals with a built-in PLL.
- 2) The CCD clock provides switching selection outputs.
- 3) Providing the output of low period-jitter clock.
- 4) Incorporating compact package VQFN20 most suited for mobile devices.
- 5) Single power supply of 3.3 V

●Applications

Generation of clocks used in digital still camera and digital video camera systems

●Lineup

	BU2394KN	BU2396KN
Supply voltage	3.0V~3.6V	3.0V~3.6V
Operating temperature range	-5~+70°C	-5~+70°C
Reference input clock	14.318182MHz 28.636363MHz	12.000000MHz
Output CCD clock	135.000000MHz 110.000000MHz 108.000000MHz 98.181818MHz	36.000000MHz 30.000000MHz 24.000000MHz
Output USB clock	48.008022MHz	12.000000MHz
Output VIDEO clock	14.318182MHz 17.734450MHz	27.000000MHz

●Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
Supply voltage	VDD	-0.5~7.0	V
Input voltage	VIN	-0.5~VDD+0.5	V
Storage Temperature range	Tstg	-30~125	°C
Power dissipation	PD	530	mW

*1 Operating temperature is not guaranteed.

*2 In the case of exceeding Ta = 25°C, 5.3mW should be reduced per 1°C.

*3 The radiation-resistance design is not carried out.

*4 Power dissipation is measured when the IC is mounted to the printed circuit board.

● Recommended Operating Range

Parameter	Symbol	Limit	Unit
Supply voltage	VDD	3.0~3.6	V
Input H voltage	VINH	0.8VDD~VDD	V
Input L voltage	VINL	0.0~0.2VDD	V
Operating temperature	Topr	-5~70	°C
Output load	CL	15(MAX)	pF

● Electrical characteristics

BU2394KN(VDD=3.3V, Ta=25°C, unless otherwise specified.)

XTAL_SEL=H with crystal oscillator at a frequency of 28.636363 MHz, while XTAL_SEL=L at 14.318182 MHz

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
【Action circuit current】	IDD	—	45	60	mA	At no load
【Output H voltage】						
CLK1	VOH1	VDD-0.5	VDD-0.2	—	V	When current load = - 9.0mA
CLK2	VOH2	VDD-0.5	VDD-0.2	—	V	When current load = - 7.0mA
REF_CLK	VOHR	VDD-0.5	VDD-0.2	—	V	When current load = - 4.5mA
【Output L voltage】						
CLK1	VOL1	—	0.2	0.5	V	When current load =11mA
CLK2	VOL2	—	0.2	0.5	V	When current load =9.0mA
REF_CLK	VOLR	—	0.2	0.5	V	When current load =5.5mA
【Pull-Up resistance value】						
FS1, FS2, FS3, CLK2ON, XTAL_SEL	Pull-Up R	125	250	375	Ω	Specified by a current value running when a voltage of 0V is applied to a measuring pin. (R=VDD/I)
【Output frequency】						
CLK1 FS2:H FS3:H	Fclk1-1	—	135.000000	—	MHz	XTAL×(1188/63)/2
CLK1 FS2:H FS3:L	Fclk1-2	—	108.000000	—	MHz	XTAL×(1056/70)/2
CLK1 FS2:L FS3:L	Fclk1-3	—	98.181818	—	MHz	XTAL×(864/63)/2
CLK1 FS2:L FS3:H	Fclk1-4	—	110.000000	—	MHz	XTAL×(968/63)/2
CLK2	Fclk2-2	—	48.008022	—	MHz	XTAL×(228/17)/4
REF_CLK FS1:H	Fref1-1	—	14.318182	—	MHz	XTAL Output
REF_CLK FS1:L	Fref1-2	—	17.734450	—	MHz	XTAL×(706/57)/10
【Output waveform】						
Duty1 100MHz or less	Duty1	45	50	55	%	Measured at a voltage of 1/2 of VDD
Duty2 100MHz or more	Duty2	—	50	—	%	Measured at a voltage of 1/2 of VDD
Rise time	Tr	—	2.5	—	nsec	Period of transition time required for the output to reach 80% from 20% of VDD.
Fall time	Tf	—	2.5	—	nsec	Period of transition time required for the output to reach 20% from 80% of VDD.
【Jitter】						
Period-Jitter 1σ	P-J1σ	—	30	—	psec	※1
Period-Jitter MIN-MAX	P-J MIN-MAX	—	180	—	psec	※2
【Output Lock-Time】	Tlock	—	—	1	msec	※3

Note) The output frequency is determined by the arithmetic (frequency division) expression of a frequency input to XTALIN. If the input frequency is set to values shown below, the output frequency will be as listed above.

When XTAL_SEL is set to H, the input frequency on XTALIN will be 28.636363 MHz.

When XTAL_SEL is set to L, the input frequency on XTALIN will be 14.318182 MHz.

BU2396N(VDD=3.3V, Ta=25°C, Crystal =12.000000MHz, unless otherwise specified.)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
【Action circuit current】	IDD	—	23	35	mA	At no load
【Output H voltage】						
TGCLK	VOHT	VDD-0.5	—	—	V	When current load =-5.0mA
VCLK	VOHV	VDD-0.5	—	—	V	When current load =-5.0mA
UCLK	VOHU	VDD-0.5	—	—	V	When current load =-5.0mA
【Output L voltage】						
TGCLK	VOLT	—	—	0.5	V	When current load =5.0mA
VCLK	VOLV	—	—	0.5	V	When current load =5.0mA
UCLK	VOLU	—	—	0.5	V	When current load =5.0mA
【Pull-Up resistance value】						
TGCLK_SEL1 TGCLK_SEL2	Pull-up R	125	250	375	K Ω	Specified by a current value running when a voltage of 0V is applied to a measuring pin. (R=VDD/I)
【Pull-Down resistance value】						
TGCLK_EN, TGCLK_PD VCLK_EN, VCLK_PD	Pull-down R	25	50	75	K Ω	Specified by a current value running when a VDD is applied to a measuring pin. (R=VDD/I)
【Output frequency】						
TGCLK SEL1:L SEL2:L	TGCLK1		24.000000		MHz	XTAL \times (48/4)/6
TGCLK SEL1:L SEL2:H	TGCLK2		30.000000		MHz	XTAL \times (60/4)/6
TGCLK SEL1:H	TGCLK3		36.000000		MHz	XTAL \times (54/3)/6
VCLK	VCLK		27.000000		MHz	XTAL \times (54/3)/8
UCLK	UCLK		12.000000		MHz	XTAL output
【Output waveform】						
Duty	Duty	45	50	55	%	Measured at a voltage of 1/2 of VDD
Rise time	Tr		2.0		nsec	Period of transition time required for the output to reach 80% from 20% of VDD.
Fall time	Tf		2.0		nsec	Period of transition time required for the output to reach 20% from 80% of VDD.
【Jitter】						
Period-Jitter 1 σ	P-J1 σ		50		psec	※1
Period-Jitter MIN-MAX	P-J MIN-MAX		300		psec	※2
【Output Lock-Time】	Tlock			1	msec	※3

Note) The output frequency is determined by the arithmetic (frequency division) expression of a frequency input to XTALIN.

If the input frequency is set to 12.000000MHz, the output frequency will be as listed above.

Common to BU2394KN, BU2396KN

※1 Period-Jitter 1 σ

This parameter represents standard deviation (=1 σ) on cycle distribution data at the time when the output clock cycles are sampled 1000 times consecutively with the TDS7104 Digital Phosphor Oscilloscope of Tektronix Japan, Ltd.

※2 Period-Jitter MIN-MAX

This parameter represents a maximum distribution width on cycle distribution data at the time when the output clock cycles are sampled 1000 times consecutively with the TDS7104 Digital Phosphor Oscilloscope of Tektronix Japan, Ltd.

※3 Output Lock-Time

The Lock-Time represents elapsed time after power supply turns ON to reach a 3.0V voltage, after the system is switched from Power-Down state to normal operation state, or after the output frequency is switched, until it is stabilized at a specified frequency, respectively.

●Reference data (BU2394KN basic data)

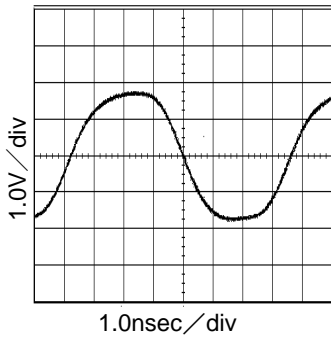


Fig.1 135MHz output wave
At VDD=3.3V and CL=15pF

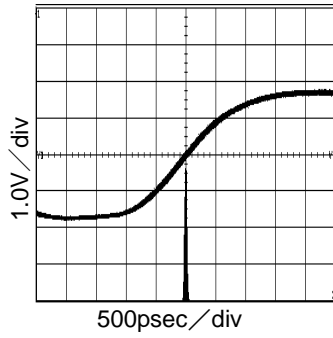


Fig.2 135MHz Period-Jitter
At VDD=3.3V and CL=15pF

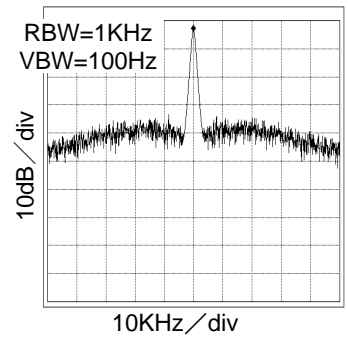


Fig.3 135MHz Spectrum
At VDD=3.3V and CL=15pF

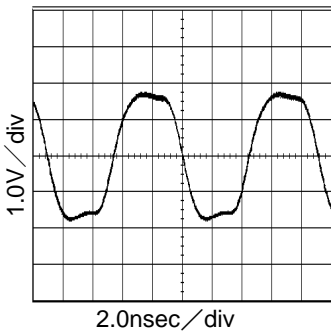


Fig.4 110MHz output wave
At VDD=3.3V and CL=15pF

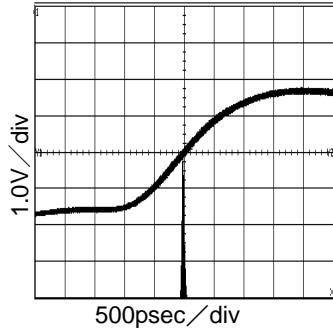


Fig.5 110MHz Period-Jitter
At VDD=3.3V and CL=15pF

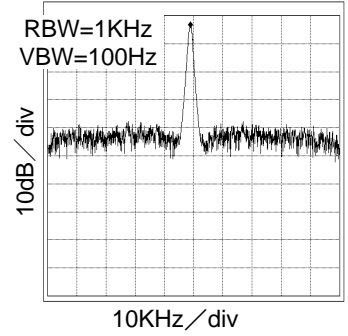


Fig.6 110MHz Spectrum
At VDD=3.3V and CL=15pF

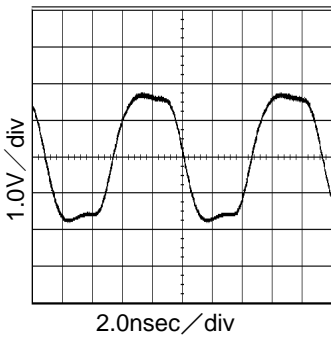


Fig.7 108MHz output wave
At VDD=3.3V and CL=15pF

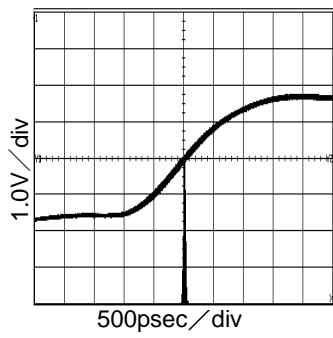


Fig.8 108MHz Period-Jitter
At VDD=3.3V and CL=15pF

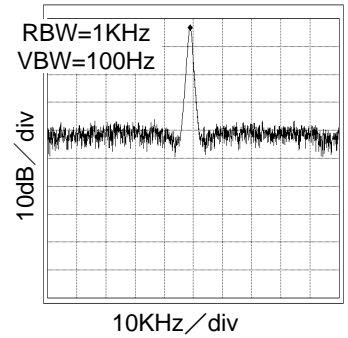


Fig.9 108MHz Spectrum
At VDD=3.3V and CL=15pF

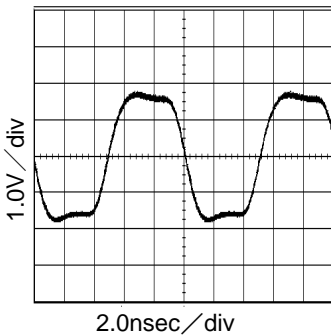


Fig.10 98MHz output wave
At VDD=3.3V and CL=15pF

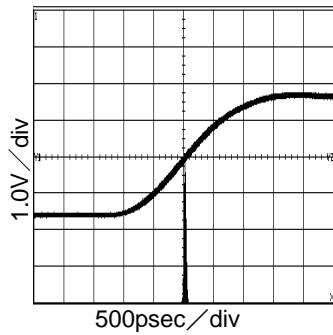


Fig.11 98MHz Period-Jitter
At VDD=3.3V and CL=15pF

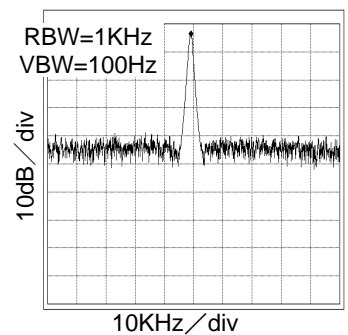


Fig.12 98MHz Spectrum
At VDD=3.3V and CL=15pF

●Reference data (BU2394KN basic data)

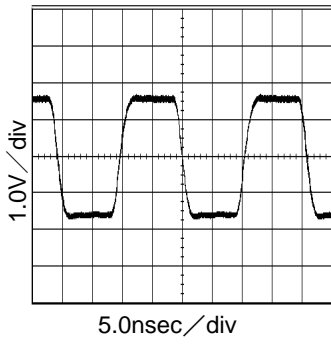


Fig.13 48MHz output wave
At VDD=3.3V and CL=15pF

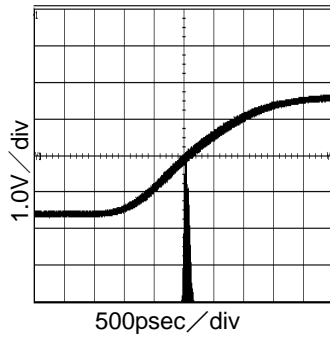


Fig.14 48MHz Period-Jitter
At VDD=3.3V and CL=15pF

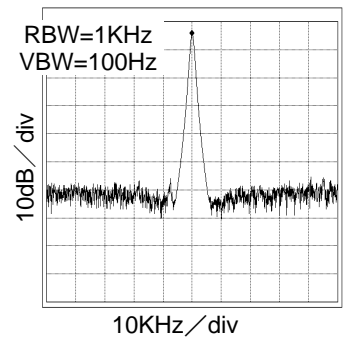


Fig.15 48MHz Spectrum
At VDD=3.3V and CL=15pF

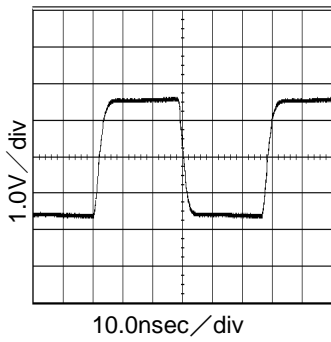


Fig.16 17.7MHz output wave
At VDD=3.3V and CL=15pF

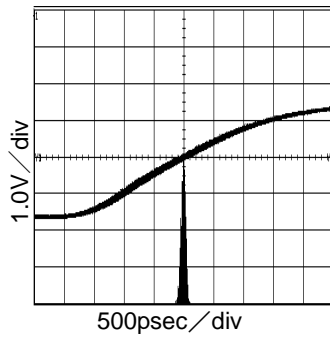


Fig.17 17.7MHz Period-Jitter
At VDD=3.3V and CL=15pF

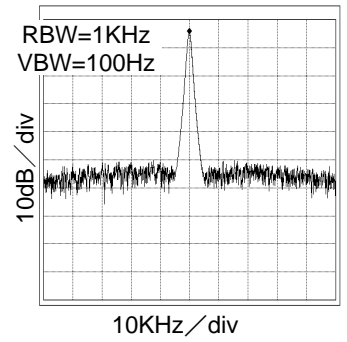


Fig.18 17.7MHz Spectrum
At VDD=3.3V and CL=15pF

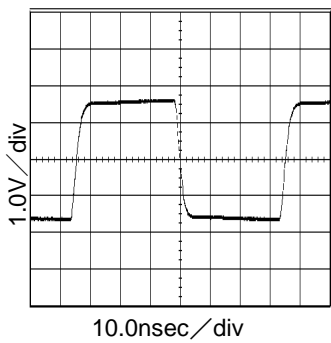


Fig.19 14.3MHz output wave
At VDD=3.3V and CL=15pF

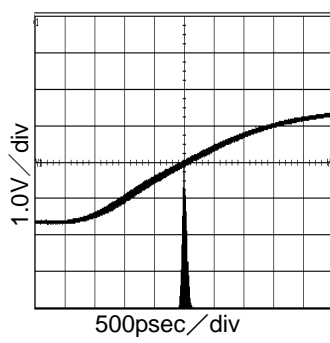


Fig.20 14.3MHz Period-Jitter
At VDD=3.3V and CL=15pF

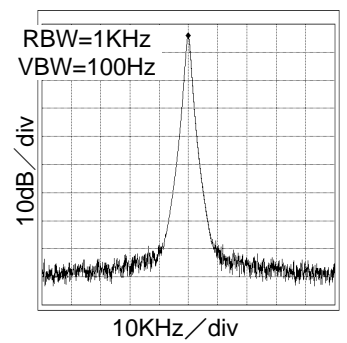
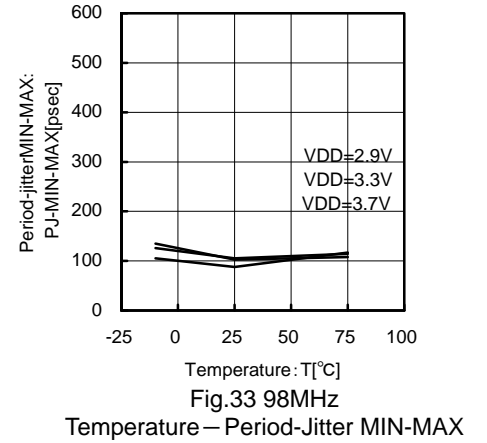
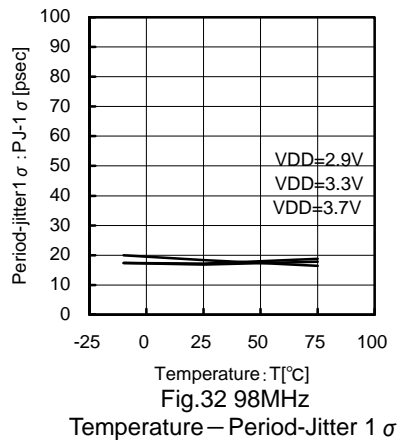
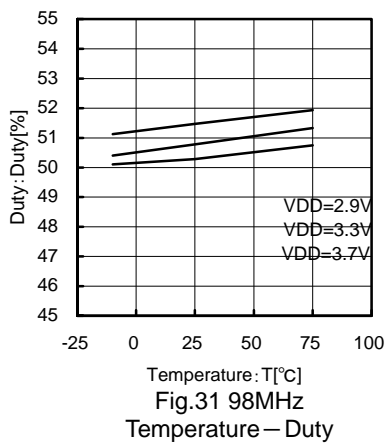
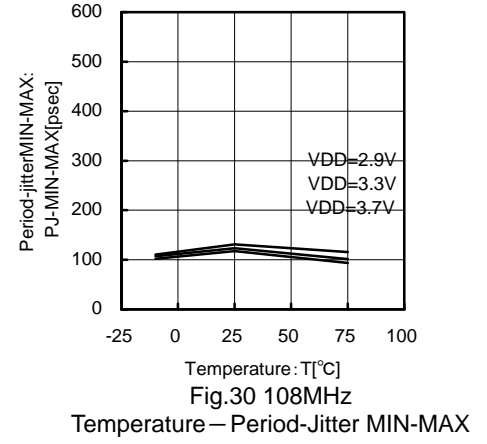
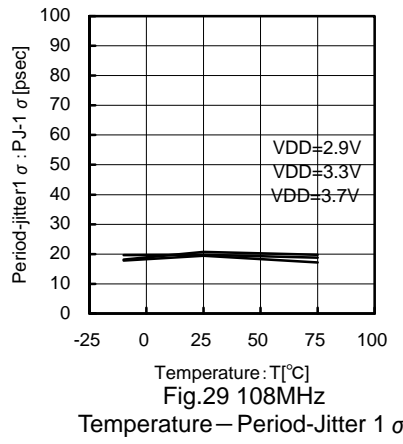
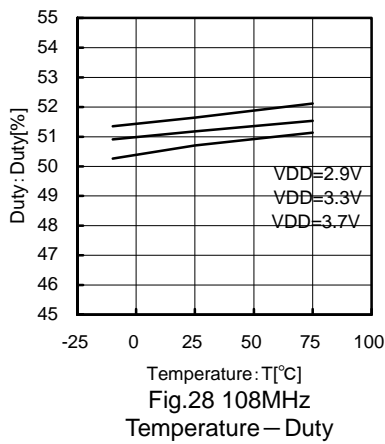
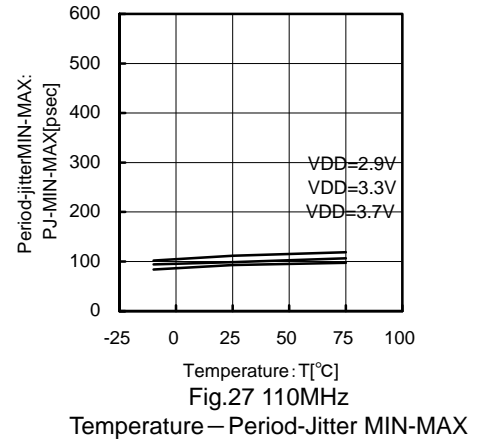
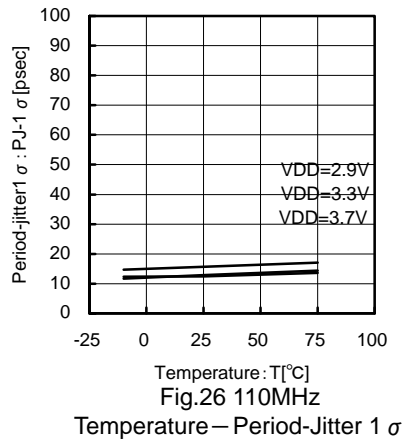
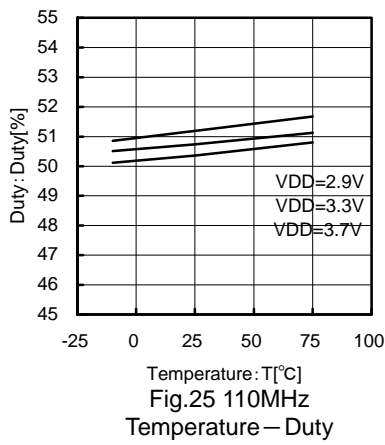
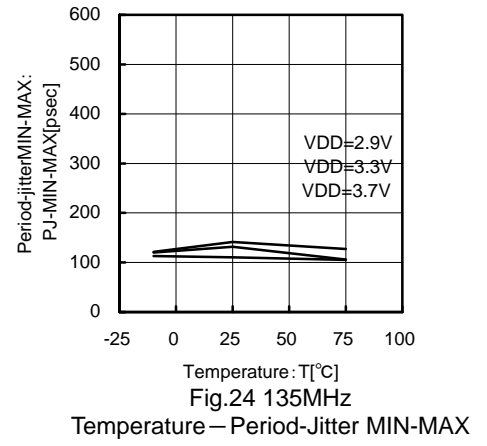
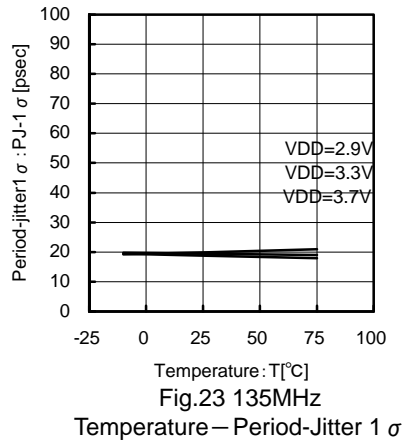
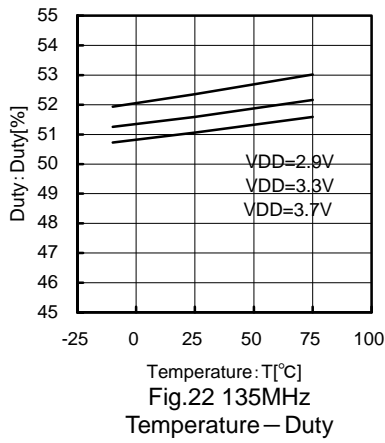
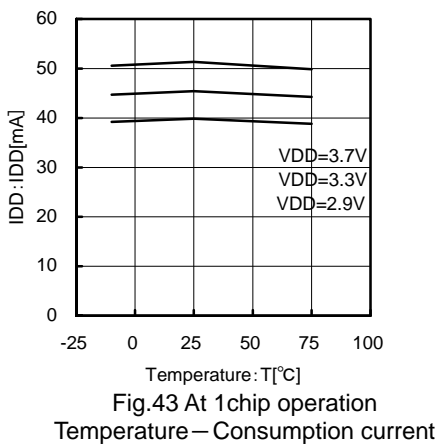
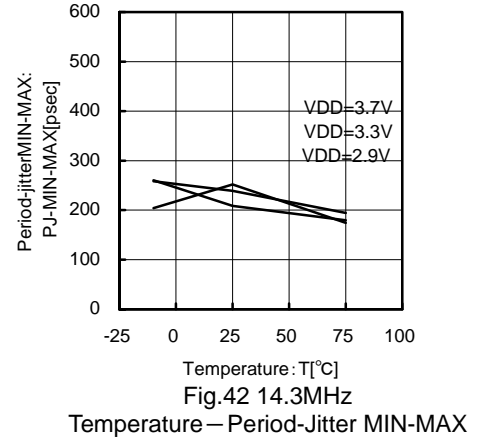
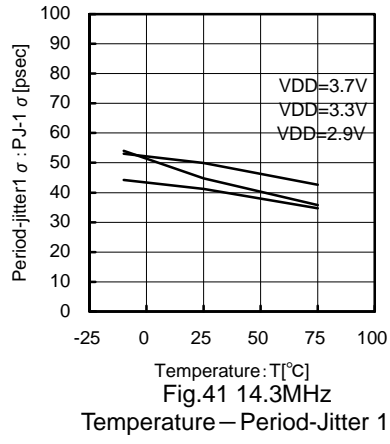
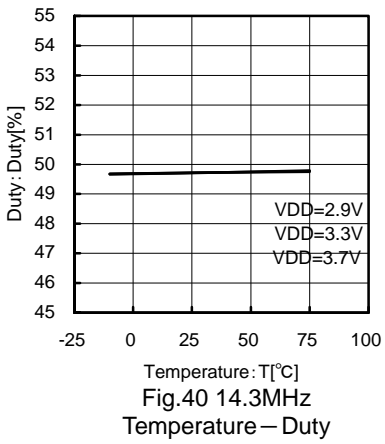
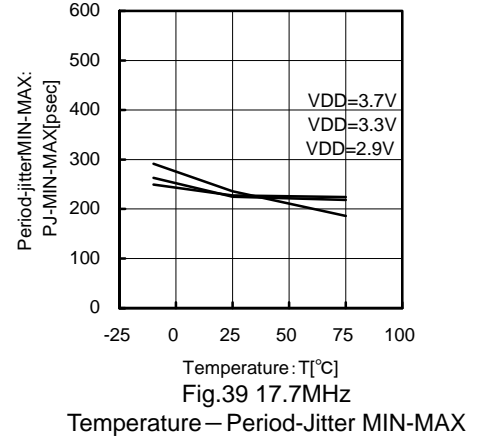
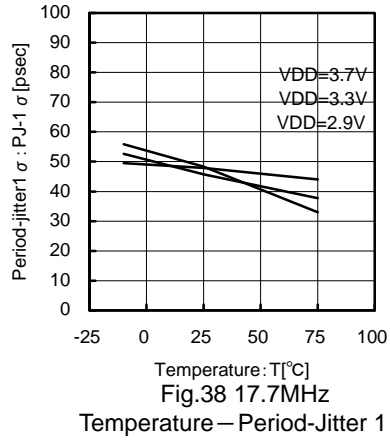
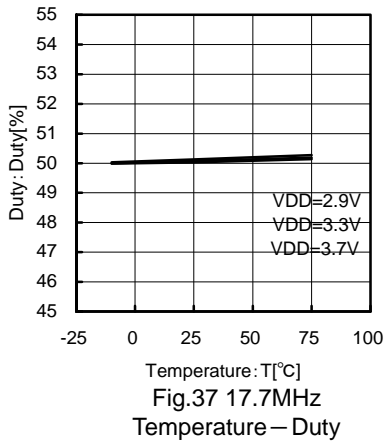
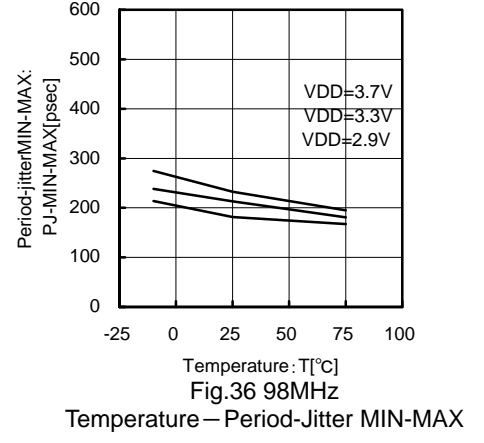
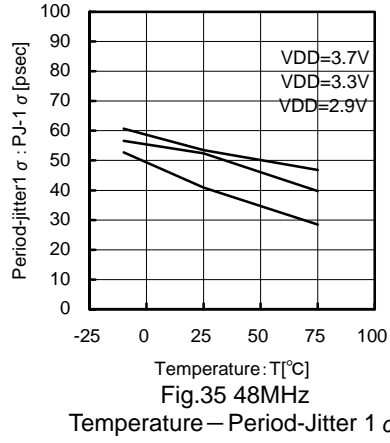
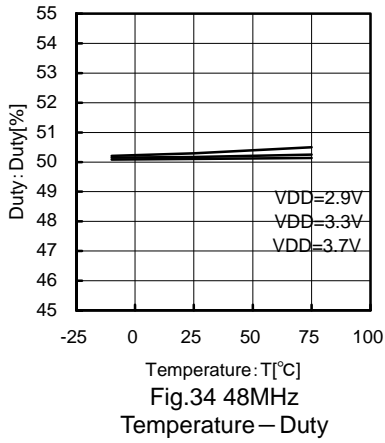


Fig.21 14.3MHz Spectrum
At VDD=3.3V and CL=15pF

● Reference data (BU2394KN Temperature and Supply voltage variations data)



● Reference data (BU2394KN Temperature and Supply voltage variations data)



●Reference data (BU2396KN basic data)

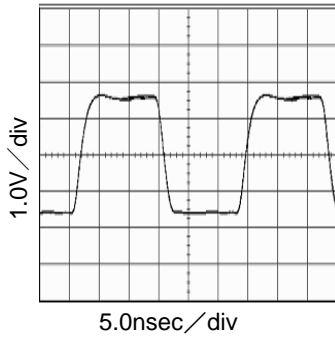


Fig.44 36MHz output waveform
At VDD=3.3V and CL=15pF

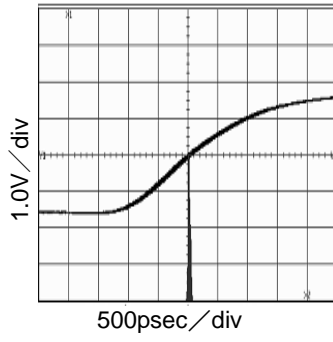


Fig.45 136MHz Period-Jitter
At VDD=3.3V and CL=15pF

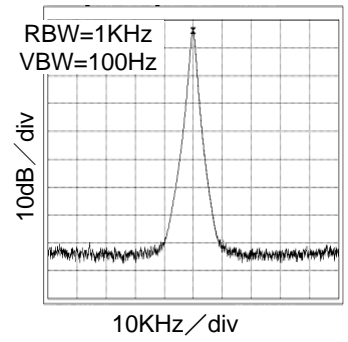


Fig.46 36MHz Spectrum
At VDD=3.3V and CL=15pF

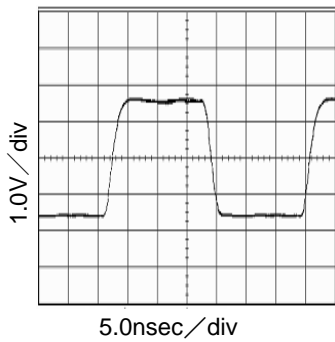


Fig.47 30MHz output waveform
At VDD=3.3V and CL=15pF

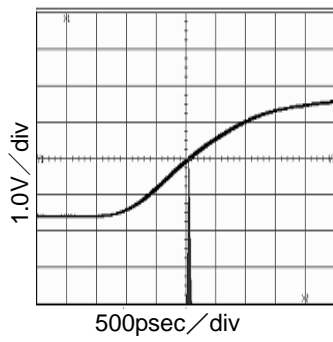


Fig.48 30MHz Period-Jitter
At VDD=3.3V and CL=15pF

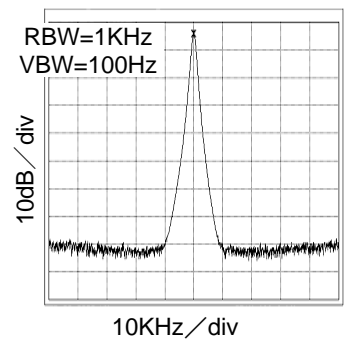


Fig.49 30MHz Spectrum
At VDD=3.3V and CL=15pF

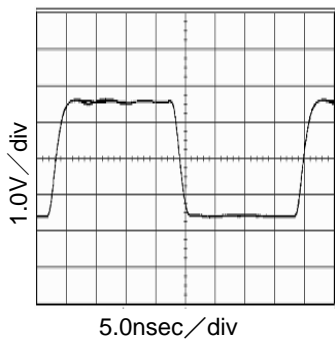


Fig.50 24MHz output waveform
At VDD=3.3V and CL=15pF

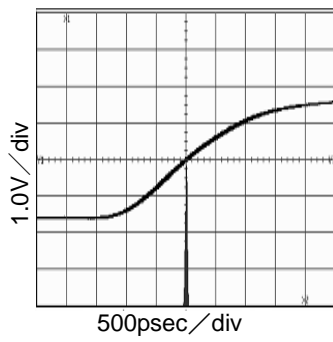


Fig.51 24MHz Period-Jitter
At VDD=3.3V and CL=15pF

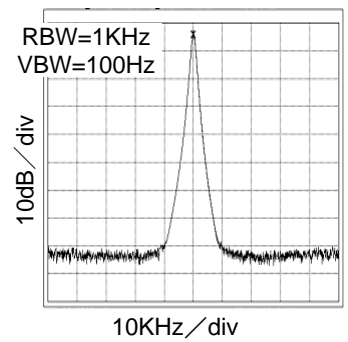


Fig.52 24MHz Spectrum
At VDD=3.3V and CL=15pF

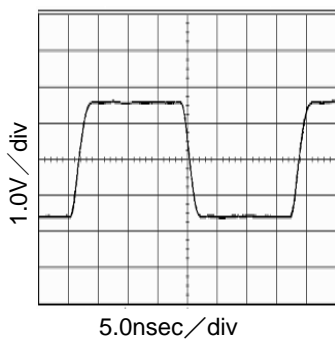


Fig.53 27MHz output waveform
At VDD=3.3V and CL=15pF

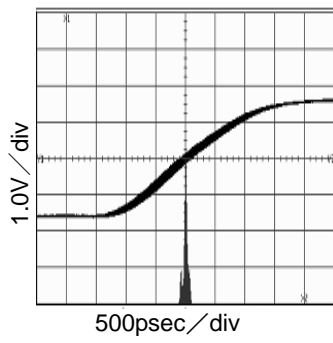


Fig.54 27MHz Period-Jitter
At VDD=3.3V and CL=15pF

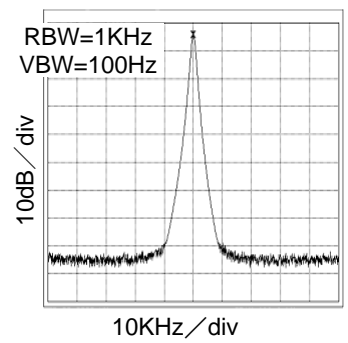


Fig.55 27MHz Spectrum
At VDD=3.3V and CL=15pF

●Reference data (BU2396KN basic data)

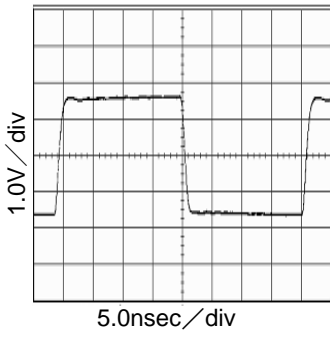


Fig.56 12MHz output waveform
At VDD=3.3V and CL=15pF

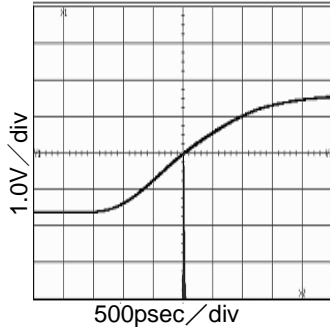


Fig.57 12MHz Period-Jitter
At VDD=3.3V and CL=15pF

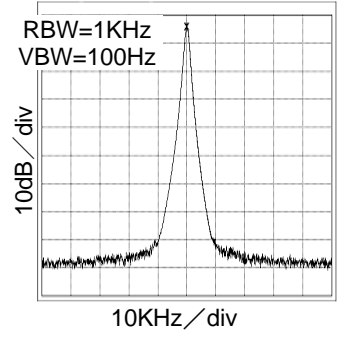


Fig.58 12MHz Spectrum
At VDD=3.3V and CL=15pF

●Reference data (BU2396KN Temperature and Supply voltage variations data)

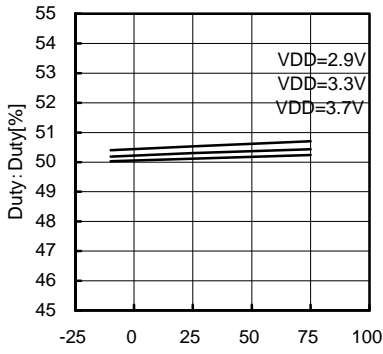


Fig.59 36MHz
Temperature - Duty

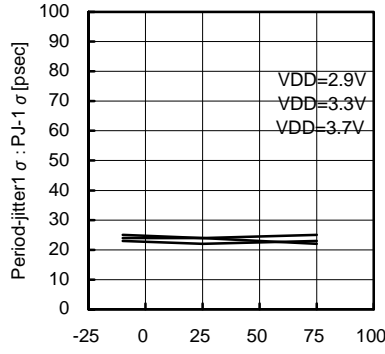


Fig.60 36MHz
Temperature - Period-Jitter 1 σ

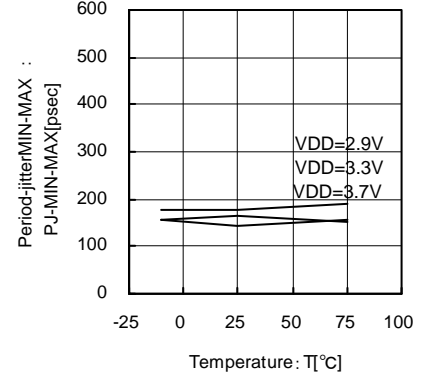


Fig.61 36MHz
Temperature - Period-Jitter MIN-MAX

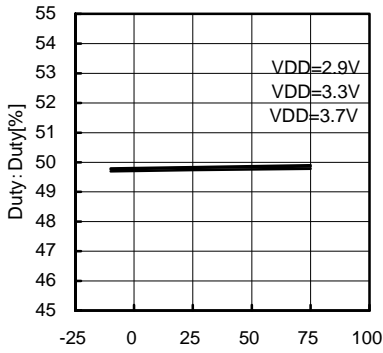


Fig.62 30MHz
Temperature - Duty

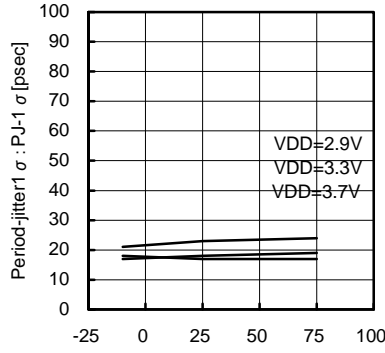


Fig.63 30MHz
Temperature - Period-Jitter 1 σ

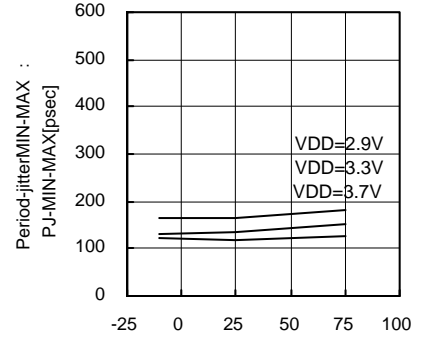


Fig.64 30MHz
Temperature - Period-Jitter MIN-MAX

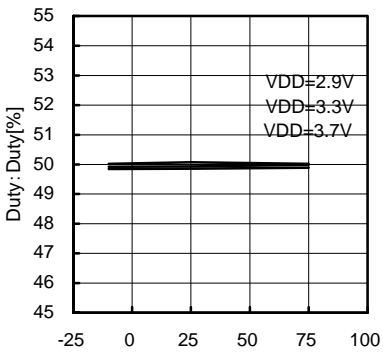


Fig.65 24MHz
Temperature - Duty

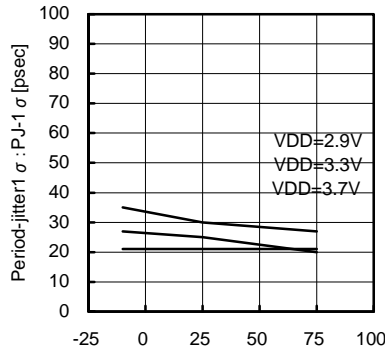


Fig.66 24MHz
Temperature - Period-Jitter 1 σ

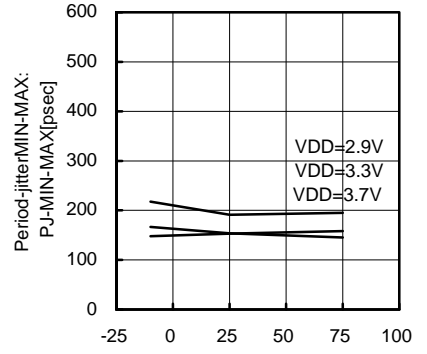
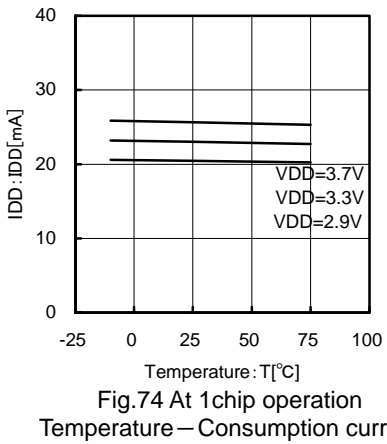
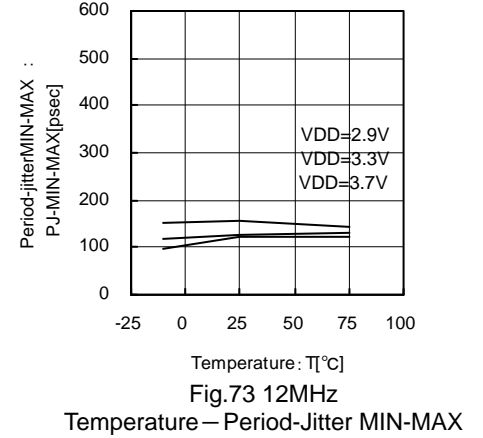
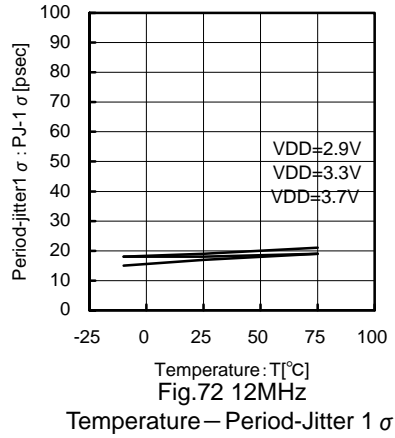
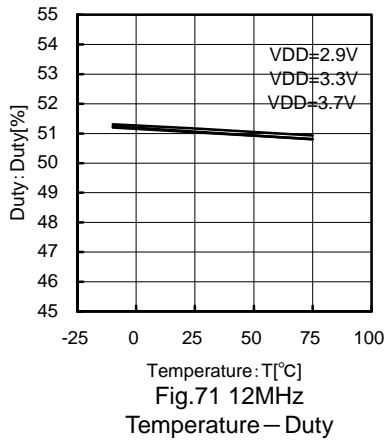
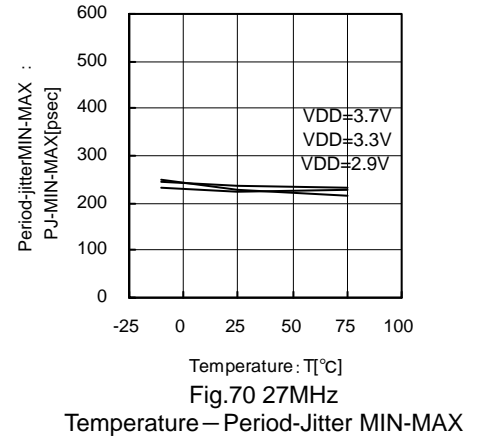
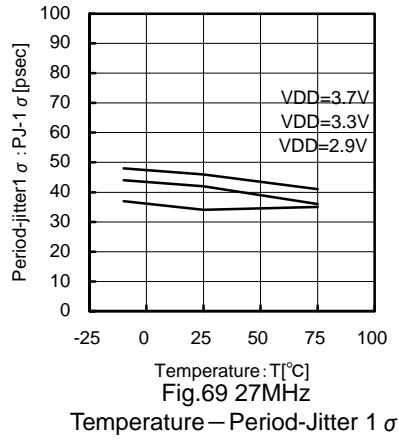
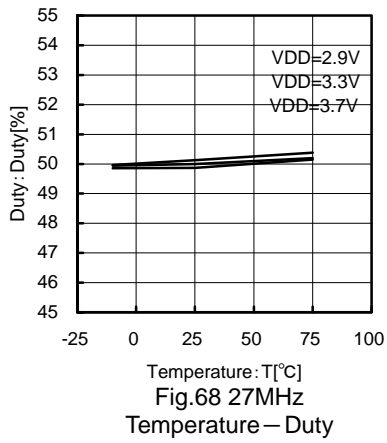


Fig.67 24MHz
Temperature - Period-Jitter MIN-MAX

● Reference data (BU2396KN Temperature and Supply voltage variations data)



●List of BU2396KN Operation Modes

When XTAL_SEL=L, (When a crystal oscillator of 14.318182-MHz frequency is used)

Xtal(MHz)	CLK2ON	FS1	FS2	FS3	CLK1(MHz)	CLK2(MHz)	REF_CLK(MHz)
14.318182	H	H	H	H	135.000000	48.008022	14.318182
14.318182	H	L	H	H	135.000000	48.008022	17.734450
14.318182	L	H	H	H	135.000000	Fixed to L	14.318182
14.318182	L	L	H	H	135.000000	Fixed to L	17.734450
14.318182	H	H	H	L	108.000000	48.008022	14.318182
14.318182	H	L	H	L	108.000000	48.008022	17.734450
14.318182	L	H	H	L	108.000000	Fixed to L	14.318182
14.318182	L	L	H	L	108.000000	Fixed to L	17.734450
14.318182	H	H	L	L	98.181818	48.008022	14.318182
14.318182	H	L	L	L	98.181818	48.008022	17.734450
14.318182	L	H	L	L	98.181818	Fixed to L	14.318182
14.318182	L	L	L	L	98.181818	Fixed to L	17.734450
14.318182	H	H	L	H	110.000000	48.008022	14.318182
14.318182	H	L	L	H	110.000000	48.008022	17.734450
14.318182	L	H	L	H	110.000000	Fixed to L	14.318182
14.318182	L	L	L	H	110.000000	Fixed to L	17.734450

When XTAL_SEL=H, (When a crystal oscillator of 28.636363MHz frequency is used)

Xtal(MHz)	CLK2ON	FS1	FS2	FS3	CLK1(MHz)	CLK2(MHz)	REF_CLK(MHz)
28.636363	H	H	H	H	135.000000	48.008022	14.318182
28.636363	H	L	H	H	135.000000	48.008022	17.734450
28.636363	L	H	H	H	135.000000	Fixed to L	14.318182
28.636363	L	L	H	H	135.000000	Fixed to L	17.734450
28.636363	H	H	H	L	108.000000	48.008022	14.318182
28.636363	H	L	H	L	108.000000	48.008022	17.734450
28.636363	L	H	H	L	108.000000	Fixed to L	14.318182
28.636363	L	L	H	L	108.000000	Fixed to L	17.734450
28.636363	H	H	L	L	98.181818	48.008022	14.318182
28.636363	H	L	L	L	98.181818	48.008022	17.734450
28.636363	L	H	L	L	98.181818	Fixed to L	14.318182
28.636363	L	L	L	L	98.181818	Fixed to L	17.734450
28.636363	H	H	L	H	110.000000	48.008022	14.318182
28.636363	H	L	L	H	110.000000	48.008022	17.734450
28.636363	L	H	L	H	110.000000	Fixed to L	14.318182
28.636363	L	L	L	H	110.000000	Fixed to L	17.734450

●List of BU2396KN Operation Modes

TGCLK_SEL1	TGCLK_SEL2	TGCLK_EN	VCLK_EN	TGCLK_PD	VCLK_PD	TGCLK Output	VCLK Output	UCLK Output	PLL1 30M,24M	PLL2 36M,27M					
0	0	0	0	0	0	Fixed to L	Fixed to L		Power-Down	Power-Down					
0	1														
1	0														
1	1														
0	0	1													
0	1														
1	0														
1	1														
0	0	0		1	0	Fixed to L	Fixed to L	Normal operation	Power-Down						
0	1														
1	0														
1	1														
0	0	1	1	1	0	Fixed to L	Fixed to L	Power-Down	Power-Down						
0	1														
1	0														
1	1														
0	0	0								1	1	24MHz output	12MHz output	Normal operation	Power-Down
0	1														
1	0														
1	1														
0	0	1	1	1	0	Fixed to L	Fixed to L	Power-Down	Power-Down						
0	1														
1	0														
1	1														
0	0	0								1	1	30MHz output	12MHz output	Normal operation	Power-Down
0	1														
1	0														
1	1														
0	0	1	1	1	0	Fixed to L	Fixed to L	Power-Down	Power-Down						
0	1														
1	0														
1	1														
0	0	0								1	1	36MHz output	12MHz output	Normal operation	Power-Down
0	1														
1	0														
1	1														
0	0	1	1	1	0	Fixed to L	Fixed to L	Power-Down	Power-Down						
0	1														
1	0														
1	1														
0	0	0								1	1	36MHz output	12MHz output	Normal operation	Power-Down
0	1														
1	0														
1	1														
0	0	1	1	1	0	Fixed to L	Fixed to L	Power-Down	Power-Down						
0	1														
1	0														
1	1														
0	0	0								1	1	27MHz output	12MHz output	Normal operation	Power-Down
0	1														
1	0														
1	1														
0	0	1	1	1	0	Fixed to L	Fixed to L	Power-Down	Power-Down						
0	1														
1	0														
1	1														
0	0	0								1	1	27MHz output	12MHz output	Normal operation	Power-Down
0	1														
1	0														
1	1														
0	0	1	1	1	0	Fixed to L	Fixed to L	Power-Down	Power-Down						
0	1														
1	0														
1	1														
0	0	0								1	1	36MHz output	12MHz output	Normal operation	Power-Down
0	1														
1	0														
1	1														
0	0	1	1	1	0	Fixed to L	Fixed to L	Power-Down	Power-Down						
0	1														
1	0														
1	1														
0	0	0								1	1	36MHz output	12MHz output	Normal operation	Power-Down
0	1														
1	0														
1	1														

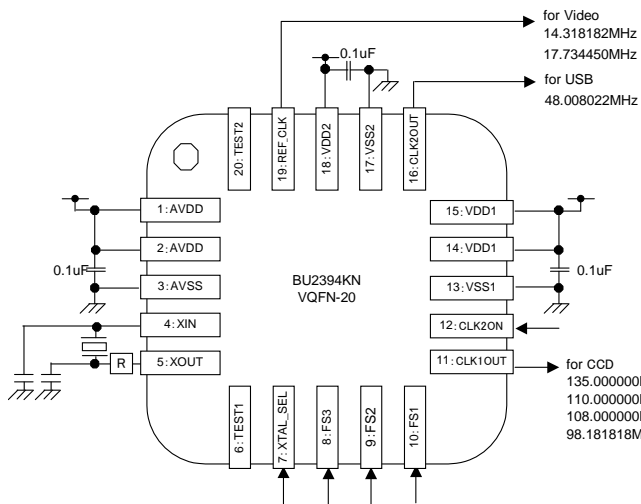


Fig.75

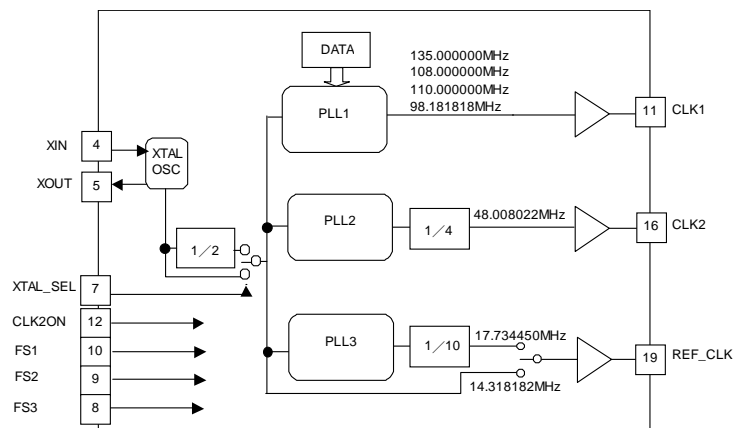


Fig.76

Description of Terminal

PIN No.	PIN NAME	Function
1	AVDD	Analog power source
2	AVDD	Analog power source
3	AVSS	Analog GND
4	XIN	Crystal IN
5	XOUT	Crystal OUT
6	TEST1	TEST pin, normally open, equipped with pull-down
7	XTAL_SEL	Crystal oscillator selection, H: 28.636 MHz, L: 14.318 MHz, equipped with pull-up
8	FS3	CLK1,2 output selection, equipped with pull-up
9	FS2	CLK1,2 output selection, equipped with pull-up
10	FS1	REFCLK output selection, equipped with pull-up
11	CLK1OUT	110M/98M/108M/135M output
12	CLK2ON	CLK2 output control, H: Enable, L: Disable, equipped with pull-up
13	VSS1	CLK1/CLK2 & Internal digital GND
14	VDD1	CLK1/2 & Internal digital power supply
15	VDD1	CLK1/2 & Internal digital power supply
16	CLK2OUT	48M output
17	VSS2	REFCLK GND
18	VDD2	REFCLK power supply
19	REF_CLK	14.3M/17.7M output
20	TEST2	TEST pin, normally open, equipped with pull-down

Note) Basically, mount ICs to the substrate for use. If the ICs are not mounted to the substrate, the characteristics of ICs may not be fully demonstrated.

Mount 0.1uF as bypass capacitors in the vicinity of the IC pins between 1&2 PIN and 3PIN, 13PIN and 14&15PIN, and 17PIN and 18PIN, respectively.

※Even though we believe that the example of the application circuit is worth of a recommendation, please be sure to thoroughly recheck the characteristics before use.

※As to the jitters, the TYP values vary with the substrate, power supply, output loads, noises, and others.

Besides, for the use, the operating margin should be thoroughly checked.

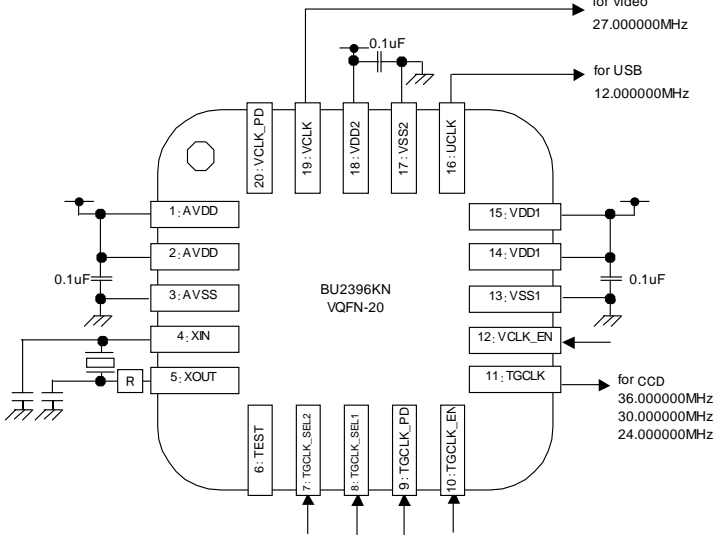


Fig.77

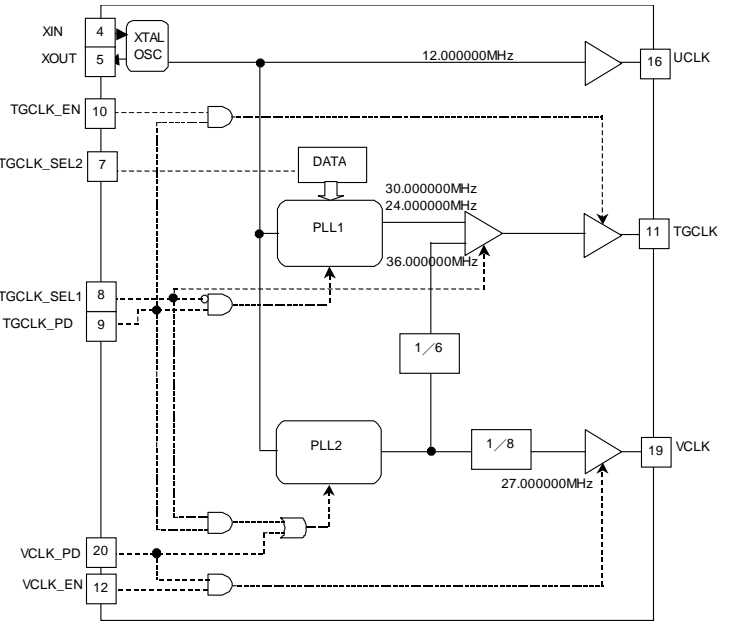


Fig.78

Description of Terminal

PIN No.	PIN NAME	Function
1	AVDD	Analog power source
2	AVDD	Analog power source
3	AVSS	Analog GND
4	XIN	Crystal IN
5	XOUT	Crystal OUT
6	TEST	TEST pin, normally open, equipped with pull-down
7	TGCLK_SEL2	TGCLK frequency selection, equipped with pull-up
8	TGCLK_SEL1	TGCLK frequency selection, equipped with pull-up
9	TGCLK_PD	TGCLK Power-Down control, H:enable, L:Power-Down, equipped with pull-down
10	TGCLK_EN	TGCLK output control, H: Enable, L: Output fixed to L, equipped with pull-down
11	TGCLK	36M, 30M, 24M output
12	VCLK_EN	VCLK output control, H:enable, L: Output fixed to L, equipped with pull-down
13	VSS1	TGCLK,UCLK & Internal digital GND
14	VDD1	TGCLK,UCLK & Internal digital power supply
15	VDD1	TGCLK,UCLK & Internal digital power supply
16	UCLK	12M output
17	VSS2	VCLK GND
18	VDD2	VCLK power source
19	VCLK	27M output
20	VCLK_PD	VCLK Power-Down control, H:enable, L:Power-Down, equipped with pull-down

Note) Basically, mount ICs to the substrate for use. If the ICs are not mounted to the substrate, the characteristics of ICs may not be fully demonstrated.

Mount 0.1uF as bypass capacitors in the vicinity of the IC pins between 1&2 PIN and 3PIN, 13PIN and 14&15PIN, and 17PIN and 18PIN, respectively.

※Even though we believe that the example of the application circuit is worth of a recommendation, please be sure to thoroughly recheck the characteristics before use.

※As to the jitters, the TYP values vary with the substrate, power supply, output loads, noises, and others. Besides, for the use, the operating margin should be thoroughly checked.

●Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as applied voltage (VDD or VIN), operating temperature range (Topr), etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Recommended operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.

In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

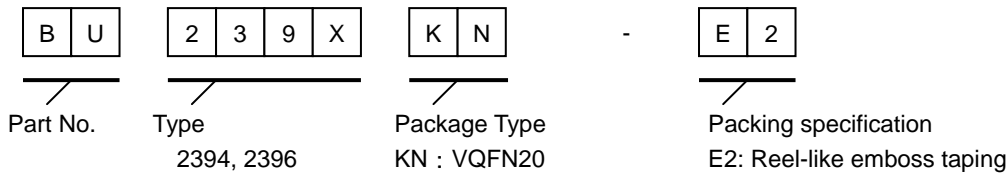
(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

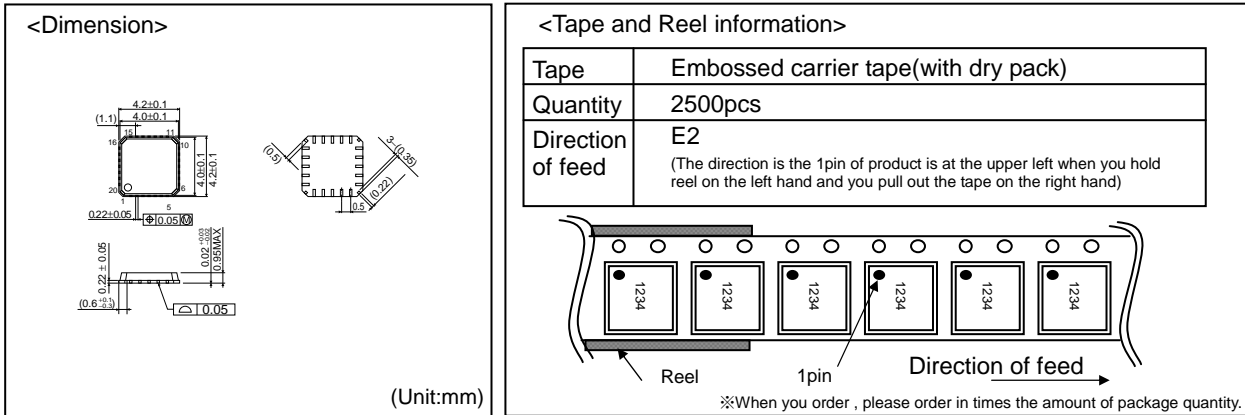
(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, et

●Name selection of ordered type



VQFN20



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Düsseldorf	TEL: +49-2154-9210	FAX: +49-2154-921400	Dongguan	TEL: +86-769-8393-3320	FAX: +86-769-8398-4140
Munich	TEL: +49-8999-216168	FAX: +49-8999-216176	Fuzhou	TEL: +86-591-8801-8698	FAX: +86-591-8801-8690
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France	TEL: +33-1-5697-3060	FAX: +33-1-5697-3080	Huizhou	TEL: +86-752-205-1054	FAX: +86-752-205-1059
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Espoo	TEL: +358-9725-54491	FAX: +358-9-7255-4499	Hong Kong	TEL: +852-2-740-6262	FAX: +852-2-375-8971
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