

500V N-Channel Power MOSFET



TO-252

123

Pin Definition:

- 1. Gate
- Drain
 Source

PRODUCT SUMMARY

V _{DS} (V)	$R_{DS(on)}(\Omega)$	$I_D(A)$	
500	1.5 @ V _{GS} =10V	2.2	

General Description

The TSM5ND50 N-Channel enhancement mode Power MOSFET is produced by planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.

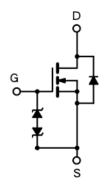
Features

- Low gate charge typical @ 20nC
- Low Crss typical @ 17pF
- Fast Switching
- 100% avalanche tested
- Improved dv/dt capability
- ESD Protection

Ordering Information

Part No.	Package	Packing
TSM5ND50CP RO	TO-252	2,500pcs / 13" Reel

Block Diagram



N-Channel MOSFET

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	±30	V
Continuous Drain Current	I _D	4.4	А
Pulsed Drain Current	I _{DM}	17.6	Α
Continuous Source Current (Diode Conduction)	Is	4.4	А
Peak Diode Recovery (Note 2)	dv/dt	4.5	V/ns
Single Pulse Drain to Source Avalanche Energy (Note 3)	E _{AS}	130	mJ
Total Power Dissipation @Ta = 25°C	P _{DTOT}	70	W
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	R⊖ _{JC}	1.78	°C/W
Thermal Resistance - Junction to Ambient	RO _{JA}	62.5	°C/W

Notes: Surface mounted on FR4 board t ≤ 10sec



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Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Тур	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250uA$	BV _{DSS}	500			V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 2.2A$	R _{DS(ON)}		1.2	1.5	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250uA$	V _{GS(TH)}	3.0		4.5	V
Zero Gate Voltage Drain Current	V _{DS} = 500V, V _{GS} = 0V	I _{DSS}			1	uA
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I _{GSS}			±10	uA
Forward Transconductance	V _{DS} = 15V, I _D = 2.2A	g _{fs}		3.1		S
Dynamic ^b						
Total Gate Charge)/ 050)/ l	Q_g		20		
Gate-Source Charge	$V_{DS} = 250V, I_D = 4.4A,$	Q _{gs}		4		nC
Gate-Drain Charge	V _{GS} = 10V	Q_{gd}		10		
Input Capacitance), OF),), O),	C _{iss}		535		
Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1.0MHz	C _{oss}		75		pF
Reverse Transfer Capacitance		C _{rss}		17		
Switching ^c						
Turn-On Delay Time		$t_{d(on)}$		21.6		
Turn-On Rise Time	$V_{GS} = 10V, I_D = 4.4A,$	t _r		11.7		
Turn-Off Delay Time	$V_{DD} = 250V, R_G = 25\Omega$	t _{d(off)}		14.5		nS
Turn-Off Fall Time		t _f		4.5]
Source Drain Diode						
Source-drain Current		I _{SD}			4.4	Α
Diode Forward Voltage	I _S = 4.4A, V _{GS} = 0V	V_{SD}		0.82	1.2	V
Reverse Recovery Time	$V_{DD} = 30V$, $I_{SD} = 4.4A$,	t _{rr}		310		nS
Reverse Recovery Charge	$dI_F/dt = 100A/us$.	Q _{rr}		1425		uC
Reverse Recovery Current	T _J =150°C	Q _{rr}		9.2		uC

Notes:

- 1. Pulse test: pulse width ≤300uS, duty cycle ≤2%
- 2. I_{SD} <4.4A, di/dt<200A/us, VDD<BV_{DSS}
- 3. Starting V_{DD} = 50V, I_{AS} =4.4A, T_{J} =25°C
- 4. For design reference only, not subject to production testing.
- 5. Switching time is essentially independent of operating temperature.

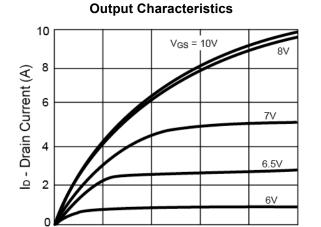


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Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)



On-Resistance vs. Drain Current

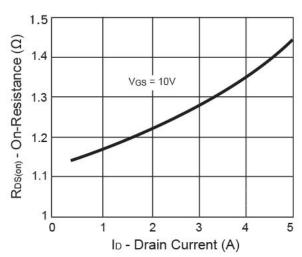
VDS - Drain-to-Source Voltage (V)

12

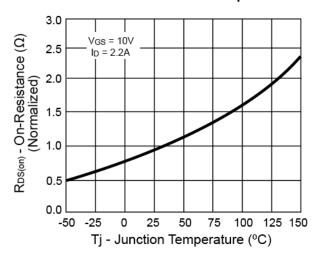
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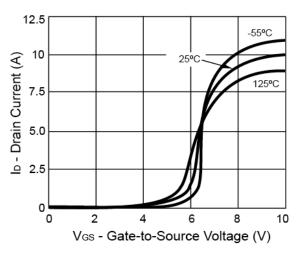
8



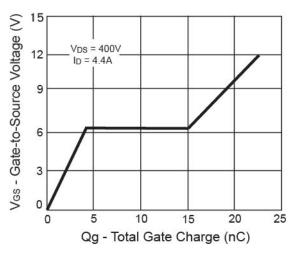
On-Resistance vs. Junction Temperature



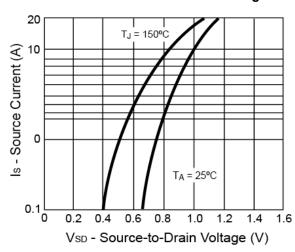
Transfer Characteristics



Gate Charge



Source-Drain Diode Forward Voltage



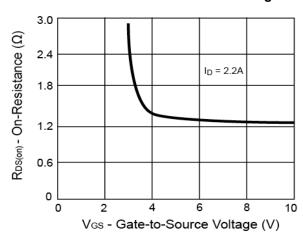


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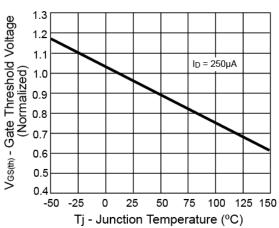


Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

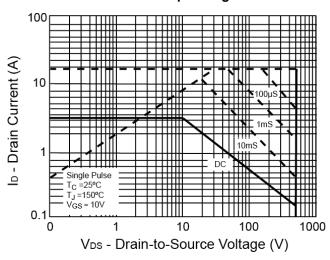
On-Resistance vs. Gate-Source Voltage



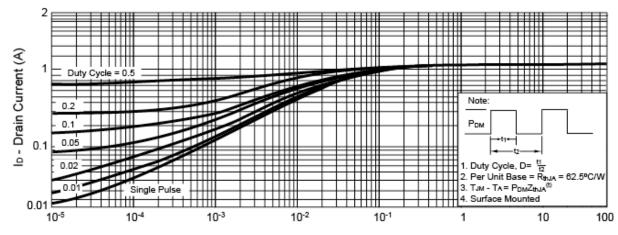
Threshold Voltage



Maximum Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



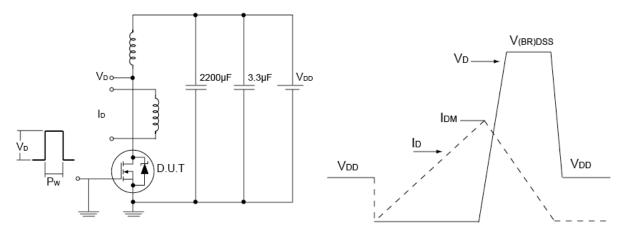
Square Wave Pulse Duration (sec)



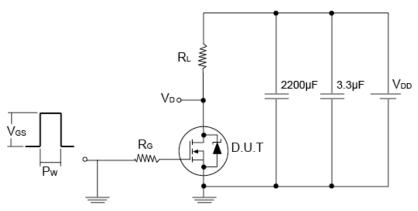
Pb RoHS

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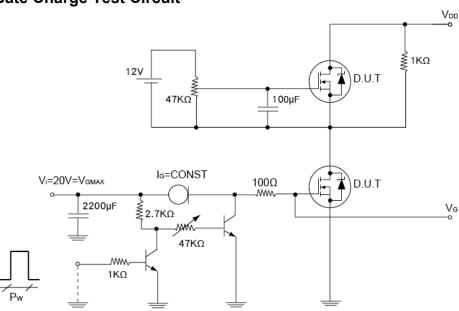
Unclamped Inductive Load Test Circuit and Waveform



Switching Time Test Circuits for Resistive Load



Gate Charge Test Circuit

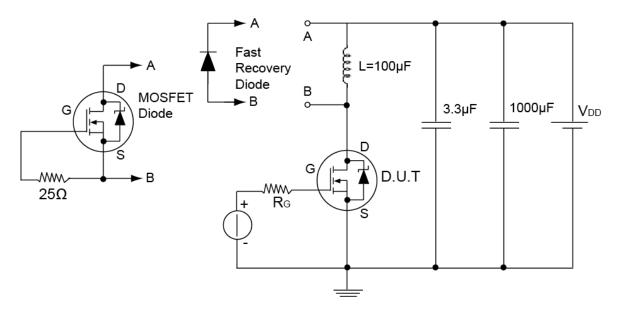




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Test Circuit for Inductive Load Switching and Diode Recovery Times

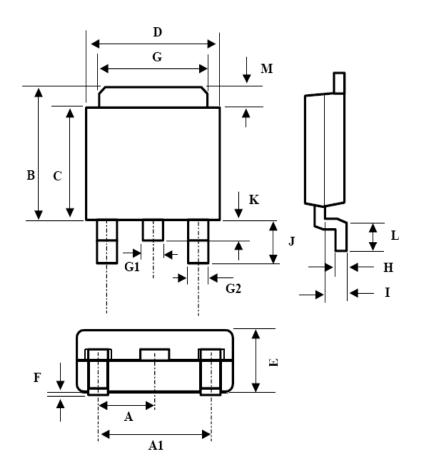






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SOT-252 Mechanical Drawing



TO OFG DIMENSION					
TO-252 DIMENSION					
DIM	MILLIMETERS		INCHES		
-	MIN	MAX MIN		MAX	
Α	2.3E	3SC	0.09	BSC	
A1	4.6E	3SC	0.18	BSC	
В	6.80	7.20	0.268	0.283	
С	5.40	5.60	0.213	0.220	
D	6.40	6.65	0.252	0.262	
Е	2.20	2.40	0.087	0.094	
F	0.00	0.20	0.000	0.008	
G	5.20	5.40	0.205	0.213	
G1	0.75	0.85	0.030	0.033	
G2	0.55	0.65	0.022	0.026	
Н	0.35	0.65	0.014	0.026	
	0.90	1.50	0.035	0.059	
J	2.20	2.80	0.087	0.110	
K	0.50	1.10	0.020	0.043	
L	0.90	1.50	0.035	0.059	
М	1.30	1.70	0.051	0.67	

Marking Diagram



Y = Year Code

M = Month Code

(A=Jan, B=Feb, C=Mar, D=Apl, E=May, F=Jun, G=Jul, H=Aug, I=Sep, J=Oct, K=Nov, L=Dec)

L = Lot Code

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Version: C07



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