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TFA3352

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Control and Monitoring IC for electronic transformer operating low-voltage halogen lamps. It triggers, monitors and turns-off RF oscillation dependent on several control and guarding function

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Control- and Monitoring-IC for Electronic Transformers operating Low-Voltage Halogen Lamps

Short Description

The bipolar monolithic integrated circuit triggers, monitors and turns-off RF-oscillations of a self-oscillating circuit for generation of a RF-shaped lamp current for Halogen lamps dependent on several control- and monitoring functions. This IC protects from overtemperature and overload, bringing the oscillations pemanently to an end. The burn voltage of the lamp is internal dimmable by phase cutting-off.

Features

- Overload and short circuit protection
- Overvoltage protection having short reaction time
- Overtemperature protection optionally acts by means of an external temperature sensor or a sensor on chip
- Low state-dependent current consumption for low loss supply from the mains
- Dimmable by phase cutting-off with ac voltage and dc voltage supply
- Automatically matching of the overload thresholds to the mode of supply
- Minimum external wiring by using enquiry routines to detect errors

Package

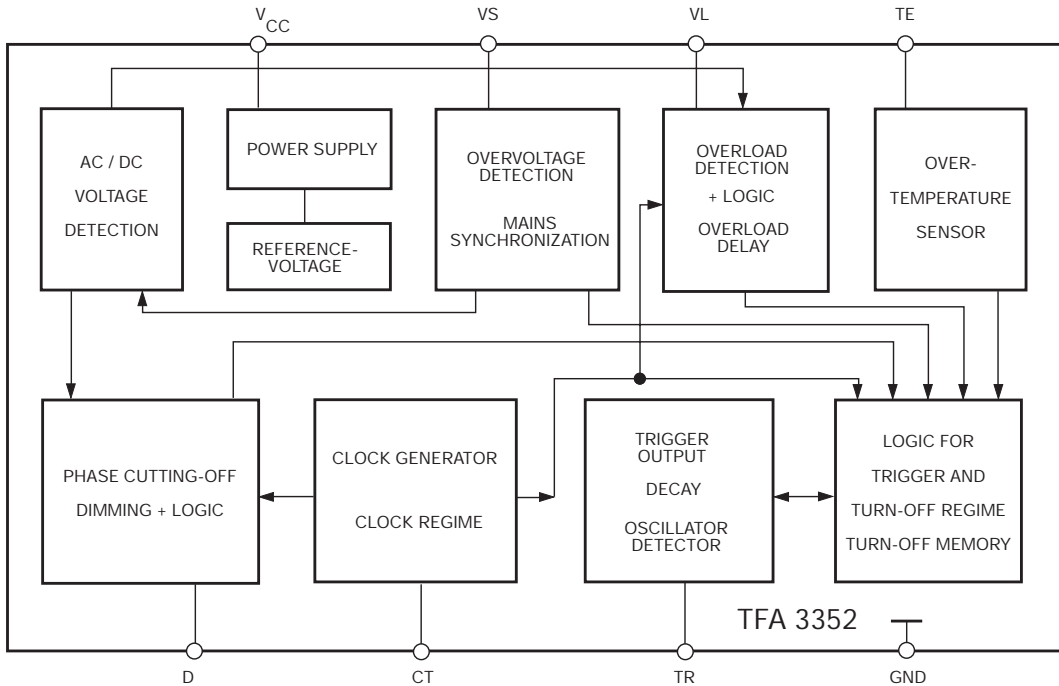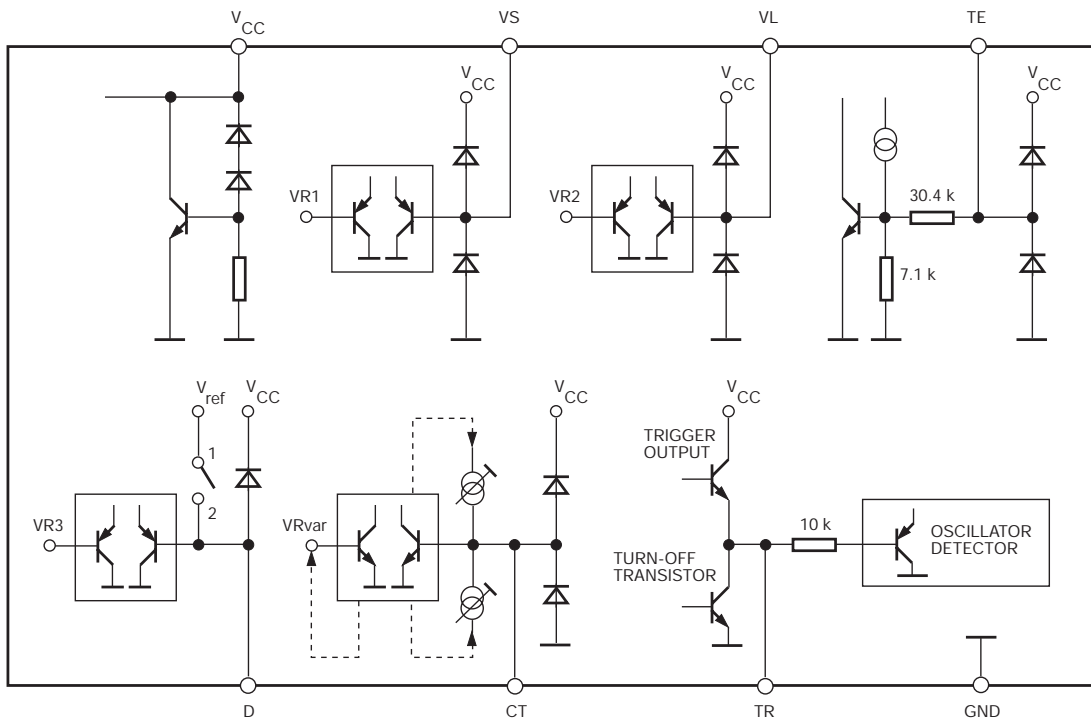- DIP 8
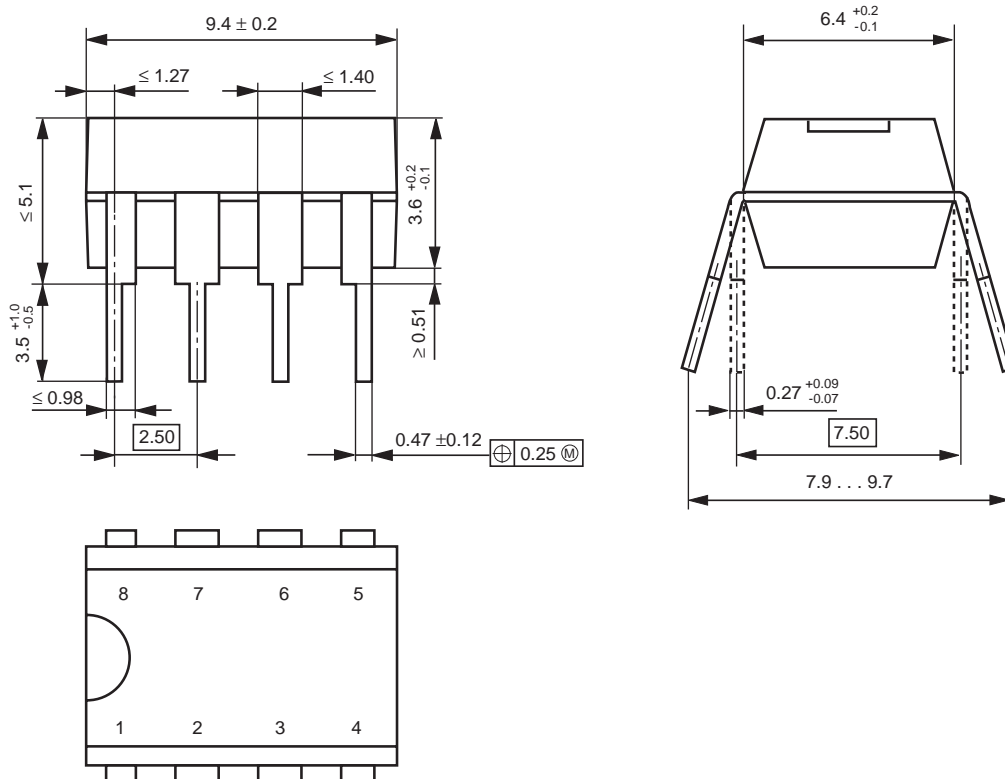
Pinning

Pin 1   D   Dim input
Pin 2   CT   Clock generator
Pin 3   TR   Trigger output, turn-off attenuation, oscillation detector
Pin 4   GND   Connection to ground
Pin 5   TE   Overtemperature protection input
Pin 6   VL   Overload input
Pin 7   VS   Overvoltage protection input, detection of zero crossings
Pin 8 V_{CC} Supply voltage

Block Diagram

Basical internal wiring

Functional Description

The integrated circuit TFA3352 implements control and monitoring functions for electronic transformers. It assisted corresponding with the circuit concerned the action principle of a push-pull flow converter, the oscillation of which is modulated with the envelope of the mains frequency rectified for ac mode operation.

By means of the switching transistors shown, the transistor connected to reference potential is controlled via its base, therefore, the integrated circuit does not come into contact with high voltages. The IC picks the oscillation frequency by a trigger pulse to this base and evaluates the control frequency applied via inductive coupling by means of an oscillation detector, in order to cut further triggers.

Furthermore, the oscillation can be attenuated via base terminal and with that reliably finished by a turn-off transistor integrated in the IC.

This principle enables affecting of the oscillation in optional time regimes.

The IC consists of several logic units responding to zero crossings, overvoltage, overload, overtemperature, as well as to the moment selected for phase cutting-off, and depending on that, it enables to control the oscillatory circuit.

A temperature stable reference voltage and the low average current consumption enables the temperature circuit to record the temperature within the chip.

Values recorded as overtemperature or overload are stored and cause the turn-off of the component.

Reset of the corresponding error memory is possible by power on reset.

Current supply takes place via an external dropping resistor, backup capacitor and an external voltage limiter containing a Zener diode. During start phase, while the supply voltage is built up, the circuit minimizes its current consumption.

Only when the flow converter successfully starts, the operating current consumption appears.

The constructional arrangement of the IC allows that short duration negative peak currents up to 300 mA can be applied to the output TR.

The IC enables the scanning of the oscillation of the switch mode power supply during dc voltage operation, thus there can also be dimmed with dc voltage supply.

Pin Description

Pin 1   D   Dim Input

An RC network is connected with the dim input D. By variation of RD it can be dimmed. In every zero crossing, the RC-network is charged to the reference voltage of 4 V with a current of 500 µA. When the subsequent discharge reaches a threshold of 2 V at input D, the turn-off transistor breaks the oscillation via output TR, and the trigger pulses are cut till to the end of the following zero crossing.

By that, a phase cutting is carried out.

The minimum resistance of the RC network should be approximately 15 kΩ because otherwise the reference voltage could be loaded by currents higher than 300 µA.

The IC is also able to dim in dc voltage operation. For this a 12.5 ms clock internally generated is used, which controls the RC network at the dim input similar to the mains zero crossings in ac voltage operation.

A dim input that is not used can be kept unconnected.

In order to prevent possible coupling-in of distortions into the non used dim input surely, it has to be blocked or to be connected with V_{CC}.

Pin 2   CT   Clock Generator

The clock generator generates clock pulses of 20 µs width with a repetition rate of 4 kHz by defined reversing the charge of the ramp capacitor of 390 pF connected to terminal CT.

From the clock rate of 250 µs there are derived all time lapses (except trigger width) generated by the IC. It has to be considered, that with modification of the clock capacitor, three cycles of the frequency to be monitored by the oscillation detector can be acquired within one clock cycle.

The capacity range of the clock capacitor has to be choiced between 200 pF and 500 pF, in order to guarantee a save adjustment of the overload thresholds in ac and dc operation.

Pin 3   TR   Trigger Output, Oscillation Detector, Turn-off attenuation

• Trigger Output

Trigger pulses are directly branched from the internal clock pulses. Via a delay line result the typical pulse width of 1.5 µs for pulses, being applied every 250 µs to the trigger output. These trigger pulses are permanently generated outside the time window of the mains zero crossings, detected by the IC, as well as separately from the blanking intervals defined by dimming, as long as the circuit starts.

• Oscillation Detector

The oscillation detector realizes the control applied to the base of the switching transistor as a stabilized oscillation for a period of a clock cycle of 250 µs, when more than three cycles of a sine-shaped less than 300 kHz having an amplitude wider than 1 Vss are applied.
After an oscillation has been realized, further trigger pulses will be cut for the output TR by means of the logic. Such an evaluation happens in every clock period. With lost load for instance by this means no oscillations are recognized and, therefore, triggers generated for periods for which an oscillation shall be applied.

• Turn-off attenuation

By a turn-off transistor with a low saturation voltage the base of the external switching transistor, applied to reference potential is surely cut, and by that the oscillation is finished during dim operation for the period of 230 µs. That 230 µs result from the clock rate minus an internal clock pulse width.
In the case of overload the turn-off transistor is statically controlled by approximately 10 mA, as long as the supply voltage at terminal V_{CC} which is breaking down by that, again switch-off the turn-off transistor with a threshold of 6 V.
The specifically designed turn-off transistor, as well as further constructive measures take over the protection of the integrated circuit against transients which can be applied via inductive control.
An external Schottky diode D of corresponding power prevents the possible increase of the current consumption of the IC caused by those negative transients.
Diode D1 (see schematic circuit) supplies the efficiency of the turn-off transistor at high power transformers.

Pin 4   GND   Connection to ground

Pin 5   TE   Overtemperature protection input

The internal protection circuit is multiple usable.
If the input TE is connected to ground, the overtemperature protection is deactivated and the range of the operating temperature runs between -10 °C and 110 °C.
The input TE enables, if it is unconnected, permanently to turn-off the oscillation circuit similar to the overload recognition via temperatures between 80 °C and 95 °C on chip.
A detected overtemperature is stored by the same enquiry cycle used with overload. The circuit can only sucessfully start after cooling down and mains interruption once again.
By wiring the temperature input with an external temperature-sensitive resistor into a divider between supply voltage and ground, a switching voltage can be generated, which deactivates the temperature monitoring for values < 0.1 V, and the temperature monitoring is directly activated for values > 3 V, therefore, the oscillation will be turned-off after the delay time.
Therefore, any optional heat source can be monitored by a sensitive resistor.
Hereby has to be taken into consideration, that an already activated temperature monitoring mode is only resetable by turning-off the mains.
Only one external resistor is required to upshift the internal switch-off temperature. The internal resistor 7.1 kΩ, shown in the internal wiring diagram, only is effective for a switch-off temperature between 80 °C and 95 °C.
If the pin TE is connected with ground, the internal resistors 7.1 kΩ and 30.4 kΩ are connected in parallel. That causes a switch-off temperature higher than 110 °C. In this case the overtemperature protection is not active in the permissible operating temperature range.
A resistor of 50 kΩ, connected between pin TE and ground increases the switch-off temperature of approximately 15 degrees.

Pin 6   VL   Overload protection input

The RF-shaped overload signal is detected at the comparator input VL (ac- switching threshold: 710 mV;
dc-switching threshold: 490 mV) via a low-valued resistor.
The overload signal only causes a response, when following conditions are met:

- After exceeding of the comparator threshold, a response delay time is activated, and the comparator threshold
  must be exceeded once again. The response delay time of more than 1 second (C_{Clock} = 390 pF) is necessary
  that cold currents in dimmed operation mode can be neglected when the load is turned-on. The cold current
  realized as overload decreases stepwise down to its final value thermally built up, according to the magnitude
  of the load and the angle of current flow in dim mode for approximately one second by every half-wave. Only
  after this delay time, when the overload still is applied, the oscillation will be attenuated and the trigger pulse
  gate and the overload memory will be set.

A new start is only possible after turning-off the mains voltage and again building-up the normal voltage. When the
event of overload is set, only the logic units required to store the overload are supplied with injector current,
therefore, the current consumption of the IC reduces to values less than 850 µA.
The turn-off transistor is as long statically controlled by 10 mA as the supply voltage breaks down to 6 V caused
by the oscillation turned-off. According to the application circuit, current is fed only via series connection of both
supply resistors. Only when the 10 mA control with 6 V is turned-off, the voltage at the backup capacitor again
increases up to the limiting voltage of the external Zener diode because of now less current consumption inspite
of less feed-in.
Because the trigger gate is set by overload memory a repeated triggering is impossible.
The instantanious value of the supply voltage on the mains sided anti-interference filter is kept stored at the
moment of cut-off, while it is dimmed by phase cutting-off. This voltage breaks down with triggering after zero
crossing according to the magnitudes of the loads differently quickly in order to increase again after that, together
with the increasing mains voltage.
Inspite of phase cutting-off in the proximity of the zero crossing, an overload signal caused by the cold current of
the load is possible, because the peak value of the mains voltage can short time be supplied. For that reason with
ac voltage the IC in principle after zero crossing neglects an overload signal applied for 1.25 ms, and blanks out
cold current parts not be evaluated as overload during dim mode operation. In dc voltage mode there is
responded to an overload by the overload test cycle described without blanking of 1.25 ms.

Pin 7   VS   Zero crossing detection, Overvoltage protection

• Zero crossing detection

At the input VS via a divider 100:1 the supply voltage is detected with 0.4 V and 1.2 V, in order to gain two zero
crossings as several functions are controlled by means of their edges. The zero crossing is used to dim mains
synchroneously, and systematically to blank the part of the cold-start current of a lamp load for the overload
detection, which is short-time generated in every half-wave. A diode is necessary, in order to be decoupled from
memory effect of a mains filter in dim mode, and to detect the zero crossings.
Without zero crossings the IC realizes the supply voltage as dc-voltage.

• Overvoltage protection

A third switching threshold at input VS detects with 4 V across the divider 100:1 a mains voltage higher than
400 V. When such a voltage is applied longer then 5 µs a self-holding logic activates for the time till to the
following internal cycle additionally two clock periods the switching transistor, i.e. the switching transistor is
activated for 500 µs up to 750 µs. At the same time, the trigger pulse gate is setted and a counter is started, which
again resets the trigger pulse gate after 12.5 ms.
The overvoltage is not valued during zero crossing, if it is shorter than the zero crossing itself. An overvoltage is
still be applied after zero crossing, however, causes an activation of the logic. By that, the oscillation is surely
blanked for 12.5 ms when overvoltage occurs.
Mains spikes with higher amplitudes can be tolerated by means of changing the divider ratio. In this case
decrease the width of threshold window of the detected zero crossings. Pay attention in case of dim mode, that a
sufficient charging of the external RC network at the dim input is possible during zero crossing.

Pin 8 V_{CC} Supply Voltage

The build-up of the supply voltage occurs in stages via a high valued first dropping resistor between supply voltage and center voltage and an additional second low valued one between center voltage and terminal V_{CC}, according to the application circuit used, the external backup capacitor is charged.

In this build-up phase only a certain part of the logic units is turned on. From a supply voltage of 7.5 V, trigger pulses are released, which have been generated until the external oscillation starts. At the same time all residual logic units are turned on.

The oscillation excited is additionally used now by the low valued feed in of the center voltage to supply the IC. By that, the voltage at the backup capacitor increases quicker and reaches the switching threshold of 8 V. Within this voltage all logic units are reset.

Therefore, the IC is able to dim and to store errors.

The increase of the current consumption by the logic units connected and a higher operating current consumption in dim mode is guaranteed by the additional current feed-in.

In dim mode operation in every half-wave is additionally required, except the typical trigger pulse current of 300 mA for 1.5 µs, a current of approximately 10 mA to control the switching-off transistor for 230 µs.

As soon as overload or overtemperature is realized, the oscillation is cut and the additional logic units are turned-off. However, the current consumption does not reduce, as the control of the internal turn-off transistor requires a current of approximately 10 mA. By that, the supply voltage breaks down. Below the operating range at 6 V, the control of the turn-off transistor is inapplicable, and the supply voltage rises again. Therefore, a maintaining operation mode is guaranteed with the same current consumption as at the building-up moment. This mode of supply voltage build-up allows starting of the IC, as well as storing the overload or overtemperature information and with corresponding dimensioning, even with dimmer installed before.

The current fed into the IC should not exceed effective 10 mA fore sure operation.

An external Zener diode at terminal V_{CC} stabilizes the supply voltage. This diode has to be made available for a voltage less than 13 V, because the internal stabilization of the IC runs between 13 V and 16 V. As soon as this limiting voltage is reached, the IC ends its operation automatically.

The operating range of the integrated circuit runs between 7.5 V and 12 V.

The backup capacitor is adjusted, that the current load by trigger and turn-off transistor during dim mode operation does not cause voltage break downs less than 7 V.

Very large values of the backup capacitor can cause a flashing of the lamp during start-phase, if the rise time of V_{CC} between 7.5 V and 8 V is too long.

The backup capacitor should be placed nearby the V_{CC} pin.

Operating Modes

The IC implements all functions of protection and control in ac- and dc voltage mode operating. It evaluates via zero crossing detection, whether is supplied by dc voltage or ac voltage. The overload evaluation is switched over by factor 1.4 according to the operation mode concerned.

The evaluation threshold is controlled by the operating mode detection. A continuous comparison of the zero crossing frequency with internal frequencies enables a secure control of the evaluation threshold.

At detected overtemperature or overload the IC remains in error mode and it is resetable only by dropping of the supply voltage below 6 V.

When overvoltage is detected, the oscillation is scanned for a moment and the IC automatically resets itself.

At missing load the IC generates trigger pulses every 250 µs, except of periods of zero crossings and the phase control periods for dim mode.

That allows a switch over / switch on of loads without power off.

Mains synchronization

The mains synchronization causes sure blanking out of overload peaks created by the stored voltage value on the mains sided noise filter in internal dimmed ac voltage operating mode directly after zero crossing.

Furthermore, in ac voltage operating the start moment of charging the capacitor at dim input is controlled by the zero crossing together with mains synchronization in dim mode.

The clock frequency from which the 12.5 ms clock is derived by a divider is defined by the capacitor at input CT. A comparison of the frequencies derived from this clock frequency with the mains frequency realized from the zero crossing enables the switching over to dc- or ac - voltage operating.

The time base defined by the ramp capacitor CT to 12.5 ms is reference basis in dc voltage operating. This time base defines the distance of the consecutive blanking intervals with dc voltage mode dimming.

Absolute Maximum Ratings

Limit value	Pin	Symbol	min	max	Unit
supply voltage	V_{CC}	V_{CC}	0	13	V
current consumption	V_{CC}	I_{CCeff}	-	20	mA
peak current for t < 100 µs	V_{CC}	I_{CCM}	-	100	mA
negative current load for t < 1µs	TR	$-I_{TR(neg)}$	-	300	mA
input voltage at over-temperature input	TE	V_{iTE}	-0.4	V_{CC}	V
input voltage at overload input	VL	V_{iVL}	-0.4	V_{CC}	V
input voltage of zero crossing detection	VS	V_{iVS}	-0.4	V_{CC}	V
input voltage at dim input	D	V_{iD}	-0.4	V_{CC}	V
resistance between dim input and ground	D	R_D-GND	15	-	kΩ
junction temperature		T_j	-	150	°C
storage temperature		T_{stg}	-50	150	°C
ambient temperature		T_{amb}	-10	110	°C
ESD protection for all terminals		V_{ESD}		2	kV

Characteristics

with T_{amb} = 25 °C, V_{CC} = 9 V, unless specified otherwise

	Pin	Symbol	min	typ	max	unit
voltage limit for I_{CC}=10 mA	V_{CC}	V_Z	13		16	V
quiescent current consumption	V_{CC}	$I_{CC(on)}$			1.55	mA
current consumption after error storage	V_{CC}	$I_{CC(off)}$			900	μA
quiescent current during start with V_{CC} = 5.3 V	V_{CC}	$I_{CC(Start)}$			900	μA
clock rate repeatition with C_{Clock} = 390 pF	TR	t_{Clock}	210		280	μs
ramp switch voltage	D	V_R	1.9		2.1	V
supply voltage (for full function V_{CC} > 8 V has once to be applied)	V_{CC}	V_{CC}	7.5		12	V
overload threshold for ac voltage mode	VL	$K_{OL(AC)}$	680		760	mV
overload threshold for dc voltage mode	VL	$K_{OL(DC)}$	470		525	mV
mains overvoltage threshold with tue > 5 μs	VS	K_{AT}	3.72		4.23	V
saturation voltage of turn-off transistor with I = 450 mA	TR	V_{TRsat}			500	mV
trigger pulse current	TR	I_{TRM}	150		500	mA
trigger pulse width with 50 % amplitude	TR	t_{TR}	0.6		2.5	μs
switching point of over-temperature turn-off		T_S	80		95	°C
switching voltage for forced overtemperature turn-off	TE	V_{TE}	3		5	V
switching voltage for deactivated overtemperature turn-off	TE	V_{TE}			0.1	V
operating frequency for a sine-shaped signal with an amplitude of 1 VSS of the oscillation detector	TR	$f_{Det.}$			300	kHz

## Values for Information

	value	unit
internal reference voltage	4	V
Threshold for connecting of trigger pulses during start and connecting of logic required for dim and protection functions	7.5	V
Threshold for release of the internal reset (full functional capability)	8	V
Threshold for switching-off the control of the turn-off transistor with overload set	6	V
blanking repetition rate with dc voltage dim for a clock rate of 250 µs	12.5	ms
Overload blanking for cold current suppression after zero crossing	1.25	ms
Control period of the turn-off transistor with dimming for 250 µs clock rate	230	µs
Control current of the turn-off transistor	10	mA
charge current for RC network at input D	500	µA
zero crossing threshold 1	1.2	V
zero crossing threshold 2	0.4	V

Dependences

Current consumption versus supply voltage
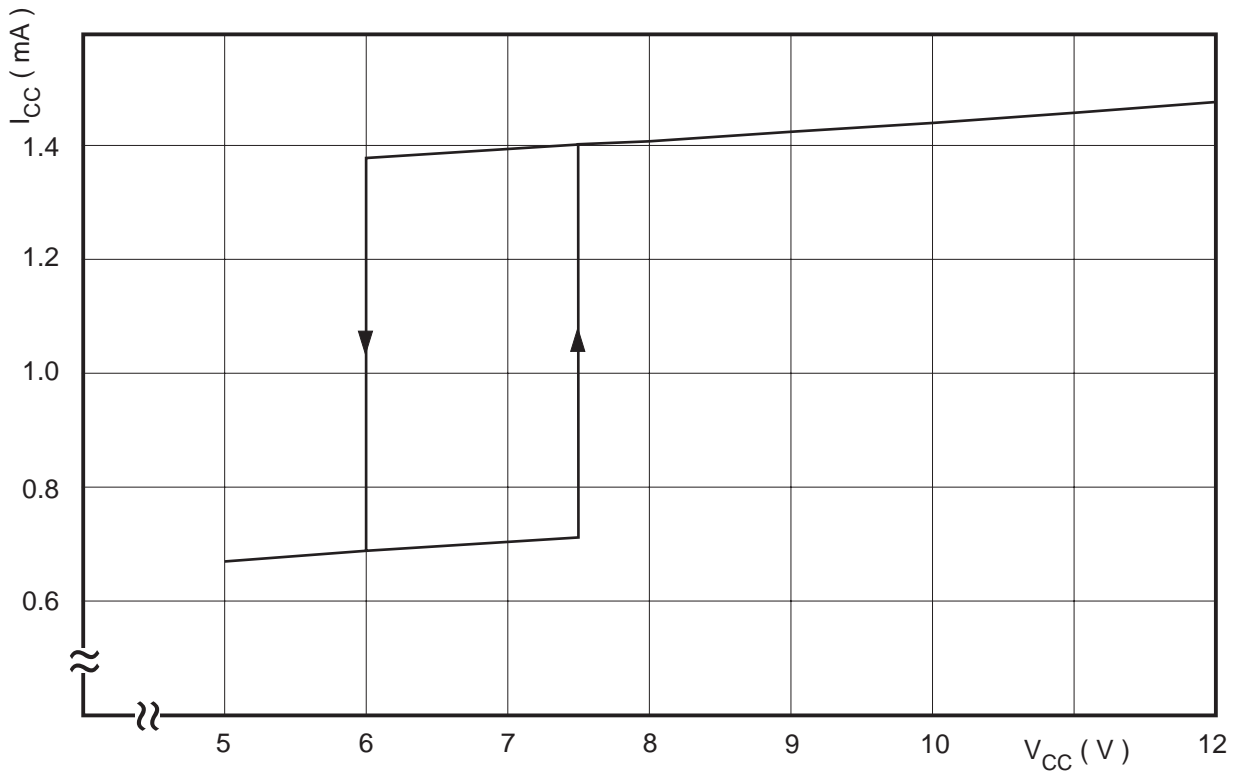
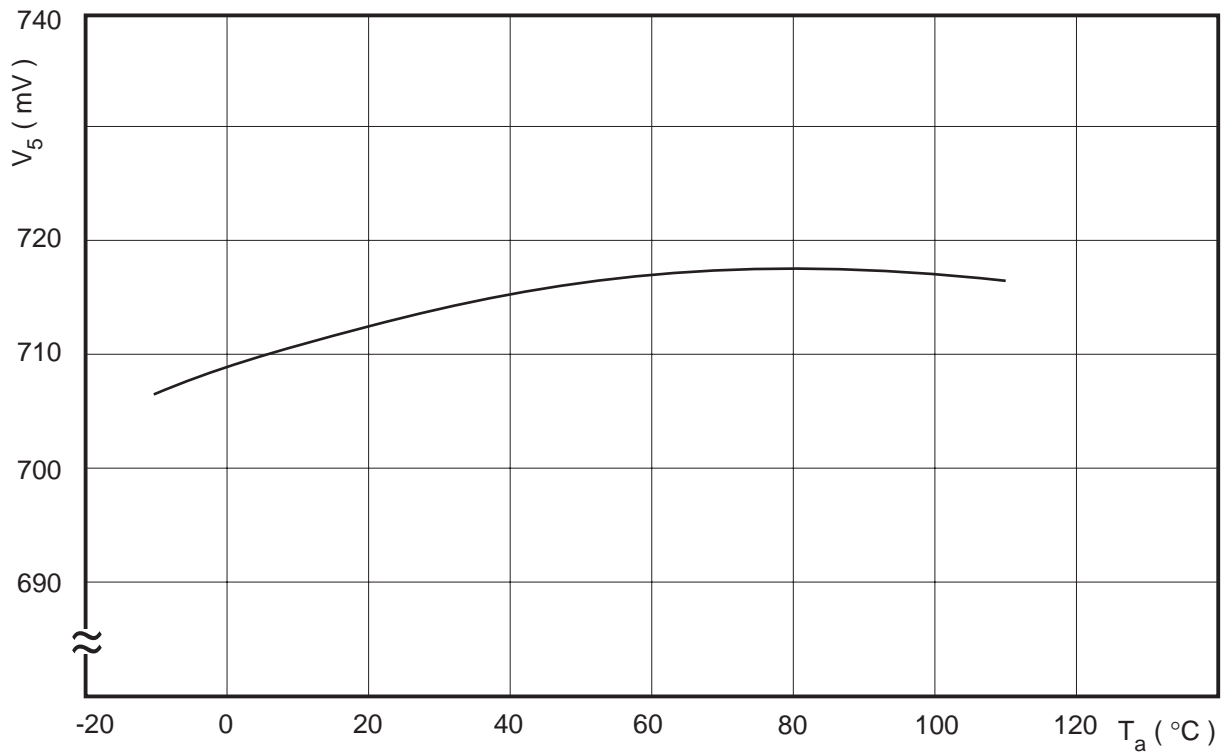
Clock frequency versus temperature
with $V_{CC} = 9$ V
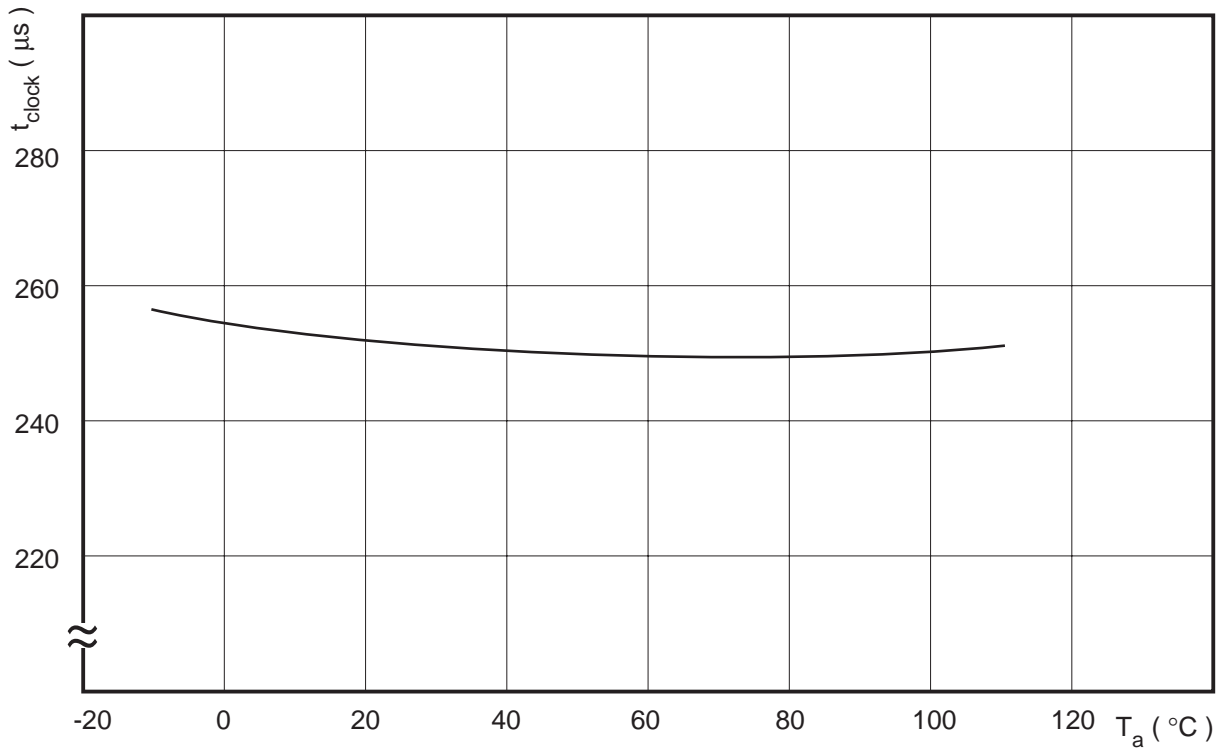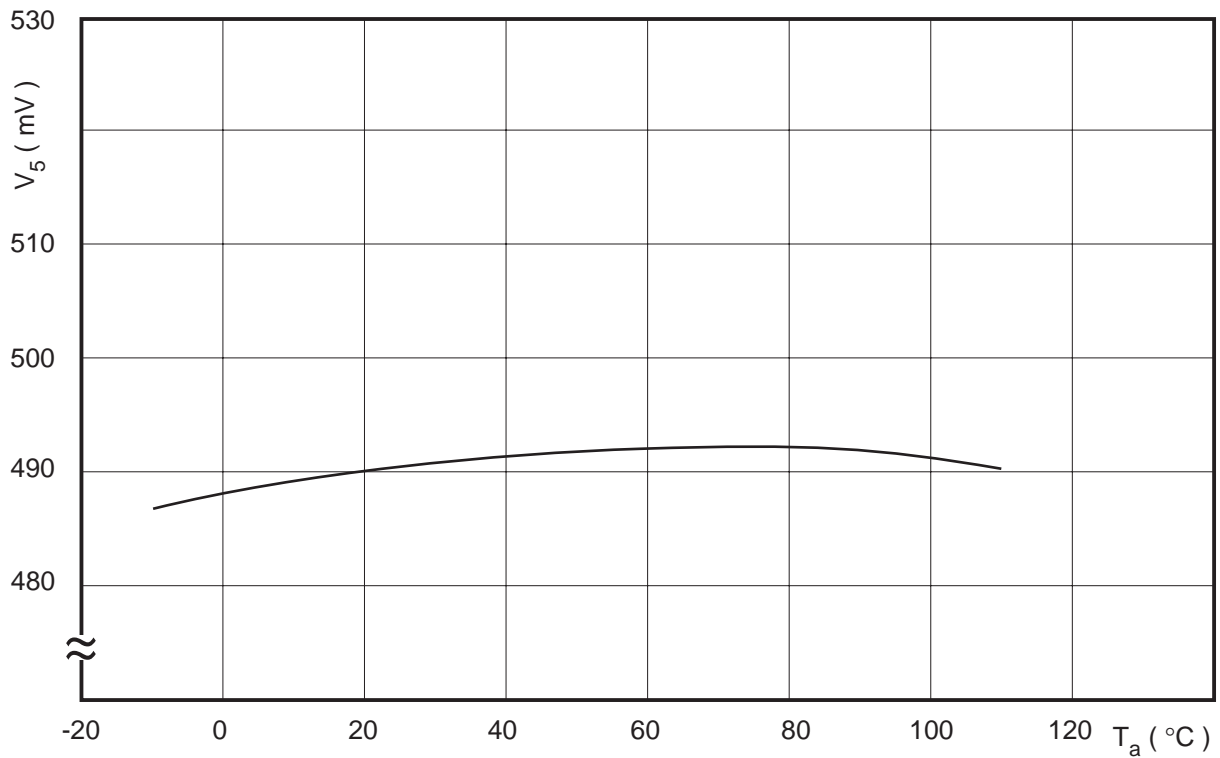
Start current versus temperature with V_{CC} = 5.3 V
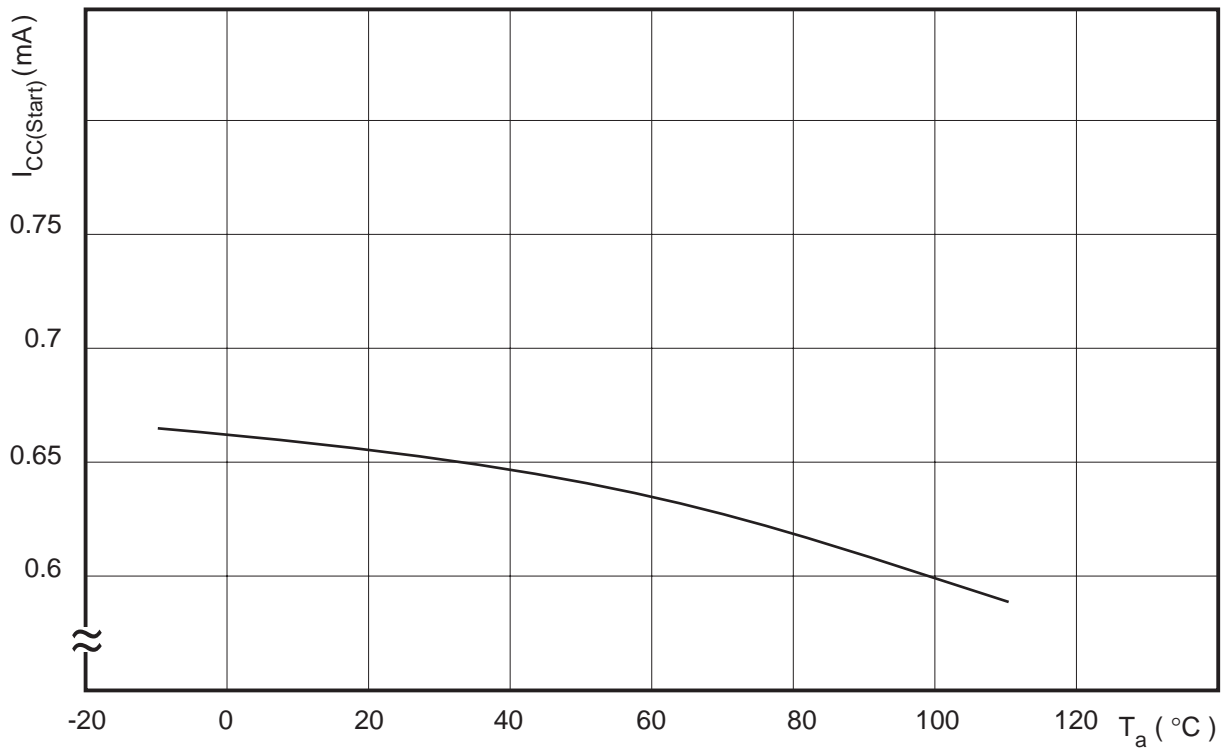
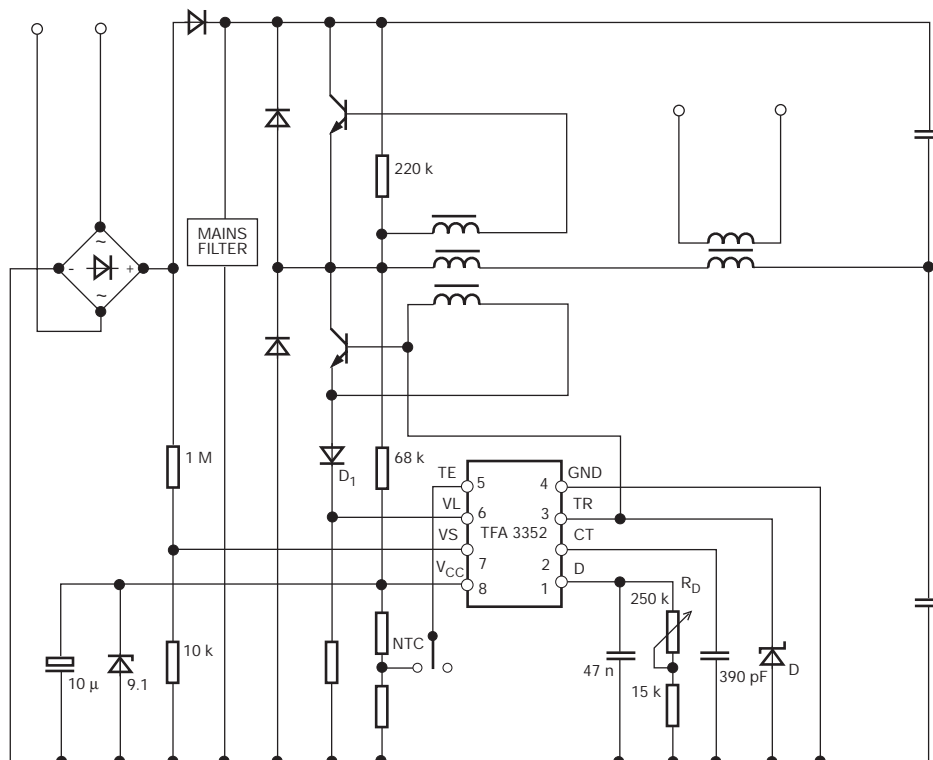## Quiescent current versus temperature with V_{CC} = 9 V
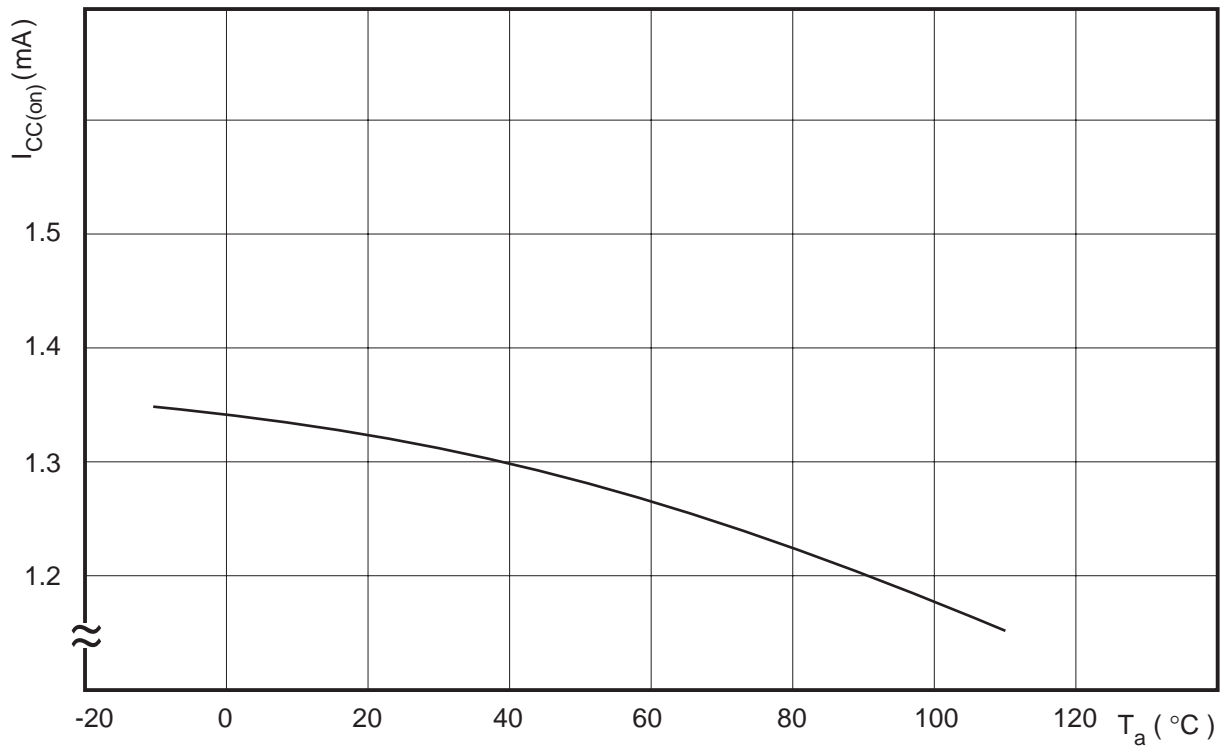
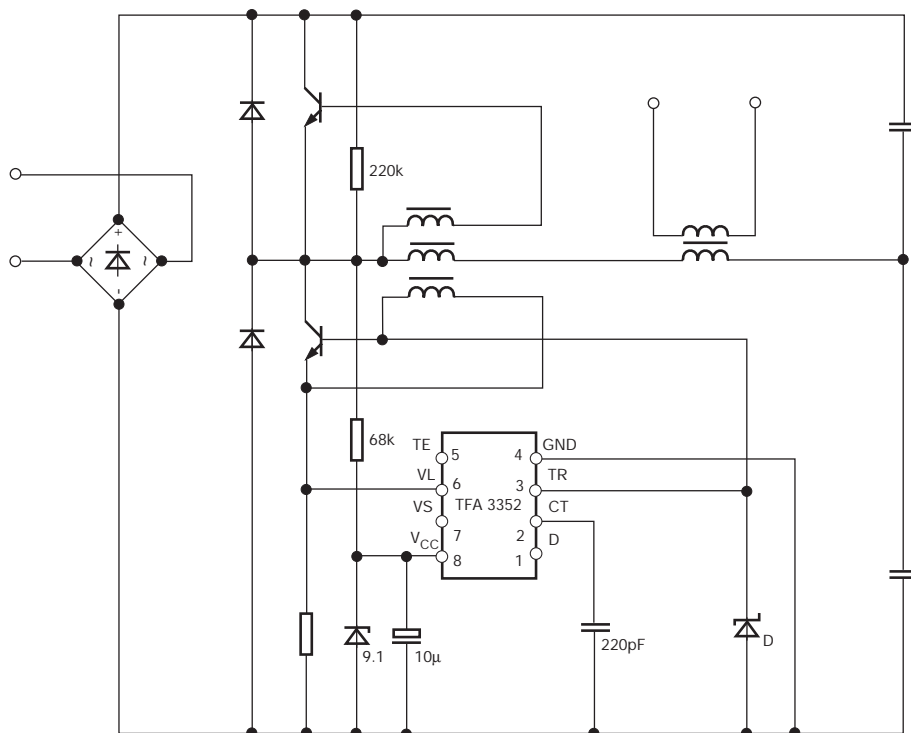## AC voltage overload threshold versus temperature with V_{CC} = 9 V and statical overload signal

DC voltage overload threshold versus temperature with V_{CC} = 9 V and statical overload signal
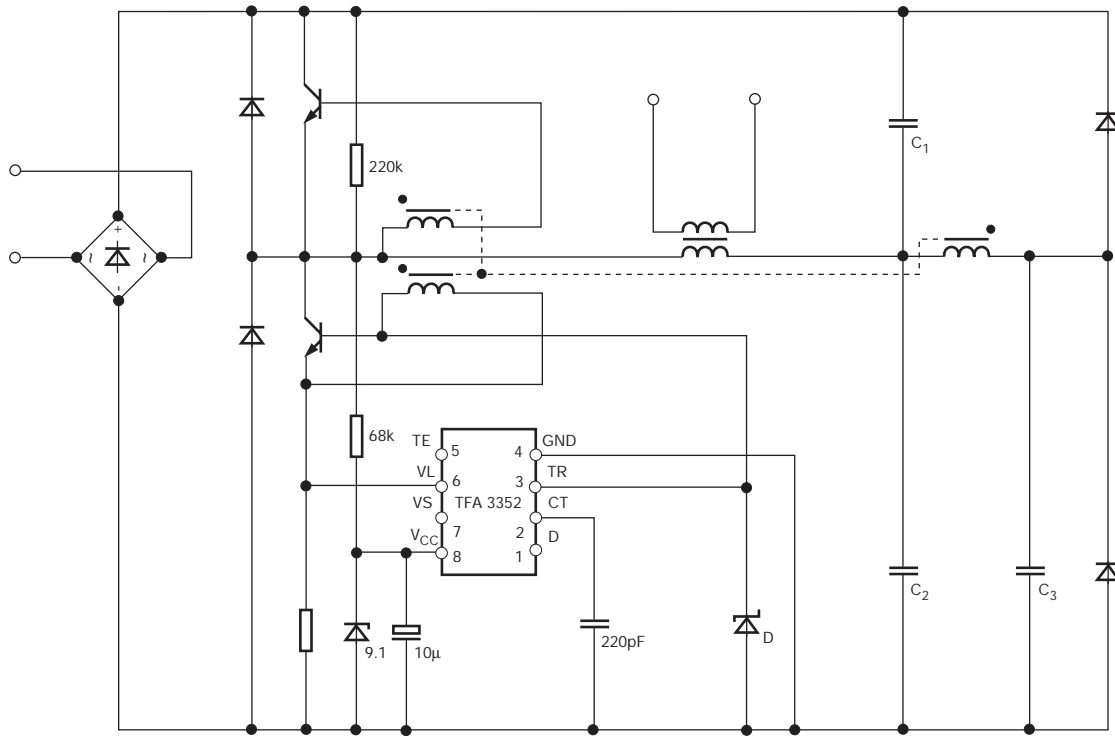
Application Circuit in Principle

Application Example 1

Minimized circuitry with following features:

- overtemperature-, overload- and short circuit protection
- oscillation detection
- no dim mode
- no overvoltage blanking
- DC supply mode (no zero crossing detection via pin VS)
  (overload threshold 490 mV)

Application Example 2

This modified circuitry allows the reducing of load at pin TR during negative voltage spikes in case of short circuit. That circuitry also influences the symmetry of the output voltage.

Dimension hints:
$$C_2 + C_3 \approx C_1$$
$$C_2 < C_3$$