Freescale Semiconductor
Technical Data

Document Number: MHL21336NN
Rev. 0, 12/2006

RoHS

3G Band
RF Linear LDMOS Amplifier

MHL21336NN

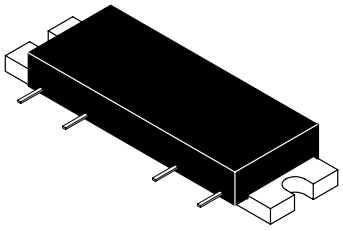
Designed for ultra-linear amplifier applications in 50 ohm systems operating in the 3G frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital CDMA modulation systems.

- Third Order Intercept: 45 dBm Typ
- Power Gain: 31 dB Typ (@ f = 2140 MHz)
- Input VSWR ≤ 1.5:1

Features

- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications
- RoHS Compliant

2110-2170 MHz
3.0 W, 31 dB
RF LINEAR LDMOS AMPLIFIER



CASE 301AP-02, STYLE 1

Table 1. Absolute Maximum Ratings (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	30	Vdc
RF Input Power	P_{in}	+5	dBm
Storage Temperature Range	T_{stg}	- 40 to +100	°C
Operating Case Temperature Range	T_C	- 20 to +100	°C

Table 2. Electrical Characteristics (V_{DD} = 26 Vdc, T_C = 25°C; 50 Ω System)

Characteristic		Symbol	Min	Typ	Max	Unit
Supply Current		I_{DD}	—	500	525	mA
Power Gain	(f = 2140 MHz)	G_p	30	31	33	dB
Gain Flatness	(f = 2110 - 2170 MHz)	G_F	—	0.15	0.4	dB
Power Output @ 1 dB Compression	(f = 2140 MHz)	P1dB	34	35	—	dBm
Third Order Intercept (f1 = 2137 MHz, f2 = 2142 MHz)		ITO	44	45	—	dBm
Noise Figure	(f = 2170 MHz)	NF	—	4.5	5	dB

NOTE - **CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

LIFETIME BUY

LAST ORDER 31 DEC 07 LAST SHIP 30 JUN 08

freescale semiconductor

TYPICAL CHARACTERISTICS

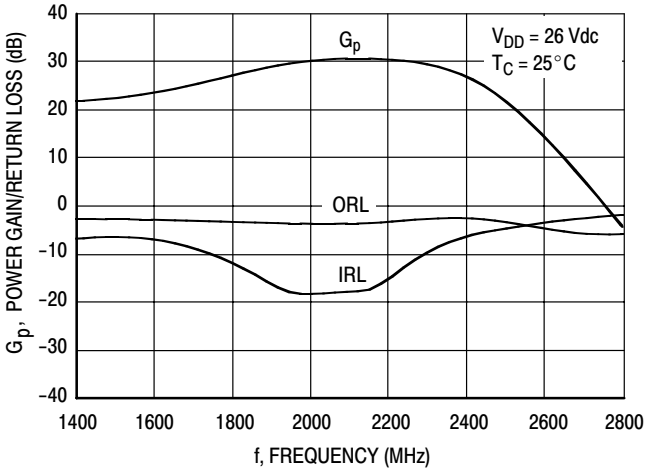


Figure 1. Power Gain, Input Return Loss, Output Return Loss versus Frequency

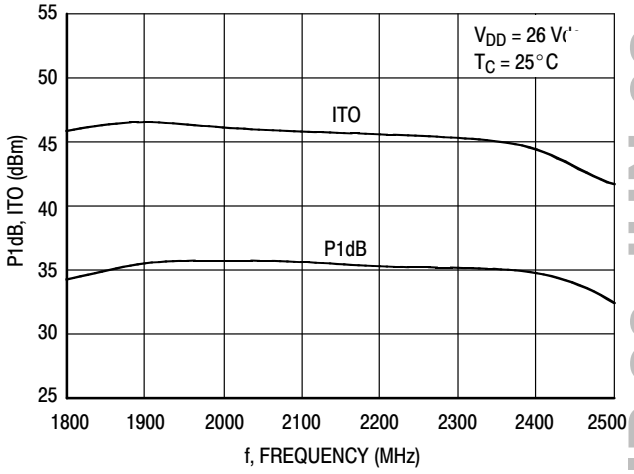


Figure 2. P1dB, ITO versus Frequency

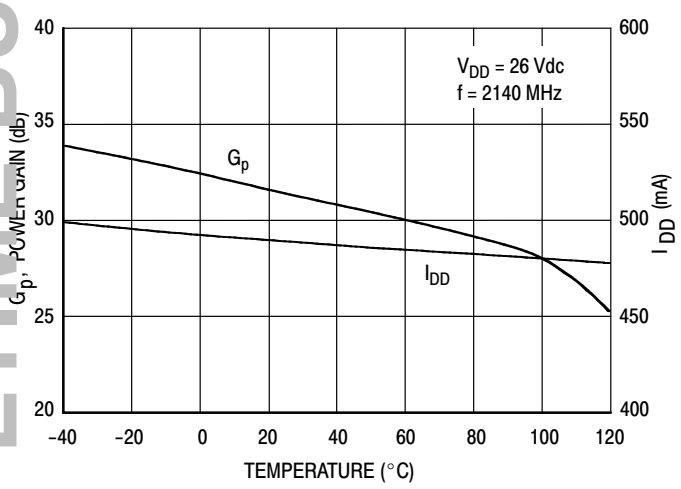


Figure 3. Power Gain, I_{DD} versus Temperature

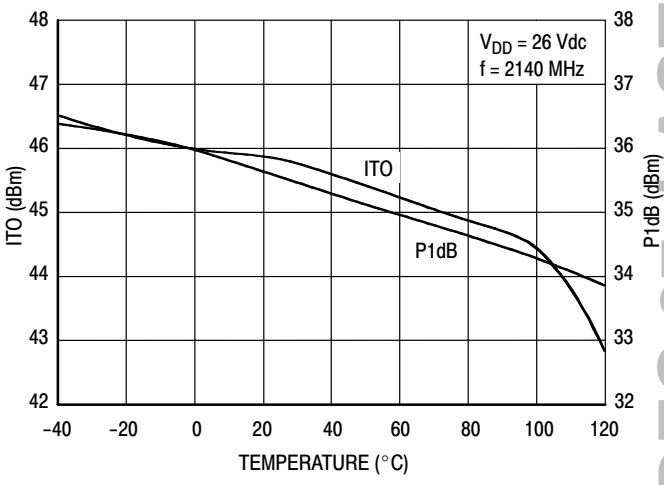


Figure 4. ITO, P1dB versus Temperature

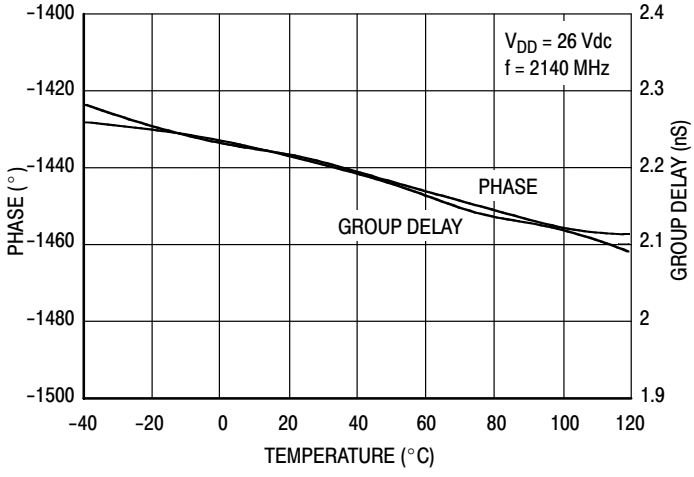


Figure 5. Phase(1), Group Delay(1) versus Temperature

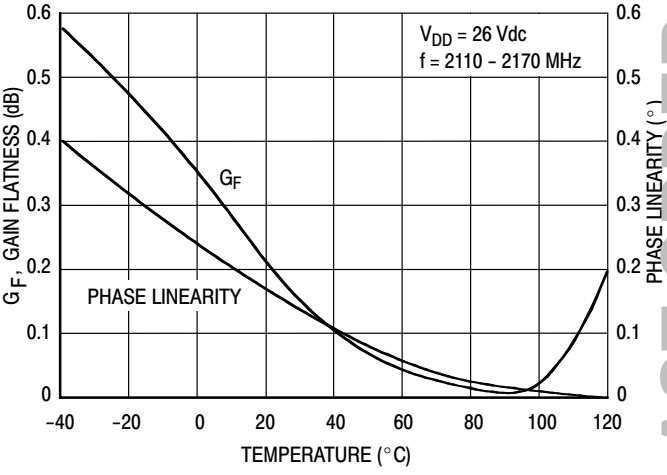


Figure 6. Gain Flatness, Phase Linearity versus Temperature

1. In Production Test Fixture

TYPICAL CHARACTERISTICS

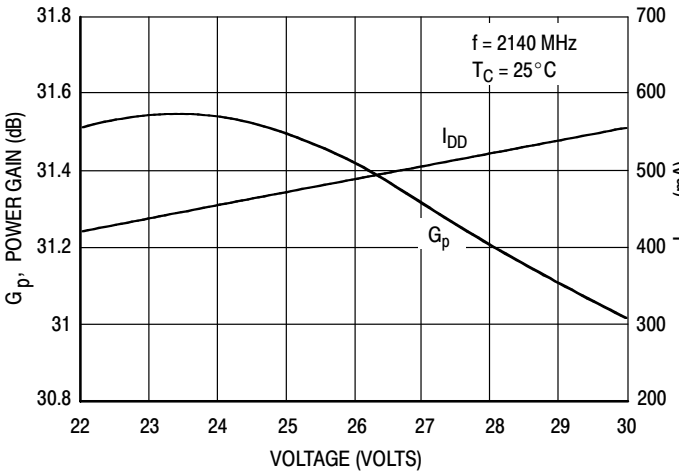


Figure 7. Power Gain, I_{DD} versus Voltage

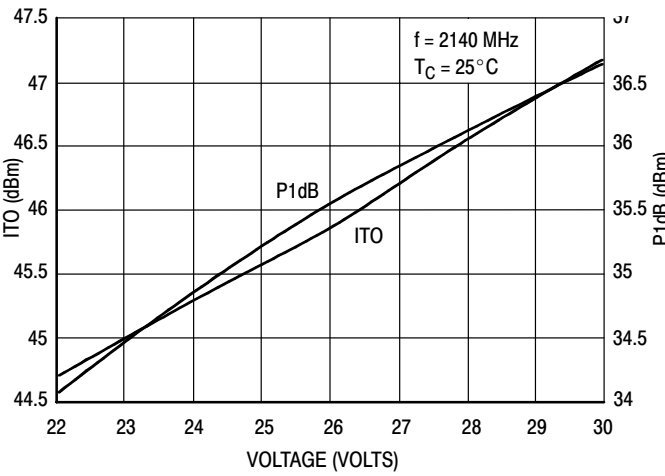


Figure 8. ITO, P1dB versus Voltage

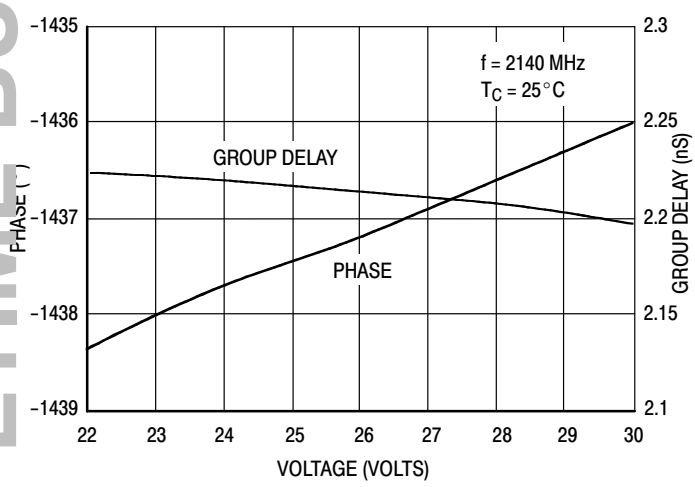


Figure 9. Phase(1), Group Delay(1) versus Voltage

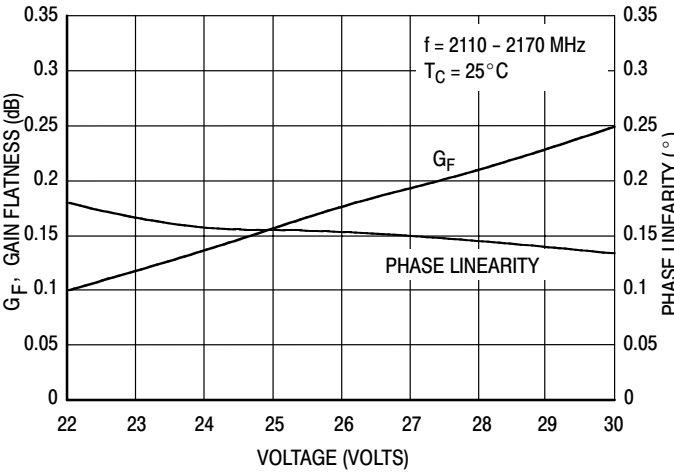
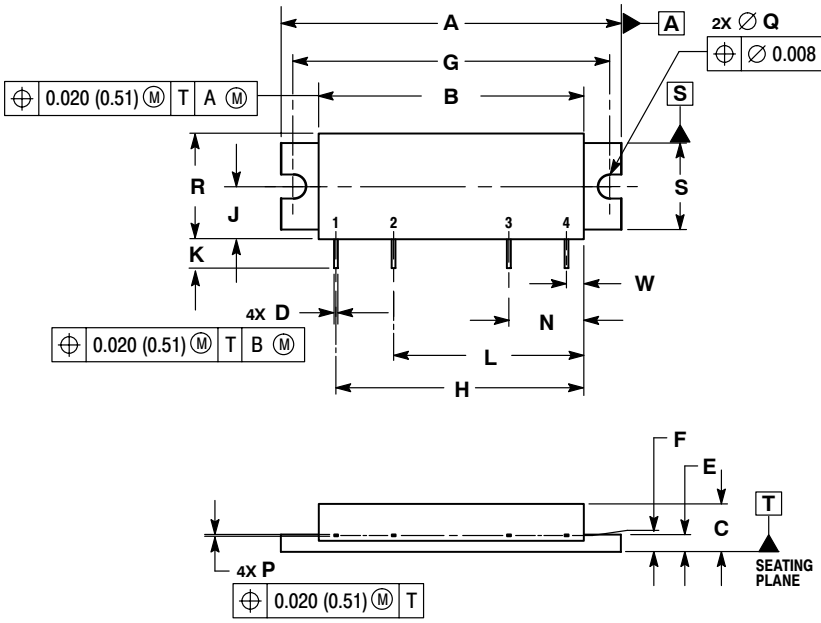


Figure 10. Phase Linearity, Gain Flatness versus Voltage

1. In Production Test Fixture

PACKAGE DIMENSIONS



NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "F" TO CENTER OF LEADS.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.760	1.780	44.70	45.21
B	1.370	1.390	34.80	35.31
C	0.245	0.265	6.22	6.73
D	0.017	0.023	0.43	0.58
E	0.080	0.100	2.03	2.54
F	0.086 BSC		2.18 BSC	
G	1.650 BSC		41.91 BSC	
H	1.290 BSC		32.77 BSC	
J	0.266	0.280	6.76	7.11
K	0.125	0.165	3.18	4.19
L	0.990 BSC		25.15 BSC	
N	0.390 BSC		9.91 BSC	
P	0.008	0.013	0.20	0.33
Q	0.118	0.132	3.00	3.35
R	0.535	0.555	13.59	14.10
S	0.445	0.465	11.30	11.81
W	0.090 BSC		2.29 BSC	

STYLE 1:
PIN 1. RF INPUT
2. VDD1
3. VDD2
4. RF OUTPUT
CASE: GROUND

CASE 301AP-02
ISSUE E

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2006	• Initial Release of Data Sheet

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For information on Freescale’s Environmental Products program, go to http://www.freescale.com/epp.

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