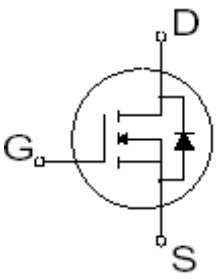
GOOD-ARK

SSFP9N20

StarMOS^T Power MOSFET

- Extremely high dv/dt capability
- Low Gate Charge Qg results in Simple Drive Requirement
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



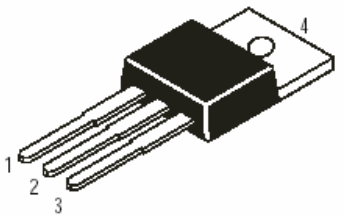
V_{DSS} = 200V

I_{D25} =9A

$R_{DS(ON)}$ =0.4 Ω

Description

StarMOS is a new generation of high voltage N–Channel enhancement mode power MOSFETs. This new technology minimises the JFET effect, increases packing density and reduces the on-resistance. StarMOS also achieves faster switching speeds through optimised gate layout with planar stripe DMOS technology.



Pin1–Gate
Pin2–Drain
Pin1–Source

Application

- Switching application

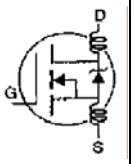
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D@Tc=25˚C	Continuous Drain Current,V_{GS}@10V	9.0	A
I_D@Tc=100˚C	Continuous Drain Current,V_{GS}@10V	5.7	
I_{DM}	Pulsed Drain Current ①	36	
P_D@Tc=25˚C	Power Dissipation	74	W
	Linear Derating Factor	0.59	W/˚C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	250	mJ
I_{AR}	Avalanche Current ①	9.0	A
E_{AR}	Repetitive Avalanche Energy ①	7.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	－55 to +150	℃
	Soldering Temperature, for 10 seconds	300(1.6mm from case)	
	Mounting Torque,6-32 or M3 screw	10 lbf•in(1.1N•m)	

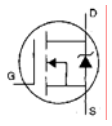
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case	—	—	1.7	℃/W
$R_{\theta CS}$	Case-to-Sink,Flat,Greased Surface	—	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

Electrical Characteristics @T_J=25℃(unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS}=0V,I_D=250μA
△$V_{(BR)DSS}$/△T_J	Breakdown Voltage Temp.Coefficient	—	0.24	—	V/℃	Reference to 25℃,I_D=1mA
$R_{DS(on)}$	Static Drain-to-Source On-resistance	—	—	0.4	Ω	V_{GS}=10V,I_D=5.4A
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS},I_D=250μA
gfs	Forward Transconductance	3.8	—	—	S	V_{DS}=50V,I_D=5.4A
I_{DSS}	Drain-to-Source Leakage current	—	—	25	μA	V_{DS}=200V,V_{GS}=0V
		—	—	250		V_{DS}=160V,V_{GS}=0V,T_J=125℃
I_{GSS}	Gate-to-Source Forward leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse leakage	—	—	-100		V_{GS}=-20V
Qg	Total Gate Charge	—	—	43	nC	I_D=5.9A
Qgs	Gate-to-Source charge	—	—	7.0		V_{DS}=160V
Qgd	Gate-to-Drain("Miller") charge	—	—	23		V_{GS}=10V
td(on)	Turn-on Delay Time	—	9.4	—	nS	V_{DD}=100V
tr	Rise Time	—	28	—		I_D=5.9A
td(off)	Turn-Off Delay Time	—	39	—		R_G=12Ω
tf	Fall Time	—	20	—		R_D=16Ω See Figure 10④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm(0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
Ciss	Input Capacitance	—	800	—	pF	V_{GS}=0V
Coss	Output Capacitance	—	240	—		V_{DS}=25V
Crss	Reverse Transfer Capacitance	—	76	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	9.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	36		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	T_J=25℃,I_S=9.0A,V_{GS}=0V ④
trr	Reverse Recovery Time	—	170	340	nS	T_J=25℃,I_F=59A
Qrr	Reverse Recovery Charge	—	1.1	2.2	nC	di/dt=100A/μs ④
ton	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by Ls + L_D)				

Notes:

① Repetitive rating;pulse width limited by max.junction temperature(see figure 11)

② L =4.6mH, I_{AS} = 9.0A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C

③ I_{SD}≤9.0A,di/dt≤120A/μS,V_{DD}≤$V_{(BR)DSS}$, TJ≤150℃

④ Pulse width≤300μS; duty cycle≤2%