RHF1401

Rad-hard 14-bit 20Msps 85mW A/D converter

Features

- Ssingle +2.5V supply operation
- Low power: 85mW @ 20Msps
- High linearity: +/- 0.3 bit DNL
- SFDR = 90dB typ. SINAD = 73dB typ. @ F_s = 20Msps, F_{in} = 5MHz
- 2.5V/3.3V compatible digital I/O
- Switchable on/off built-in reference voltage
- Hermetic package
- Rad-hard: 300kRad(Si) TID
- Failure immune (SEFI) and latchup immune (SEL) up to 120 MeV-cm^2/mg at 2.7V and 125°C
- Qml-V qualification on-going, smd 5962-06260

Applications

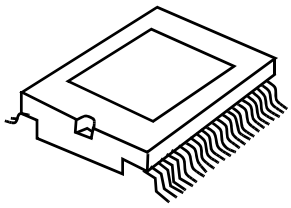
- Digital communication satellites
- Space data acquisition systems
- Aerospace instrumentation
- Nuclear and high-energy physics

Description

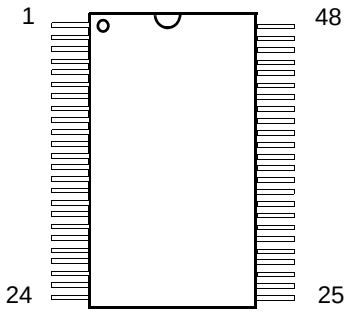
The RHF1401 is a 14-bit, 20MHz maximum sampling frequency analog-to-digital converter using pure (ELDRS-free) CMOS 0.25µm technology combining high performance, radiation robustness and very low power consumption.

The RHF1401 is based on a pipeline structure and digital error correction to provide excellent static linearity. Its very low internal noise permits to achieve more than 11.8 ENOB with a 2.2V_{pp} 5MHz input.

SO-48 package



Pin connections (top view)



Specifically designed for optimizing power consumption, the RHF1401 only dissipates 85mW at 20Msps, while maintaining a high level of performance. It integrates a proprietary track-and-hold structure to ensure an effective resolution bandwidth of 70MHz.

A voltage reference is integrated in the circuit to simplify the design and minimize external components. A tri-state capability is available on the outputs, to allow common bus sharing.

A data-ready signal which is raised when the data is valid on the output can be used for synchronization purposes.

The RHF1401 has an operating temperature range of -55°C to +125°C and is available in a small 48-pin hermetic SO-48 package.

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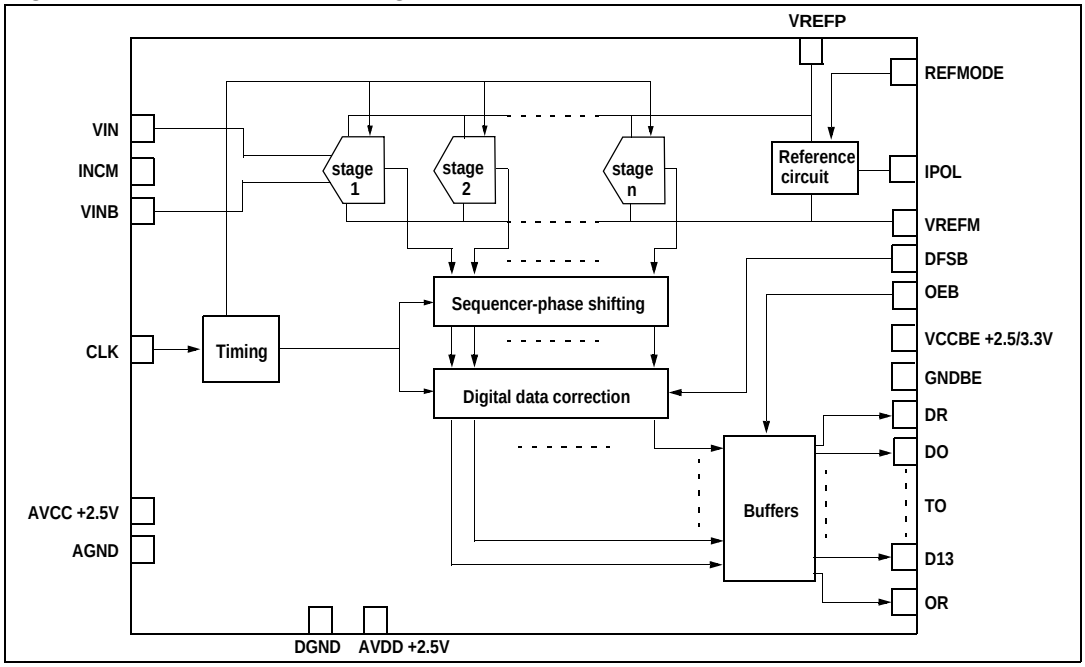
1 Block diagram

Figure 1. RHF1401 block diagram



2 Pinout

Figure 2. S0-48 pin connections (top view)

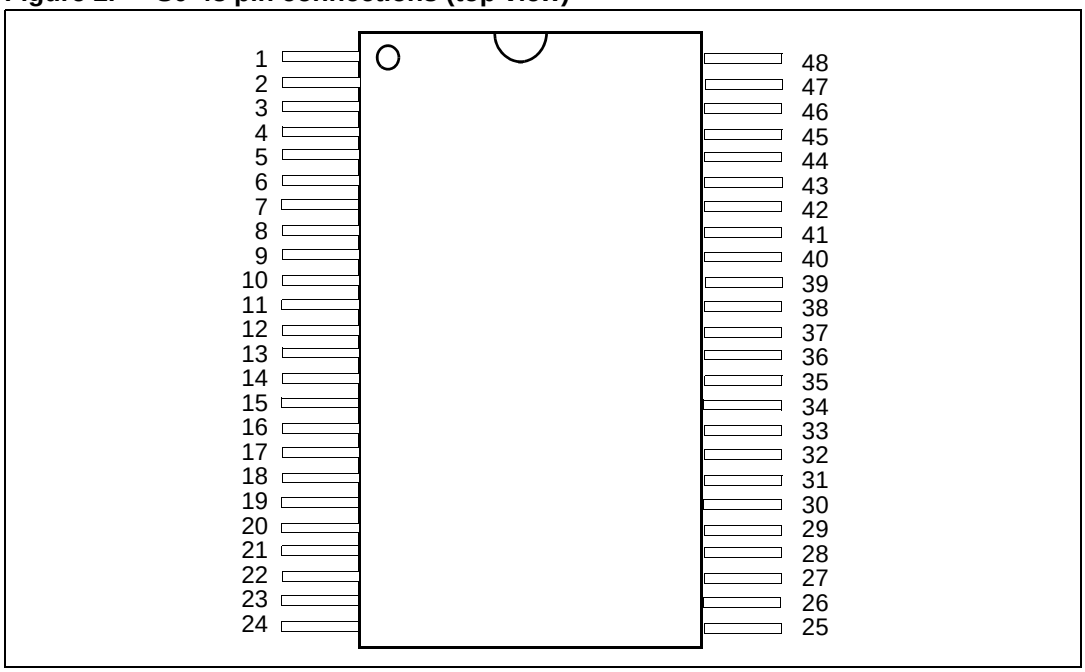


Table 1. Pin descriptions

Pin	Name	Description	Observations	Pin	Name	Description	Observations
1	GNDBI	Digital buffer ground	0 V	25	REFMODE	Ref. mode control input	2.5 V/3.3 V CMOS input
2	GNDBE	Digital buffer ground	0 V	26	OEB	Output enable input	2.5 V/3.3 V CMOS input
3	VCCBE	Digital buffer power supply	2.5 V/3.3 V	27	DFSB	Data format select input	2.5 V/3.3 V CMOS input
4		NC	Non connected	28	AVCC	Analog power supply	2.5 V
5		NC	Non connected	29	AVCC	Analog power supply	2.5 V
6	OR	Out of range output	CMOS output (2.5 V/3.3 V)	30	AGND	Analog ground	0 V
7	D13(MSB)	Most significant bit output	CMOS output (2.5 V/3.3 V)	31	IPOL	Analog bias current input	
8	D12	Digital output MSB	CMOS output (2.5 V/3.3 V)	32	VREFP	Top voltage reference	1 V
9	D11	Digital output	CMOS output (2.5 V/3.3 V)	33	VREFM	Bottom voltage reference	0 V
10	D10	Digital output	CMOS output (2.5 V/3.3 V)	34	AGND	Analog ground	0 V
11	D9	Digital output	CMOS output (2.5 V/3.3 V)	35	VIN	Analog input	1 V_{pp}
12	D8	Digital output	CMOS output (2.5 V/3.3 V)	36	AGND	Analog ground	0 V
13	D7	Digital output	CMOS output (2.5 V/3.3 V)	37	VINB	Inverted analog input	1 V_{pp}
14	D6	Digital output	CMOS output (2.5 V/3.3 V)	38	AGND	Analog ground	0 V
15	D5	Digital output	CMOS output (2.5 V/3.3 V)	39	INCM	Input common mode	0.5 V
16	D4	Digital output	CMOS output (2.5 V/3.3 V)	40	AGND	Analog ground	0 V
17	D3	Digital output	CMOS output (2.5V /3.3 V)	41	AVCC	Analog power supply	2.5 V
18	D2	Digital output	CMOS output (2.5 V/3.3 V)	42	AVCC	Analog power supply	2.5 V
19	D1	Digital output	CMOS output (2.5 V/3.3 V)	43	DVCC	Digital power supply	2.5 V
20	D0(LSB)	Digital output LSB	CMOS output (2.5 V/3.3 V)	44	DVCC	Digital power supply	2.5 V
21	DR	Data ready output(1)	CMOS output (2.5 V/3.3 V)	45	DGND	Digital ground	0 V
22	VCCBE	Digital buffer power supply	2.5 V/3.3 V	46	CLK	Clock input	2.5 V compatible CMOS input
23	GNDBE	Digital buffer ground	0 V	47	DGND	Digital ground	0 V
24	VCCBI	Digital buffer power supply	2.5 V	48	DGND	Digital ground	0 V

1. See load considerations in *Section 3: Timing*.

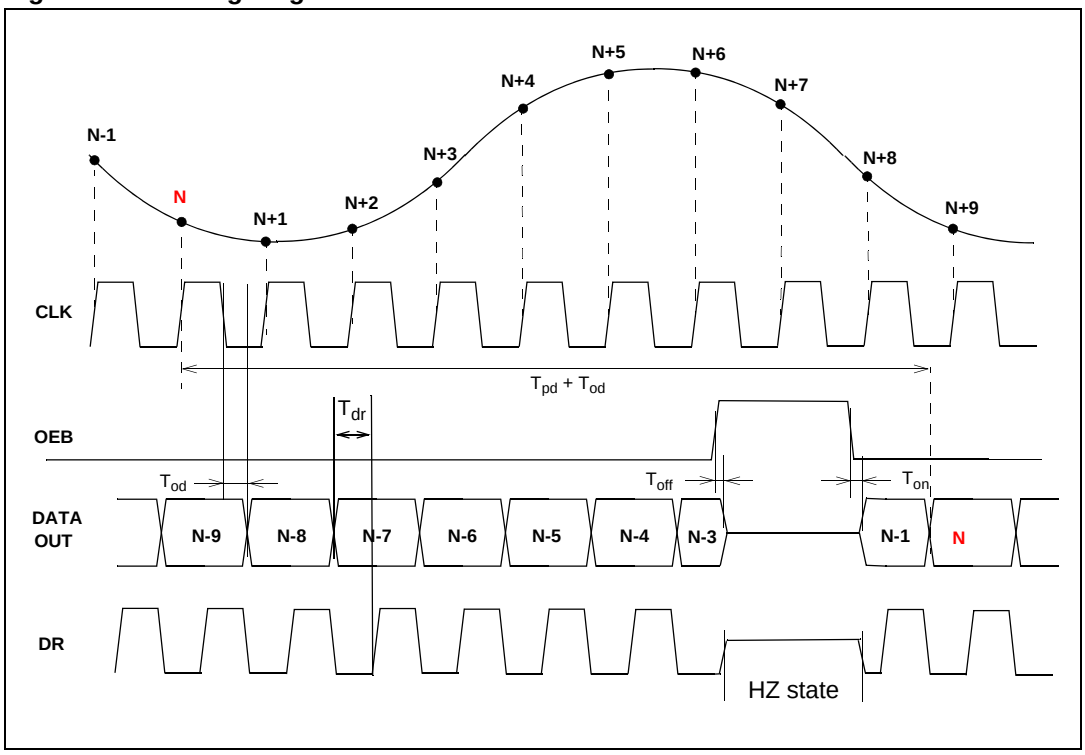
3 Timing

Table 2. Timing characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_s	Sampling frequency(1)		1.5		20	MHz
T_{ck}	Sampling clock cycle(1)		50		667	ns
DC	Clock duty cycle	F_s = 20 Msps		50		%
T_{C1}	Clock pulse width (high)			25		ns
T_{C2}	Clock pulse width (low)			25		ns
T_{od}	Data output delay (fall of clock to data valid) (2)	10 pF load capacitance	5	7.5	13	ns
T_{pd}	Data pipeline delay		8.5	8.5	8.5	cycles
T_{dr}	Data ready rising edge delay after data change			0.5		cycles
T_{on}	Falling edge of OEB to digital output valid data			1		ns
T_{off}	Rising edge of OEB to digital output tri-state			1		ns
T_{rD}	Data rising time	10 pF load capacitance		6		ns
T_{fD}	Data falling time	10 pF load capacitance		3		ns

1. See clock recommendations in *Section 7.2: Clock signal requirements on page 19*
2. See *Figure 3* and discussion below.

Figure 3. Timing diagram



The input signal is sampled on the rising edge of the clock while digital outputs are synchronized on the falling edge of the clock.

Load considerations

The size of the internal output buffers limits the maximum load on the data output signals and Data Ready to 10pF equivalent load. In particular, the shape and amplitude of the Data Ready signal, toggling at the clock frequency can be weakened by a higher equivalent load.

In applications that impose higher load conditions, it is recommended to use the falling edge of the master clock instead of the Data Ready signal. This is possible because the output transitions are internally synchronized with the falling edge of the clock. For implementation information, refer to *Section 7.2: Clock signal requirements on page 19*.

An alternative is to re-buffer the DR signal externally to avoid any risk of modifying the clock signal.

4 Absolute maximum ratings and operating conditions

Table 3. Absolute maximum ratings

Symbol	Parameter	Values	Unit
AV_{CC}	Analog supply voltage(1)	0 to 3.3	V
DV_{CC}	Digital supply voltage(1)	0 to 3.3	V
V_{CCBI}	Digital buffer supply voltage(1)	0 to 3.3	V
V_{CCBE}	Digital buffer supply voltage(1)	0 to 3.6	V
I_{Dout}	Digital output current	-100 to 100	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thjc}	Junction - case thermal resistance	22	°C/W
ESD	Electrostatic discharge – HBM: human body model (2)	2	kV

1. All voltage values, except differential voltage, are with respect to the network ground terminal. The magnitude of input and output voltages must never exceed -0.3 V or V_{CC}+0.3 V.
2. Human body model: 100pF discharged through a 1.5kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.

Table 4. Operating conditions

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
AV_{CC}	Analog supply voltage		2.3	2.5	2.7	V
DV_{CC}	Digital supply voltage		2.3	2.5	2.7	V
V_{CCBI}	Digital internal buffer supply		2.3	2.5	2.7	V
V_{CCBE}	Digital output buffer supply		2.3	2.5	3.4	V
V_{REFP}	Forced top voltage reference		0.5	1	1.4	V
V_{REFM}	Bottom internal reference voltage		0	0	0.5	V

5 Electrical characteristics (unchanged after 300kRad)

Test conditions are the following (unless otherwise specified):

- $AV_{CC} = DV_{CC} = V_{CCB} = 2.5$ V
- $F_s = 20$ Msps
- $F_{in} = 2$ MHz
- V_{in}@ -1 dBSF
- $V_{REFM} = 0$ V
- $T_{amb} = 25°$ C

Table 5. Analog inputs

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IN}-V_{INB}	Full scale reference voltage	V_{REFP}= 1 V		2		V_{pp}
C_{in}	Input capacitance			8		pF
Z_{in}	Input impedance	F_s= 20 Msps		3.3		kOhms
ERB	Effective resolution bandwidth(1)			70		MHz

1. See *Section 8: Definitions of specified parameters on page 24* for more information.

Table 6. Internal references

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
R_{out}	Output resistance of internal ref	REFMODE='0' internal reference on		30		Ohm
		REFMODE='1' internal reference off		7.5		kOhm
V_{REFP}	Top internal reference voltage	REFMODE='0'		0.84		V
V_{REFM}	Bottom internal ref. voltage	REFMODE='0'		0		V
V_{INCM}	Input common mode voltage	REFMODE='0'		0.44		V

Table 7. External references

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{REFP}	Forced top reference voltage	REFMODE='1'	0.8		1.4	V
V_{REFM}	Forced bottom ref. voltage	REFMODE='1'	0		0.2	V
V_{INCM}	Forced common mode voltage	REFMODE='1'	0.4		1	V

Table 8. Static accuracy

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
DNL	Differential non linearity(1)	F_s=1.5 Msps		+/-0.3		LSB
INL	Integral non linearity(2)	F_s=1.5 Msps		+/-2		LSB
	Monotonicity and no missing codes		Guaranteed			

1. See*Figure 13* and *Section 8: Definitions of specified parameters on page 24* for more information.
2. See *Figure 14* and *Section 8: Definitions of specified parameters on page 24* for more information.

Table 9. Digital inputs and outputs

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Clock input						
V_{IL}	Logic "0" voltage	DV_{CC} = 2.5 V	0	0	0.8	V
V_{IH}	Logic "1" voltage	DV_{CC} = 2.5 V	2.0		2.5	V
Digital inputs						
V_{IL}	Logic "0" voltage	V_{CCBE} = 2.5 V	0		0.25 x V_{CCBE}	V
V_{IH}	Logic "1" voltage	V_{CCBE} = 2.5 V	0.75 x V_{CCBE}		V_{CCBE}	V
Digital outputs						
V_{OL}	Logic "0" voltage	I_{OL} = -1 mA		0	0.2	V
V_{OH}	Logic "1" voltage	I_{OH} = 1 mA	V_{CCBE} -0.2			V
I_{OZ}	High impedance leakage current	OEB set to V_{IH}	-15		15	µA
C_L	Output load capacitance				15	pF

Table 10. Dynamic characteristics

Symbol	Parameter[1]	Test conditions	Min	Typ	Max	Unit
SFDR	Spurious free dynamic range	F_{in} = 10 MHz, internal reference		-91		dBFS
		F_{in} = 10 MHz, V_{REFP} =1 V		-89		
SNR	Signal to noise ratio	F_{in} = 10 MHz, internal reference		70		dB
		F_{in}= 10 MHz, V_{REFP} = 1 V		71.5		
THD	Total harmonic distortion	F_{in}= 10 MHz, internal reference		-86		dBc
		F_{in}= 10 MHz, V_{REFP} = 1 V		-85		
SINAD	Signal to noise and distortion ratio	F_{in}= 10 MHz, internal reference		70		dB
		F_{in}= 10 MHz, V_{REFP} = 1 V		71		
ENOB	Effective number of bits	F_{in}= 10 MHz, internal reference		11.5		bits
		F_{in}= 10 MHz, V_{REFP} = 1 V		11.7		

1. See *Section 8: Definitions of specified parameters on page 24* for more information.

Higher values of SNR, SINAD and ENOB can be obtained by increasing the analog input full scale range. This is illustrated in *Figure 11 on page 13*, *Figure 18*, and *Figure 19 on page 17* with V_{REFP}= 1.25V, and also in *Figure 15* and *Figure 16 on page 16* with V_{REFP} up to 1.4V.

6 Typical performance characteristics

Because of its intrinsic high-speed low-power capabilities, most of the characterization measurements for the RHF1401 were done in the analog frequency range from 1MHz to 100MHz.

An evaluation board designed to operate in this range, and including a transformer to generate on-board differential signals to input to the RHF1401 was used in characterization testing. This configuration is illustrated in *Figure 21 on page 18*.

For best performance, the RHF1401 also requires a high enough sampling frequency or, in other terms, that the clock period is not too long, to avoid current leakage which would impact conversion accuracy. The recommended lowest sampling frequency is 1.5Msps. Note that under 1.2Msps, the RHF1401 performance is degraded. For more information on sampling frequency, see *Section 7.2: Clock signal requirements*, and *Section 7.3: Power consumption optimization*.

Figure 4. Linearity vs. F_{in}, internal references, F_S = 20 MHz, I_{cca} = 40 mA

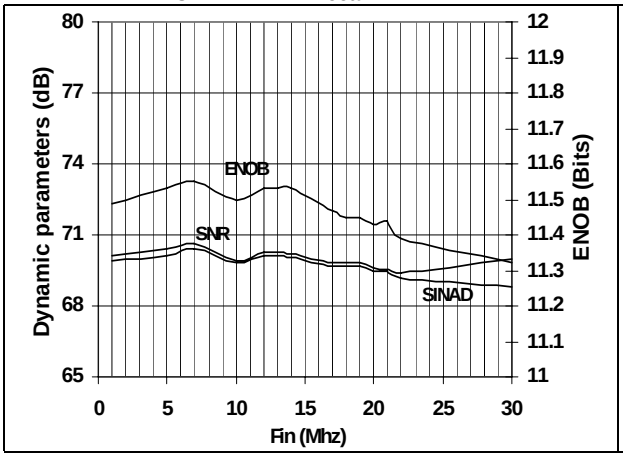


Figure 5. Linearity vs. F_{in}, external references (REFP = 1 V), F_S = 20 MHz, I_{cca}= 28 mA

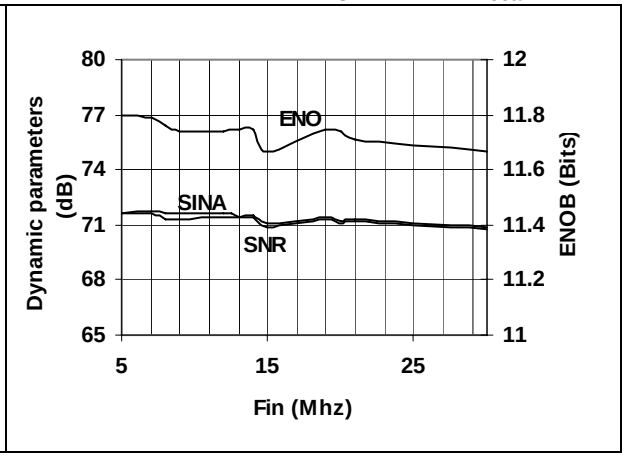


Figure 6. Distortion vs. F_{in}, internal refs, F_S = 20 MHz, I_{cca} = 40 mA

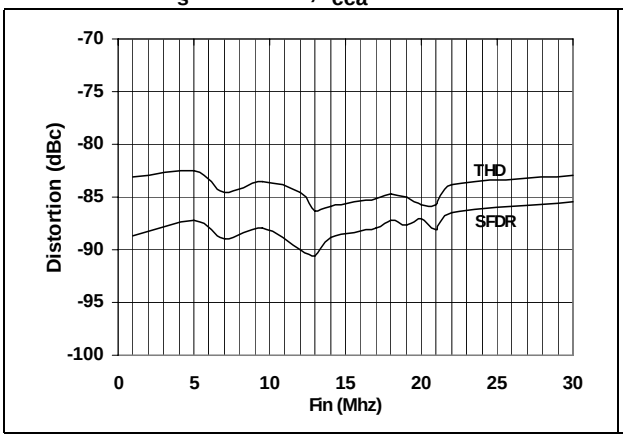


Figure 7. Distortion vs. F_{in}, external ref, (REFP = 1 V) F_S = 20 MHz; I_{cca} = 28 mA

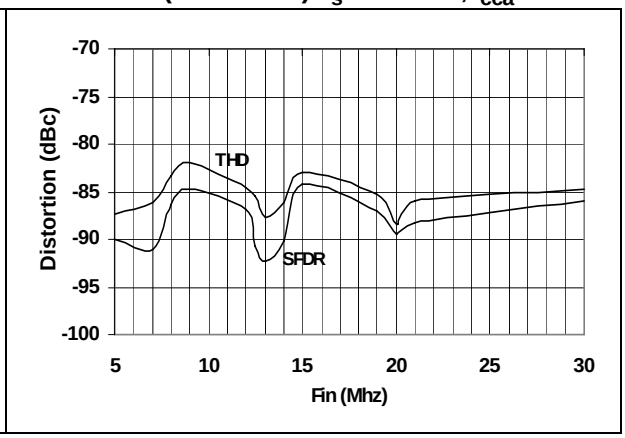


Figure 8. 2^{nd} & 3^{rd} harmonics vs. F_{in}, internal refs, F_S = 20 MHz; I_{cca} = 40 mA

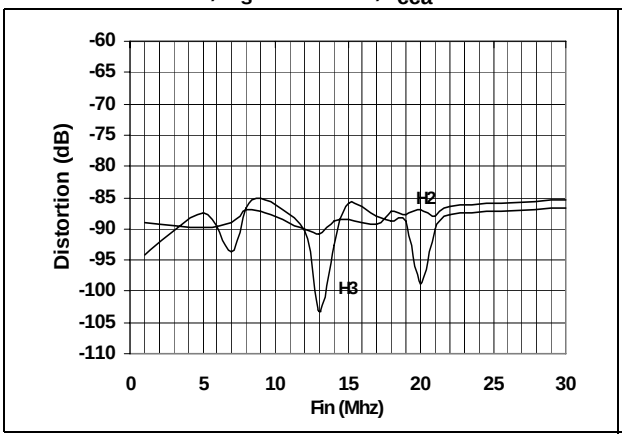


Figure 9. 2^{nd} & 3^{rd} harmonics vs. F_{in}, external ref REFP=1 V, F_S=20MHz; I_{cca}=28mA

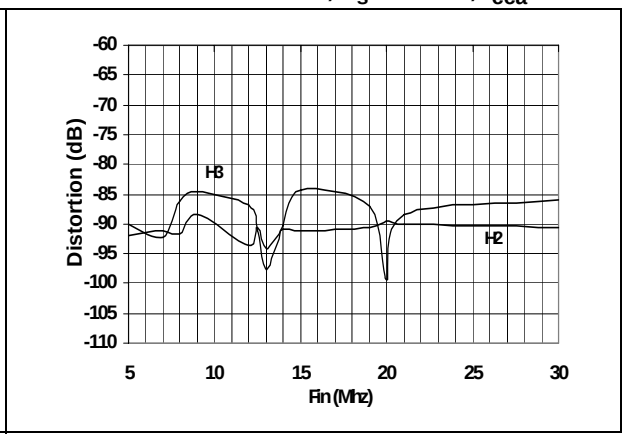
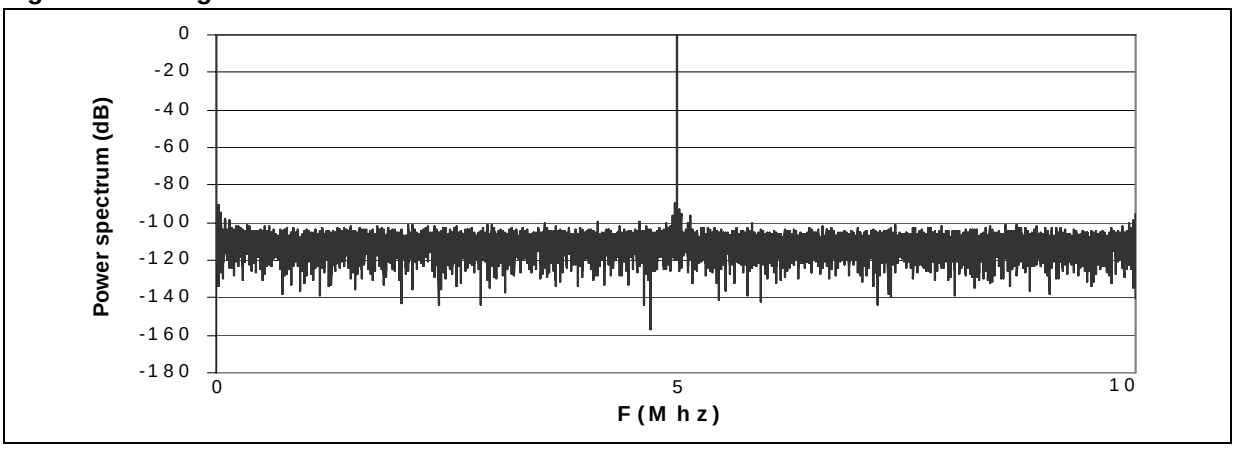
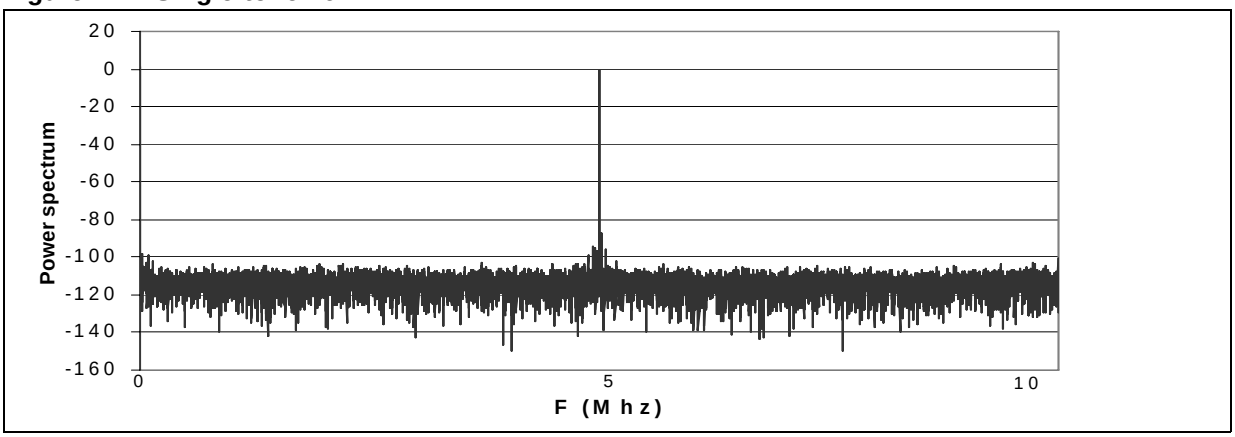


Figure 10. Single-tone 16K FFT



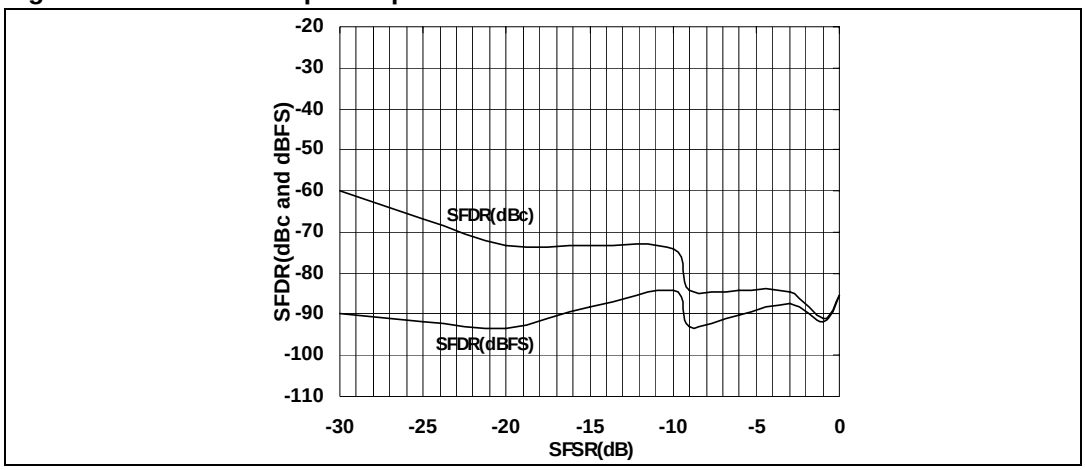
1. At F_S = 20 Msps, internal references, F_{in} = 5 MHz, I_{cca} = 40 mA, V_{in}@-1 dBFS, SFDR = -89.3 dBc, THD = -84.5 dBc, SNR = 70.5 dB, SINAD = 70.3 dB, ENOB = 11.5 bits

Figure 11. Single-tone 16K FFT



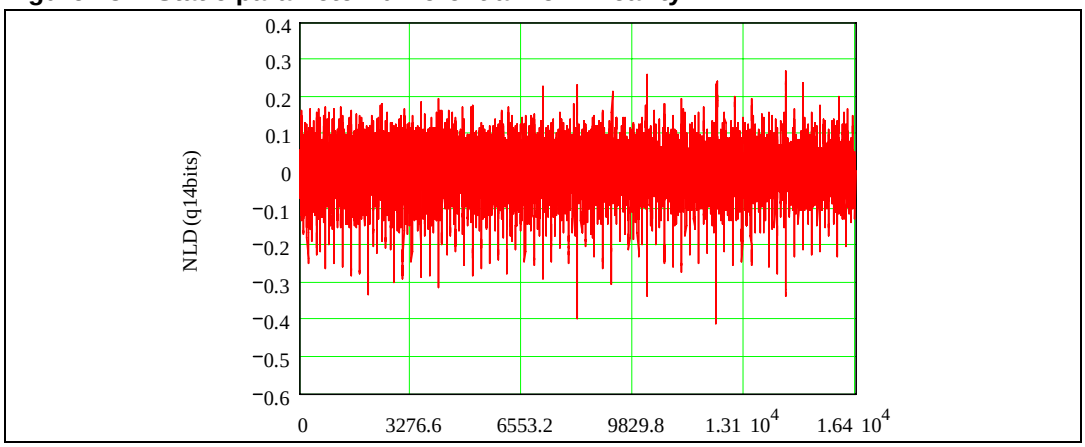
1. At F_S=20 Msps, external references, F_{in}= 5 MHz, I_{cca}= 40 mA, V_{in}@-1 dBFS, V_{REFP}= 1.25V, SFDR = -87.5 dBc, THD = -85.4 dBc, SNR = 73.3 dB, SINAD = 73 dB, ENOB = 11.84 bits

Figure 12. SFDR vs. input amplitude



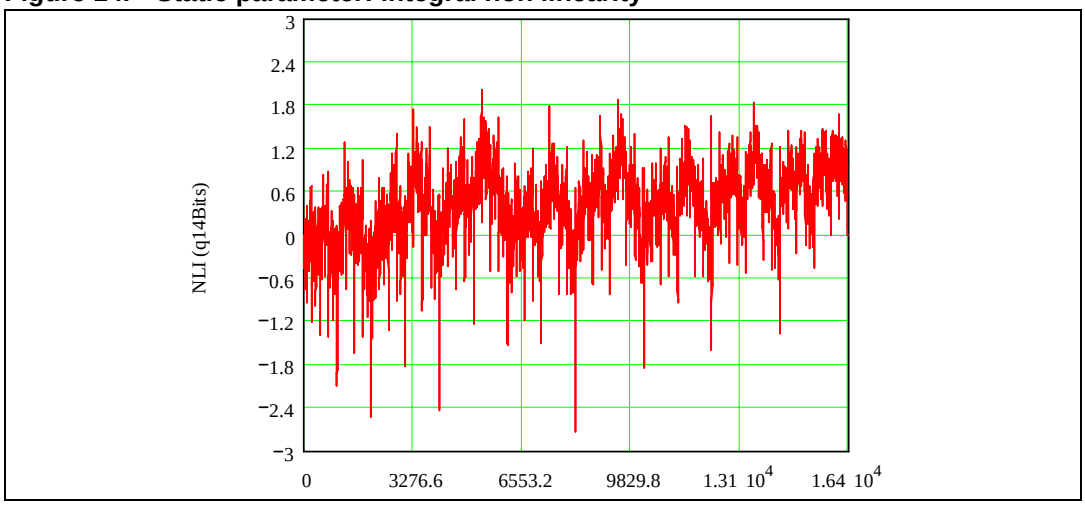
1. (Full scale = 2 x 0.86 V), F_s = 20 Msps, F_{in} = 5 MHz, I_{cca} = 40 mA

Figure 13. Static parameter: differential non linearity



1. F_s = 1.5 Msps acquisition over 128 DC linear ramping input signals

Figure 14. Static parameter: integral non linearity



1. F_s = 1.5 Msps acquisition over 128 DC linear ramping input signals

7 Application information

The RHF1401 is a high speed analog-to-digital converter based on a pipeline architecture and the ST 0.25µm CMOS process in order to achieve the best performance in terms of linearity, power consumption and radiation hardness.

The pipeline structure consists of 14 internal conversion stages in which the analog signal is fed and sequentially converted into digital data.

Each of the first 13 stages consists of an **analog to digital converter**, a **digital to analog converter**, a **sample and hold** and an **amplifier with a gain of 2**. A 1.5-bit conversion resolution is done at each stage. The last stage is a 2-bit flash ADC. Each resulting LSB-MSB couple is then time-shifted to recover from the delay caused by conversion. Digital data correction completes the processing by recovering from the redundancy of the (LSB-MSB) couple for each stage. The corrected data is output through the digital buffers.

Signal input is sampled on the rising edge of the clock while digital outputs are synchronized on the falling edge of the clock.

The advantages of this converter reside in the combination of a SEFI-free pipeline architecture and advanced low-voltage CMOS technology. The highest dynamic performance is achieved while consumption remains at the lowest level.

7.1 Analog input configuration

7.1.1 Setting the analog input range and references

To optimize the high resolution and speed of the RHF1401, we strongly advise you to drive the analog input differentially. The half full-scale of RHF1401 is adjusted through the voltage values of V_{REFP} and V_{REFM}:

$$V_{IN} - V_{INB} = \text{Full Scale} = 2(V_{REFP} - V_{REFM})$$

The differential analog input signal always has a common mode voltage of:

$$V_{CM} = \frac{V_{IN} + V_{INB}}{2}$$

To select the references according to the constraints of your particular application, a control pin, REFMODE, allows you to switch from internal to external references.

Internal references, common mode:

When REFMODE is set to V_{IL} level, the RHF1401 operates with its own reference voltage generated by its internal bandgap. If the VREFM pin is connected externally to the analog ground while VREFP is set to its internal voltage (0.86 V), the full scale of the ADC is 2 x 0.86 = 1.72V.

In this case, VREFP, VREFM and INCM are low impedance outputs. The INCM pin (voltage generator 0.46 V) may be used to supply the common mode, CM, of the analog input signal.

External references, common mode:

In applications that require a different full scale magnitude, it is possible to force the VREFP and VREFM pins from an external voltage reference device. In this configuration, the RHF1401 has better performance, as illustrated in *Figure 15* and *Figure 16*.

Setting REFMODE to V_{IH} level will put the internal references in standby mode, turning VREFP, VREFM and INCM into high impedance inputs that have to be forced by external references.

Figure 15. Linearity vs. REFP(1)

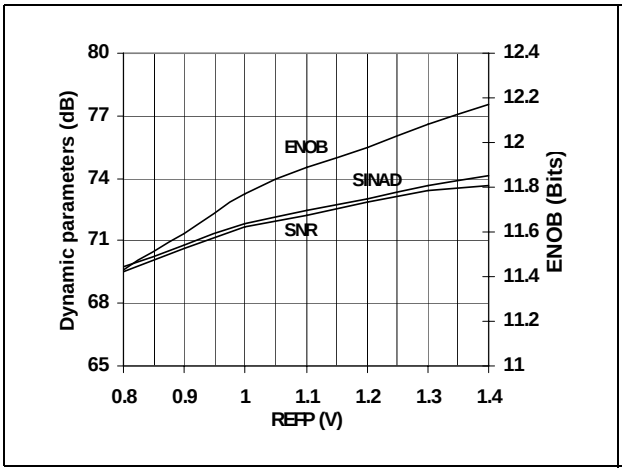
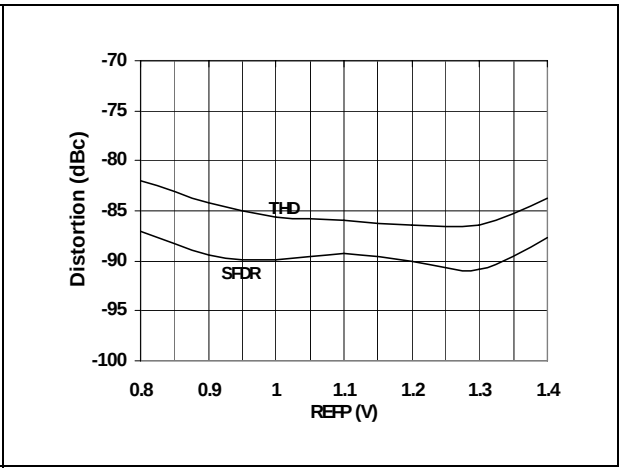


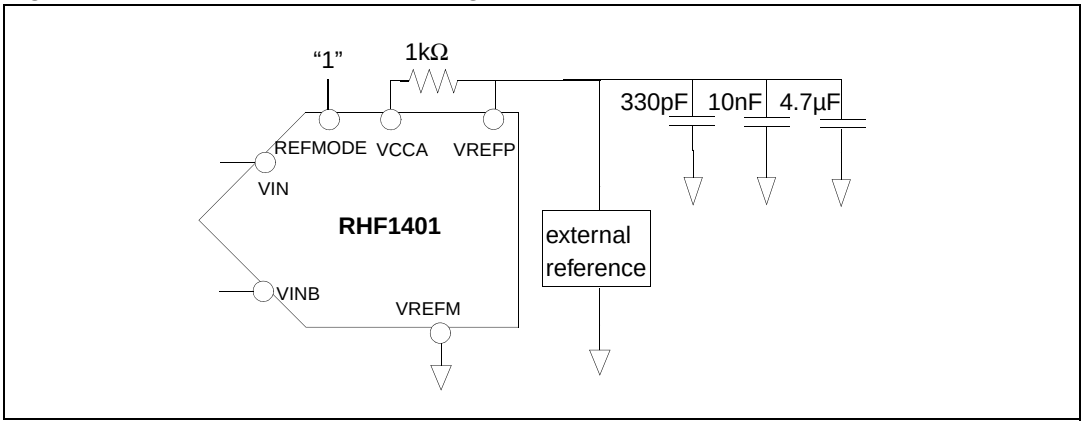
Figure 16. Distortion vs. REFP(1)



1. F_{in} = 5 MHz; F_s = 20 Mhz; I_{cca} = 26 mA; V_{INCM}=0.45 V

Using the RHF1401 with an external voltage reference device yields optimum performance when configured as shown in *Figure 17*.

Figure 17. External reference setting



Note: In multi-channel applications, the high impedance input of the references allows you to drive several ADCs with only one voltage reference device.

In the case of a 1.25V external reference, the full scale is increased to 2.5 V_{pp} differential. The improved dynamic performance is shown in *Figure 18* and *Figure 19*.

Figure 18. Linearity vs. F_S (1)

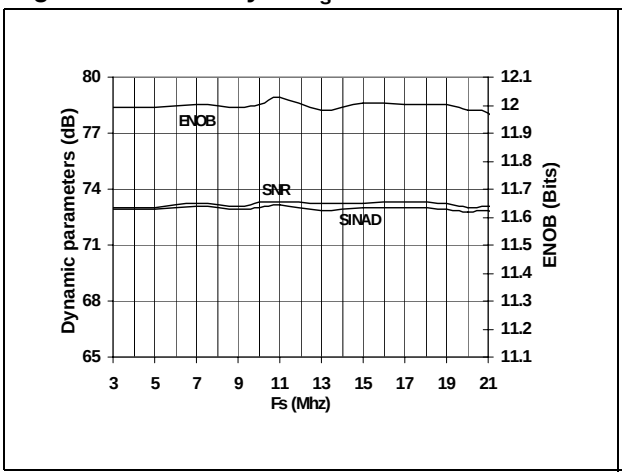
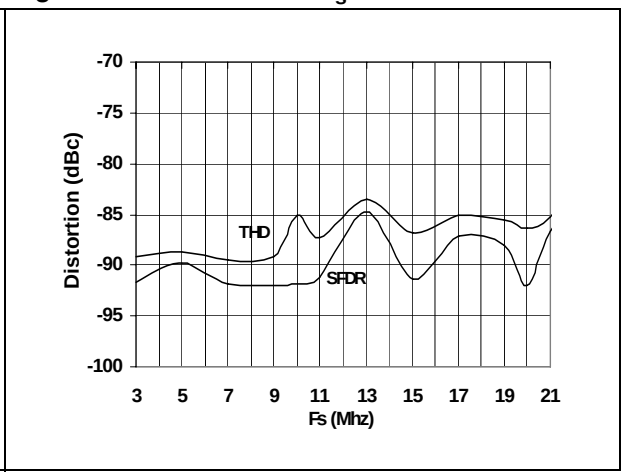


Figure 19. Distortion vs. F_S (1)



1. At F_{in} = 5 MHz, using external REFP = 1.25 V, I_{cca} optimized, V_{INCM} = 0.65 V

The magnitude of the analog input common mode, CM should stay close to $V_{REFP}/2$. Higher levels will introduce more distortion.

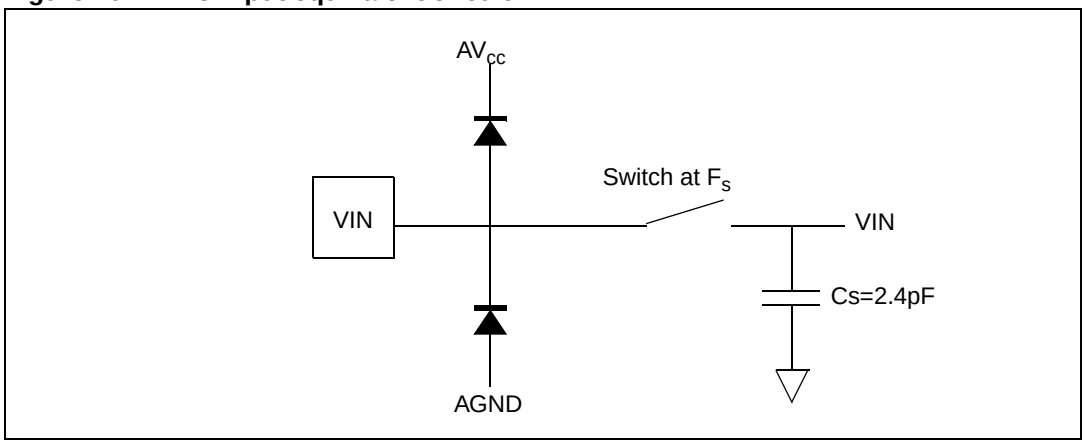
7.1.2 Driving the analog inputs

The RHF1401 is designed to be differentially driven for better noise immunity. Measurements done with single-ended signals show reduced levels of performance.

The switch-capacitor input structure of RHF1401 has a high input impedance (3.3 kΩ at F_S = 20MHz) but it is not constant in time (see the equivalent input circuit in *Figure 20*) because, at the end of each conversion, the charge update of the sampling capacitor draws or injects a small transient current on the input signal.

One method of masking this transient current is a low-pass RC filter as shown in *Figure 21* and *Figure 22*. A capacitor with a higher value than the sampling capacitor of 2.4 pF, mounted in parallel with the two analog input signals, will absorb the transient glitches.

Figure 20. ADC input equivalent circuit

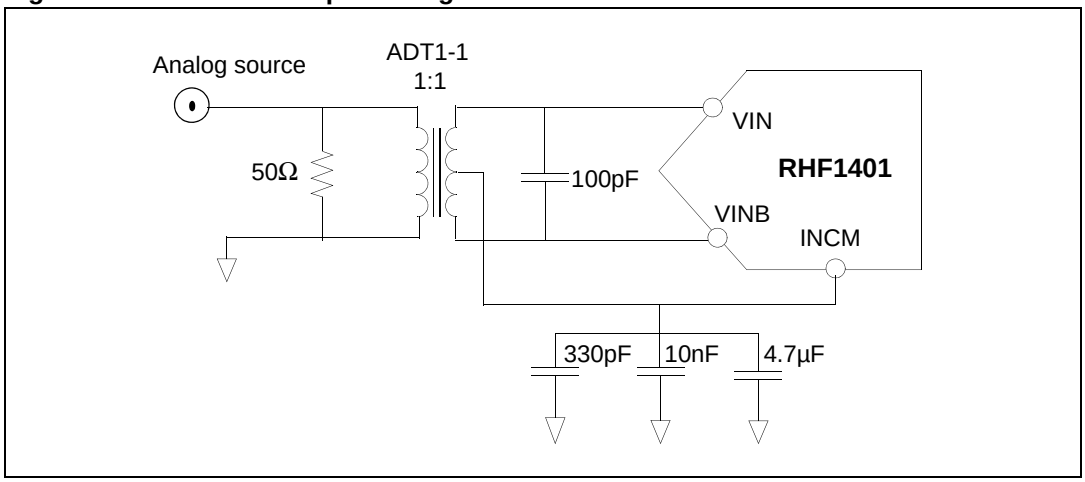


Single-ended signal with transformer

Using an RF transformer is an efficient method of achieving high performance.

Figure 21 shows the schematic view. The input signal is fed to the primary of the transformer, while the secondary drives both ADC inputs.

Figure 21. Differential input configuration with transformer

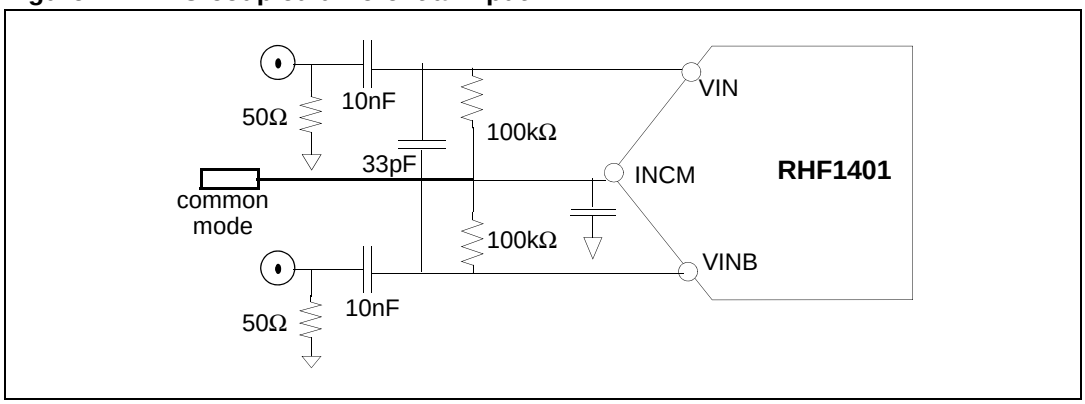


The internal common mode voltage of the ADC (INCM) is connected to the center-tap of the secondary of the transformer in order to bias the input signal around this common voltage, internally set to 0.46 V. The INCM is decoupled to maintain a low noise level on this node. Our evaluation board is mounted with a 1:1 ADT1-1WT transformer from Minicircuits. You might also use a higher impedance ratio (1:2 or 1:4) to reduce the driving requirement on the analog signal source.

AC coupled differential input:

Figure 22 represents the biasing of a differential input signal in AC-coupled differential input configuration. Both inputs V_{IN} and V_{INB} are centered around the common mode voltage CM, that can be forced through INCM or supplied externally (in this case, INCM may be left internal).

Figure 22. AC-coupled differential input



7.2 Clock signal requirements

The signal applied to the CLK pin is critical to obtain full performance from the RHF1401. It is recommended to use a 0V to 2.5V square signal with fast transition times, and to place proper termination resistors as close as possible to the device.

It is the rising edge of the clock signal that determines the sampling instant. The jitter associated with this instant must be as low as possible to avoid SNR degradation on fast moving input signals. To achieve less than 0.5 LSB error, the total jitter T_j must satisfy the following condition for a full scale input signal:

$$T_j < \frac{1}{\pi \cdot F_{in} \cdot 2^{n+1}}$$

For example, the total jitter with 14-bit resolution for a 10 MHz full scale input should be no more than 1 picosecond (rms).

In most cases, it is the clock signal jitter that is the major contributor to the total jitter. Therefore, you must pay particular attention to the clock signal in the case of acquisition of fast signals with a low frequency clock. For further considerations on low sampling conditions, refer to *Section 7.4 on page 20*.

The clock signal must be active when you power up the device. Clock gating (stopping the clock) is not recommended due to possible undertermined states inside the circuit when the clock is off.

7.3 Power consumption optimization

The internal architecture of the RHF1401 makes it possible for you to optimize the analog power consumption depending on the sampling frequency by adjusting the R_{pol} resistor. This resistor is placed between the IPOL pin and the analog ground.

Input signal below 10MHz

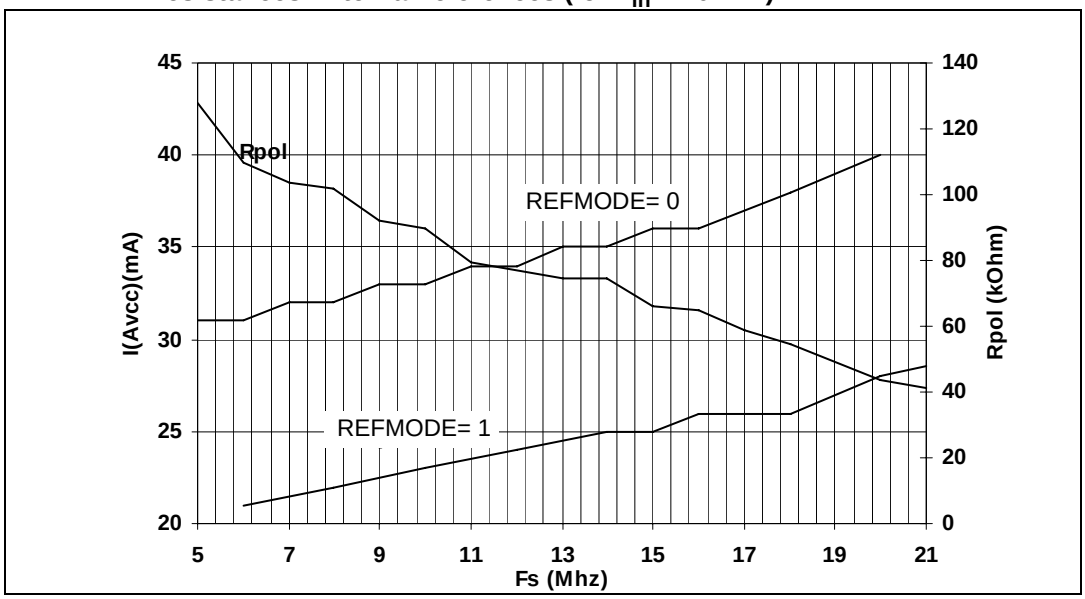
Depending of the application sampling speed, the R_{pol} value should be set between 120 kΩ (low sampling speed, low current) and 40 kΩ (high sampling speed, high current). With a low sampling speed, you should use a high value for R_{pol} (for example 100 kΩ) in order to minimize the power consumption, often critical in space applications. This method is efficient with an input signal in the range from DC up to 10MHz.

With a sampling frequency of 20 MHz, an R_{pol} value of 41 kΩ provides optimized power consumption.

Figure 23 shows the optimized power consumption of the circuit versus the sampling frequency in two different configurations:

- REFMODE=0 internal references with I_{AVCC} in the range 30-40 mA
- REFMODE=1 external references with I_{AVCC} in the range 20-30 mA

Figure 23. Analog current consumption vs. F_s according to value of R_{pol} polarization resistances: internal references (for F_{in} < 10MHz)



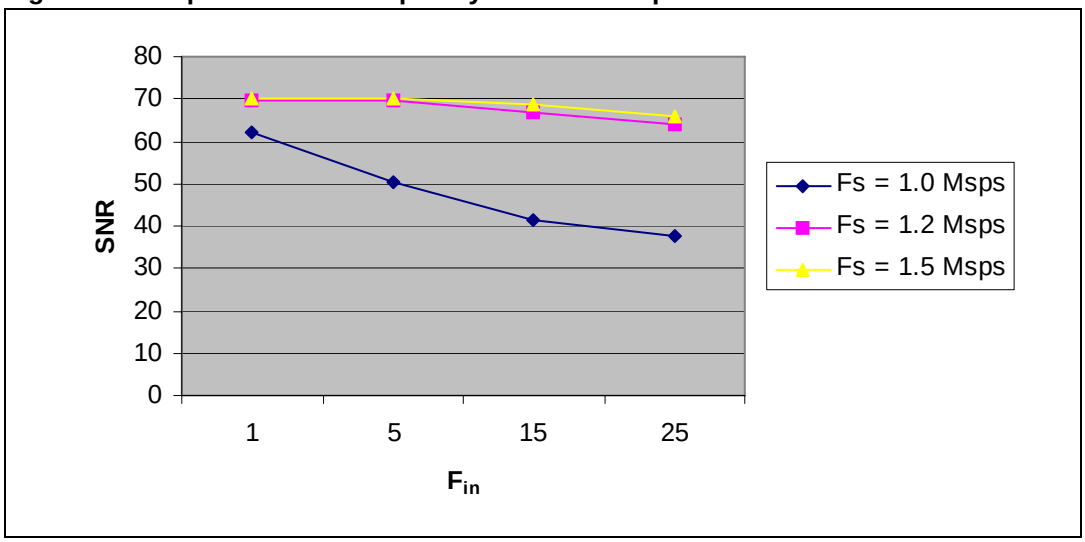
Input signal above 10MHz

However, with a higher frequency input signal (for example, in the 10-70MHz range), a high R_{pol} value does not supply enough current to the internal amplifiers, thus resulting in degraded SNR and THD performance. With an input signal in this range, the recommended value for R_{pol} is in the 30-50 kΩ range.

7.4 Low sampling rate recommendations

The RHF1401 offers a wide range of sampling rates from 1.5Msps to 20Msps with the minimum power consumption. However, under the minimum, the performance of the device deteriorates. *Figure 24* shows the degradation in performance at sampling frequencies under 1.2Msps. The recommended minimum sampling frequency is 1.5Msps.

Figure 24. Impact of clock frequency on RHF1401 performance



In the case of under-sampling, that is when the sampling rate is much lower than the input signal frequency (for example a 2Msps sampling rate with a 41.3MHz input signal), there are two critical parameters to consider:

- The value of the R_{pol} resistor
- The clock jitter

7.5 Digital inputs/outputs

Data format select (DFSB)

When set to low level (V_{IL}), the digital input DFSB provides a two's complement digital output MSB. This can be of interest when performing further signal processing.

When set to high level (V_{IH}), DFSB provides a standard binary output coding.

Output enable (OEB)

When set to low level (V_{IL}), all digital outputs remain active and are in low impedance state. When set to high level (V_{IH}), all digital output buffers are in high impedance state. It results in lower consumption while the converter goes on sampling.

When OEB is set to low level again, the data is then delivered on the output with a very short T_{on} delay.

Out of range (OR)

This function is implemented on the output stage in order to set up an "Out of range" flag whenever the digital data is over the full scale range.

Typically, there is a detection of all the data at '0' or all the data at '1'. This ends up with an output signal OR which is in low level state (V_{OL}) when the data is within the range, or in high level state (V_{OH}) when the data is out of the range.

Data ready (DR)

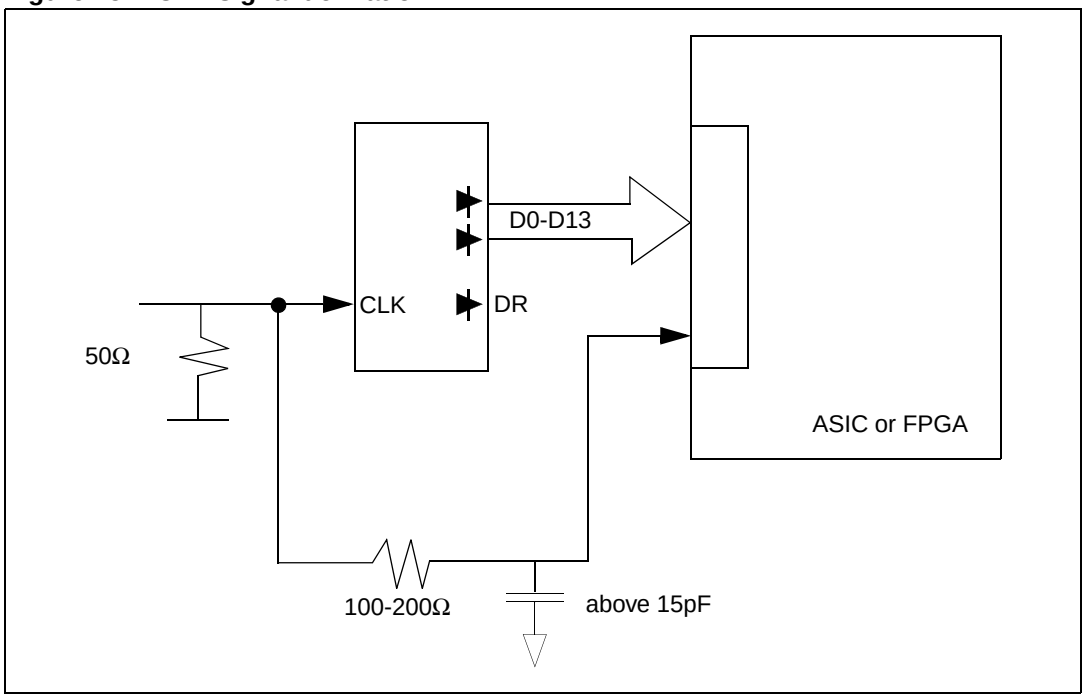
The data ready output signal is an image of the clock being synchronized on the output data (D0 to D13). This is a very helpful signal that simplifies the synchronization of the measurement equipment or the controlling DSP.

As all other digital outputs, DR goes into high impedance state when OEB reaches high level as described in *Figure 3: Timing diagram on page 7*.

Caution: Because the driving force of data outputs and the DR signal is relatively low, it is recommended to limit the equivalent load on these signals to 10-15pF maximum. This is to avoid a weak signal when the RHF1401 is clocked at full speed (20Msps). The DR signal is potentially the most affected because it has the highest frequency (20MHz maximum).

If the equivalent load on the data outputs is slightly higher than 15pF, you can avoid resorting to external re-buffering of the data bus and DR signal by connecting the data bus to the acquisition device directly without using the DR. In this case, you can obtain a good validation signal from a derivation of the clock because the clock falling edge is used by the RHF1401 internally to generate data output transitions. A series resistor of approximately 100-200 Ohms should be placed at the derivation to avoid the effect of current spikes on the critical CLK node. This configuration is illustrated in *Figure 25*.

Figure 25. CLK signal derivation



7.6 PCB layout precautions

To use the ADC circuits most efficiently at high frequencies, some precautions have to be taken for power supplies:

- First of all, the implementation of 4 separate proper supplies and ground planes (analog, digital, internal and external buffer ones) on the PCB is recommended for high speed circuit applications to provide low-inductance and low-resistance common return.
- The separation of the analog signal from the digital part and from the buffers power supply is essential to prevent noise from coupling onto the input signal.
- Power supply bypass capacitors must be placed as close as possible to the IC pins in order to improve high frequency bypassing and reduce harmonic distortion.
- Proper termination of all inputs and outputs is needed; with output termination resistors, the amplifier load is resistive only and the stability of the amplifier is improved. All leads must be wide and as short as possible especially for the analog input in order to decrease parasitic capacitance and inductance.
- To keep the capacitive loading as low as possible at digital outputs, short lead lengths of routing are essential to minimize currents when the output changes. To minimize this output capacitance, use buffers or latches close to the output pins. It is also helpful to use 47 Ω to 56 Ω series resistors at the ADC output pins, located as close to the ADC output pins as possible.
- Choose component sizes as small as possible (SMD).

8 Definitions of specified parameters

8.1 Static parameters

Static measurements are performed using the histograms method on a 2 MHz input signal, sampled at 50 Msps, which is high enough to fully characterize the test frequency response. The input level is +1 dBFS to saturate the signal.

Differential non linearity (DNL)

The average deviation of any output code width from the ideal code width of 1LSB.

Integral non linearity (INL)

An ideal converter exhibits a transfer function which is a straight line from the starting code to the ending code. The INL is the deviation from this ideal line for each transition.

8.2 Dynamic parameters

Dynamic measurements are performed by spectral analysis, applied to an input sinewave of various frequencies and sampled at 50 Msps.

Spurious free dynamic range (SFDR)

The ratio between the power of the worst spurious signal (not always an harmonic) and the amplitude of fundamental tone (signal power) over the full Nyquist band. It is expressed in dBc.

Total harmonic distortion (THD)

The ratio of the rms sum of the first five harmonic distortion components to the rms value of the fundamental line. It is expressed in dB.

Signal to noise ratio (SNR)

The ratio of the rms value of the fundamental component to the rms sum of all other spectral components in the Nyquist band ($F_S/2$) excluding DC, fundamental and the first five harmonics. SNR is reported in dB.

Signal to noise and distortion ratio (SINAD)

A similar ratio to the SNR but including the harmonic distortion components in the noise figure (not the DC signal). It is expressed in dB.

From the SINAD, the Effective Number of Bits (ENOB) can easily be deduced using the formula:

$$SINAD = 6.02 \times ENOB + 1.76\ dB.$$

When the applied signal is not Full Scale (FS), but has an A_0 amplitude, the SINAD expression becomes:

$$SINAD = 6.02 \times ENOB + 1.76\ dB + 20\ log\ (2A_0/FS)$$

The ENOB is expressed in bits.

Analog input bandwidth

The maximum analog input frequency at which the spectral response of a full power signal is reduced by 3 dB. Higher values can be achieved with smaller input levels.

Pipeline delay

Delay between the initial sample of the analog input and the availability of the corresponding digital data output, on the output bus. Also called data latency. It is expressed as a number of clock cycles.

9 Package information

Figure 26. SO-48 package mechanical drawing

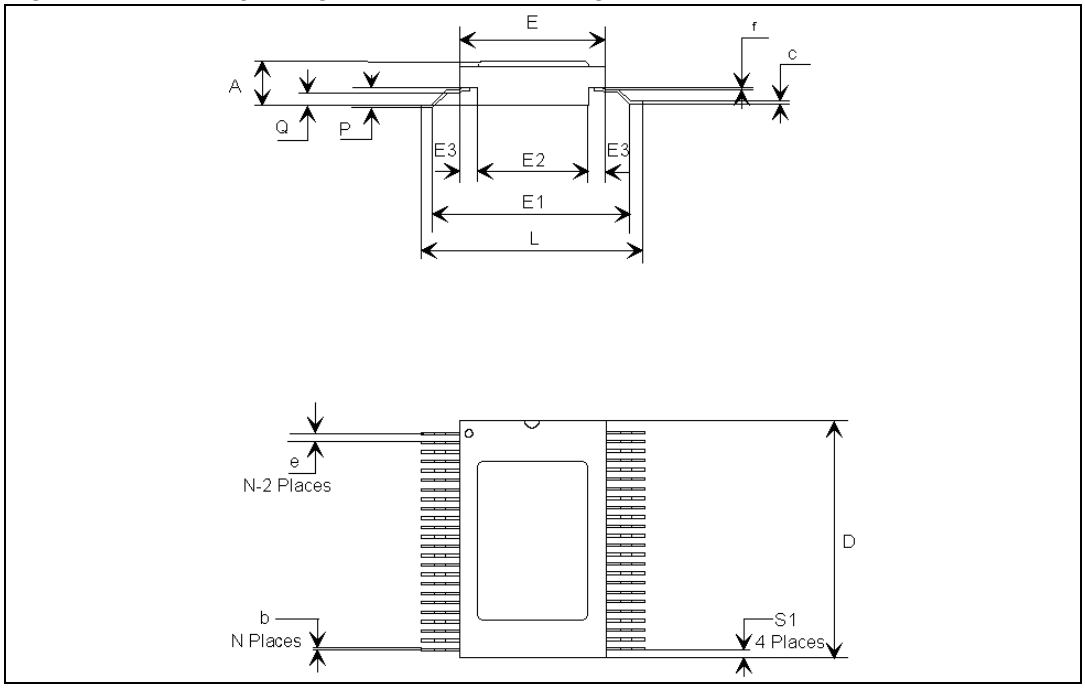


Table 11. SO-48 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18	2.47	2.72	0.086	0.097	0.107
b	0.20	0.254	0.30	0.008	0.010	0.012
c	0.12	0.15	0.18	0.005	0.006	0.007
D	15.57	15.75	15.92	0.613	0.620	0.627
E	9.52	9.65	9.78	0.375	0.380	0.385
E1		10.90			0.429	
E2	6.22	6.35	6.48	0.245	0.250	0.255
E3	1.52	1.65	1.78	0.060	0.065	0.070
e		0.635			0.025	
f		0.20			0.008	
L	12.28	12.58	12.88	0.483	0.495	0.507
P	1.30	1.45	1.60	0.051	0.057	0.063
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.25	0.43	0.61	0.010	0.017	0.024

10 Ordering information

Table 12. Order codes

Part number	Temperature range	Package	Marking
RHF1401KSO1	-55 °C to 125 °C	SO-48	RHF1401KSO1
RHF1401KSO2			RHF1401KSO2
RHF1401KSO-01V			F0626001VXC

11 Revision history

Table 13. Document revision history

Date	Revision	Changes
29-Jun-2007	1	First public release. Failure immune and latchup immune value increased to 120 MeV-cm^2/mg. Updated package mechanical information. Removed reference to non rad-hard components from *External references, common mode: on page 16*.
29-Oct-2007	2	Updated *Figure 1: RHF1401 block diagram*. Added explanation on *Figure 3: Timing diagram*. Added introduction to *Section 6: Typical performance characteristics*. Updated *Section 7.2: Clock signal requirements* and *Section 7.3: Power consumption optimization*. Added *Section 7.4: Low sampling rate recommendations*. Updated information on Data Ready signal in *Section 7.5: Digital inputs/outputs*. Added *Figure 24: Impact of clock frequency on RHF1401 performance* and *Figure 25: CLK signal derivation*.

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