Freescale Semiconductor
Data Sheet: Technical Data

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MCF5271 Integrated Microprocessor Hardware Specification

by: Microcontroller Solutions Group

The MCF5271 family is a highly integrated implementation of the ColdFire® family of reduced instruction set computing (RISC) microprocessors. This document describes pertinent features and functions of the MCF5271 family. The MCF5271 family includes the MCF5271 and MCF5270 microprocessors. The differences between these parts are summarized below in Table 1. This document is written from the perspective of the MCF5271 and unless otherwise noted, the information applies also to the MCF5270.

The MCF5271 family combines low cost with high integration on the popular version 2 ColdFire core with over 144 (Dhrystone 2.1) MIPS at 150 MHz. Positioned for applications requiring a cost-sensitive 32-bit solution, the MCF5271 family features a 10/100 Ethernet MAC and optional hardware encryption to ensure the application can be connected and protected. In addition, the MCF5271 family features an enhanced multiply accumulate unit (eMAC), large on-chip memory (64 Kbytes SRAM, 8 Kbytes configurable cache), and a 32-bit SDR SDRAM memory controller.

Contents

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MCF527x products in 196 MAPBGA packages

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1 MCF5271 Family Configurations

Table 1. MCF5271 Family Configurations

Module	MCF5270	MCF5271
ColdFire V2 Core with EMAC and Hardware Divide	x	x
System Clock	150 MHz	
Performance (Dhrystone/2.1 MIPS)	144	
Instruction/Data Cache	8 Kbytes	
Static RAM (SRAM)	64 Kbytes	
Interrupt Controllers (INTC)	2	2
Edge Port Module (EPORT)	x	x
External Interface Module (EIM)	x	x
4-channel Direct-Memory Access (DMA)	x	x
SDRAM Controller	x	x
Fast Ethernet Controller (FEC)	x	x
Hardware Encryption	—	x
Watchdog Timer (WDT)	x	x
Four Periodic Interrupt Timers (PIT)	x	x
32-bit DMA Timers	4	4
QSPI	x	x
UART(s)	3	3
I^2C	x	x
General Purpose I/O Module (GPIO)	x	x
JTAG - IEEE 1149.1 Test Access Port	x	x
Package	160 QFP, 196 MAPBGA	160 QFP, 196 MAPBGA

2 Block Diagram

The superset device in the MCF5271 family comes in a 196 mold array plastic ball grid array (MAPBGA) package. Figure 1 shows a top-level block diagram of the MCF5271.

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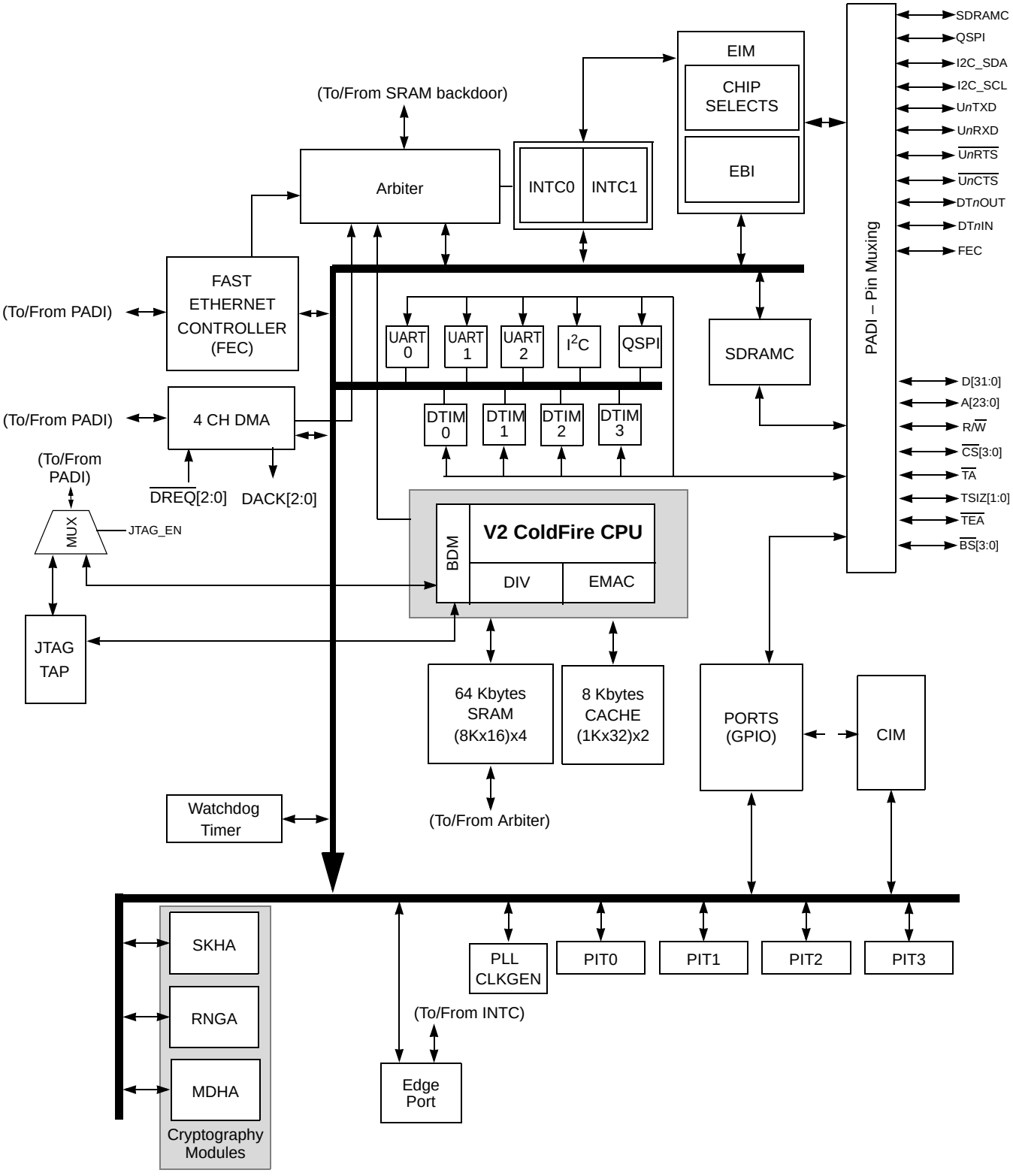

Figure 1. MCF5271 Block Diagram

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3 Features

For a detailed feature list see the MCF5271 Reference Manual (MCF5271RM).

4 Signal Descriptions

This section describes signals that connect off chip, including a table of signal properties. For a more detailed discussion of the MCF5271 signals, consult the *MCF5271 Reference Manual* (MCF5271RM).

4.1 Signal Properties

Table 4 lists all of the signals grouped by function. The "Dir" column is the direction for the primary function of the pin. Refer to Section 6, "Mechanicals/Pinouts and Part Numbers," for package diagrams.

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., A24), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO will default to their GPIO functionality.

Table 2. MCF5270 and MCF5271 Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
Reset						
$\overline{\text{RESET}}$	—	—	—	I	83	N13
$\overline{\text{RSTOUT}}$	—	—	—	O	82	P13
Clock						
EXTAL	—	—	—	I	86	M14
XTAL	—	—	—	O	85	N14
CLKOUT	—	—	—	O	89	K14
Mode Selection						
CLKMOD[1:0]	—	—	—	I	20,21	G5,H5
$\overline{\text{RCON}}$	—	—	—	I	79	K10
External Memory Interface and Ports						
A[23:21]	PADDR[7:5]	$\overline{\text{CS}}$[6:4]	—	O	126, 125, 124	B11, C11, D11

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Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
A[20:0]	—	—	—	O	123:115, 112:106, 102:98	A12, B12, C12, A13, B13, B14, C13, C14, D12, D13, D14, E11, E12, E13, E14, F12, F13, F14, G11, G12, G13
D[31:16]	—	—	—	O	22:30, 33:39	G1, G2, H1, H2, H3, H4, J1, J2, J3, J4, K1, K2, K3, K4, L1, L2
D[15:8]	PDATAH[7:0]	—	—	O	42:49	M1, N1, M2, N2, P2, L3, M3, N3
D[7:0]	PDATAL[7:0]	—	—	O	50:52, 56:60	P3, M4, N4, P4, L5, M5, N5, P5
$\overline{BS}$[3:0]	PBS[7:4]	$\overline{CAS}$[3:0]	—	O	143:140	B6, C6, D7, C7
$\overline{OE}$	PBUSCTL7	—	—	O	62	N6
$\overline{TA}$	PBUSCTL6	—	—	I	96	H11
$\overline{TEA}$	PBUSCTL5	$\overline{DREQ1}$	—	I	—	J14
R/$\overline{W}$	PBUSCTL4	—	—	O	95	J13
$\overline{TSIZ1}$	PBUSCTL3	DACK1	—	O	—	P6
$\overline{TSIZ0}$	PBUSCTL2	DACK0	—	O	—	P7
$\overline{TS}$	PBUSCTL1	DACK2	—	O	97	H13
$\overline{TIP}$	PBUSCTL0	DREQ0	—	O	—	H12
Chip Selects						
$\overline{CS}$[7:4]	PCS[7:4]	—	—	O	—	B9, A10, C10, A11
$\overline{CS}$[3:2]	PCS[3:2]	SD_CS[1:0]	—	O	132,131	A9, C9
$\overline{CS1}$	PCS1	—	—	O	130	B10
$\overline{CS0}$	—	—	—	O	129	D10
SDRAM Controller						
$\overline{SD\_WE}$	PSDRAM5	—	—	O	92	K13
$\overline{SD\_SCAS}$	PSDRAM4	—	—	O	91	K12
$\overline{SD\_SRAS}$	PSDRAM3	—	—	O	90	K11
SD_CKE	PSDRAM2	—	—	O	—	E8
$\overline{SD\_CS}$[1:0]	PSDRAM[1:0]	—	—	O	—	L12, L13

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Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
External Interrupts Port						
$\overline{\text{IRQ}}$[7:3]	PIRQ[7:3]	—	—	I	IRQ7=63 IRQ4=64	N7, M7, L7, P8, N8
$\overline{\text{IRQ2}}$	PIRQ2	$\overline{\text{DREQ2}}$	—	I	—	M8
$\overline{\text{IRQ1}}$	PIRQ1	—	—	I	65	L8
FEC						
EMDC	PFECI2C3	I2C_SCL	U2TXD	O	151	D4
EMDIO	PFECI2C2	I2C_SDA	U2RXD	I/O	150	D5
ECOL	—	—	—	I	9	E2
ECRS	—	—	—	I	8	E1
ERXCLK	—	—	—	I	7	D1
ERXDV	—	—	—	I	6	D2
ERXD[3:0]	—	—	—	I	5:2	D3, C1, C2, B1
ERXER	—	—	—	O	159	B2
ETXCLK	—	—	—	I	158	A2
ETXEN	—	—	—	I	157	C3
ETXER	—	—	—	O	156	B3
ETXD[3:0]	—	—	—	O	155:152	A3, A4, C4, B4
I^2C						
I2C_SDA	PFECI2C1	—	—	I/O	—	J12
I2C_SCL	PFECI2C0	—	—	I/O	—	J11
DMA						
DACK[2:0] and $\overline{\text{DREQ}}$[2:0] do not have a dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ and DT2OUT for DACK2, TSIZ1and DT1OUT for DACK1, TSIZ0 and DT0OUT for DACK0, $\overline{\text{IRQ2}}$ and DT2IN for $\overline{\text{DREQ2}}$, $\overline{\text{TEA}}$ and $\overline{\text{DT1IN}}$ for $\overline{\text{DREQ1}}$, and $\overline{\text{TIP}}$ and DT0IN for $\overline{\text{DREQ0}}$.					—	—
QSPI						
QSPI_CS1	PQSPI4	SD_CKE	—	O	139	B7
QSPI_CS0	PQSPI3	—	—	O	146	A6
QSPI_CLK	PQSPI2	I2C_SCL	—	O	147	C5
QSPI_DIN	PQSPI1	I2C_SDA	—	I	148	B5
QSPI_DOUT	PQSPI0	—	—	O	149	A5

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Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
UARTs						
U2TXD	PUARTH1	—	—	O	—	A8
U2RXD	PUARTH0	—	—	I	—	A7
$\overline{\text{U1CTS}}$	PUARTL7	$\overline{\text{U2CTS}}$	—	I	136	B8
$\overline{\text{U1RTS}}$	PUARTL6	$\overline{\text{U2RTS}}$	—	O	135	C8
U1TXD	PUARTL5	—	—	O	133	D9
U1RXD	PUARTL4	—	—	I	134	D8
$\overline{\text{U0CTS}}$	PUARTL3	—	—	I	12	F3
$\overline{\text{U0RTS}}$	PUARTL2	—	—	O	15	G3
U0TXD	PUARTL1	—	—	O	14	F1
U0RXD	PUARTL0	—	—	I	13	F2
DMA Timers						
DT3IN	PTIMER7	$\overline{\text{U2CTS}}$	QSPI_CS2	I	—	H14
DT3OUT	PTIMER6	$\overline{\text{U2RTS}}$	QSPI_CS3	O	—	G14
DT2IN	PTIMER5	$\overline{\text{DREQ2}}$	DT2OUT	I	66	M9
DT2OUT	PTIMER4	DACK2	—	O	—	L9
DT1IN	PTIMER3	$\overline{\text{DREQ1}}$	DT1OUT	I	61	L6
DT1OUT	PTIMER2	DACK1	—	O	—	M6
DT0IN	PTIMER1	$\overline{\text{DREQ0}}$	—	I	10	E4
DT0OUT	PTIMER0	DACK0	—	O	11	F4
BDM/JTAG[2]						
DSCLK	—	TRST	—	O	70	N9
PSTCLK	—	TCLK	—	O	68	P9
$\overline{\text{BKPT}}$	—	TMS	—	O	71	P10
DSI	—	TDI	—	I	73	M10
DSO	—	TDO	—	O	72	N10
JTAG_EN	—	—	—	I	78	K9
DDATA[3:0]	—	—	—	O	—	M12, N12, P12, L11
PST[3:0]	—	—	—	O	77:74	M11, N11, P11, L10

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Table 2. MCF5270 and MCF5271 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5270 MCF5271 160 QFP	MCF5270 MCF5271 196 MAPBGA
Test						
TEST	—	—	—	I	19	F5
PLL_TEST	—	—	—	I	—	
Power Supplies						
VDDPLL	—	—	—	I	87	M13
VSSPLL	—	—	—	I	84	L14
OVDD	—	—	—	I	1, 18, 32, 41, 55, 69, 81, 94, 105, 114, 128, 138, 145	E5, E7, E10, F7, F9, G6, G8, H7, H8, H9, J6, J8, J10, K5, K6, K8
VSS	—	—	—	I	17, 31, 40, 54, 67, 80, 88, 93, 104, 113, 127, 137, 144, 160	A1, A14, E6, E9, F6, F8, F10, G7, G9, H6, J5, J7, J9, K7, P1, P14
VDD	—	—	—	I	16, 53, 103	D6, F11, G4, L4

1 Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

2 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

5 Design Recommendations

5.1 Layout

- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF5271.
- See application note AN1259, *System Design and Layout Techniques for Noise Reduction in Processor-Based Systems*.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

5.2 Power Supply

- 33 μF, 0.1 μF, and 0.01 μF across each power supply

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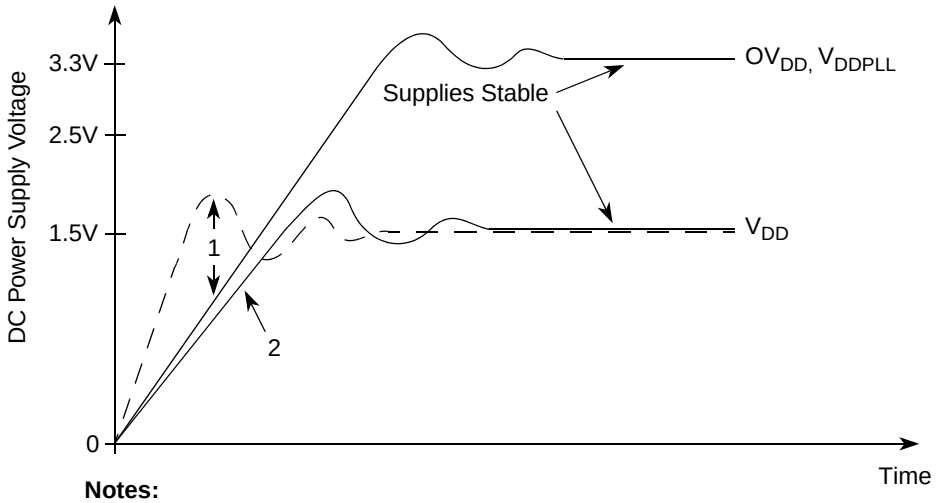
5.2.1 Supply Voltage Sequencing and Separation Cautions

Figure 2 shows situations in sequencing the I/O V_{DD} (OV_{DD}), PLL V_{DD} (V_{DDPLL}), and Core V_{DD} (V_{DD}). OV_{DD} is specified relative to V_{DD}.



Notes:
1. VDD should not exceed OVDD or VDDPLL by more than 0.4 V at any time, including power-up.
2. Recommended that VDD should track OVDD/VDDPLL up to 0.9 V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (OVDD, VDD, or VDDPLL) by more than 0.5 V at any time, including during power-up.
4. Use 1 ms or slower rise time for all supplies.

Figure 2. Supply Voltage Sequencing and Separation Cautions

5.2.1.1 Power Up Sequence

If OV_{DD} is powered up with V_{DD} at 0 V, then the sense circuits in the I/O pads cause all pad output drivers connected to the OV_{DD} to be in a high impedance state. There is no limit on how long after OV_{DD} powers up before V_{DD} must power up. V_{DD} should not lead the OV_{DD} or V_{DDPLL} by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 μs to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 ms or slower rise time for all supplies.
2. V_{DD} and OV_{DD}/V_{DDPLL} should track up to 0.9 V, then separate for the completion of ramps with OV_{DD} going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

5.2.1.2 Power Down Sequence

If V_{DD} is powered down first, then sense circuits in the I/O pads cause all output drivers to be in a high impedance state. There is no limit on how long after V_{DD} powers down before OV_{DD}/V_{DDPLL} must power down. V_{DD} should not lag OV_{DD} or V_{DDPLL} going low by more than 0.4 V during power down or there

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will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop V_{DD} to 0 V.
2. Drop OV_{DD}/V_{DDPLL} supplies.

5.3 Decoupling

- Place the decoupling caps as close to the pins as possible, but they can be outside the footprint of the package.
- 0.1 μF and 0.01 μF at each supply input

5.4 Buffering

- Use bus buffers on all data/address lines for all off-board accesses and for all on-board accesses when excessive loading is expected. See Section 7, “Electrical Characteristics.”

5.5 Pull-up Recommendations

- Use external pull-up resistors on unused inputs. See pin table.

5.6 Clocking Recommendations

- Use a multi-layer board with a separate ground plane.
- Place the crystal and all other associated components as close to the EXTAL and XTAL (oscillator pins) as possible.
- Do not run a high frequency trace around crystal circuit.
- Ensure that the ground for the bypass capacitors is connected to a solid ground trace.
- Tie the ground trace to the ground pin nearest EXTAL and XTAL. This prevents large loop currents in the vicinity of the crystal.
- Tie the ground pin to the most solid ground in the system.
- Do not connect the trace that connects the oscillator and the ground plane to any other circuit element. This tends to make the oscillator unstable.
- Tie XTAL to ground when an external oscillator is clocking the device.

5.7 Interface Recommendations

5.7.1 SDRAM Controller

5.7.1.1 SDRAM Controller Signals in Synchronous Mode

Table 3 shows the behavior of SDRAM signals in synchronous mode.

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Table 3. Synchronous DRAM Signal Connections

Signal	Description
$\overline{\text{SD\_SRAS}}$	Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. $\overline{\text{SD\_SRAS}}$ should be connected to the corresponding SDRAM $\overline{\text{SD\_SRAS}}$. Do not confuse $\overline{\text{SD\_SRAS}}$ with the DRAM controller's $\overline{\text{SD\_CS}}$[1:0], which should not be interfaced to the SDRAM $\overline{\text{SD\_SRAS}}$ signals.
$\overline{\text{SD\_SCAS}}$	Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. $\overline{\text{SD\_SCAS}}$ should be connected to the corresponding signal labeled $\overline{\text{SD\_SCAS}}$ on the SDRAM.
$\overline{\text{DRAMW}}$	DRAM read/write. Asserted for write operations and negated for read operations.
$\overline{\text{SD\_CS}}$[1:0]	Row address strobe. Select each memory block of SDRAMs connected to the MCF5271. One $\overline{\text{SD\_CS}}$ signal selects one SDRAM block and connects to the corresponding $\overline{\text{CS}}$ signals.
SD_CKE	Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality.
$\overline{\text{BS}}$[3:0]	Column address strobe. For synchronous operation, $\overline{\text{BS}}$[3:0] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs.
CLKOUT	Bus clock output. Connects to the CLK input of SDRAMs.

5.7.1.2 Address Multiplexing

See the SDRAM controller module chapter in the *MCF5271 Reference Manual* for details on address multiplexing.

5.7.2 Ethernet PHY Transceiver Connection

The FEC supports both an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 4.

Table 4. MII Mode

Signal Description	MCF5271 Pin
Transmit clock	ETXCLK
Transmit enable	ETXEN
Transmit data	ETXD[3:0]
Transmit error	ETXER
Collision	ECOL
Carrier sense	ECRS
Receive clock	ERXCLK
Receive enable	ERXDV
Receive data	ERXD[3:0]

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Table 4. MII Mode (continued)

Signal Description	MCF5271 Pin
Receive error	ERXER
Management channel clock	EMDC
Management channel serial data	EMDIO

The serial mode interface operates in what is generally referred to as AMD mode. The MCF5271 configuration for seven-wire serial mode connections to the external transceiver are shown in Table 5.

Table 5. Seven-Wire Mode Configuration

Signal Description	MCF5271 Pin
Transmit clock	ETXCLK
Transmit enable	ETXEN
Transmit data	ETXD[0]
Collision	ECOL
Receive clock	ERXCLK
Receive enable	ERXDV
Receive data	ERXD[0]
Unused, configure as PB14	ERXER
Unused input, tie to ground	ECRS
Unused, configure as PB[13:11]	ERXD[3:1]
Unused output, ignore	ETXER
Unused, configure as PB[10:8]	ETXD[3:1]
Unused, configure as PB15	EMDC
Input after reset, connect to ground	EMDIO

Refer to the M5271EVB evaluation board user's manual for an example of how to connect an external PHY. Schematics for this board are accessible at the MCF5271 site by navigating to: http://www.freescale.com/coldfire.

5.7.3 BDM

Use the BDM interface as shown in the M5271EVB evaluation board user's manual. The schematics for this board are accessible at the Freescale website at: http://www.freescale.com/coldfire.

6 Mechanicals/Pinouts and Part Numbers

This section contains drawings showing the pinout and the packaging and mechanical characteristics of the MCF5271 devices. See Table 4 for a list the signal names and pin locations for each device.

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6.1 Pinout—196 MAPBGA

The following figure shows a pinout of the MCF5270/71CVMxxx package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	ETXCLK	ETXD3	ETXD2	QSPI_ DOUT	QSPI_CS0	U2RXD	U2TXD	$\overline{\text{CS3}}$	$\overline{\text{CS6}}$	$\overline{\text{CS4}}$	A20	A17	VSS	A
B	ERXD0	ERXER	ETXER	ETXD0	QSPI_DIN	$\overline{\text{BS3}}$	QSPI_CS1	U1CTS	$\overline{\text{CS7}}$	$\overline{\text{CS1}}$	A23	A19	A16	A15	B
C	ERXD2	ERXD1	ETXEN	ETXD1	QSCK	$\overline{\text{BS2}}$	$\overline{\text{BS0}}$	RTS1	$\overline{\text{CS2}}$	$\overline{\text{CS5}}$	A22	A18	A14	A13	C
D	ERXCLK	ERXDV	ERXD3	EMDC	EMDIO	Core VDD_4	$\overline{\text{BS1}}$	U1RXD1	U1TXD	$\overline{\text{CS0}}$	A21	A12	A11	A10	D
E	ECRS	ECOL	NC	TIN0	VDD	VSS	VDD	SD_CKE	VSS	VDD	A9	A8	A7	A6	E
F	U0TXD	U0RXD	U0CTS	DTOUT0	TEST	VSS	VDD	VSS	VDD	VSS	Core VDD_3	A5	A4	A3	F
G	D31	D30	U0RTS	Core VDD_1	CLK MOD1	VDD	VSS	VDD	VSS	NC	A2	A1	A0	DTOUT3	G
H	D29	D28	D27	D26	CLK MOD0	VSS	VDD	VDD	VDD	NC	$\overline{\text{TA}}$	$\overline{\text{TIP}}$	$\overline{\text{TS}}$	DTIN3	H
J	D25	D24	D23	D22	VSS	VDD	VSS	VDD	VSS	VDD	I2C_SCL	I2C_SDA	R/$\overline{\text{W}}$	$\overline{\text{TEA}}$	J
K	D21	D20	D19	D18	VDD	VDD	VSS	VDD	JTAG_EN	$\overline{\text{RCON}}$	$\overline{\text{SD_ RAS}}$	$\overline{\text{SD_ CAS}}$	$\overline{\text{SD_ WE}}$	CLKOUT	K
L	D17	D16	D10	Core VDD_2	D3	DTIN1	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ1}}$	DTOUT2	PST0	DDATA0	$\overline{\text{SD_ CS1}}$	$\overline{\text{SD_ CS0}}$	VSSPLL	L
M	D15	D13	D9	D6	D2	DTOUT1	$\overline{\text{IRQ6}}$	$\overline{\text{IRQ2}}$	DTIN2	TDI/DSI	PST3	DDATA3	VDDPLL	EXTAL	M
N	D14	D12	D8	D5	D1	$\overline{\text{OE}}$	$\overline{\text{IRQ7}}$	$\overline{\text{IRQ3}}$	$\overline{\text{TRST}}$/ DSCLK	TDO/DSO	PST2	DDATA2	$\overline{\text{RESET}}$	XTAL	N
P	VSS	D11	D7	D4	D0	TSIZ1	TSIZ0	$\overline{\text{IRQ4}}$	TCLK/ PSTCLK	$\overline{\text{TMS}}$/ $\overline{\text{BKPT}}$	PST1	DDATA1	$\overline{\text{RSTOUT}}$	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 3. MCF5270/71CVMxxx Pinout (196 MAPBGA)

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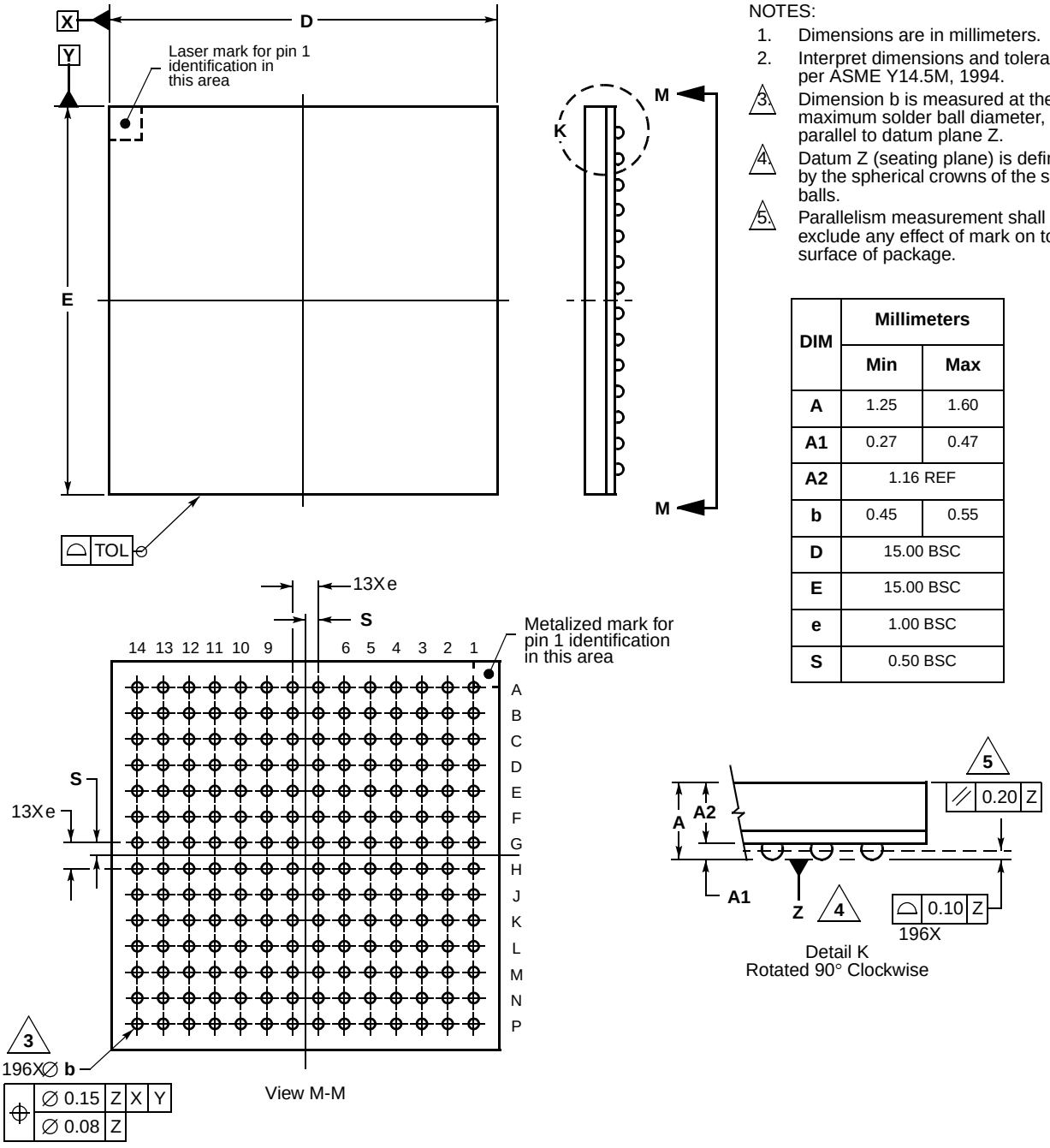
6.2 Package Dimensions—196 MAPBGA

Figure 4 shows MCF5270/71CVMxxx package dimensions.



NOTES:
1. Dimensions are in millimeters.
2. Interpret dimensions and tolerances per ASME Y14.5M, 1994.
3. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane Z.
4. Datum Z (seating plane) is defined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

DIM	Millimeters	
	Min	Max
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.45	0.55
D	15.00 BSC	
E	15.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 4. 196 MAPBGA Package Dimensions (Case No. 1128A-01)

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6.3 Pinout—160 QFP

Figure 5 shows a pinout of the MCF5271CABxxx package.

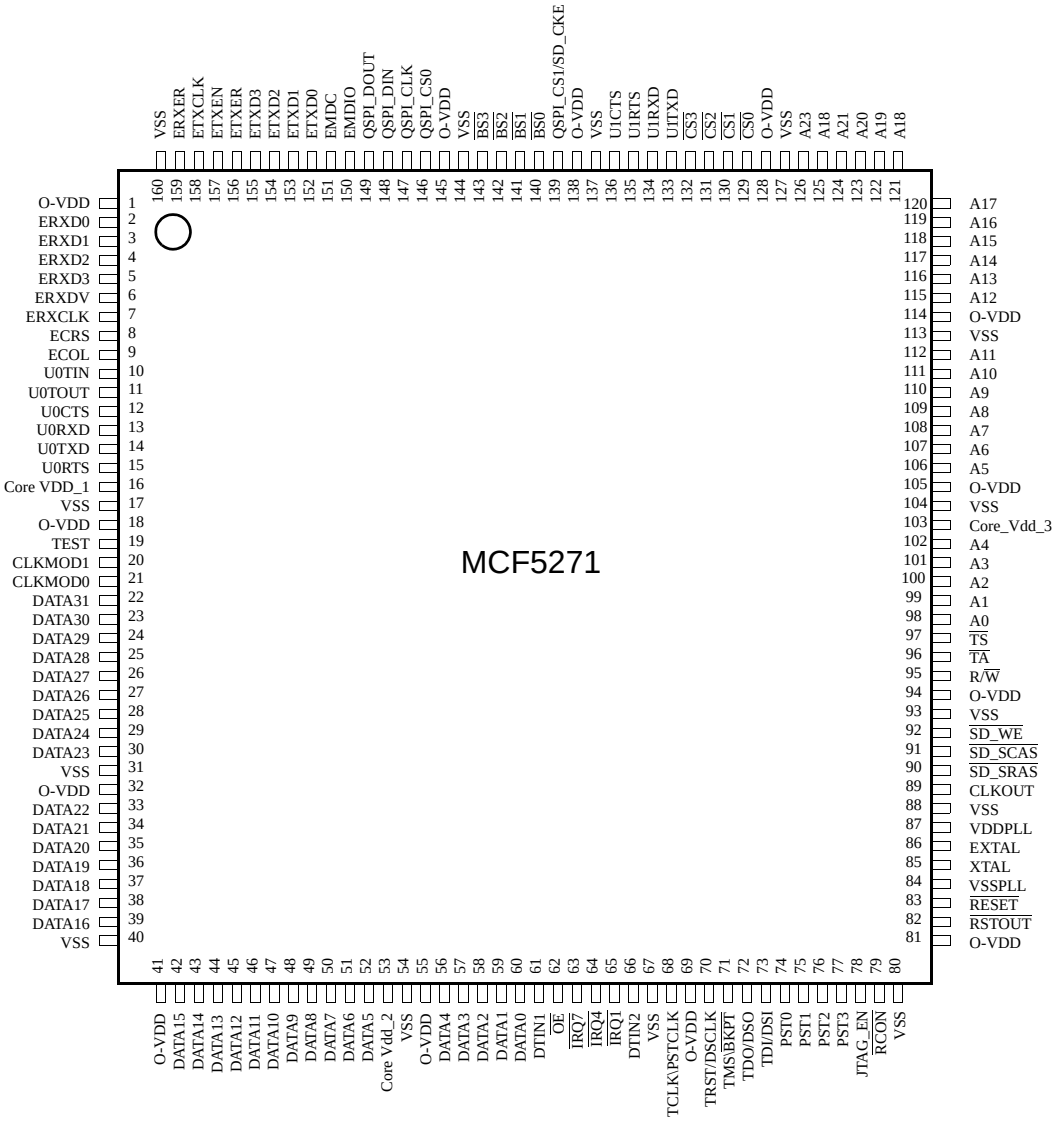

Figure 5. MCF5270/71CABxxx Pinout (160 QFP)

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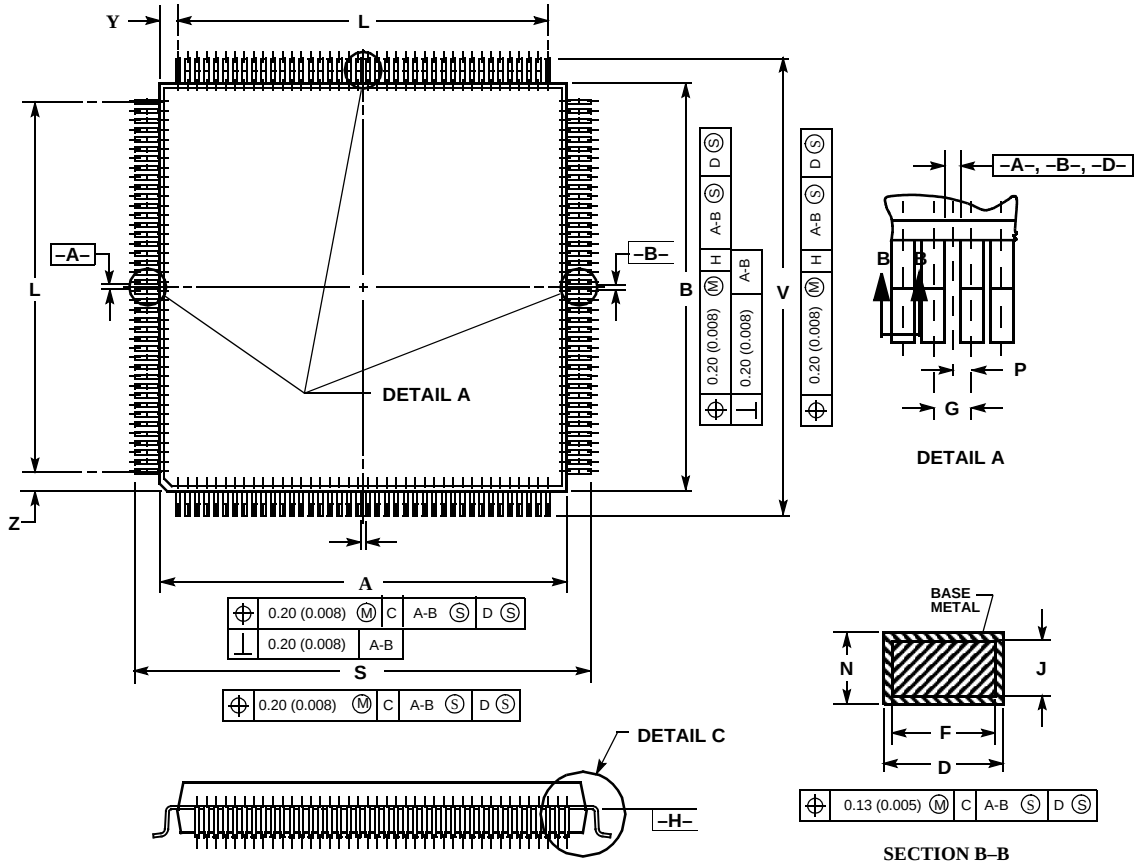
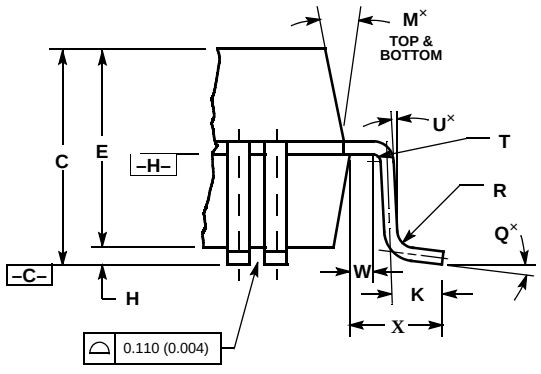
6.4 Package Dimensions—160 QFP

Figure 6 shows MCF5270/71CAB80 package dimensions.





DETAIL C

NOTES

1. DIMENSIONING AND TOLERINCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DATUM PLAN -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B-, AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.35	3.85	0.132	1.106
D	0.22	0.38	0.009	0.015
E	3.20	3.50	0.126	0.138
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 REF	
H	0.25	0.35	0.010	0.014
J	0.11	0.23	0.004	0.009
K	0.70	0.90	0.028	0.035
L	25.35 BSC		0.998 REF	
M	5°	16°	5°	16°
N	0.11	0.19	0.004	0.007
P	0.325 BSC		0.013 REF	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	—	0.005	—
U	0°	—	0°	—
V	31.00	31.40	1.220	1.236
W	0.4	—	0.016	—
X	1.60 REF		0.063 REF	
Y	1.33 REF		0.052 REF	
Z	1.33 REF		0.052 REF	

Case 864A-03

Figure 6. 160 QFP Package Dimensions

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6.5 Ordering Information

Table 6. Orderable Part Numbers

Freescale Part Number	Description	Package	Speed	Lead-Free?	Temperature
MCF5270AB100	MCF5270 RISC Microprocessor	160 QFP	100MHz	Yes	0° to +70° C
MCF5270CAB100	MCF5270 RISC Microprocessor	160 QFP	100MHz	Yes	-40° to +85° C
MCF5270VM100	MCF5270 RISC Microprocessor	196 MAPBGA	100MHz	Yes	0° to +70° C
MCF5270CVM150	MCF5270 RISC Microprocessor	196 MAPBGA	150MHz	Yes	-40° to +85° C
MCF5271CAB100	MCF5271 RISC Microprocessor	160 QFP	100MHz	Yes	-40° to +85° C
MCF5271CVM100	MCF5271 RISC Microprocessor	196 MAPBGA	100MHz	Yes	-40° to +85° C
MCF5271CVM150	MCF5271 RISC Microprocessor	196 MAPBGA	150MHz	Yes	-40° to +85° C

7 Electrical Characteristics

This chapter contains electrical specification tables and reference timing diagrams for the MCF5271 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5271.

NOTE

The parameters specified in this processor document supersede any values found in the module specifications.

7.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to +2.0	V
Pad Supply Voltage	OV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	V_{DDPLL}	– 0.3 to +4.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to + 4.0	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3,4,5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 65 to 150	°C

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

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2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or OV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and OV_{DD}.

5 Power supply must maintain regulation within operating OV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > OV_{DD}$) is greater than I_{DD}, the injection current may flow out of OV_{DD} and could result in external power supply going out of regulation. Insure external OV_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power (ex; no clock).Power supply must maintain regulation within operating OV_{DD} range during instantaneous and operating maximum current conditions.

7.2 Thermal Characteristics

The below table lists thermal resistance values.

Table 8. Thermal Characteristics

Characteristic		Symbol	196 MAPBGA	160QFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	32[1,2]	40[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	29[1,2]	36[1,2]	°C/W
Junction to board		θ_{JB}	20[3]	25[3]	°C/W
Junction to case		θ_{JC}	10[4]	10[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	2[1,5]	°C/W
Maximum operating junction temperature		T_j	104	105	°C

1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Motorola recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

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T_A= Ambient Temperature, °C

Θ_{JMA}= Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$= Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^{\ 2} \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

7.3 DC Electrical Specifications

Table 9. DC Electrical Specifications[1]

Characteristic	Symbol	Min	Typical	Max	Unit
Core Supply Voltage	V_{DD}	1.4	—	1.6	V
Pad Supply Voltage	OV_{DD}	3.0	—	3.6	V
PLL Supply Voltage	V_{DDPLL}	3.0	—	3.6	V
Input High Voltage	V_{IH}	$0.7 \times OV_{DD}$	—	3.65	V
Input Low Voltage	V_{IL}	$V_{SS} - 0.3$	—	$0.35 \times OV_{DD}$	V
Input Hysteresis	V_{HYS}	$0.06 \times OV_{DD}$	—	—	mV
Input Leakage Current $V_{in} = V_{DD}$ or V_{SS}, Input-only pins	I_{in}	–1.0	—	1.0	μA
High Impedance (Off-State) Leakage Current $V_{in} = V_{DD}$ or V_{SS}, All input/output and output pins	I_{OZ}	–1.0	—	1.0	μA
Output High Voltage (All input/output and all output pins) I_{OH} = –5.0 mA	V_{OH}	OV_{DD} - 0.5	—	—	V
Output Low Voltage (All input/output and all output pins) I_{OL} = 5.0mA	V_{OL}	—	—	0.5	V
Weak Internal Pull Up Device Current, tested at V_{IL} Max.[2]	I_{APU}	–10	—	– 130	μA
Input Capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	—	 7 7	pF

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Table 9. DC Electrical Specifications[1] (continued)

Characteristic	Symbol	Min	Typical	Max	Unit
Load Capacitance[4] Low drive strength High drive strength	C_L		— —	25 50	pF pF
Core Operating Supply Current [5] Master Mode	I_{DD}	—	135	150	mA
Pad Operating Supply Current Master Mode Low Power Modes	OI_{DD}	— —	100 TBD	— —	mA μA
DC Injection Current [3, 6, 7, 8] $V_{NEGCLAMP} = V_{SS} - 0.3$ V, $V_{POSCLAMP} = V_{DD} + 0.3$ Single Pin Limit Total processor Limit, Includes sum of all stressed pins	I_{IC}	 –1.0 –10		 1.0 10	 mA mA

1 Refer to Table 10 for additional PLL specifications.
2 Refer to the MCF5271 signals section for pins having weak internal pull-up devices.
3 This parameter is characterized before qualification rather than 100% tested.
4 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination. See High Speed Signal Propagation: Advanced Black Magic by Howard W. Johnson for design guidelines.
5 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.
6 All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.
7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
8 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Insure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the processor is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, system clock is not present during the power-up sequence until the PLL has attained lock.

7.4 Oscillator and PLLMRFM Electrical Characteristics

Table 10. HiP7 PLLMRFM Electrical Specifications[1]

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference 1:1 mode (NOTE: $f_{sys/2} = 2 \times f_{ref\_1:1}$)	 $f_{ref\_crystal}$ f_{ref_ext} $f_{ref\_1:1}$	 8 8 24	 25 25 75	MHz
2	Core frequency CLKOUT Frequency [2] External reference On-Chip PLL Frequency	f_{sys} $f_{sys/2}$	 0 $f_{ref} \div 32$	150 75 75	MHz MHz MHz
3	Loss of Reference Frequency [3, 5]	f_{LOR}	100	1000	kHz
4	Self Clocked Mode Frequency [4, 5]	f_{SCM}	10.25	15.25	MHz
5	Crystal Start-up Time [5, 6]	t_{cst}	—	10	ms

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Table 10. HiP7 PLLMRFM Electrical Specifications[1] (continued)

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
6	XTAL Load Capacitance[5]		5	30	pF
7	PLL Lock Time [5, 7,13]	t_{lpll}	—	750	µs
8	Power-up To Lock Time [5, 6,8] With Crystal Reference (includes 5 time) Without Crystal Reference[9]	t_{lplk}	 — —	 11 750	 ms µs
9	1:1 Mode Clock Skew (between CLKOUT and EXTAL) [10]	t_{skew}	–1	1	ns
10	Duty Cycle of reference [5]	t_{dc}	40	60	%
11	Frequency un-LOCK Range	f_{UL}	–3.8	4.1	% $f_{sys/2}$
12	Frequency LOCK Range	f_{LCK}	–1.7	2.0	% $f_{sys/2}$
13	CLKOUT Period Jitter, [5, 6, 8,11, 12] Measured at $f_{sys/2}$ Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter (Averaged over 2 ms interval)	C_{jitter}	 — —	 5.0 .01	% $f_{sys/2}$
14	Frequency Modulation Range Limit[13,14] ($f_{sys/2}$ Max must not be exceeded)	C_{mod}	0.8	2.2	%$f_{sys/2}$
15	ICO Frequency. $f_{ico} = f_{ref} \times 2 \times (MFD+2)$ [15]	f_{ico}	48	150	MHz

1 All values given are initial design targets and subject to change.
2 All internal registers retain data at 0 Hz.
3 "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.
4 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR} with default MFD/RFD settings.
5 This parameter is guaranteed by characterization before qualification rather than 100% tested.
6 Proper PC board layout procedures must be followed to achieve specifications.
7 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
8 Assuming a reference is available at power up, lock time is measured from the time V_{DD} and V_{DDSYN} are valid to $\overline{RSTOUT}$ negating. If the crystal oscillator is being used as the reference for the PLL, then the crystal start up time must be added to the PLL lock time to determine the total start-up time.
9 $t_{lpll} = (64 * 4 * 5 + 5\ \tau)\ T_{ref}$, where $T_{ref} = 1/F_{ref\_crystal} = 1/F_{ref\_ext} = 1/F_{ref\_1:1}$, and $\tau = 1.57x10^{-6}\ 2(MFD + 2)$.
10 PLL is operating in 1:1 PLL mode.
11 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys/2}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDSYN} and V_{SSSYN} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.
12 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of Cjitter+Cmod.
13 Modulation percentage applies over an interval of 10µs, or equivalently the modulation rate is 100KHz.
14 Modulation rate selected must not result in $f_{sys/2}$ value greater than the $f_{sys/2}$ maximum specified value. Modulation range determined by hardware design.
15 $f_{sys/2} = f_{ico} / (2 * 2^{RFD})$

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7.5 External Interface Timing Characteristics

Table 11 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the CLKOUT output.

All other timing relationships can be derived from these values.

Table 11. Processor Bus Input Timing Specifications

Name	Characteristic[1]	Symbol	Min	Max	Unit
freq	System bus frequency	$f_{sys/2}$	50	75	MHz
B0	CLKOUT period	t_{cyc}	—	1/75	ns
Control Inputs					
B1a	Control input valid to CLKOUT high[2]	t_{CVCH}	9	—	ns
B1b	$\overline{BKPT}$ valid to CLKOUT high[3]	t_{BKVCH}	9	—	ns
B2a	CLKOUT high to control inputs invalid[2]	t_{CHCII}	0	—	ns
B2b	CLKOUT high to asynchronous control input $\overline{BKPT}$ invalid[3]	t_{BKNCH}	0	—	ns
Data Inputs					
B4	Data input (D[31:0]) valid to CLKOUT high	t_{DIVCH}	4	—	ns
B5	CLKOUT high to data input (D[31:0]) invalid	t_{CHDII}	0	—	ns

1 Timing specifications are tested using full drive strength pad configurations in a 50ohm transmission line environment..
2 $\overline{TEA}$ and $\overline{TA}$ pins are being referred to as control inputs.
3 Refer to figure A-19.

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Timings listed in Table 11 are shown in Figure 7.

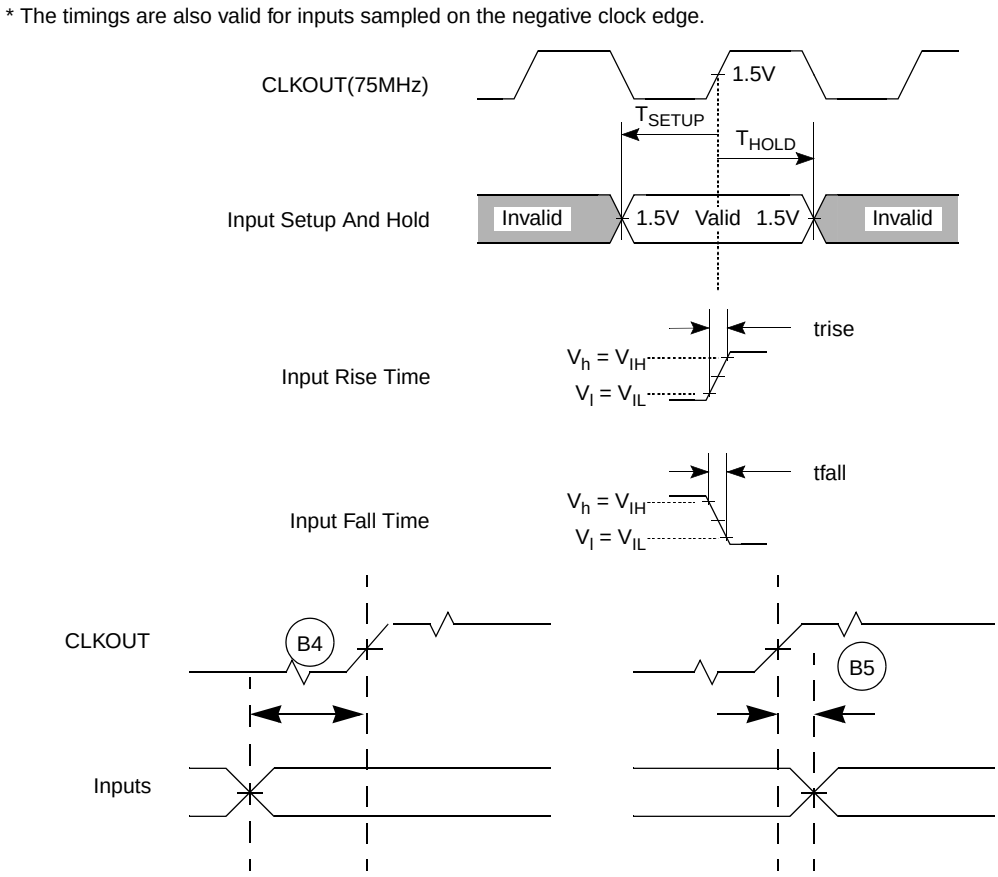

Figure 7. General Input Timing Requirements

7.6 Processor Bus Output Timing Specifications

Table 12 lists processor bus output timings.

Table 12. External Bus Output Timing Specifications

Name	Characteristic	Symbol	Min	Max	Unit
Control Outputs					
B6a	CLKOUT high to chip selects valid [1]	t_{CHCV}	—	$0.5t_{CYC}$ +5	ns
B6b	CLKOUT high to byte enables ($\overline{BS}$[3:0]) valid[2]	t_{CHBV}	—	$0.5t_{CYC}$ +5	ns
B6c	CLKOUT high to output enable ($\overline{OE}$) valid[3]	t_{CHOV}	—	$0.5t_{CYC}$ +5	ns
B7	CLKOUT high to control output ($\overline{BS}$[3:0], $\overline{OE}$) invalid	t_{CHCOI}	$0.5t_{CYC}$+1.5	—	ns
B7a	CLKOUT high to chip selects invalid	t_{CHCI}	$0.5t_{CYC}$+1.5	—	ns

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Table 12. External Bus Output Timing Specifications (continued)

Name	Characteristic	Symbol	Min	Max	Unit
Address and Attribute Outputs					
B8	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) valid	t_{CHAV}	—	9	ns
B9	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, $\overline{TSIZ}$[1:0], $\overline{TIP}$, R/$\overline{W}$) invalid	t_{CHAI}	1.5	—	ns
Data Outputs					
B11	CLKOUT high to data output (D[31:0]) valid	t_{CHDOV}	—	9	ns
B12	CLKOUT high to data output (D[31:0]) invalid	t_{CHDOI}	1.5	—	ns
B13	CLKOUT high to data output (D[31:0]) high impedance	t_{CHDOZ}	—	9	ns

1 $\overline{CS}$ transitions after the falling edge of CLKOUT.
2 $\overline{BS}$ transitions after the falling edge of CLKOUT.
3 $\overline{OE}$ transitions after the falling edge of CLKOUT.

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Read/write bus timings listed in Table 12 are shown in Figure 8, Figure 9, and Figure 10.

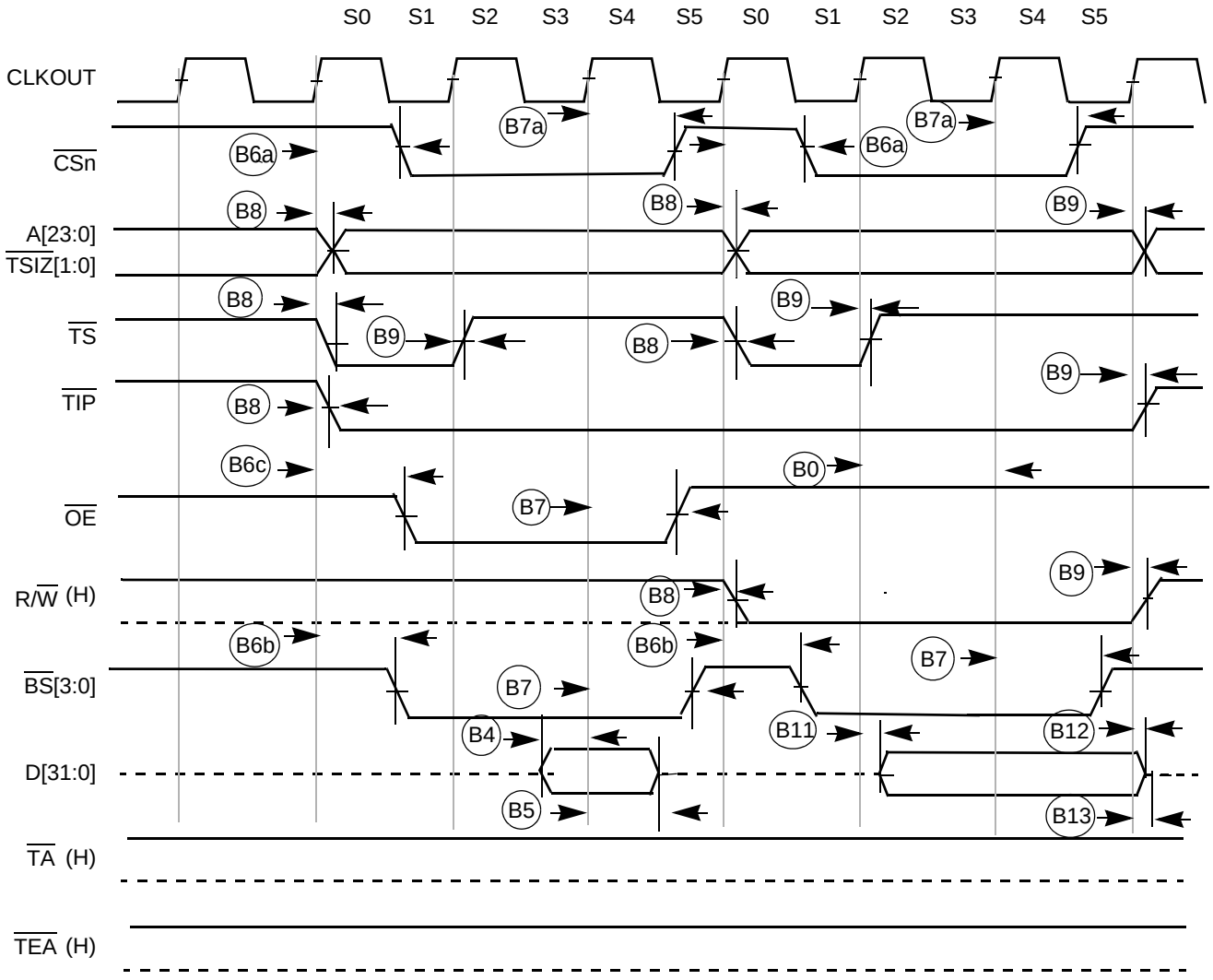

Figure 8. Read/Write (Internally Terminated) SRAM Bus Timing

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MCF527x products in 196 MAPBGA packages

Figure 9 shows a bus cycle terminated by $\overline{TA}$ showing timings listed in Table 12.

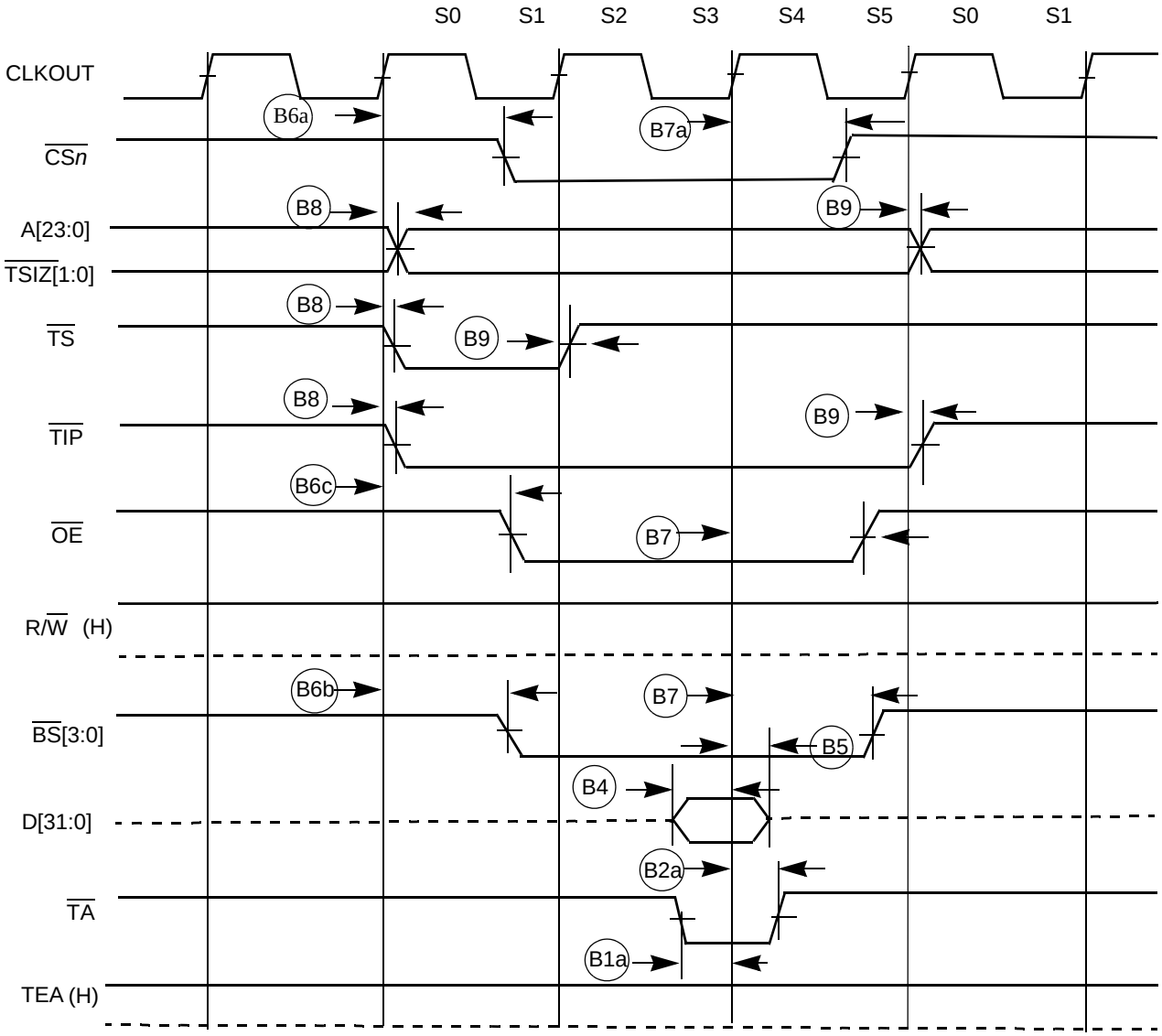

Figure 9. SRAM Read Bus Cycle Terminated by $\overline{TA}$

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Figure 10 shows an SRAM bus cycle terminated by $\overline{\text{TEA}}$ showing timings listed in Table 12.

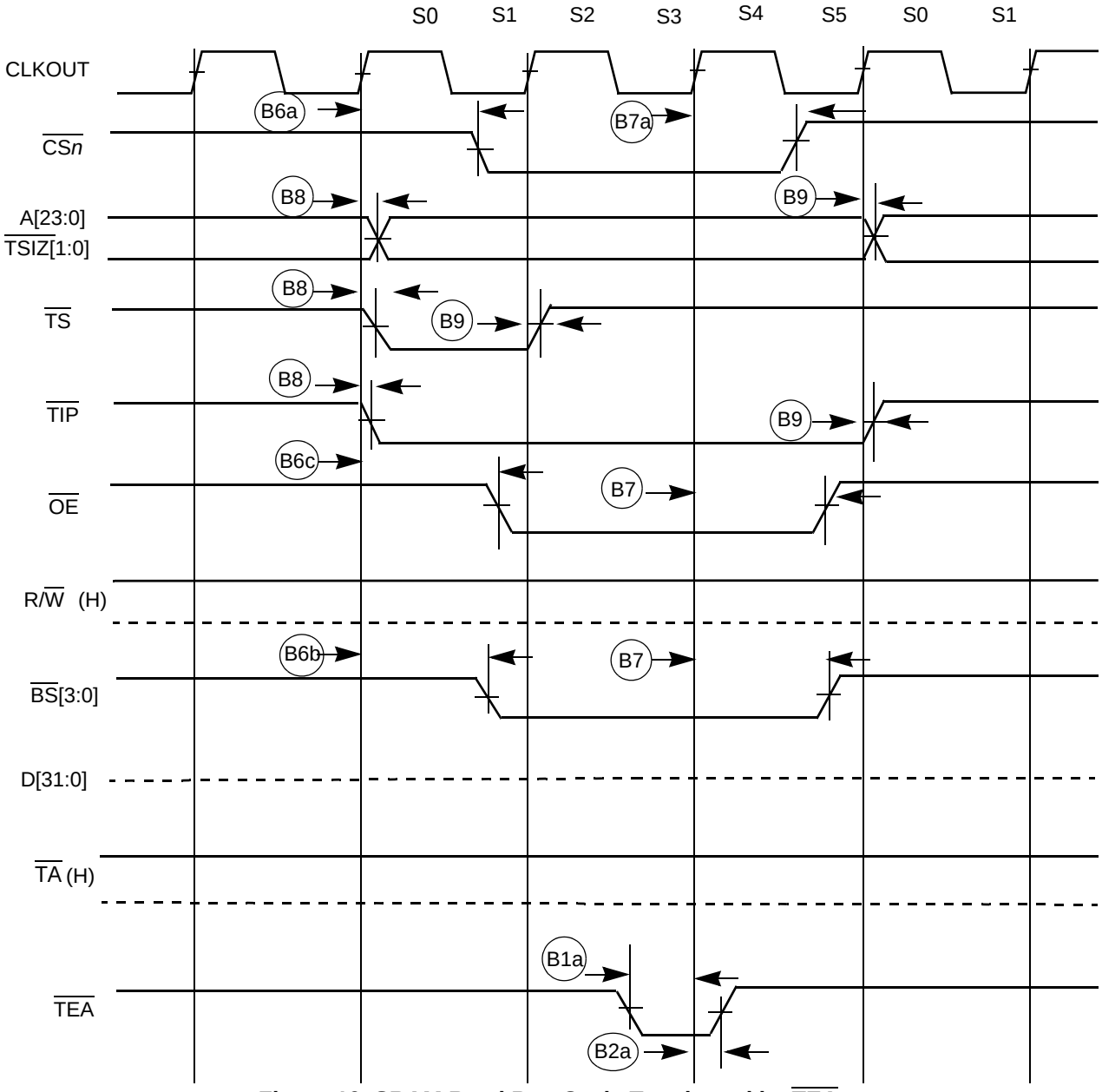

Figure 10. SRAM Read Bus Cycle Terminated by $\overline{\text{TEA}}$

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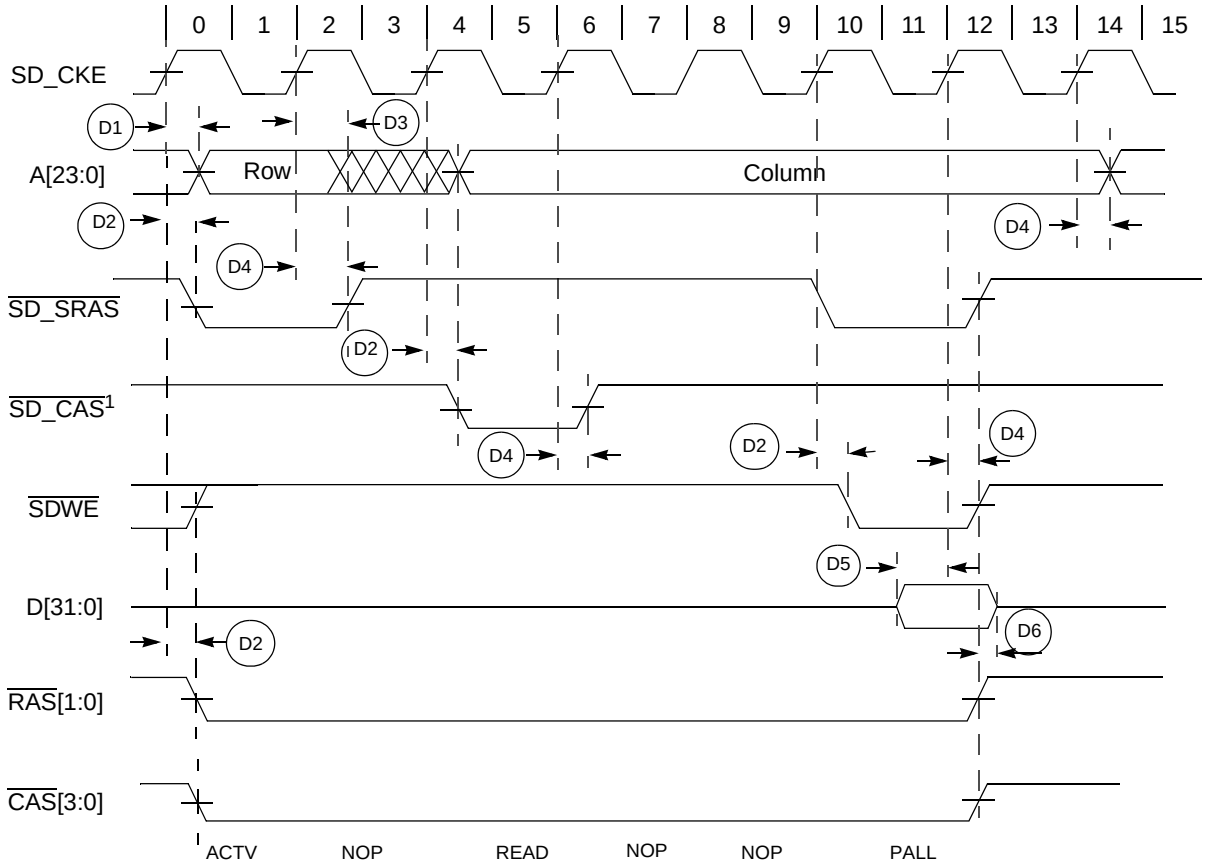
Figure 11 shows an SDRAM read cycle.



1 DACR[CASL] = 2

Figure 11. SDRAM Read Cycle

Table 13. SDRAM Timing

NUM	Characteristic	Symbol	Min	Max	Unit
D1	CLKOUT high to SDRAM address valid	t_{CHDAV}	—	9	ns
D2	CLKOUT high to SDRAM control valid	t_{CHDCV}	—	9	ns
D3	CLKOUT high to SDRAM address invalid	t_{CHDAI}	1.5	—	ns
D4	CLKOUT high to SDRAM control invalid	t_{CHDCI}	1.5	—	ns
D5	SDRAM data valid to CLKOUT high	t_{DDVCH}	4	—	ns
D6	CLKOUT high to SDRAM data invalid	t_{CHDDI}	1.5	—	ns
D7[1]	CLKOUT high to SDRAM data valid	t_{CHDDVW}	—	9	ns
D8[1]	CLKOUT high to SDRAM data invalid	t_{CHDDIW}	1.5	—	ns

1 D7 and D8 are for write cycles only.

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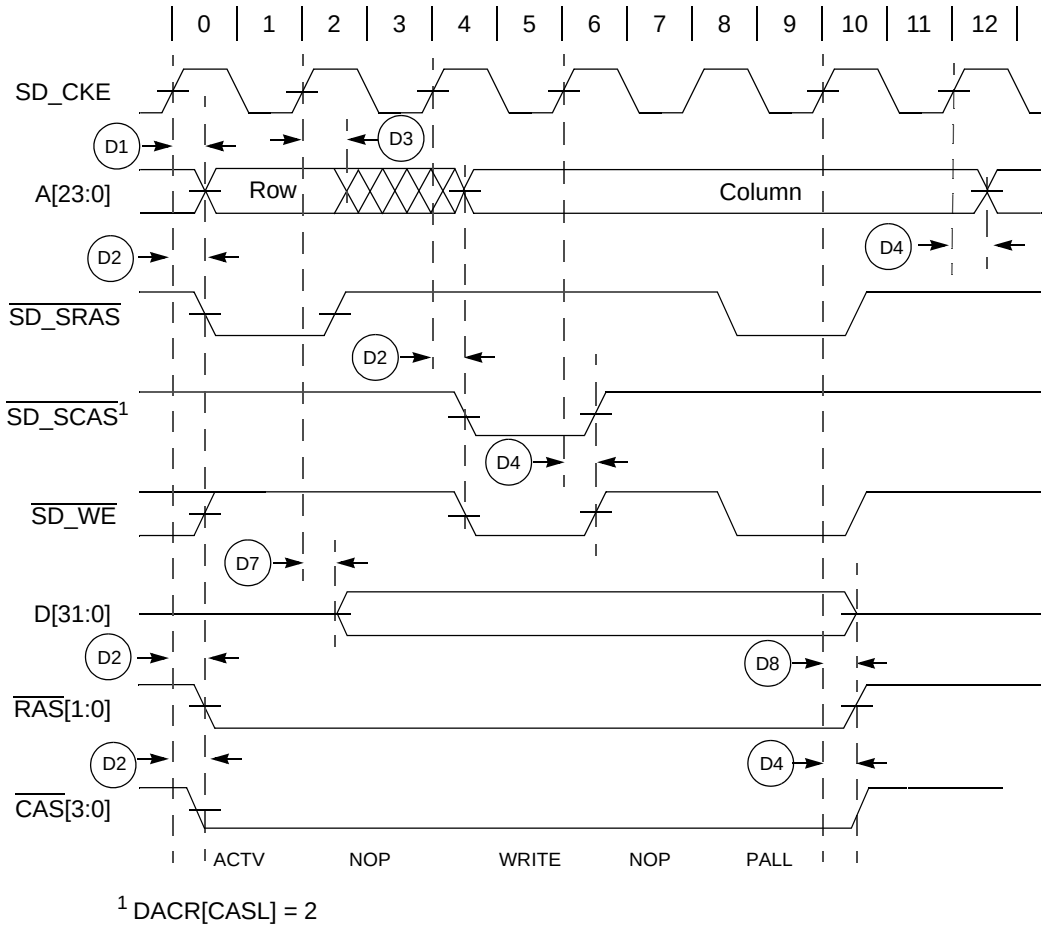
Figure 12 shows an SDRAM write cycle.



1 DACR[CASL] = 2

Figure 12. SDRAM Write Cycle

7.7 General Purpose I/O Timing

Table 14. GPIO Timing[1]

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

1 GPIO pins include: INT, UART, Timer, $\overline{\text{DREQ}n}$ and $\overline{\text{DACK}n}$ pins.

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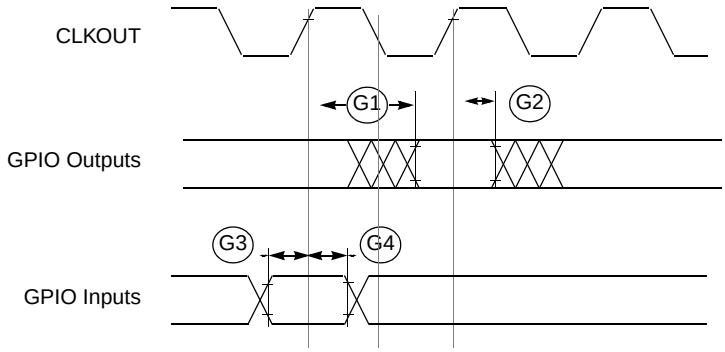

Figure 13. GPIO Timing

7.8 Reset and Configuration Override Timing

Table 15. Reset and Configuration Override Timing
(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, $T_A = T_L$ to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

1 All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.
2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

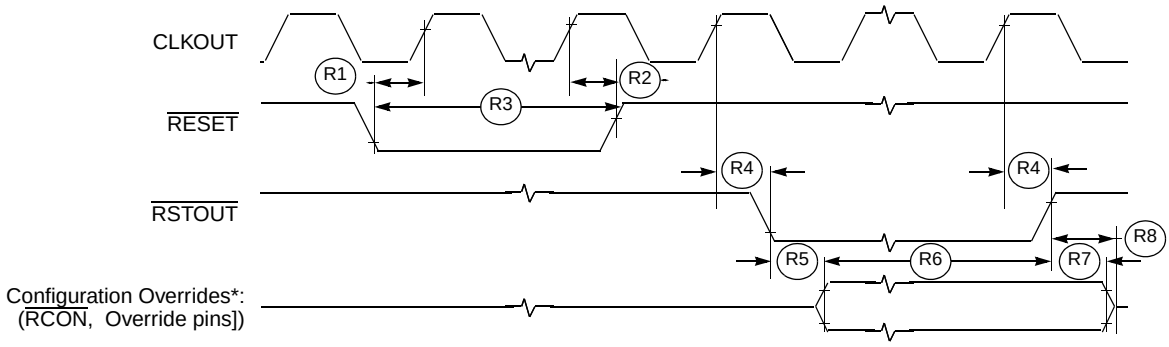

Figure 14. $\overline{\text{RESET}}$ and Configuration Override Timing

Refer to the chip configuration module (CCM) chapter in the device's reference manual for more information.

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7.9 I²C Input/Output Timing Specifications

Table 16 lists specifications for the I²C input timing parameters shown in Figure 15.

Table 16. I²C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	t_{cyc}
I2	Clock low period	8	—	t_{cyc}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	t_{cyc}
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	t_{cyc}
I9	Stop condition setup time	2	—	t_{cyc}

Table 17 lists specifications for the I²C output timing parameters shown in Figure 15.

Table 17. I²C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6	—	t_{cyc}
I2 [1]	Clock low period	10	—	t_{cyc}
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	7	—	t_{cyc}
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10	—	t_{cyc}
I7 [1]	Data setup time	2	—	t_{cyc}
I8 [1]	Start condition setup time (for repeated start condition only)	20	—	t_{cyc}
I9 [1]	Stop condition setup time	10	—	t_{cyc}

1 Note: Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 17. The I²C interface is designed to scale the actual data transition time to move it to the middle of the I2C_SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 17 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 15 shows timing for the values in Table 16 and Table 17.

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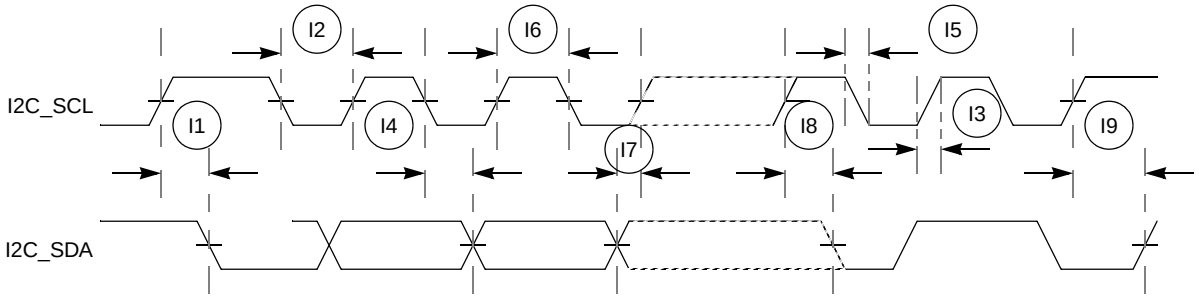

Figure 15. I²C Input/Output Timings

7.10 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

7.10.1 MII Receive Signal Timing (ERXD[3:0], ERXDV, ERXER, and ERXCLK)

The receiver functions correctly up to a ERXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the ERXCLK frequency.

Table 18 lists MII receive channel timings.

Table 18. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	ERXD[3:0], ERXDV, ERXER to ERXCLK setup	5	—	ns
M2	ERXCLK to ERXD[3:0], ERXDV, ERXER hold	5	—	ns
M3	ERXCLK pulse width high	35%	65%	ERXCLK period
M4	ERXCLK pulse width low	35%	65%	ERXCLK period

Figure 16 shows MII receive signal timings listed in Table 18.

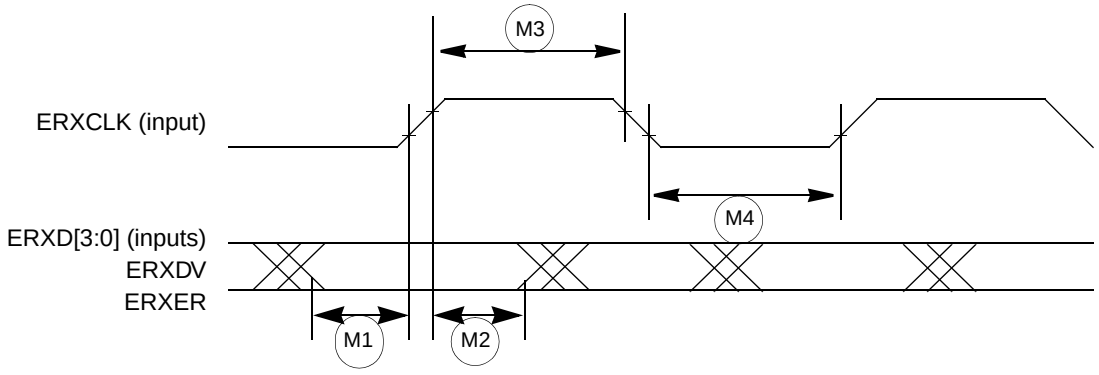

Figure 16. MII Receive Signal Timing Diagram

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7.10.2 MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK)

Table 19 lists MII transmit channel timings.

The transmitter functions correctly up to a ETXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the ETXCLK frequency.

Table 19. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	ETXCLK to ETXD[3:0], ETXEN, ETXER invalid	5	—	ns
M6	ETXCLK to ETXD[3:0], ETXEN, ETXER valid	—	25	ns
M7	ETXCLK pulse width high	35%	65%	ETXCLK period
M8	ETXCLK pulse width low	35%	65%	ETXCLK period

Figure 17 shows MII transmit signal timings listed in Table 19.

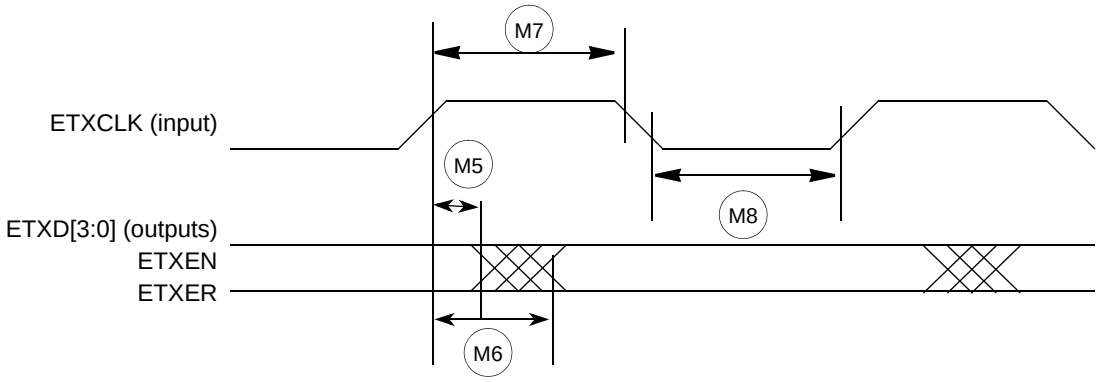

Figure 17. MII Transmit Signal Timing Diagram

7.10.3 MII Async Inputs Signal Timing (ECRS and ECOL)

Table 20 lists MII asynchronous inputs signal timing.

Table 20. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	ECRS, ECOL minimum pulse width	1.5	—	ETXCLK period

Figure 18 shows MII asynchronous input timings listed in Table 20.

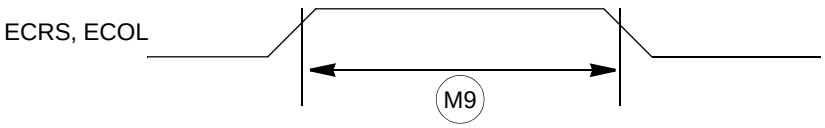

Figure 18. MII Async Inputs Timing Diagram

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7.10.4 MII Serial Management Channel Timing (EMDIO and EMDC)

Table 21 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 21. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	EMDC falling edge to EMDIO output invalid (minimum propagation delay)	0	—	ns
M11	EMDC falling edge to EMDIO output valid (max prop delay)	—	25	ns
M12	EMDIO (input) to EMDC rising edge setup	10	—	ns
M13	EMDIO (input) to EMDC rising edge hold	0	—	ns
M14	EMDC pulse width high	40%	60%	MDC period
M15	EMDC pulse width low	40%	60%	MDC period

Figure 19 shows MII serial management channel timings listed in Table 21.

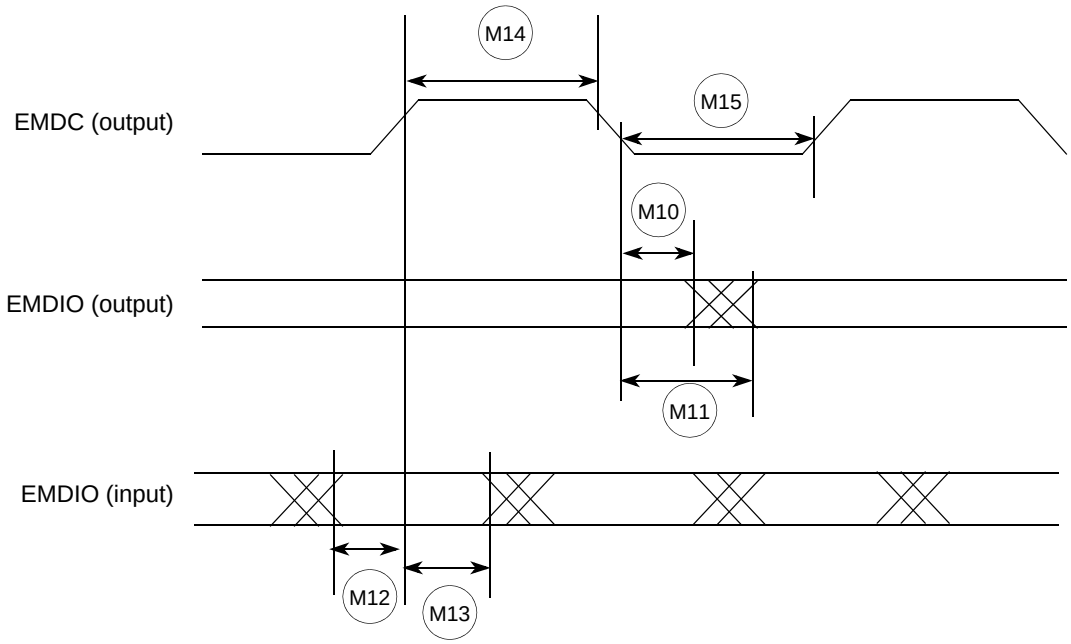

Figure 19. MII Serial Management Channel Timing Diagram

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7.11 32-Bit Timer Module AC Timing Specifications

Table 22 lists timer module AC timings.

Table 22. Timer Module AC Timing Specifications

Name	Characteristic	0–66 MHz		Unit
		Min	Max	
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

7.12 QSPI Electrical Specifications

Table 23 lists QSPI timings.

Table 23. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[1:0] to QSPI_CLK	1	510	tcyc
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 23 correspond to Figure 20.

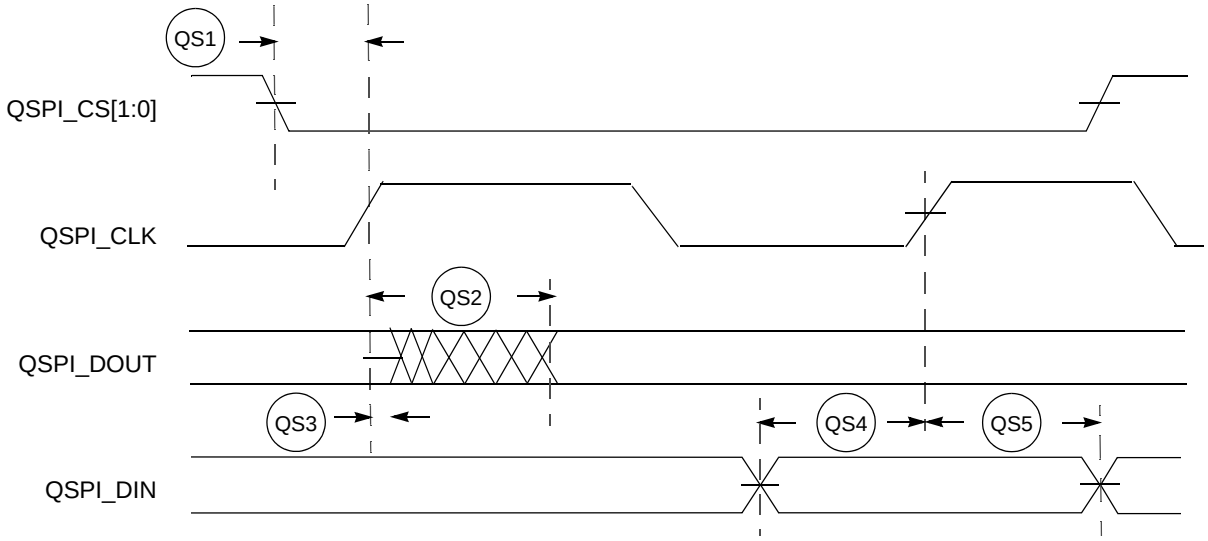

Figure 20. QSPI Timing

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7.13 JTAG and Boundary Scan Timing

Table 24. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

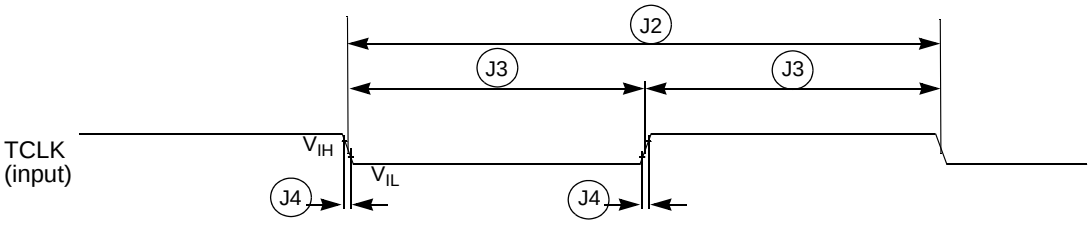

Figure 21. Test Clock Input Timing

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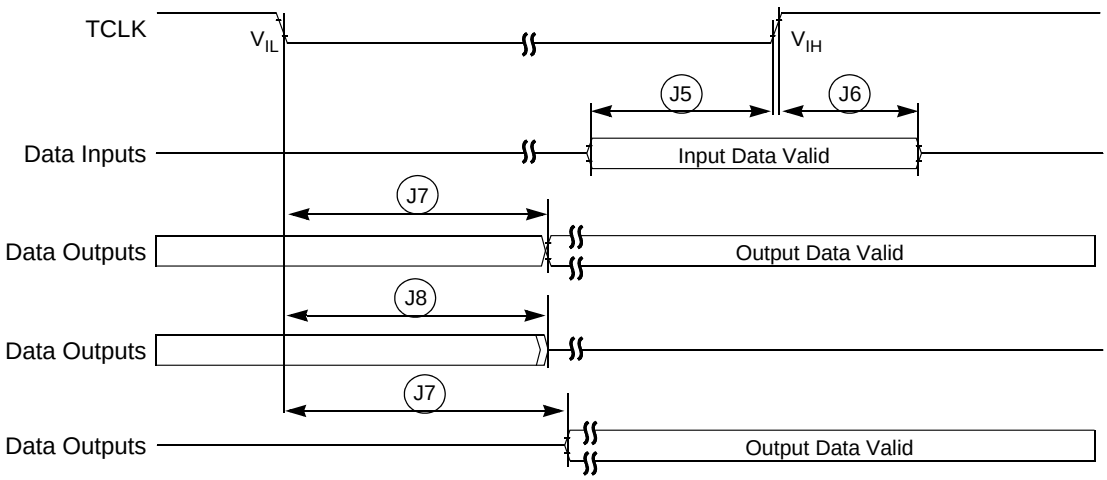

Figure 22. Boundary Scan (JTAG) Timing

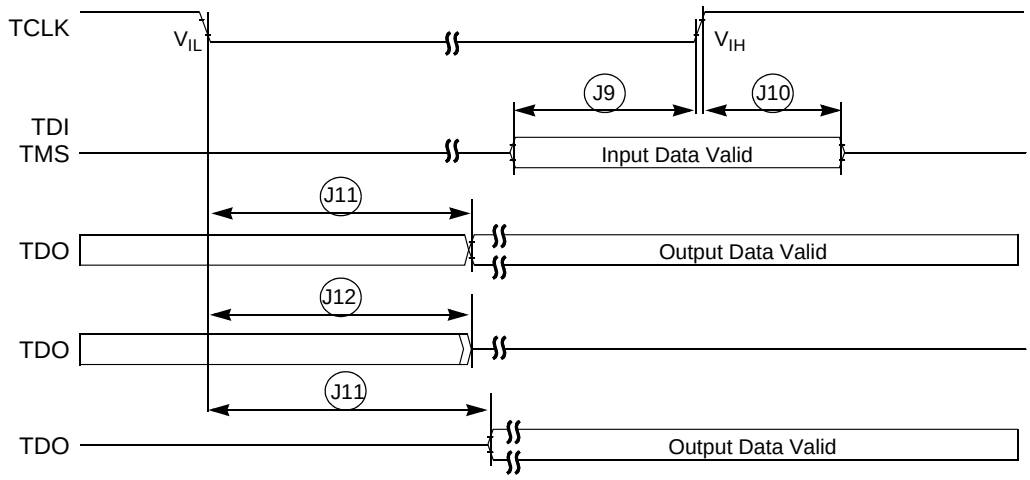

Figure 23. Test Access Port Timing

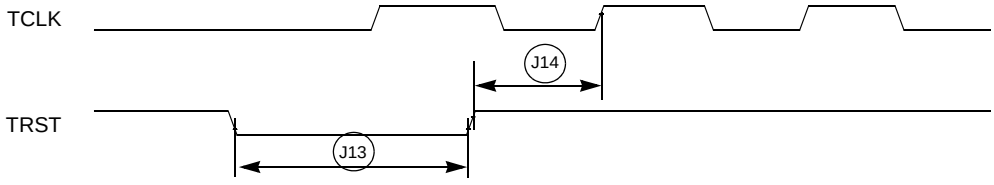

Figure 24. $\overline{\text{TRST}}$ Timing

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7.14 Debug AC Timing Specifications

Table 25 lists specifications for the debug AC timing parameters shown in Figure 26.

Table 25. Debug AC Timing Specification

Num	Characteristic	150 MHz		Units
		Min	Max	
DE0	PSTCLK cycle time	—	0.5	t_{cyc}
DE1	PST valid to PSTCLK high	4	—	ns
DE2	PSTCLK high to PST invalid	1.5	—	ns
DE3	DSCLK cycle time	5	—	t_{cyc}
DE4	DSI valid to DSCLK high	1	—	t_{cyc}
DE5[1]	DSCLK high to DSO invalid	4	—	t_{cyc}
DE6	$\overline{\text{BKPT}}$ input data setup time to CLKOUT rise	4	—	ns
DE7	CLKOUT high to $\overline{\text{BKPT}}$ high Z	0	10	ns

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 25 shows real-time trace timing for the values in Table 25.

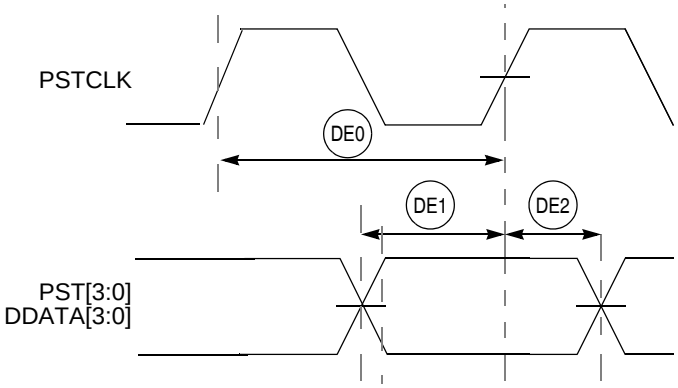

Figure 25. Real-Time Trace AC Timing

Figure 26 shows BDM serial port AC timing for the values in Table 25.

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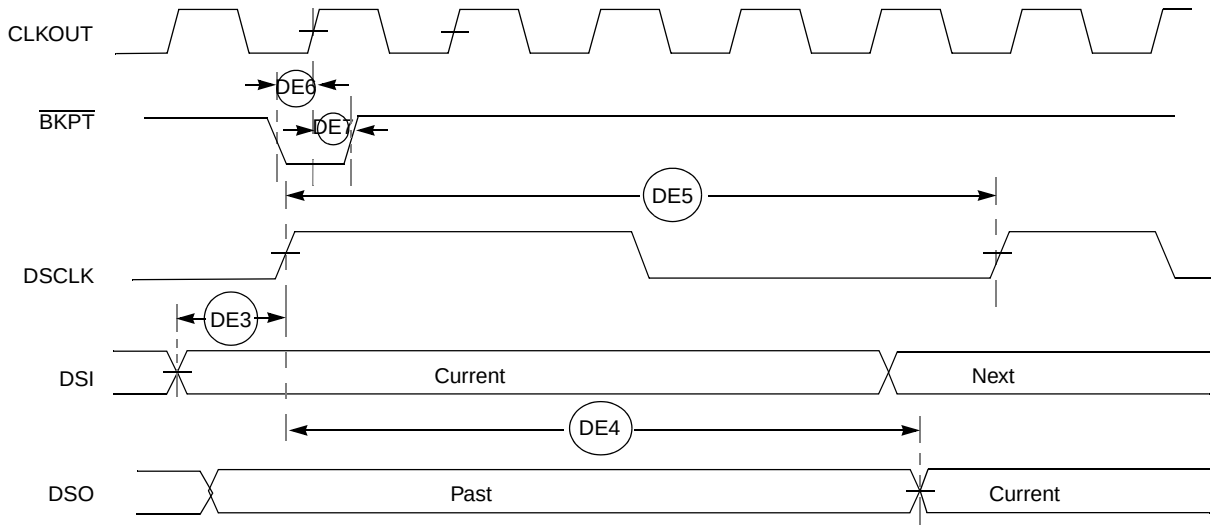

Figure 26. BDM Serial Port AC Timing

8 Documentation

Documentation regarding the MCF5271 and their development support tools is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale web address at http://www.freescale.com/coldfire.

9 Document Revision History

The below table provides a revision history for this document.

Table 26. MCF5271EC Revision History

Rev. No.	Substantive Change(s)
0	Initial release
1	• Fixed several clock values. • Updated Signal List table
1.1	• Removed duplicate information in the module description sections. The information is all in the Signals Description Table.
1.2	• Removed detailed signal description section. This information can be found in the MCF5271RM Chapter 2. • Removed detailed feature list. This information can be found in the MCF5271RM Chapter 1. • Changed instances of Motorola to Freescale • Added values for ‘Maximum operating junction temperature’ in Table 8. • Added typical values for ‘Core operating supply current (master mode)’ in Table 9. • Added typical values for ‘Pad operating supply current (master mode)’ in Table 9. • Removed unnecessary PLL specifications, #6-9, in Table 10.

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Table 26. MCF5271EC Revision History (continued)

Rev. No.	Substantive Change(s)
1.3	• Device is now available in 150 MHz versions. Updated specs where necessary to reflect this improvement. • Added 2 new part numbers to Table 6: MCF5270CVM150 and MCF5271CVM150. • Removed features list. This information can be found in the MCF5271RM. • Removed SDRAM address multiplexing section. This information can be found in the MCF5271RM.
1.4	• Added Section 5.2.1, “Supply Voltage Sequencing and Separation Cautions.” • Updated 196MAPBGA package dimensions, Figure 4.
2	• Table 2: Changed SD_CKE pin location from 139 to “—” for the 160QFP device. • Table 2: Changed QSPI_CS1 pin location from “—” to 139 for the 160QFP device. • Table 2: Changed DT3IN pin’s alternate 2 function from “—” to QSPI_CS2. • Table 2: Changed DT3OUT pin’s alternate 2 function from “—” to QSPI_CS3. • Figure 5: Changed pin 139 label from “SD_CKE/QSPI_CS1” to “QSPI_CS1/SD_CKE”. • Removed second sentence from Section 7.10.1, “MII Receive Signal Timing (ERXD[3:0], ERXDV, ERXER, and ERXCLK),” and Section 7.10.2, “MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK),” regarding no minimum frequency requirement for TXCLK. • Removed third and fourth paragraphs from Section 7.10.2, “MII Transmit Signal Timing (ETXD[3:0], ETXEN, ETXER, ETXCLK),” as this feature is not supported on this device.
3	• Section 5.2.1, “Supply Voltage Sequencing and Separation Cautions” changed $PLLV_{DD}$ to V_{DDPLL} to match rest of document. • Section 5.2.1, “Supply Voltage Sequencing and Separation Cautions” Changed V_{DDPLL} voltage level from 1.5V to 3.3V throughout section. • Section 5.2.1.1, “Power Up Sequence” first bullet, changed “Use 1 µs” to “Use 1 ms”. • Corrected position of spec D5 in Figure 11. • Figure 3: Corrected M4 ball location from DATA5 to DATA6, changed DATA*n* labels to D*n* for consistency • Table 14: Added $\overline{\text{DACK}}n$ and $\overline{\text{DREQ}}n$ to footnote. • Table 9, added PLL supply voltage row
4	• Added part number MCF5270CAB100 in Table 6

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