19-5252; Rev 0; 4/10

High-Bandwidth, ±15kV ESD Protection LVDS Switch

General Description

The MAX14979E is optimized for high-speed differential switching applications. The device is ideal for low-voltage differential signal (LVDS) and low-voltage positive emitter-coupled logic (LVPECL) switching applications. The MAX14979E provides enhanced electrostatic discharge (ESD) protection up to ±15kV and excellent high-frequency response, making this device especially useful for interfaces that must go to an outside connection.

The MAX14979E provides extremely low capacitance (C_{ON}) as well as low resistance (R_{ON}) for low-insertion loss and bandwidth up to 650MHz (1.3Gbps). In addition to the four pairs of double-pole/double-throw (DPDT) switches, the MAX14979E provides low-frequency (up to 50MHz) and AUX switching that can be used for LED lighting or other applications.

The MAX14979E is available in a space-saving 36-pin TQFN package and operates over the standard -40°C to +85°C temperature range.

Applications

Notebook Computers

Switch LVDS to Graphics Panels

LVDS and LVPECL Switching

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14979EETX+	-40°C to +85°C	36 TQFN-EP*

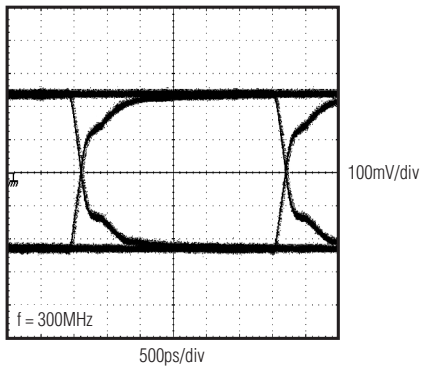
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Operating Circuit appears at end of data sheet.

Features

- **±15kV ESD Protected per MIL-STD-883, Method 3015**
- **Single +3.0V to +3.6V Power-Supply Voltage**
- **Low On-Resistance (R_{ON}): 4Ω (typ), 6.5Ω (max)**
- **Low On-Capacitance (C_{ON}): 8pF (typ)**
- **-23dB Return Loss (100MHz)**
- **-3dB Bandwidth: 650MHz**
- **Built-In AUX Switches for Switching Indicators**
- **Low 450µA (max) Quiescent Current**
- **Bidirectional 8 to 16 Multiplexer/Demultiplexer**
- **Space-Saving, Lead-Free, 36-Pin, 6mm x 6mm TQFN Package**

Eye Diagram



High-Bandwidth, ±15kV ESD Protection LVDS Switch

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)
V+ .....-0.3V to +4.0V
All Other Pins.....-0.3V to (V+ + 0.3V)
Continuous Current (COM_ _ to NC_ _/NO_ _) ..... ±120mA
Continuous Current (AUX0_ to AUX1_/AUX2_)..... ±40mA
Peak Current (COM_ _ to NC_ _/NO_ _)
(pulsed at 1ms, 10% duty cycle)..... ±240mA
Current into Any Other Pin ..... ±20mA
Continuous Power Dissipation (T_A = +70°C)
36-Pin TQFN (derate 35.7mW/°C above +70°C) 2.85mW
ESD Protection, Human Body Model (HBM) .....±15kV

Junction-to-Ambient Thermal Resistance
θ_{JA} (Note 1) .....8°C/W
Junction-to-Case Thermal Resistance
θ_{JC} (Note 1) .....1°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +3.0V to +3.6V, T_A = T_J = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Operating Power-Supply Range	V_{CC}			+3.0		+3.6	V
ANALOG SWITCH							
On-Resistance	R_{ON}	V+ = 3V, $I_{COM\_\_}$ = -40mA, $V_{COM\_\_}$ = 0V, 1.5V, 3V	T_A = +25°C		4	5.5	Ω
			T_{MIN} to T_{MAX}			6.5	
On-Resistance AUX Switches	R_{ONAUX}	V+ = 3V, $I_{AUX0\_}$ = -40mA, $V_{AUX0\_}$ = 0V, 1.5V, 3V				40	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V+ = 3V, $I_{COM\_\_}$ = -40mA, $V_{COM\_\_}$ = 0V, 3V (Note 3)	T_A = +25°C		0.5	1.5	Ω
			T_{MIN} to T_{MAX}			2	
On-Resistance Flatness	$R_{FLAT(ON)}$	V+ = 3V, $I_{COM\_\_}$ = -40mA, $V_{COM\_\_}$ = 0V, 1.5V			0.01		Ω
Off-Leakage Current	$I_{LCOM\_\_(OFF)}$	V+ = 3.6V, $V_{COM\_\_}$ = 0.3V, 3.3V; $V_{NC\_\_}$ or $V_{NO\_\_}$ = 3.3V, 0.3V		-1		+1	µA
On-Leakage Current	$I_{LCOM\_\_(ON)}$	V+ = 3.6V, $V_{COM\_\_}$ = 0.3V, 3.3V; $V_{NC\_\_}$ or $V_{NO\_\_}$ = 3.3V, 0.3V or unconnected		-1		+1	µA
SWITCH AC PERFORMANCE							
Insertion Loss	I_{LOS}	R_S = R_L = 50Ω, unbalanced, f = 1MHz, (Note 3)			0.6		dB
Return Loss	R_{LOS}	f = 100MHz			-23		dB
Crosstalk	V_{CT1}	Any switch to any switch; R_S = R_L = 50Ω, unbalanced, Figure 1	f = 25MHz		-50		dB
	V_{CT2}		f = 125MHz		-26		
SWITCH AC CHARACTERISTICS							
-3dB Bandwidth	BW	R_S = R_L = 50Ω, unbalanced			650		MHz
Off-Capacitance	C_{OFF}	f = 1MHz, COM_ _			3.5		pF
On-Capacitance	C_{ON}	f = 1MHz, COM_ _			8		pF

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +3.0V to +3.6V, $T_A = T_J = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at V+ = +3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Turn-On Time	t_{ON}	$V_{COM\_\_}$ = 1V, R_L = 100Ω, Figure 2			50	ns
Turn-Off Time	t_{OFF}	$V_{COM\_\_}$ = 1V, R_L = 100Ω, Figure 2			50	ns
Propagation Delay	t_{PLH}, t_{PHL}	$R_S = R_L$ = 50Ω, unbalanced, Figure 3		0.1		ns
Output Skew Between Ports	$t_{SK(o)}$	Skew between any two ports, Figure 4		0.01		ns
SWITCH LOGIC						
Input-Voltage Low	V_{IL}	V+ = 3.0V			0.8	V
Input-Voltage High	V_{IH}	V+ = 3.6V	2.0			V
Input-Logic Hysteresis	V_{HYST}	V+ = 3.3V		100		mV
Input Leakage Current	I_{SEL}	V+ = 3.6V, V_{SEL} = 0V or V+	-5		+5	µA
Quiescent Supply Current	I+	V+ = 3.6V, V_{SEL} = 0V or V+		280	450	µA
ESD PROTECTION						
ESD Protection		COM_ _, NC_ _, NO_ _ HBM (spec MIL-STD-883, Method 3015)		±15		kV
All Other Pins		HBM (spec MIL-STD-883, Method 3015)		±2		kV

Note 2: Specifications at T_A = -40°C are guaranteed by design.
Note 3: Guaranteed by design.

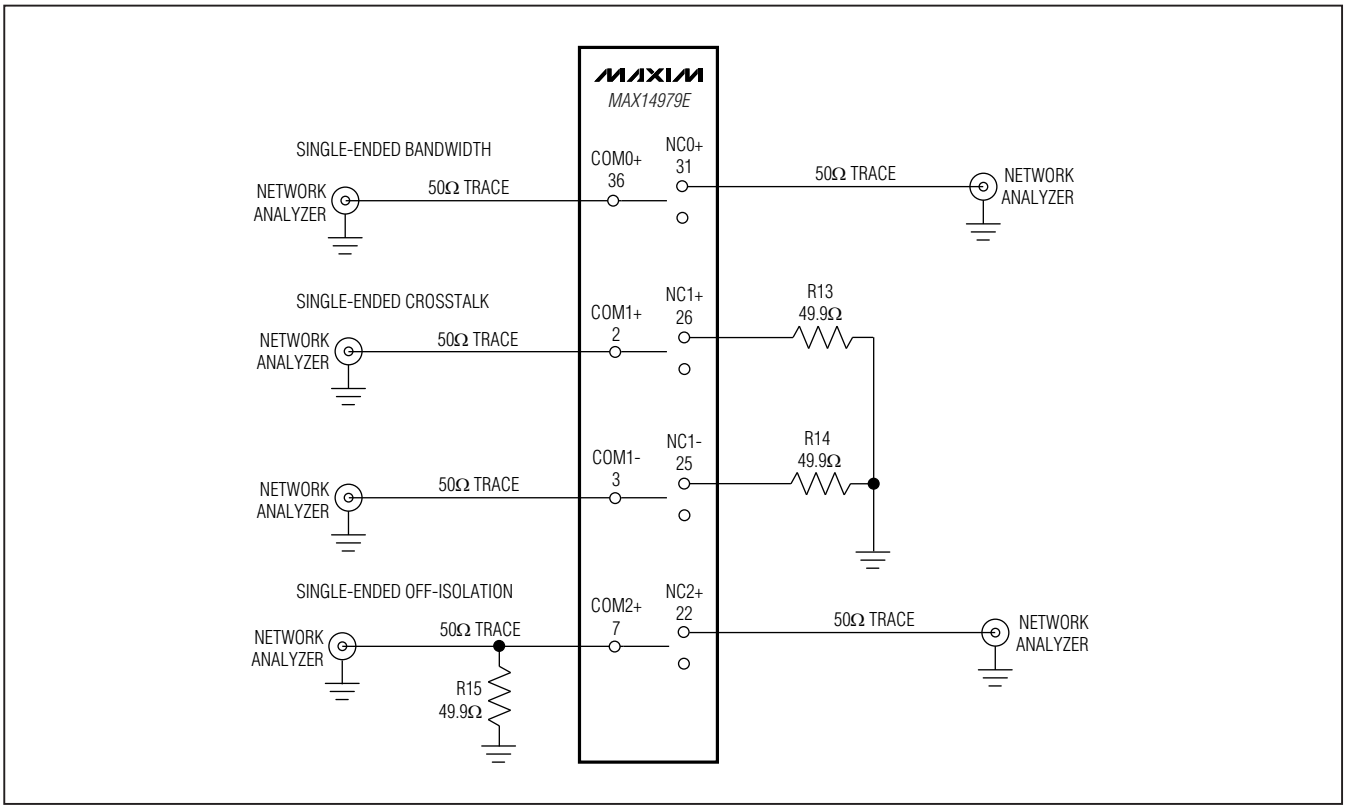


Figure 1. Single-Ended Bandwidth, Crosstalk, and Off-Isolation

High-Bandwidth, ±15kV ESD Protection LVDS Switch

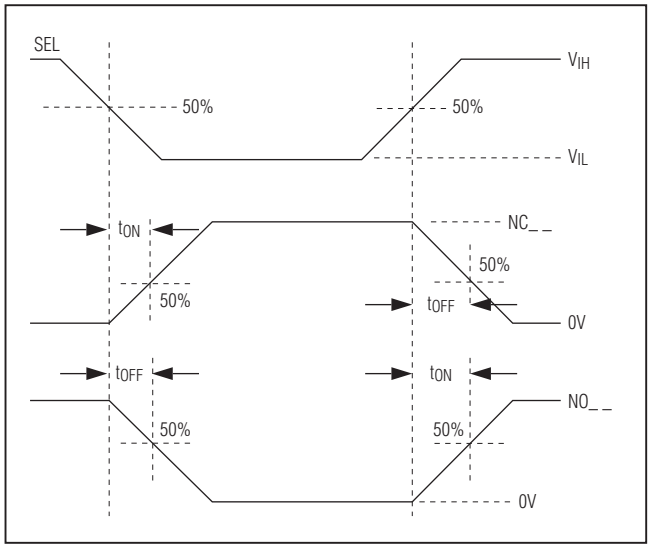


Figure 2. Turn-On and Turn-Off Times

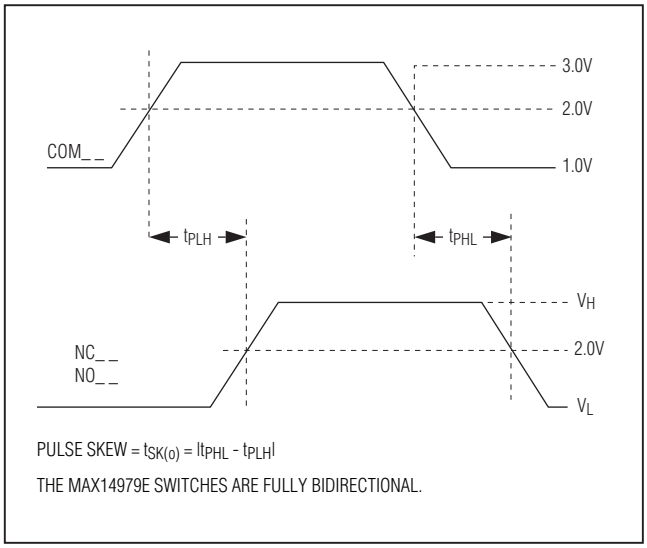


Figure 3. Propagation Delay Times

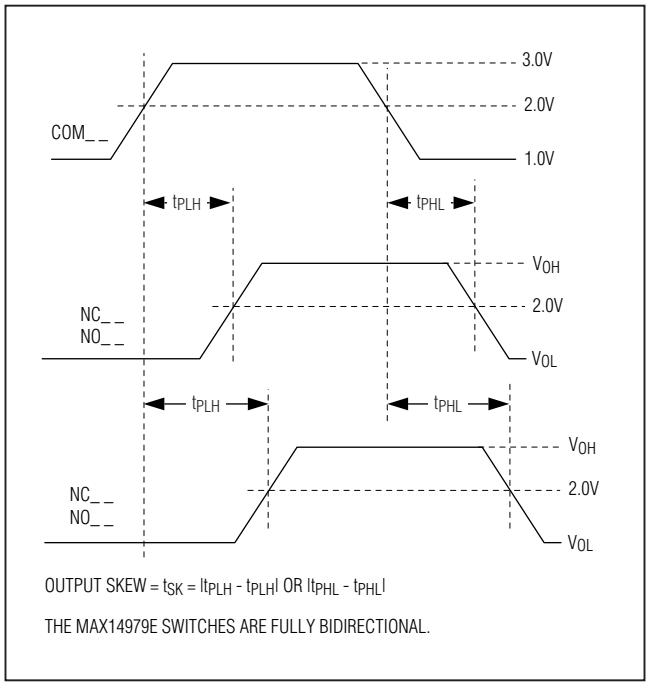
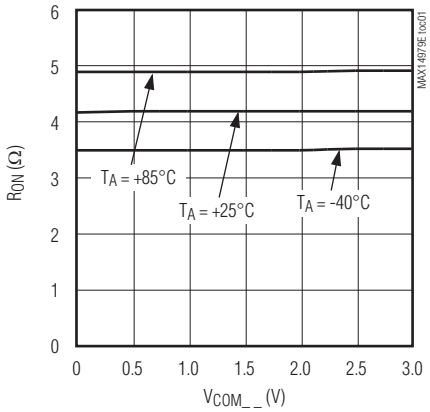


Figure 4. Output Skew

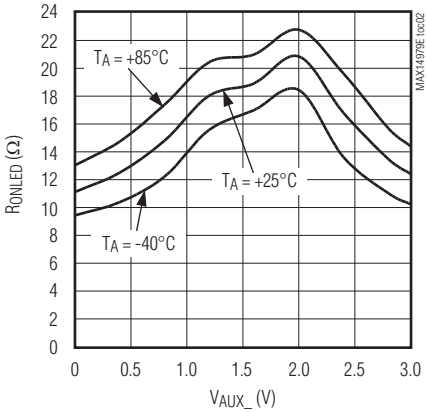
Typical Operating Characteristics

(V+ = 3.3V, T_A = +25°C, unless otherwise noted.)

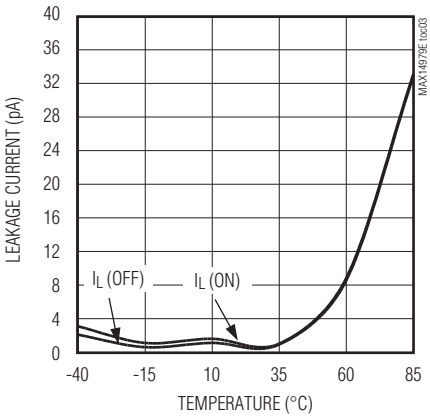
ON-RESISTANCE vs. $V_{COM\_\_}$



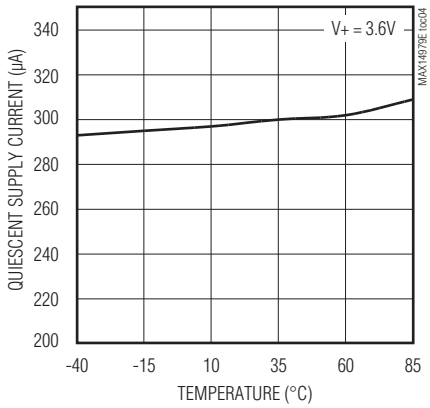
AUX_ ON-RESISTANCE vs. $V_{AUX\_}$



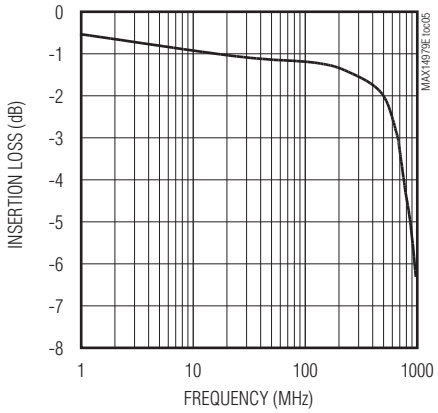
LEAKAGE CURRENT vs. TEMPERATURE



QUIESCENT SUPPLY CURRENT vs. TEMPERATURE

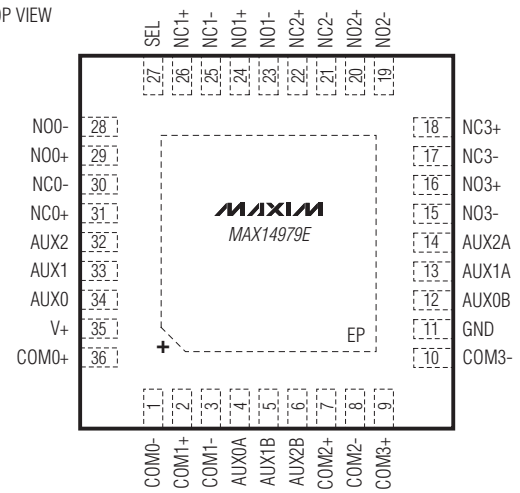


SINGLE-ENDED INSERTION LOSS vs. FREQUENCY



High-Bandwidth, ±15kV ESD Protection LVDS Switch

Pin Configuration



TQFN
(6mm × 6mm)

Pin Description

PIN	NAME	FUNCTION
1	COM0-	Common LVDS Differential Terminal for Switch 0
2	COM1+	Common LVDS Differential Terminal for Switch 1
3	COM1-	Common LVDS Differential Terminal for Switch 1
4	AUX0A	AUX0A Input
5	AUX1B	AUX1B Output. Drive SEL low (SEL = 0) to connect AUX0A to AUX1B.
6	AUX2B	AUX2B Output. Drive SEL high (SEL = 1) to connect AUX0A to AUX2B.
7	COM2+	Common LVDS Differential Terminal for Switch 2
8	COM2-	Common LVDS Differential Terminal for Switch 2
9	COM3+	Common LVDS Differential Terminal for Switch 3
10	COM3-	Common LVDS Differential Terminal for Switch 3
11	GND	Ground
12	AUX0B	AUX0B Input
13	AUX1A	AUX1A Output. Drive SEL low (SEL = 0) to connect AUX0B to AUX1A.
14	AUX2A	AUX2A Output. Drive SEL high (SEL = 1) to connect AUX0B to AUX2A.
15	NO3-	Normally Open LVDS Differential Terminal for Switch 3
16	NO3+	Normally Open LVDS Differential Terminal for Switch 3
17	NC3-	Normally Closed LVDS Differential Terminal for Switch 3
18	NC3+	Normally Closed LVDS Differential Terminal for Switch 3
19	NO2-	Normally Open LVDS Differential Terminal for Switch 2
20	NO2+	Normally Open LVDS Differential Terminal for Switch 2
21	NC2-	Normally Closed LVDS Differential Terminal for Switch 2

Pin Description (continued)

PIN	NAME	FUNCTION
22	NC2+	Normally Closed LVDS Differential Terminal for Switch 2
23	NO1-	Normally Open LVDS Differential Terminal for Switch 1
24	NO1+	Normally Open LVDS Differential Terminal for Switch 1
25	NC1-	Normally Closed LVDS Differential Terminal for Switch 1
26	NC1+	Normally Closed LVDS Differential Terminal for Switch 1
27	SEL	Select Input. SEL selects switch connection. See Table1.
28	NO0-	Normally Open LVDS Differential Terminal for Switch 0
29	NO0+	Normally Open LVDS Differential Terminal for Switch 0
30	NC0-	Normally Closed LVDS Differential Terminal for Switch 0
31	NC0+	Normally Closed LVDS Differential Terminal for Switch 0
32	AUX2	AUX2 Output. Drive SEL high (SEL = 1) to connect AUX0 to AUX2.
33	AUX1	AUX1 Output. Drive SEL low (SEL = 0) to connect AUX0 to AUX1.
34	AUX0	AUX0 Input
35	V+	Positive-Supply Voltage Input. Bypass V+ to GND with a 0.1µF ceramic capacitor.
36	COM0+	Common LVDS Differential Terminal for Switch 0
—	EP	Exposed Pad. Connect exposed pad to GND or leave it unconnected.

Detailed Description

The MAX14979E is a high-speed analog switch targeted at LVDS and other low-voltage switching up to 600MHz. In a typical application, the MAX14979E switches two sets of LVDS sources to a laptop LVDS panel. For extra security, the MAX14979E is protected against ±15kV ESD shocks. See the *Functional Diagram.*

With its low resistance and capacitance, as well as high-ESD protection, the MAX14979E can be used to switch most low-voltage differential signals, such as LVDS and LVPECL, as long as the signals do not exceed the maximum ratings of the device.

The MAX14979E switches provide low capacitance and on-resistance to meet low insertion loss and return-loss specifications. The MAX14979E has three additional AUX switches.

Digital Control Inputs

The MAX14979E provides a single digital control SEL. SEL controls the switches as well as the AUX switches, as shown in Table 1.

Analog-Signal Levels

The on-resistance of the MAX14979E is very low and stable as the analog input signals are swept from ground to V+ (see the *Typical Operating Characteristics*). The switches are bidirectional, allowing COM_ _ and NC_ _/NO_ _ to be configured as either inputs or outputs.

ESD Protection

The MAX14979E is characterized using the HBM for ±15kV of ESD protection. Figure 5 shows the HBM. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor. All signal and control pins are ESD protected to ±15kV HBM.

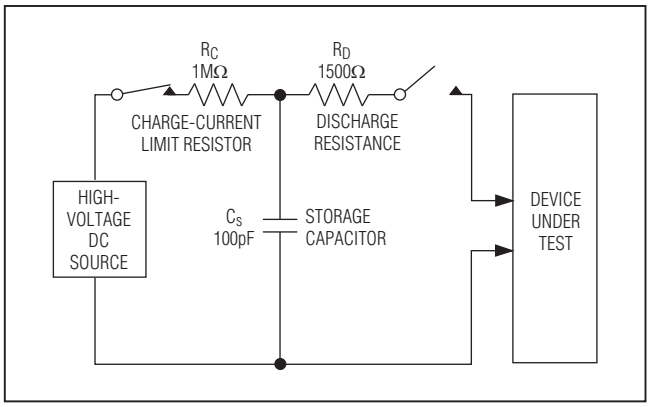


Figure 5. Human Body ESD Test Model (MIL-STD-883, Method 3015)

High-Bandwidth, ±15kV ESD Protection LVDS Switch

Functional Diagram

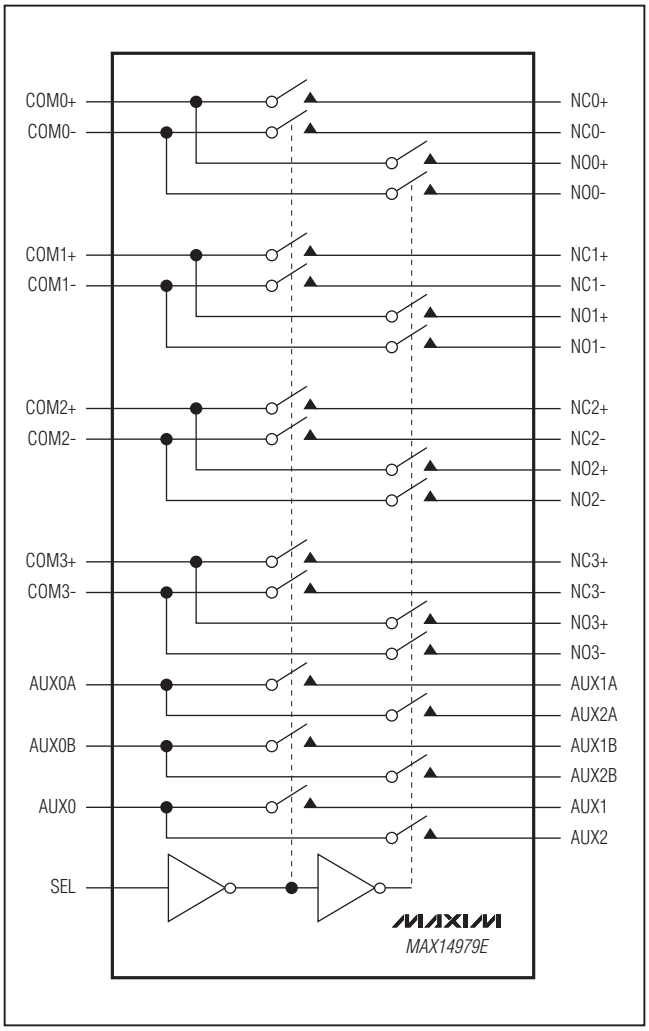


Table 1. Truth Table

SEL	CONNECTION
0	COM_ _ to NC_ _, AUX0_ to AUX1_
1	COM_ _ to NO_ _, AUX0_ to AUX2_

Applications Information

Typical Operating Circuit

The *Typical Operating Circuit* shows the MAX14979E in a dual graphics application.

Power-Supply Sequencing and Overvoltage Protection

Caution: Do not exceed the absolute maximum ratings. Stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals, especially if the analog signal is not current limited.

Layout

High-speed switches require proper layout and design procedures for optimum performance. Keep design-controlled-impedance PCB traces as short as possible. Ensure that bypass capacitors are as close as possible to the device. Use large ground planes where possible.

Chip Information

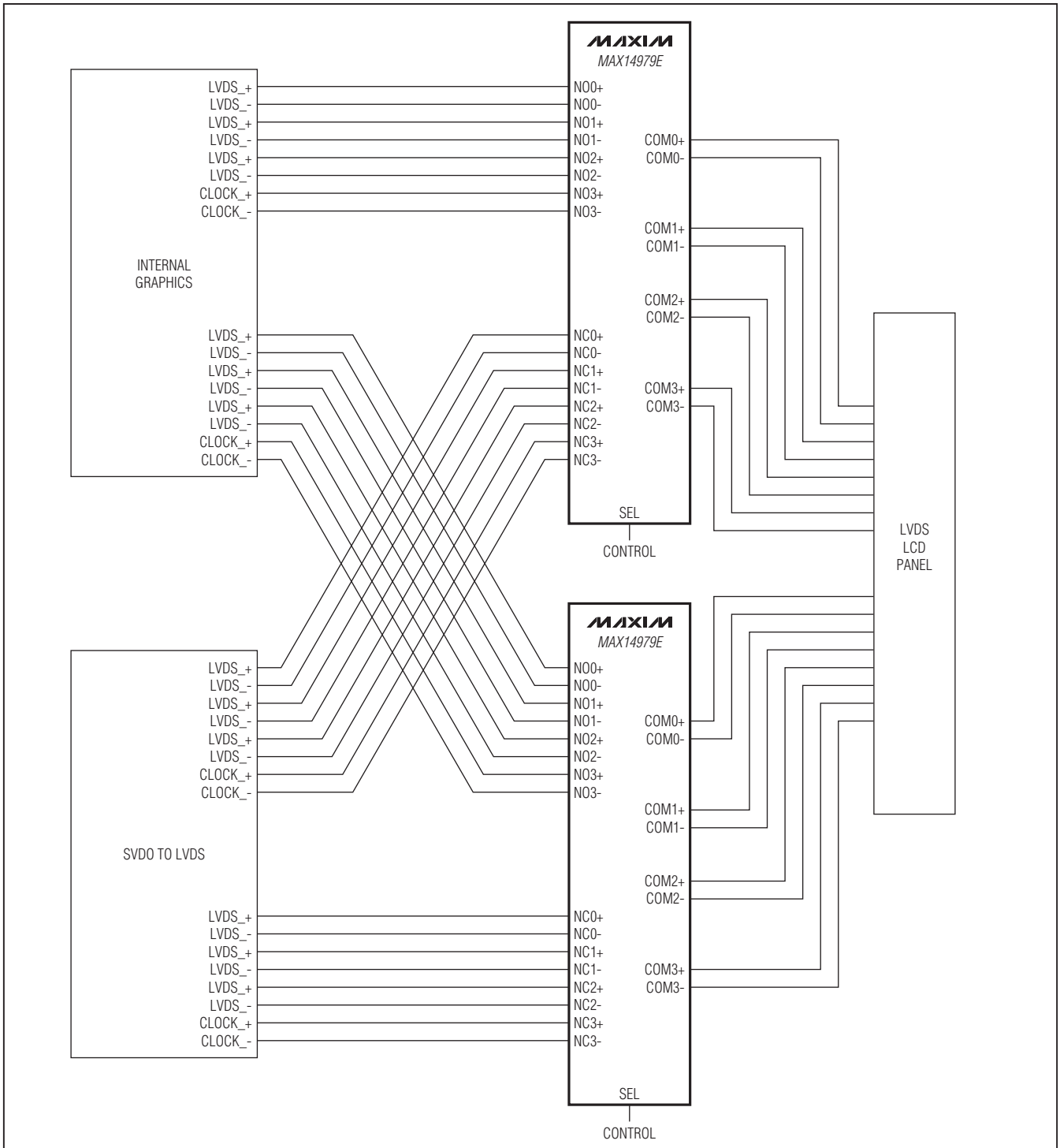
PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
36 TQFN-EP	T3666+3	21-0141

Typical Operating Circuit



NOTE: THE MAX14979E HAS THREE SPDT AUXILLIARY SWITCHES (AUX) THAT CAN BE USED FOR OTHER SWITCHING SUCH AS LEDs AND I^2C. THESE ARE NOT SHOWN IN THE DIAGRAM.

High-Bandwidth, ±15kV ESD Protection LVDS Switch

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/10	Initial release	—