





Phase Control Thyristor

Preliminary Information

DS5810-1.4 September 2009 (LN26859)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Conditions	
DCR3030V42 DCR3030V40 DCR3030V35 DCR3030V30	4200 4000 3500 3000	$\begin{split} T_{vj} &= \text{-}40^{\circ}\text{C to 125}^{\circ}\text{C}, \\ I_{DRM} &= I_{RRM} = 200\text{mA}, \\ V_{DRM}, V_{RRM} t_p &= 10\text{ms}, \\ V_{DSM} \& V_{RSM} &= \\ V_{DRM} \& V_{RRM} + 100V \\ respectively \end{split}$

Lower voltage grades available.

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR3030V42

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

4200V
3030A
40600A
1500V/µs
400A/μs

* Higher dV/dt selections available

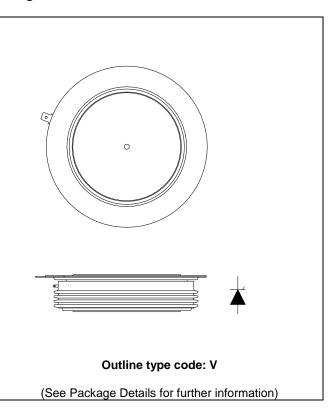


Fig. 1 Package outline





CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Si	de Cooled			
I _{T(AV)}	Mean on-state current	Half wave resistive load	3030	А
I _{T(RMS)}	RMS value	-	4760	А
I _T	Continuous (direct) on-state current	-	4550	А

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I _{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T _{case} = 125°C	40.6	kA
l ² t	I ² t for fusing	$V_R = 0$	8.24	MA ² s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Condition	Test Conditions		Max.	Units
R _{th(j-c)}	Thermal resistance – junction to case	Double side cooled	DC	-	0.00746	°C/W
		Single side cooled	Anode DC	-	0.0130	°C/W
			Cathode DC	-	0.0178	°C/W
R _{th(c-h)}	Thermal resistance – case to heatsink	Clamping force 54kN Double side		-	0.002	°C/W
		(with mounting compound)	Single side	-	0.004	°C/W
T _{vj}	Virtual junction temperature	(blocking)		-	125	°C
T _{stg}	Storage temperature range			-55	125	°C
Fm	Clamping force			48.0	59.0	kN





DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditio	Test Conditions		Max.	Units
I _{RRM} /I _{DRM}	Peak reverse and off-state current	At V _{RRM} /V _{DRM} , T _{case} = 125°C		-	200	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM} , $T_j = 125$ °C, ga	ate open	-	1500	V/µs
dl/dt	Rate of rise of on-state current	From 67% V _{DRM} to 2x I _{T(AV)}	Repetitive 50Hz	-	200	A/µs
		Gate source 30V, 10Ω , $t_r < 0.5\mu s$, $T_i = 125^{\circ}C$	Non-repetitive	-	400	A/µs
V _{T(TO)}	Threshold voltage – Low level	200A to 1700A at T _{case} = 125	I 5°C	-	0.82	V
	Threshold voltage – High level	1700A to 7000A at T _{case} = 125°C		-	0.98	V
r _T	On-state slope resistance – Low level	200A to 1700A at T _{case} = 125°C		-	0.292	mΩ
	On-state slope resistance – High level	1700A to 7000A at T _{case} = 125°C		-	0.198	mΩ
t _{gd}	Delay time	V_D = 67% V_{DRM} , gate source 30V, 10Ω t_r = 0.5μs, T_j = 25°C		TBD	TBD	μs
t _q	Turn-off time	T_j = 125°C, V_R = 200V, dI/dt = 1A/ μ s, dV_{DR}/dt = 20V/ μ s linear		250	500	μs
Qs	Stored charge	T_j = 125°C, dl/dt – 1A/ μ s, $V_{R pk}$ =3000V, V_{RM} = 1700V		1600	3500	μC
ΙL	Latching current	$T_j = 25^{\circ}C, V_D = 5V$		-	3	А
I _H	Holding current	$T_j = 25^{\circ}\text{C}, R_{G-K} = \infty, I_{TM} = 50^{\circ}$	0A, I _T = 5A	-	300	mA





GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol Parameter		Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V _{DRM} = 5V, T _{case} = 25°C	1.5	V
V_{GD}	Gate non-trigger voltage	At V _{DRM} , T _{case} = 125°C	TBD	V
I _{GT}	Gate trigger current	V _{DRM} = 5V, T _{case} = 25°C	250	mA
I _{GD}	Gate non-trigger current	V _{DRM} = 5V, T _{case} = 25°C	TBD	mA

CURVES

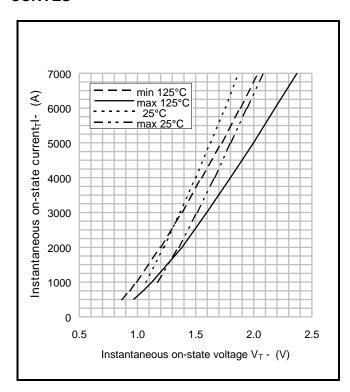


Fig.2 Maximum & minimum on-state characteristics

 V_{TM} EQUATION Where A = 0.866995 B = -0.042053

 $V_{TM} = A + Bln (I_T) + C.I_T + D.\sqrt{I_T}$ C = 0.000100

D = 0.014062

these values are valid for T_j = 125°C for I_T 500A to 10000A



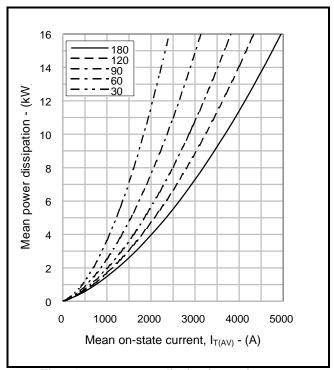


Fig.3 On-state power dissipation – sine wave

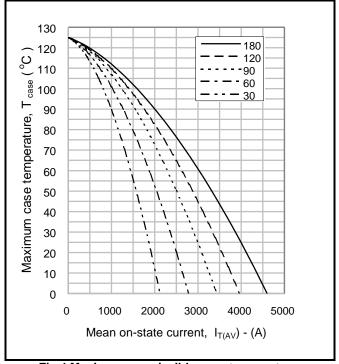


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

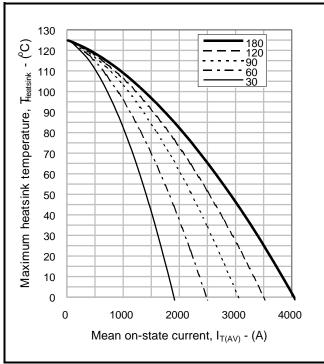


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

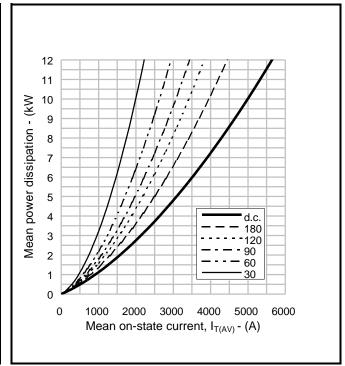
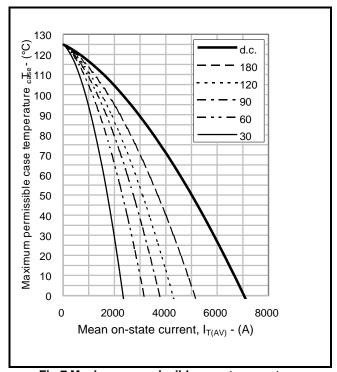
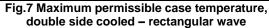


Fig.6 On-state power dissipation - rectangular wave







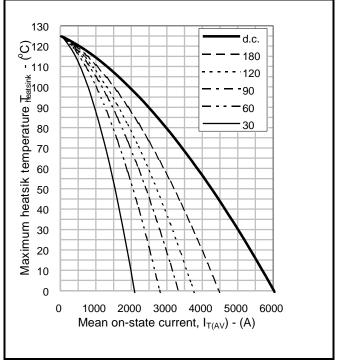
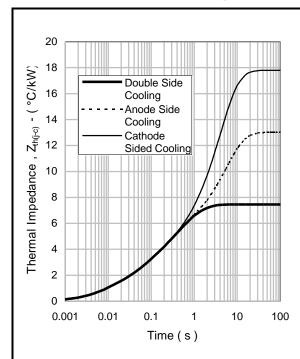


Fig.8 Maximum permissible heatsink temperature, double side cooled - rectangular wave



		1	2	3	4
Double side cooled	R _i (°C/kW)	0.9206	1.8299	3.4022	1.3044
	T _i (s)	0.0076807	0.0579454	0.4078613	1.2085
Anode side cooled	R _i (°C/kW)	0.9032	1.6719	3.0101	7.4269
	T _i (s)	0.0075871	0.0536531	0.3144537	5.624
Cathode side cooled	R _i (°C/kW)	0.9478	2.0661	1.6884	13.0847
	T. (s)	0.0078442	0.0645541	0.3004300	4 1447

 $Z_{th} = \sum [R_i x (1-exp. (t/t_i))]$ [1]

 $\Delta R_{\text{th(j-c)}}$ Conduction

Tables show the increments of thermal resistance $R_{\text{th}(j\text{-}c)}$ when the device operates at conduction angles other than d.c.

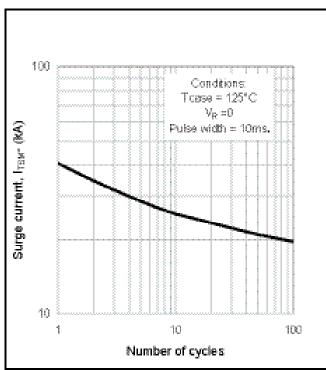
Double side cooling					
	ΔZ_{th} (z)			
θ°	sine.	rect.			
180	1.34	0.88			
120	1.57	1.30			
90	1.83	1.54			
60	2.08	1.81			
30	2.27	2.11			

Double side cooling				Cooling	
$\Delta Z_{th}(z)$				ΔZ_t	_h (z)
sine.	rect.		θ°	sine.	rect.
1.34	0.88		180	1.34	0.88
1.57	1.30		120	1.57	1.30
1.83	1.54		90	1.84	1.54
2.08	1.81		60	2.08	1.81
2.27	2.11		30	2.28	2.11
2.36	2.28		15	2.37	2.28
	ΔZ _{th} (sine. 1.34 1.57 1.83 2.08 2.27	ΔZ _{th} (z) sine. rect. 1.34 0.88 1.57 1.30 1.83 1.54 2.08 1.81 2.27 2.11	ΔZ _{th} (z) sine. rect. 1.34 0.88 1.57 1.30 1.83 1.54 2.08 1.81 2.27 2.11	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$

Ca	$\Delta Z_{th}(z)$				
θ°	sine.	rect.			
180	1.33	0.88			
120	1.57	1.29			
90	1.83	1.53			
60	2.07	1.80			
30	2.26	2.10			
4.5		0.00			

Fig.9 Maximum (limit) transient thermal impedance - junction to case (°C/kW)





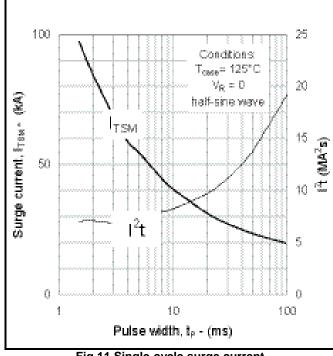
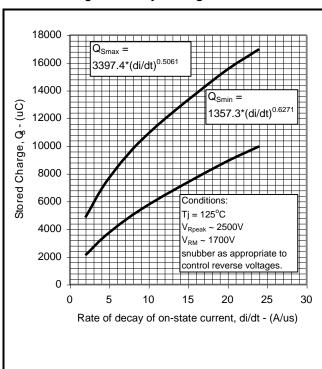


Fig.10 Multi-cycle surge current

Fig.11 Single-cycle surge current



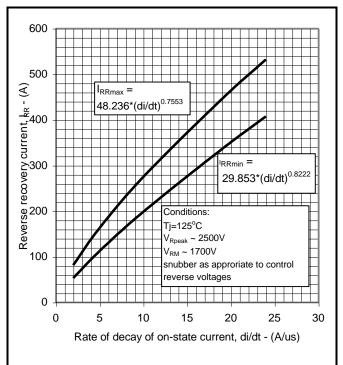


Fig. 12 Stored Charge

Fig. 13 Reverse Recovery Current

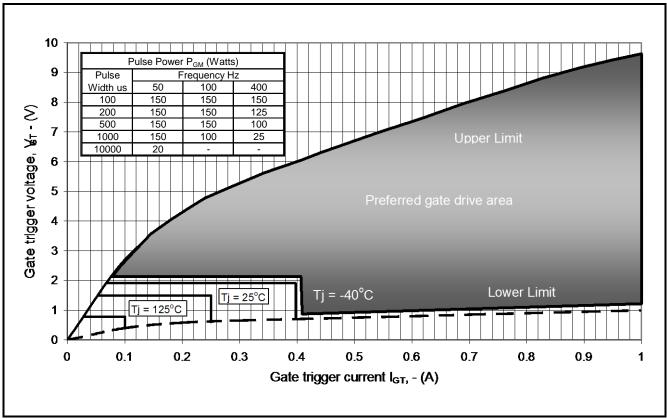


Fig14 Gate Characteristics

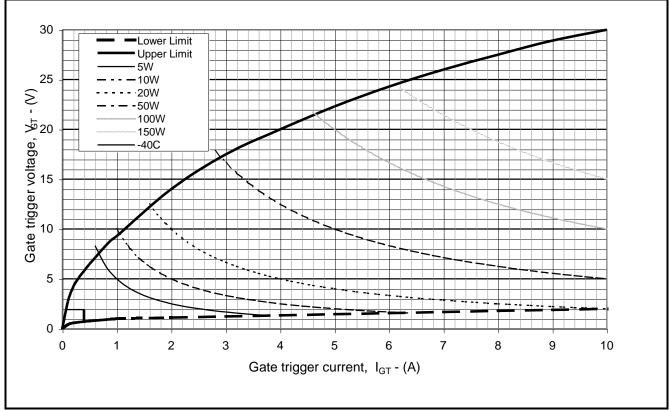


Fig. 15 Gate characteristics





PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

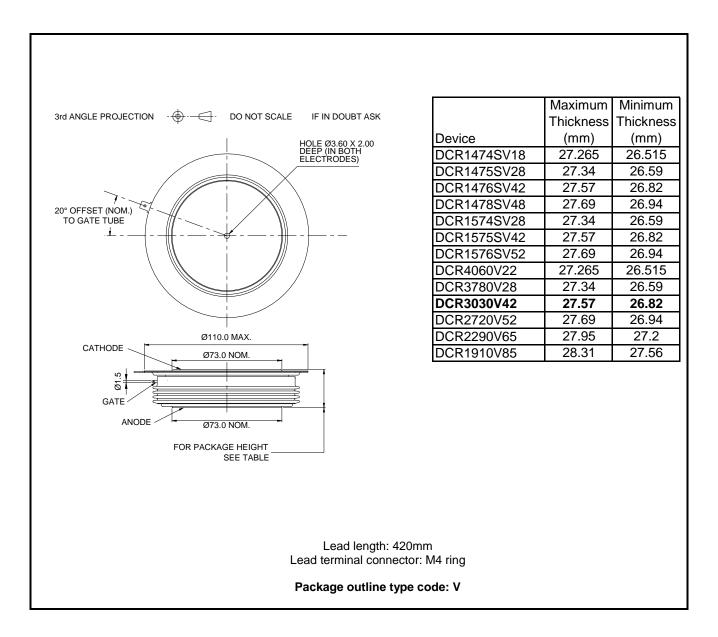


Fig.16Package outline





POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.



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