



FXL3SD206

Level Shifting Voltage Translator

Two-Port SDIO MUX/DEMUX with Three Configurable Power Supplies for SDIO Device Port Expansion

Features

- Bi-Directional Interface between Two Levels: 1.65 to 3.6V
- Fully Configurable: Inputs and Outputs Track V_{DD}
- Flexible and Programmable V_{DD} of B and C Ports
- Non-Preferential Power-up; either V_{DD} Can Power Up First
- Output Remains in 3-State until Active V_{DD} Level is Reached
- Output Switches to 3-state if either V_{DD} is at GND
- Power-off Protection
- Bus-Hold on Data Input Eliminates the Need for SDIO Pull-up Resistors
- 2:1 MUX/DEMUX of SDIO Devices in 24-Terminal Micro-MLP Package (2.5mm x 3.4mm)
- Direction Control is Automatic
- Power Switching Time (V_{DD_HI} to V_{DD_LO} or Reverse) is Less than 1.7 μ s
- 60Mbps Throughput
- ESD Protection Exceeds:
 - 12KV HBM (A, B, and C port I/O to GND) (per JESD22-A114)
 - 1KV CDM (per ESD STM5.3)

Applications

- SDIO Devices
- Cell Phone, PDA, Digital Camera, Portable GPS

Description

FXL3SD206 is a voltage translator with multiplexing and de-multiplexing functions for SDIO devices. It is designed for voltage translation over a wide range of input and output levels, from 1.65V to 3.6V.


The multiplexing/de-multiplexing function of this device allows expansion of a host SDIO interface to two SDIO peripheral devices. When selected, each SDIO peripheral can communicate with the host through the same host interface. An alternative application allows two host devices to interface with a single SDIO peripheral.

Port A is intended to connect to a host device and the voltage level tracks the V_{DDA} . Ports B and C are intended to connect to peripheral devices. Peripheral I/O voltage levels track either V_{DD_HI} or V_{DD_LO} as determined by the VDD_SEL pin. During normal operation, V_{DD_HI} must be greater than or equal to V_{DD_LO} . The CH_SEL , VDD_SEL , and OE pins are referenced to V_{DD_CON} . Channel communication from either Port A to Port B or Port A to Port C is controlled by the CH_SEL pin.

The selected channel remains in 3-state until the V_{DD} of each side reaches an active level and the OE pin reaches a valid high. Internal power-down circuitry places the selected channel of the device in 3-state if either side V_{DD} removed.

The direction of data is controlled automatically by the device. No direction control pin is required. The device senses input signals on any port automatically and transfers the data to the corresponding output.

Ordering Information

Part Number	Operating Temperature Range	 Eco Status	Package	Packing Method
FXL3SD206UMX	-40 to +85°C	Green	24-Pin, Micro-MLP, Quad, .6mm Thick, 2.5mm x 3.4mm Body	Tape & Reel

 For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Application Diagrams

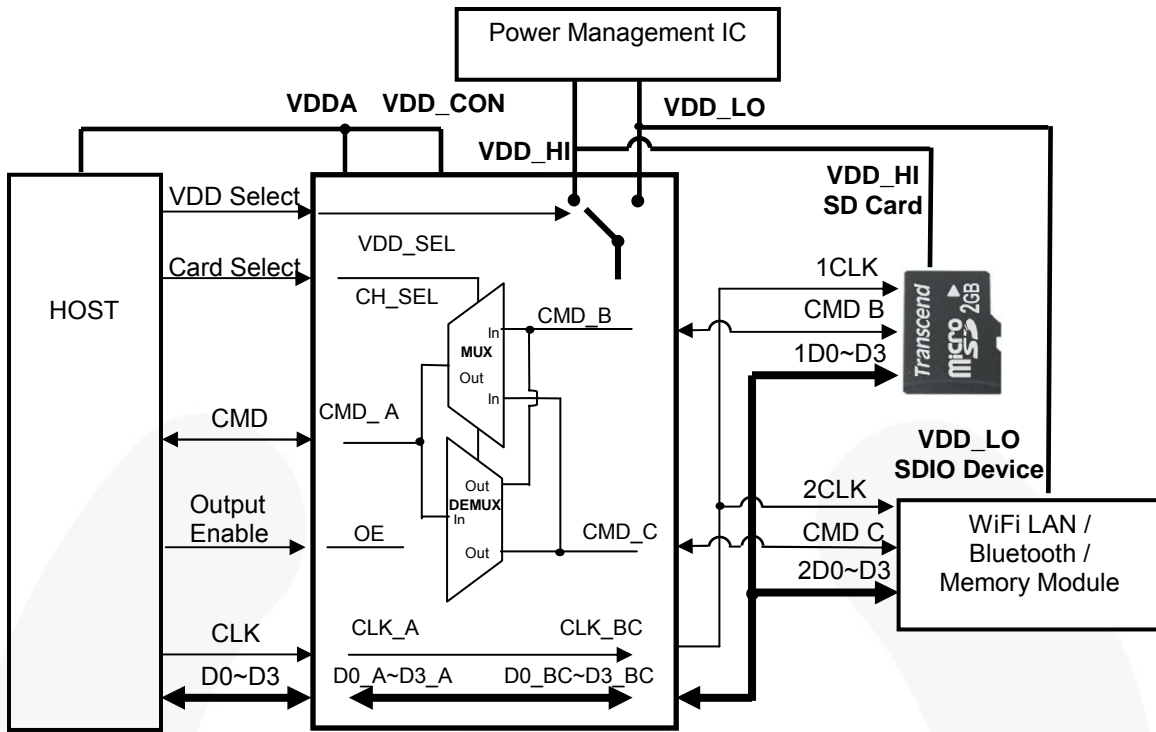


Figure 1. Single Host to Two SDIO Application Diagram

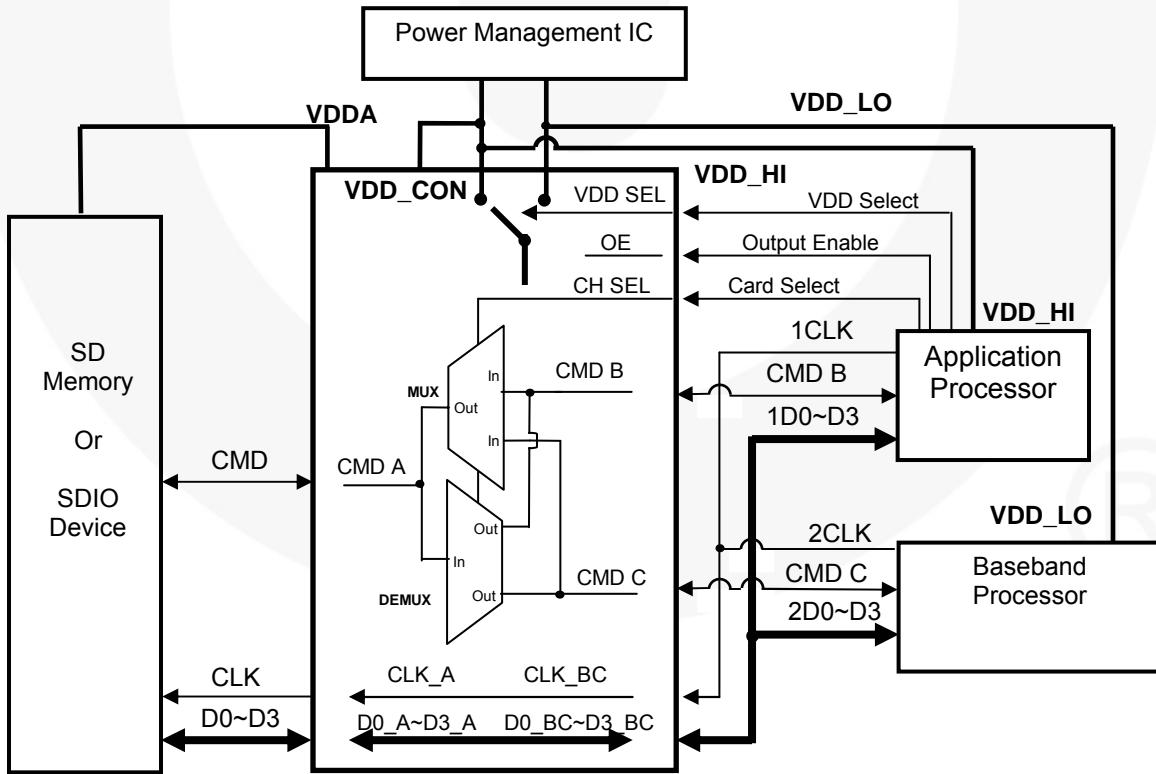


Figure 2. Dual Host to Single SDIO Application

Pin Configuration

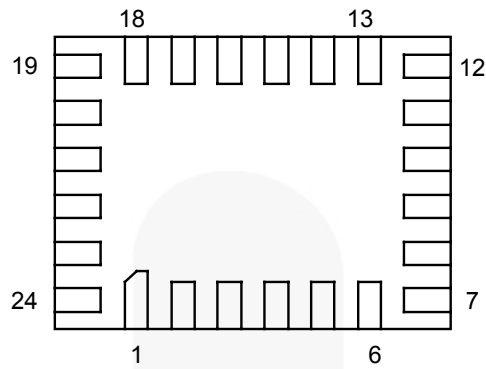


Figure 3. Pin Configuration (Top Through View)

Pin Definitions

Pin #	Name	Type	Description
1	D0_A	Data	Data Pin of A Port
2	D1_A	Data	Data Pin of A Port
3	D2_A	Data	Data Pin of A Port
4	D3_A	Data	Data Pin of A Port
5	CLK_A	Data	Clock Pin of A Port
6	----	NC	No Connect
7	CMD_A	Data	Command Pin of A Port
8	----	NC	No Connect
9	GND	Power	Ground
10	CMD_C	Data	Command Pin of C Port
11	----	NC	No Connect
12	CMD_B	Data	Command Pin of B Port
13	CLK_BC	Data	Clock Pin of B or C Port
14	D3_BC	Data	Data Pin of B or C Port
15	D2_BC	Data	Data Pin of B or C Port
16	D1_BC	Data	Data Pin of B or C Port
17	D0_BC	Data	Data Pin of B or C Port
18	VDD_LO	Power	B or C Port, Low Power Supply
19	VDD_HI	Power	B or C Port, High Power Supply
20	VDD_CON	Power	Control Pin Power Supply
21	VDDA	Power	A-Port Power Supply
22	VDD_SEL	Control	Power Supply Select Pin of B and C Ports
23	CH_SEL	Control	Channel Select Pin
24	OE	Control	Output Enable Pin

Function Diagram

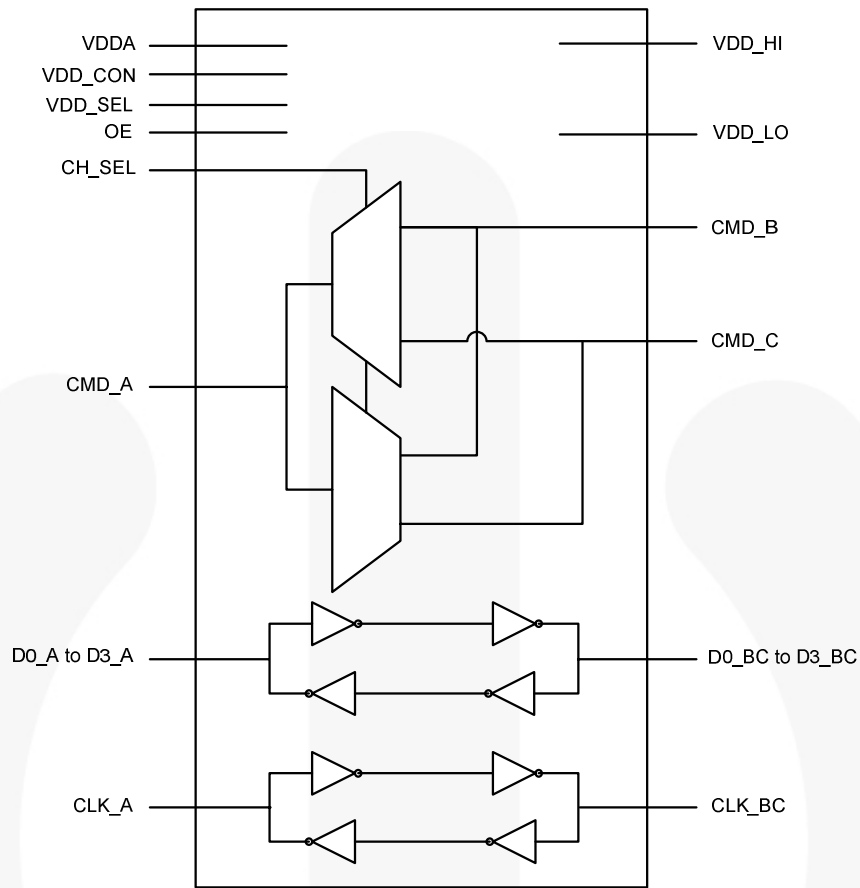


Figure 4. Function Diagram

Function Table

OE	CH_SEL	VDD_SEL	Output
LOW	Don't Care	Don't Care	3-State
HIGH	HIGH	HIGH	Normal operation; Port A to Port B channel selected; Port B tracks VDD_HI level
HIGH	HIGH	LOW	Normal operation; Port A to Port B channel selected; Port B tracks VDD_LO level
HIGH	LOW	HIGH	Normal operation; Port A to Port C channel selected; Port C tracks VDD_HI level
HIGH	LOW	LOW	Normal operation; Port A to Port C channel selected; Port C tracks VDD_LO level

Note:

- VDD_CON: This is a power supply pin that is used by the three control pins (VDD_SEL, CH_SEL, and OE). In single host mode, VDD_CON should be tied to the same supply as the VDDA pin. In dual host mode, VDD_CON should be tied to the same supply as either the VDD_HI or the VDD_LO pin, depending upon which host is used to drive the control pins.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{DD}	Supply Voltage	VDDA, VDD_HI, VDD_LO, VDD_CON	-0.5	4.6	V
V _I	DC Input Voltage	Data Ports A, B, and C	-0.5	4.6	V
		Control Inputs (OE, CH_SEL, VDD_SEL)	-0.5	4.6	V
V _O	Output Voltage ⁽²⁾	Output 3-State	-0.5	4.6	V
		Output Active (Port A)	-0.5	V _{DDA} +0.5	
		Output Active (Port B or C)	-0.5	V _{DD_HI} +0.5	
		Output Active (Port B or C)	-0.5	V _{DD_LO} +0.5	
I _{IK}	DC Input Diode Current	V _I <0V		-50	mA
I _{OK}	DC Output Diode Current	V _O <0V		-50	mA
		V _O >V _{CC}		+50	
I _{OH} /I _{OL}	DC Output Source/Sink Current		-50	+50	mA
I _{DD}	DC V _{DD} or Ground Current per Supply Pin			±100	mA
T _{STG}	Storage Temperature Range		-65	+150	°C

Note:

2. I_O absolute maximum rating must be observed.

Recommended Operating Conditions⁽³⁾

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{DD}	Power Supply Operating	VDDA, VDD_HI, VDD_LO, VDD_CON	1.65	3.60	V
		V _{DD_HI} ≥ V _{DD_LO} ⁽⁴⁾			
V _{IN}	Input Voltage	Port A	0	V _{DDA}	V
		Port B and C ⁽⁵⁾	0	V _{DD_HI}	
		Port B and C ⁽⁵⁾	0	V _{DD_LO}	
T _A	Free Air Operation Temperature		-40	+85	°C
dt/dV	Minimum Input Edge Rate	Data Port A at V _{DDA} =1.65 to 3.6V		10	ns/V
		Data Ports B and C at V _{DD_n} =1.65 to 3.6V		10	
		OE, CH_SEL, VDD_SEL at V _{DD_CON} =1.65V to 3.6V		10	

Notes:

3. All unused inputs and input/outputs must be held at V_{DDn} or GND.
4. During normal operation, V_{DD_HI} must be greater than or equal to V_{DD_LO}.
5. The input and output voltages of Ports B and C are determined by which V_{DD} is selected.

Application Information

Power-Up / Power-Down Sequencing

FXL translators offer an advantage in that any V_{DD} may be powered up first. This benefit derives from the chip design. When V_{DDA} or both V_{DD_HI} and V_{DD_LO} pins are at 0 volts, outputs are in a high-impedance state (see *Power Up Operation table below*). As a multiplexer, the device allows the unselected port to remain in a high-impedance state for power saving. The control inputs (OE, CH_SEL, VDD_SEL) are designed to track V_{DD_CON} . An external pull-down resistor tying OE to GND should be used to ensure that bus contention, excessive current, or oscillations do not occur during power-up/power-down. The size of the pull-down resistor is based upon the current-sinking capability of the device driving the OE pin.

During normal operation, V_{DD_HI} must be greater than or equal to V_{DD_LO} . During power-up or power-down, V_{DD_LO} may exceed V_{DD_HI} without damaging the device.

The recommended power-up sequence is:

1. Apply the power to the first V_{DD} .
2. Apply the power to the second V_{DD} .
3. Set the CH_SEL and VDD_SEL pin according to the application.
4. Drive the OE input high to enable the device.

The recommended the power-down sequence is:

1. Drive the OE input low to disable the device.
2. Remove the setting of CH_SEL and VDD_SEL pin.
3. Remove power from either V_{DD} .
4. Remove power from other V_{DD} .

Table 1. Power-Up Operation

VDDA	VDD_HI	VDD_LO	VDD_SEL	Port B or C Outputs
OFF	Don't Care	Don't Care	Don't Care	High Impedance
ON	OFF	OFF	Don't Care	High Impedance
ON	ON	OFF	HIGH	Enabled, Reference to V_{DD_HI}
			LOW	High Impedance
ON	OFF	ON	HIGH	High Impedance
			LOW	Enabled, Reference to V_{DD_LO}
ON	ON	ON	HIGH	Enabled, Reference to V_{DD_HI}
			LOW	Enabled, Reference to V_{DD_LO}

DC Electrical Characteristics

T_A=-40°C to 85°C unless otherwise specified.

Symbol	Parameter	Condition	V _{DD_A} , V _{DD_n} (V)	Min.	Max.	Units
V _{IHA}	High Level Input Voltage ⁽⁶⁾	Data Inputs Dn_A, CMD_A, CLK_A,	1.65 – 3.6	0.6 x V _{DD_A}		V
V _{IHB}		Data Inputs Dn_BC, CMD_B, CLK_BC, CH_SEL=H	1.65 – 3.6	0.6 x V _{DD_n}		V
V _{IHC}		Data Inputs Dn_BC, CMD_C, CLK_BC, CH_SEL=L	1.65 – 3.6	0.6 x V _{DD_n}		V
V _{IH}		OE, VDD_SEL, CH_SEL	1.65 – 3.6	0.6 x V _{DD_CON}		V
V _{ILA}	Low Level Input Voltage ⁽⁶⁾	Data Inputs Dn_A, CMD_A, CLK_A,	1.65 – 3.6		0.35 x V _{DD_A}	V
V _{ILB}		Data Inputs Dn_BC, CMD_B, CLK_BC, CH_SEL=H	1.65 -3.6		0.35 x V _{DD_n}	V
V _{ILC}		Data Inputs Dn_BC, CMD_C, CLK_BC, CH_SEL=L	1.65 -3.6		0.35 x V _{DD_n}	V
V _{IL}		OE, VDD_SEL, CH_SEL	1.65 – 3.6		0.35 x V _{DD_CON}	V
V _{OHA}	High Level Output Voltage ^(6, 7)	Data Outputs Dn_A, CMD_A, CLK_A, I _{HOLD} =-20μA	1.65 – 3.6	0.75 x V _{DD_A}		V
V _{OHB}		Data Outputs Dn_BC, CMD_B, CLK_BC, CH_SEL=H, I _{HOLD} =-20μA	1.65 – 3.6	0.75 x V _{DD_n}		V
V _{OHC}		Data Outputs Dn_BC, CMD_B, CLK_BC, CH_SEL=L, I _{HOLD} =-20μA	1.65 – 3.6	0.75 x V _{DD_n}		V
V _{OLA}	Low Level Output Voltage ^(6, 7)	Data Outputs Dn_A, CMD_A, CLK_A, I _{HOLD} =+20μA	1.65 – 3.6	0.25 x V _{DD_A}		V
V _{OLB}		Data Outputs Dn_BC, CMD_B, CLK_BC, CH_SEL=H, I _{HOLD} =+20μA	1.65 – 3.6	0.25 x V _{DD_n}		V
V _{OLC}		Data Outputs Dn_BC, CMD_B, CLK_BC, CH_SEL=L, I _{HOLD} =+20μA	1.65 – 3.6	0.25 x V _{DD_n}		V

Notes:

6. Port B and Port C share the same data and clock pin, and VDD_n refers to VDD_HI or VDD_LO, whichever is selected. During normal operation, VDD_HI must be greater than or equal to VDD_LO.
7. This is the output voltage for static conditions. Dynamic drive specifications are given in “Dynamic Output Electrical Characteristics.”

DC Electrical Characteristics (Continued)

T_A=-40°C to 85°C unless otherwise specified.

Symbol	Parameter	Condition	V _{DD_A} (V)	V _{DD_n} (V)	Min.	Max.	Units
I _{IODH}	Bushold Input Overdrive High Current ⁽⁸⁾	Data Inputs Dn_A, CMD_A, CLK_A Dn_BC, CMD_B, CMD_C, CLK_BC	3.6	3.6	450		μA
			2.7	2.7	300		μA
			1.95	1.95	200		μA
I _{IODL}	Bushold Input Overdrive Low Current ⁽⁹⁾	Data Inputs Dn_A, CMD_A, CLK_A Dn_BC, CMD_B, CMD_C, CLK_BC	3.6	3.6	-450		μA
			2.7	2.7	-300		μA
			1.95	1.95	-200		μA
I _I	Input Leakage Current	Control Inputs OE, CH_SEL, VDD_SEL, V _I =V _{DD_CON} or GND	1.65 -3.6	3.6		±1.0	μA
I _{OFF}	Power Off Leakage Current	Dn_A, CMD_A, CLK_A; V _O =0 to 3.6V	0	3.6		±2.0	μA
		Dn_BC, CMD_B, CMD_C, CLK_BC; V _O =0 to 3.6V	3.6	0		±2.0	μA
I _{OZ}	3-state Output Leakage	Dn_A, CMD_A, CMD_B, CMD_C, Dn_BC, CLK_A, CLK_BC; V _O =0V or 3.6V; OE=V _{IL}	3.6	3.6		±2.0	μA
		Dn_A, CMD_A, CLK_BC; V _O =0V or 3.6V; OE=Don't Care ⁽¹⁰⁾	3.6	0		±2.0	μA
		Dn_BC, CMD_B, CMD_C, CLK_BC; V _O =0V or 3.6V; OE=Don't Care ⁽¹⁰⁾	0	3.6		±2.0	μA
I _{CC}	Quiescent Supply Current ^(11, 12)	V _I =V _{DDI} or GND; I _O =0	1.65 – 3.6	1.65 – 3.6		5.0	μA
			0	1.65 – 3.6		2.0	μA
			1.65 - 3.6	0		2.0	μA
I _{CCZ}	Quiescent Supply Current ⁽¹¹⁾	V _I =V _{DDI} or GND; I _O =0, OE=V _{IL}	1.65 – 3.6	1.65 – 3.6		5.0	μA

Notes:

8. An external driver must source at least the specified current to switch LOW-to-HIGH.
9. An external driver must source at least the specified current to switch HIGH-to-LOW.
10. "Don't care" indicates any valid logic level.
11. V_{DDI} is the V_{DD} associated with the input side.
12. Reflects current per supply, V_{DD_A} or V_{DD_n}.

Dynamic Output Electrical Characteristics

A Port (Dn_A, CMD_A, CLK_A), B and C Port (CMD_B, CMD_C)

Output Load: $C_L=15\text{pF}$, $R_L \geq 1\text{M}\Omega$ ($C_{I/O}=10\text{pF}$). $T_A=-40^\circ\text{C}$ to 85°C .

Symbol	Parameter	$V_{DD}=2.8\text{V to }3.6\text{V}$		$V_{DD}=2.3\text{V to }2.7\text{V}$		$V_{DD}=1.65\text{V to }1.95\text{V}$		Units
		Typ.	Max.	Typ.	Max.	Typ.	Max.	
t_{rise}	Output Rise Time A Port ⁽¹³⁾		3.0		3.5		4.0	ns
t_{fall}	Output Fall Time A Port ⁽¹⁴⁾		3.0		3.5		4.0	ns
I_{OHD}	Dynamic Output Current High ⁽¹³⁾	-14.0		-10.0		-6.2		mA
I_{OLD}	Dynamic Output Current Low ⁽¹⁴⁾	+14.0		+10.0		+6.2		mA

B and C Port (Dn_BC, CLK_BC)

Output Load: $C_L=30\text{pF}$, $R_L \geq 1\text{M}\Omega$ ($C_{I/O}=10\text{pF}$). $T_A=-40^\circ\text{C}$ to 85°C .

Symbol	Parameter	$V_{DD}=2.8\text{V to }3.6\text{V}$		$V_{DD}=2.3\text{V to }2.7\text{V}$		$V_{DD}=1.65\text{V to }1.95\text{V}$		Units
		Typ.	Max.	Typ.	Max.	Typ.	Max.	
t_{rise}	Output Rise Time B and C Port ⁽¹³⁾		3.0		3.5		4.0	ns
t_{fall}	Output Fall Time B and C Port ⁽¹⁴⁾		3.0		3.5		4.0	ns
I_{OHD}	Dynamic Output Current High ⁽¹³⁾	-22.4		-15.8		-10.0		mA
I_{OLD}	Dynamic Output Current Low ⁽¹⁴⁾	+22.4		+15.8		+10.0		mA

Notes:

- 13. See Figure 9.
- 14. See Figure 10.

AC Characteristics

$V_{DD_A}=2.8V$ to $3.6V$ and $T_A=-40^{\circ}C$ to $85^{\circ}C$.

Symbol	Parameter	$V_{DD_n}=2.8V$ to $3.6V$		$V_{DD_n}=2.3V$ to $2.7V$		$V_{DD_n}=1.65V$ to $1.95V$		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} , t_{PHL}	A to B/C	0.2	3.5	0.3	3.9	0.5	5.4	ns
	B/C to A	0.2	3.5	0.2	3.8	0.3	5.0	ns
t_{PZL} , t_{PZH}	OE to A		1.7		1.7		1.7	μs
	OE to B/C							
t_{PCH}	CH_SEL B to C or \bar{C} to B		1.7		1.7		1.7	μs
t_{skew}	A, B, C Port ⁽¹⁵⁾		0.5		0.5		1.0	ns

$V_{DD_A}=2.3V$ to $2.7V$ and $T_A=-40^{\circ}C$ to $85^{\circ}C$.

Symbol	Parameter	$V_{DD_n}=2.8V$ to $3.6V$		$V_{DD_n}=2.3V$ to $2.7V$		$V_{DD_n}=1.65V$ to $1.95V$		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} , t_{PHL}	A to B/C	0.2	3.8	0.4	4.5	0.5	5.6	ns
	B/C to A	0.3	3.9	0.4	4.5	0.5	5.5	ns
t_{PZL} , t_{PZH}	OE to A		1.7		1.7		1.7	μs
	OE to B/C							
t_{PCH}	CH_SEL B to C or \bar{C} to B		1.7		1.7		1.7	μs
t_{skew}	A, B, C Port ⁽¹⁵⁾		0.5		0.5		1.0	ns

$V_{DD_A}=1.65V$ to $1.95V$ and $T_A=-40^{\circ}C$ to $85^{\circ}C$.

Symbol	Parameter	$V_{DD_n}=2.8V$ to $3.6V$		$V_{DD_n}=2.3V$ to $2.7V$		$V_{DD_n}=1.65V$ to $1.95V$		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} , t_{PHL}	A to B/C	0.3	5.0	0.5	5.5	0.8	6.7	ns
	B/C to A	0.5	5.4	0.5	5.6	0.8	6.7	ns
t_{PZL} , t_{PZH}	OE to A		1.7		1.7		1.7	μs
	OE to B/C							
t_{PCH}	CH_SEL B to C or \bar{C} to B		1.7		1.7		1.7	μs
t_{skew}	A, B, C Port ⁽¹⁵⁾		1.0		1.0		1.0	ns

Note:

15. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port and switching with the same polarity (LOW to HIGH or HIGH to LOW). See Figure 12. Skew is guaranteed, but not tested.

Maximum Data Rate⁽¹⁶⁾

T_A=-40°C to 85°C.

V _{DD_A}	Direction	V _{DD_n} =2.8V to 3.6V	V _{DD_n} =2.3V to 2.7V	V _{DD_n} =1.65V to 1.95V	Units
		Min.	Min.	Min.	
V _{DD_A} =2.8 to 3.6V	A to B/C	100	100	80	Mbps
	B/C to A	100	100	80	
V _{DD_A} =2.3 to 2.7V	A to B/C	100	100	80	Mbps
	B/C to A	100	100	80	
V _{DD_A} =1.65 to 1.95V	A to B/C	80	80	60	Mbps
	B/C to A	80	80	60	

Note:

16. Maximum Data Rate is specified in megabits per second. See Figure 11. It is equivalent to two times the f_{TOGGLE} frequency, specified in megahertz. For example, 100Mbps is equivalent to 50MHZ.

Capacitance

T_A=+25°C.

Symbol	Parameter	Conditions	Typical	Units	
C _{IN}	Input Capacitance Control Pins (OE, VDD_SEL, CH_SEL)	V _{DD_CON} =GND	4.0	pF	
C _{I/O}	Input/Output Capacitance	Dn_A, CMD_A, CLK_A	V _{DD_A} =V _{DD_n} =3.3V, OE=V _{DD_A} ,	5.0	pF
		Dn_BC, CMD_B, CMD_C, CLK_BC	CH_SEL=V _{DD_A} or GND	6.5	
C _{PD}	Power Dissipation Capacitance	V _{DD_A} =V _{DD_n} =3.3V, V _I =0V or V _{DD} , f=10MHZ	25	pF	

Test Diagrams

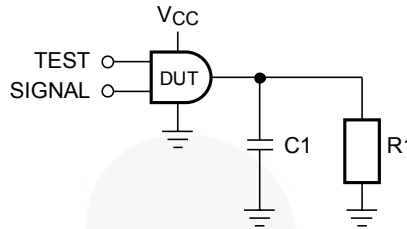


Figure 5. AC Test Circuit

Table 2. AC Test Conditions

Test	Input Signal	Output Enable Control
t_{PLH} , t_{PHL}	Data Pulses	$V_I = V_{DD_CON}$
t_{PZL}	0V	LOW to HIGH Switch
t_{PZH}	V_{CCI}	LOW to HIGH Switch

Table 3. AC Load

V_{CCO}	C_L		R_L
Port A, B, or C	Port A, CMD_B, CMD_C	Dn_BC, CLK_BC	Port A, B, or C
$1.8V \pm 0.15V$	15pF	30pF	1M Ω
$2.5V \pm 0.2V$	15pF	30pF	1M Ω
2.8V to 3.6V	15pF	30pF	1M Ω

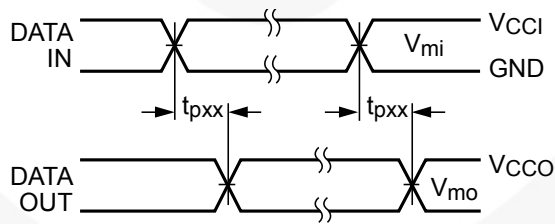


Figure 6. Waveform for Inverting and Non-Inverting Functions

Notes:

- 17. Input $t_R = t_F = 2.0ns$, 10% to 90%.
- 18. Input $t_R = t_F = 2.5ns$, 10% to 90%, at $V_I = 3.0V$ to 3.6V only.

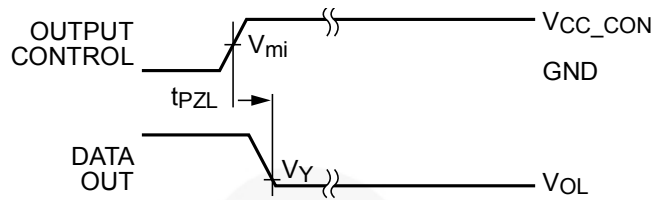


Figure 7. 3-State Output Low Enable Time for Low Voltage Logic

Notes:

- 19. Input $t_R = t_F = 2.0\text{ns}$, 10% to 90%.
- 20. Input $t_R = t_F = 2.5\text{ns}$, 10% to 90%, at $V_I = 3.0\text{V}$ to 3.6V only.

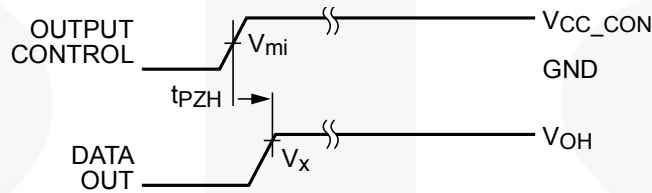
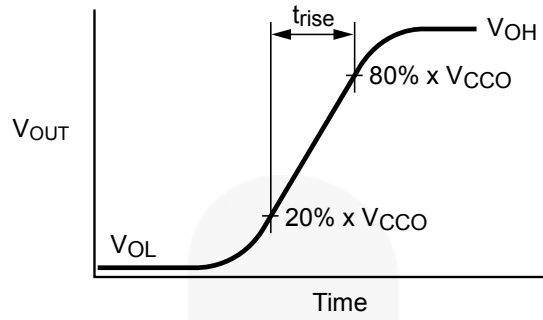


Figure 8. 3-State Output High Enable Time for Low Voltage Logic

Notes:

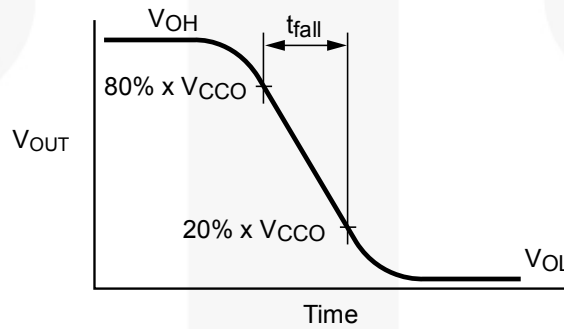
- 21. Input $t_R = t_F = 2.0\text{ns}$, 10% to 90%.
- 22. Input $t_R = t_F = 2.5\text{ns}$, 10% to 90%, at $V_I = 3.0\text{V}$ to 3.6V only.

Symbol	V_{DD}
V_{MI}	$V_{DDI} / 2$
V_{MO}	$V_{DDO} / 2$
V_X	$0.9 \times V_{DDO}$
V_Y	$0.1 \times V_{DDO}$



$$I_{OHD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(20\% - 80\%) \cdot V_{CCO}}{t_{RISE}}$$

Figure 9. Active Output Rise Time and Dynamic Output Current High



$$I_{OHD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(80\% - 20\%) \cdot V_{CCO}}{t_{FALL}}$$

Figure 10. Active Output Fall Time and Dynamic Output Current Low

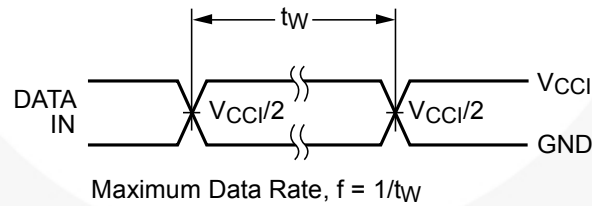
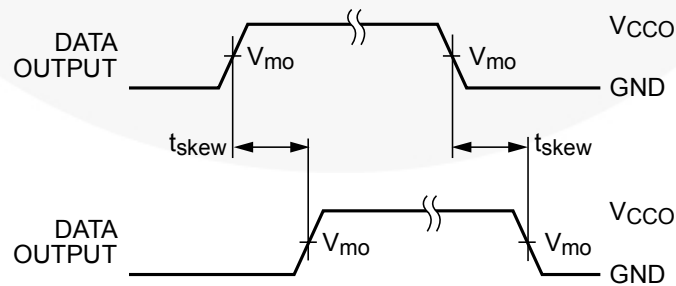


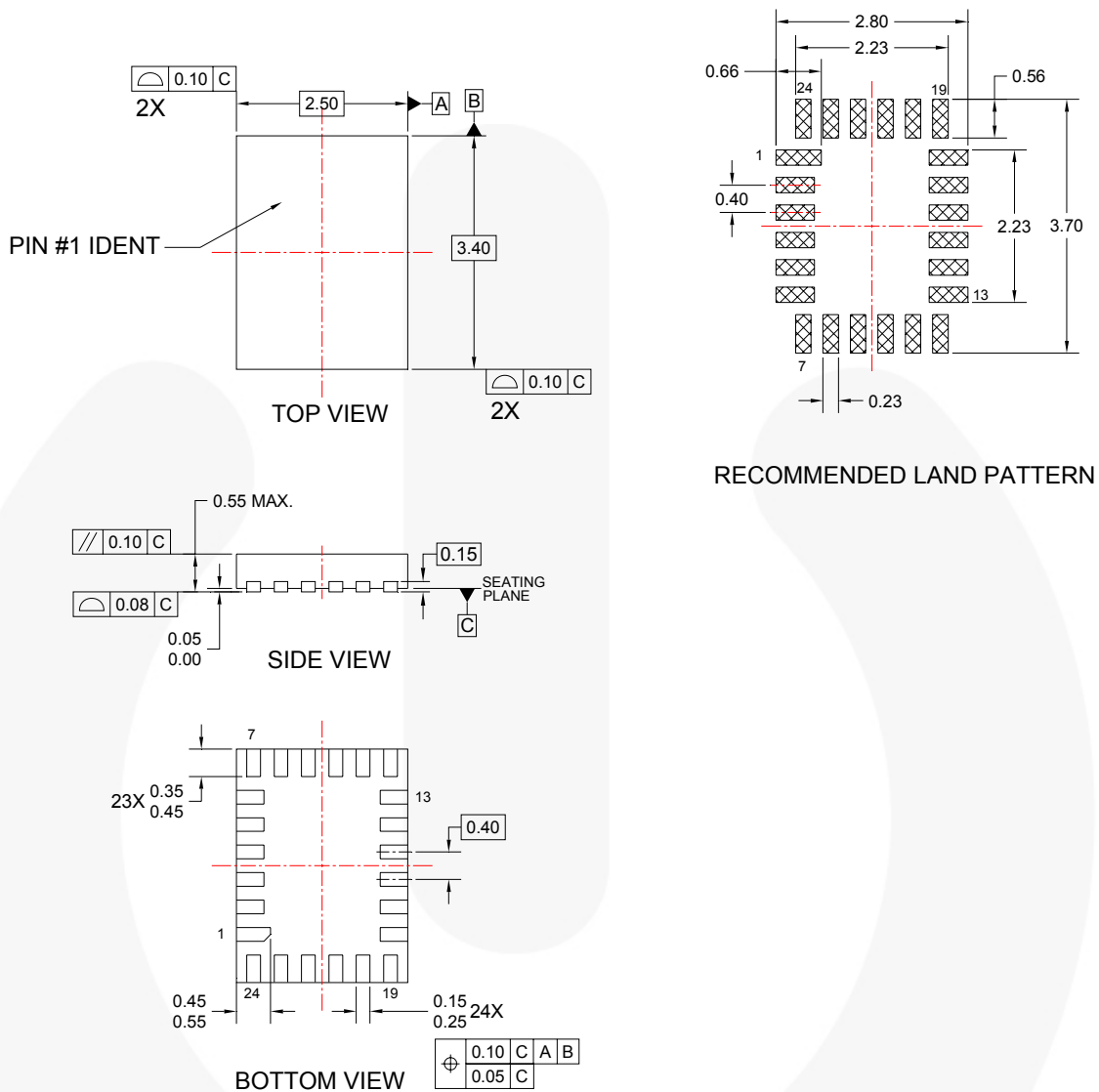
Figure 11. Maximum Data Rate



$$t_{skew} = (t_{pHLmax} - t_{pHLmin}) \text{ or } (t_{pLHmax} - t_{pLHmin})$$

Figure 12. Output Skew Time

Physical Dimensions



NOTES:

- A. NO JEDEC STANDARD APPLIES
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. DRAWING FILENAME: MKT-UMLP24Arev1.

Figure 13. 24-Pin, Micro-MLP, Quad, .6mm Thick, 2.5mm x 3.4mm Body






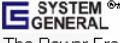
Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
<http://www.fairchildsemi.com/packaging/>



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- | | | | |
|---|---|---|---|
| Build it Now™ | FRFET® | Programmable Active Droop™ |  |
| CorePLUS™ | Global Power Resource™ | QFET® | TinyBoost™ |
| CorePOWER™ | Green FPS™ | QS™ | TinyBuck™ |
| CROSSVOLT™ | Green FPS™ e-Series™ | Quiet Series™ | TinyLogic® |
| CTL™ | GT0™ | RapidConfigure™ | TINYOPTO™ |
| Current Transfer Logic™ | IntelliMAX™ |  | TinyPower™ |
| EcoSPARK® | ISOPLANAR™ | Saving our world, 1mW/W/kW at a time™ | TinyPWM™ |
| EfficientMax™ | MegaBuck™ | SmartMax™ | TinyWire™ |
| EZSWITCH™ | MICROCOUPLER™ | SMART START™ | TriFault Detect™ |
|  | MicroFET™ | SPM® | TRUECURRENT™ |
|  | MicroPak™ | STEALTH™ | µSerDes™ |
| Fairchild® | MillerDrive™ | SuperFET™ |  |
| Fairchild Semiconductor® | MotionMax™ | SuperSOT™3 | UHC® |
| FACT Quiet Series™ | Motion-SPM™ | SuperSOT™6 | Ultra FRFET™ |
| FACT® | OPTOLOGIC® | SuperSOT™8 | UniFET™ |
| FAST® | OPTOPLANAR® | SupreMOS™ | VCC™ |
| FastvCore™ |  | SyncFET™ | VisualMax™ |
| FlashWriter® | PDP SPM™ |  | XST™ |
| FPST™ | Power-SPM™ | The Power Franchise® | |
| F-PFST™ | PowerTrench® | | |
| | PowerXS™ | | |

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I39