



#### REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Apr.28.2006
Rev. 1.1	Revised Package Outline Dimension(TSOP-II)	Apr.12.2007
Rev. 1.2	Revised $V_{TERM}$ to $V_{T1}$ and $V_{T2}$ Revised Test Condition of $I_{CC}/I_{SB1}/I_{DR}$ Revised <b>FEATURES &amp; ORDERING INFORMATION</b> <b><u>Lead free and green package available</u></b> to <b><u>Green package available</u></b> Deleted $T_{SOLDER}$ in <b><u>ABSOLUTE MAXIMUM RATINGS</u></b> Added packing type in <b><u>ORDERING INFORMATION</u></b>	Apr.17.2009

## FEATURES

- Fast access time : 10/12/15ns
- Low power consumption:  
Operating current: 200/180/150mA (TYP.)  
Standby current: 1mA (TYP.)
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 44-pin 400 mil TSOP-II

## GENERAL DESCRIPTION

The LY615128 is a 4,194,304-bit low power CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

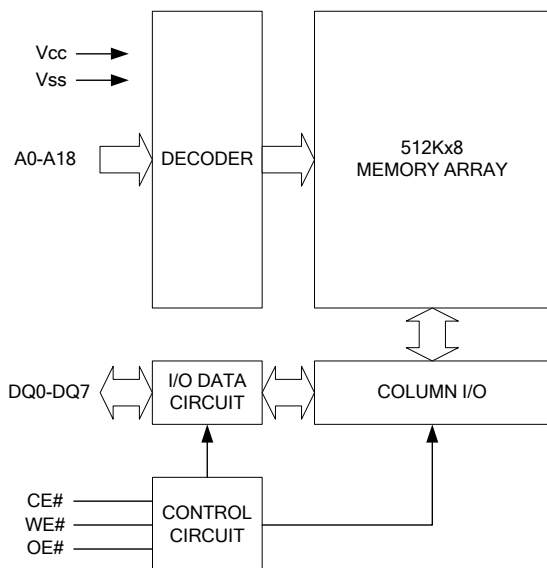
The LY615128 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The LY615128 operates from a single power supply of 5V and all inputs and outputs are fully TTL compatible

## PRODUCT FAMILY

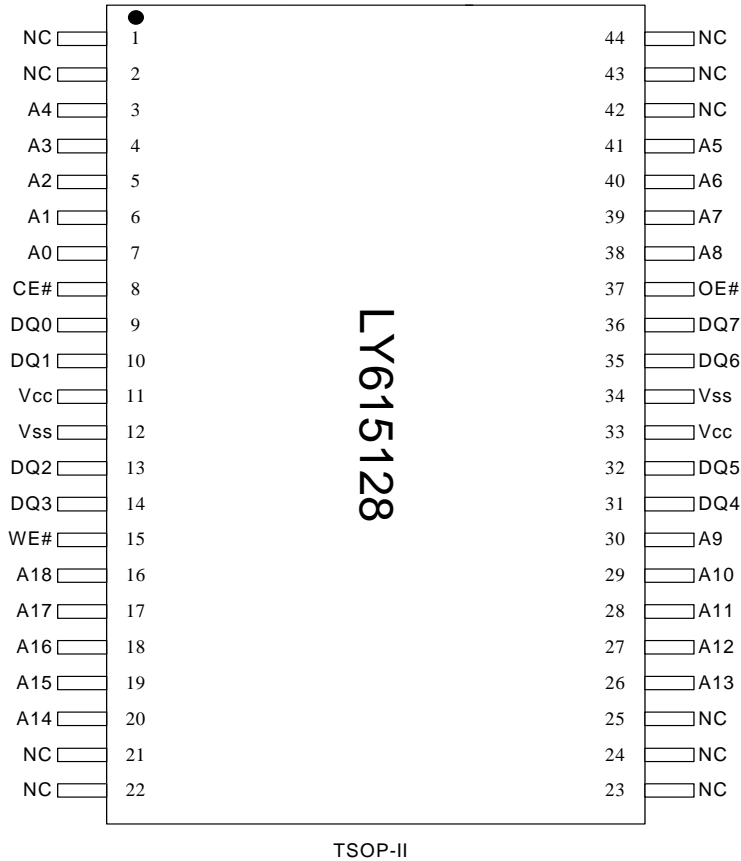
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(Isb1,TYP.)	Operating(Icc,TYP.)
LY615128	0 ~ 70°C	4.5 ~ 5.5V	10/12/15 ns	1mA	200/180/150mA

## FUNCTIONAL BLOCK DIAGRAM



## PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

**PIN CONFIGURATION**

**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	$V_{T1}$	-0.5 to 4.6	V
Voltage on any other pin relative to Vss	$V_{T2}$	-0.5 to Vcc+0.5	V
Operating Temperature	$T_A$	0 to 70(C grade)	°C
Storage Temperature	$T_{STG}$	-65 to 150	°C
Power Dissipation	$P_D$	1	W
DC Output Current	$I_{OUT}$	50	mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.



#### TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I <sub>SB</sub> , I <sub>SB1</sub>
Output Disable	L	H	H	High-Z	I <sub>CC</sub>
Read	L	L	H	DOUT	I <sub>CC</sub>
Write	L	X	L	DIN	I <sub>CC</sub>

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

#### DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>4</sup>	MAX.	UNIT	
Supply Voltage	V <sub>CC</sub>		4.5	5.0	5.5	V	
Input High Voltage	V <sub>IH</sub> <sup>1</sup>		2.2	-	V <sub>CC</sub> +0.3	V	
Input Low Voltage	V <sub>IL</sub> <sup>2</sup>		- 0.3	-	0.6	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>	- 1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled	- 1	-	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4mA	2.4	-	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA	-	-	0.4	V	
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = Min. CE# = V <sub>IL</sub> , I <sub>I/O</sub> = 0mA Others at V <sub>IL</sub> or V <sub>IH</sub>	-10	-	220	280	mA
			-12	-	200	250	mA
			-15	-	180	220	mA
Standby Power Supply Current	I <sub>SB</sub>	CE# = V <sub>IH</sub> , others at V <sub>IL</sub> or V <sub>IH</sub>	-	5	50	mA	
	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> - 0.2V Others at 0.2V or V <sub>CC</sub> - 0.2V	-	1	10 <sup>*5</sup>	mA	

Notes:

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C
- 1mA for special request

#### CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	-	8	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.



### AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -8mA/16mA$

### AC ELECTRICAL CHARACTERISTICS

#### (1) READ CYCLE

PARAMETER	SYM.	LY615128-10		LY615128-12		LY615128-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	10	-	12	-	15	-	ns
Address Access Time	t <sub>AA</sub>	-	10	-	12	-	15	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	10	-	12	-	15	ns
Output Enable Access Time	t <sub>OE</sub>	-	5	-	6	-	7	ns
Chip Enable to Output in Low-Z	t <sub>CLZ</sub> *	2	-	3	-	4	-	ns
Output Enable to Output in Low-Z	t <sub>OLZ</sub> *	0	-	0	-	0	-	ns
Chip Disable to Output in High-Z	t <sub>CHZ</sub> *	-	5	-	6	-	7	ns
Output Disable to Output in High-Z	t <sub>OHZ</sub> *	-	5	-	6	-	7	ns
Output Hold from Address Change	t <sub>OH</sub>	3	-	3	-	3	-	ns

#### (2) WRITE CYCLE

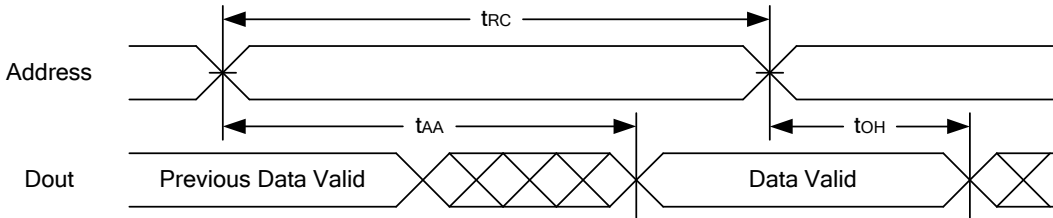
PARAMETER	SYM.	LY615128-10		LY615128-12		LY615128-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	10	-	12	-	15	-	ns
Address Valid to End of Write	t <sub>AW</sub>	8	-	10	-	12	-	ns
Chip Enable to End of Write	t <sub>CW</sub>	8	-	10	-	12	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	0	-	ns
Write Pulse Width	t <sub>WP</sub>	8	-	9	-	10	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	0	-	0	-	ns
Output Active from End of Write	t <sub>OW</sub> *	2	-	3	-	4	-	ns
Write to Output in High-Z	t <sub>WHZ</sub> *	-	6	-	7	-	8	ns

\*These parameters are guaranteed by device characterization, but not production tested.

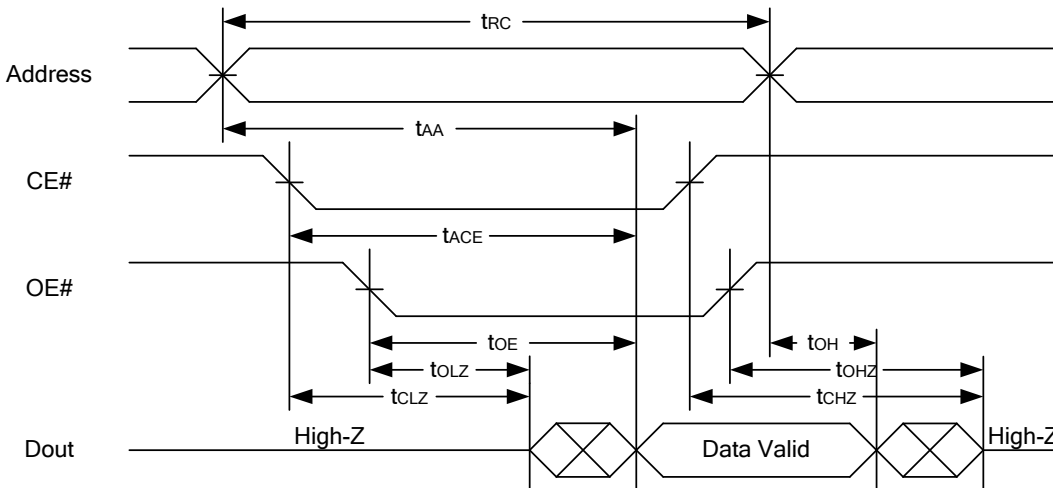


### TIMING WAVEFORMS

#### READ CYCLE 1 (Address Controlled) (1,2)



#### READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

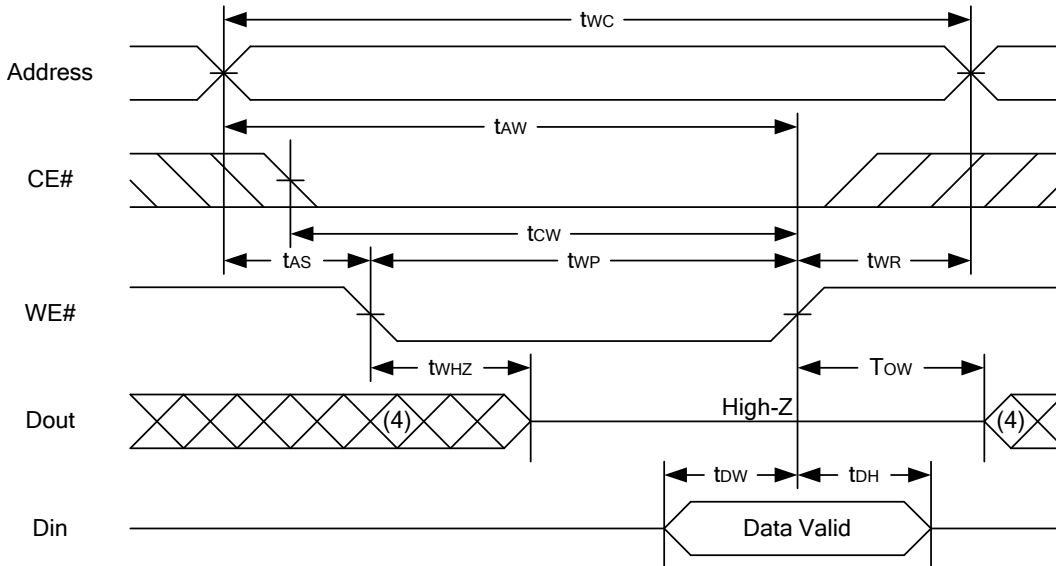


Notes :

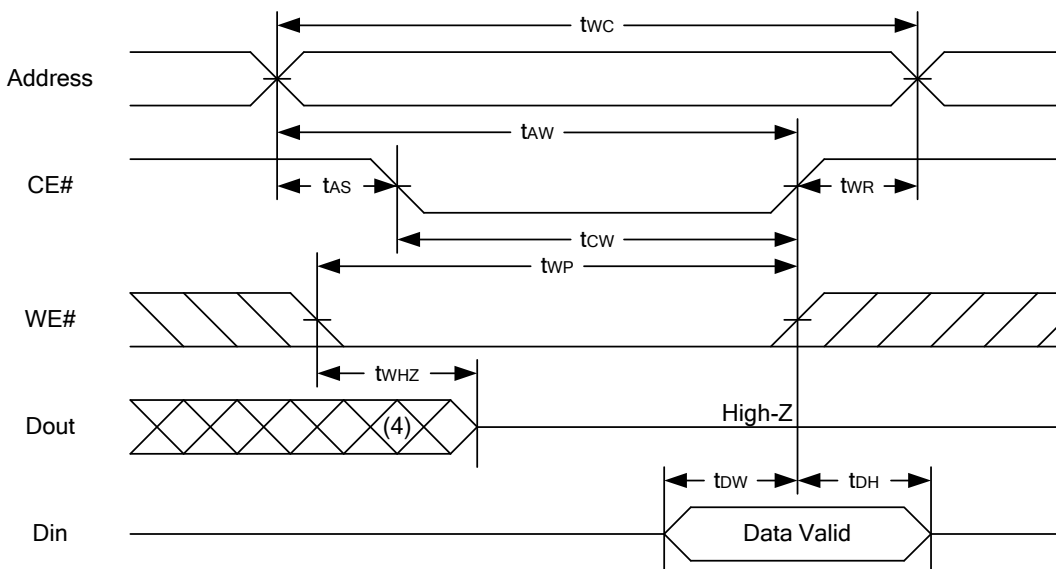
1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise tAA is the limiting parameter.
4. tCLZ, tOLZ, tCHZ and tOHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tOHZ is less than tOLZ.



#### WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



#### WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



#### Notes :

1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{DW}$  to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.

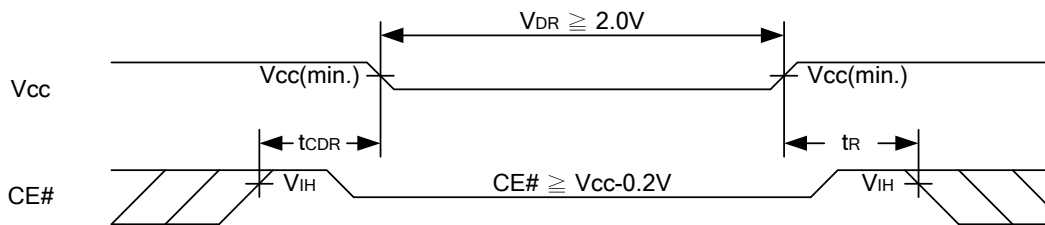


#### DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V	2.0	-	5.5	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 2.0V CE# ≥ V <sub>CC</sub> - 0.2V Others at 0.2V or V <sub>CC</sub> - 0.2V	-	0.5	1	mA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t <sub>R</sub>		t <sub>RC*</sub>	-	-	ns

t<sub>RC\*</sub> = Read Cycle Time

#### DATA RETENTION WAVEFORM

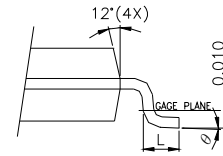
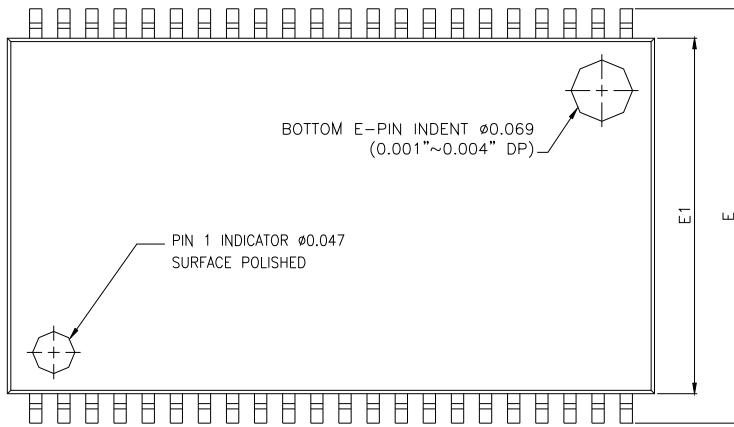




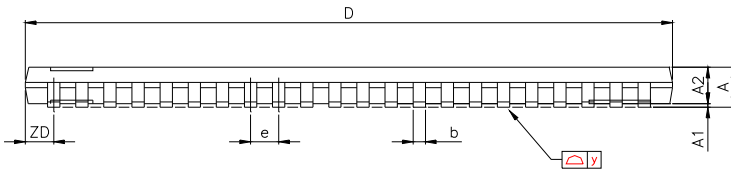


**PACKAGE OUTLINE DIMENSION**

**44-pin 400mil TSOP-II Package Outline Dimension**



DETAIL B

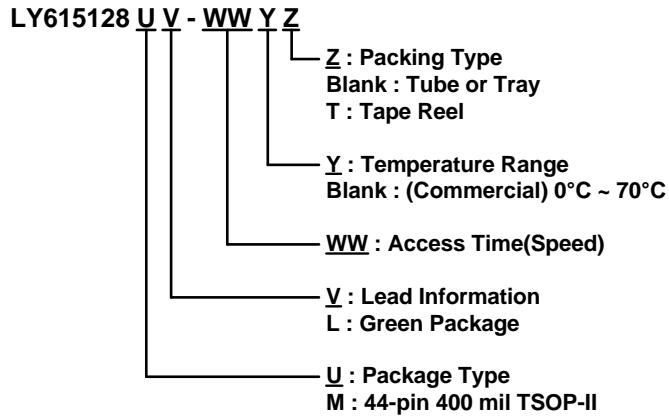


DETAIL B

SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°



#### ORDERING INFORMATION





**Lyontek Inc.**

**LY615128**

Rev. 1.2

**5V 512K X 8 BIT HIGH SPEED CMOS SRAM**

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