Structure Silicon Monolithic Integrated Circuit
Product Series 7-Channel Switching Regulator Controller for Digital Camera

Type **ＢＤ９７５９MWV**

Package Fig.1
Pin Assignment Fig.2
Block Diagram Fig.3
Application Fig.4
Function
- 3.3V minimum input operating
- Contains cross converter(1ch), step-down converter(3ch), inverting(1ch), step-up converter(1ch), step-up converter for LED(1ch),
- Contains LDO(1ch), constant current driver for LED(1ch)
- Contains load switch for step-up converter
- Contains output interception circuit when over load
- It is possible separately control except CH1, CH2, CH3
- Thermally enhanced UQFN056V7070 package(7mm x 7mm, 0.4mm pitch)

○ Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Units
Power Supply Voltage	VCC, PVCC	−0.3～12	V
	PVCCH, PVCCL	-0.3～15	V
Power Input Voltage	HX2, 3, 4	−0.3～12	V
	LX11	−0.3～12	V
	VOUT1, LX12	−0.3～7	V
	LX6, 7	−0.3～20	V
	SWIN6, 7	−0.3～20	V
	REGIN, LEDIN	−0.3～12	V
Power Dissipation	Pd	420(*1)	mW
		930(*2)	mW
Operating Temperature	Topr	−25～+85	℃
Junction Temperature	Tstg	−55～+150	℃

(*1)Without external heat sink, the power dissipation reduces by 4.2mW/℃ over 25℃.
(*2) Reduced by 9.3mW/℃ over 25℃, when mounted on a PCB (70.0mm×70.0mm×1.6mm).
Recommended operating conditions

○ Recommended operating conditions

Parameter	Symbol	Limits			Units
		MIN	TYP	MAX	
VREF Pin Connecting Capacitor	CVREF	0.47	1.0	4.7	μF
VREGA Pin Connecting Capacitor	CVREGA	0.47	1.0	4.7	μF
SCP Pin Connecting Capacitor	CSCP	0.001	−	2.2	μF
REGOUT Pin Connecting Capacitor	CREGOUT	0.47	1.0	10	μF
LEDOUT Pin Connecting Capacitor	CLEDOUT	0.47	1.0	10	μF
【Oscillator】					
Oscillator Frequency	Fosc	0.6	1.2	1.5	MHz
OSC Timing Resistor	RT	47	68	120	kΩ
【Driver】					
LX11 Pin Input Voltage	VLX11	−	−	10	V
CH1 Output set up area	VVOUT1	3.9	−	5.5	V
HX2, 3, 4 Pin Input Voltage	VHX2, 3, 4	−	−	10	V
CH1 Output Current	Ioutch1	−	−	1	A
CH2 Output Current	Ioutch2	−	−	600	mA
CH3, 4 Output Current	Ioutch3, 4	−	−	500	mA
CH6 Output Current	Ioutch6	−	−	100	mA
CH7 Output Current	Ioutch7	−	−	50	mA
【SW Circuit】					
SWOUT6 Pin Source Current	ISWOUT6	−	−	100	mA
SWOUT7 Pin Source Current	ISWOUT7	−	−	50	mA

◎ It is strongly recommended that a capacitor be connect to VREF, VREGA pin to prevent oscillation.
※) The IC may not operate correctly by an unsettled state of the internal logic when voltage is applied on VCC rapidly while STB pin is ON. Make sure STB pin is OFF in this case.

○ Recommended operating conditions

Parameter	Symbol	Limit	Unit
Power Supply Voltage	VCC, PVCC	3.3 ～ 10	V
	PVCCL	3.75 ～ 14	V
	PVCCH	VCC+3.75 ～ 14	V

Status of this document
The Japanese version of this document is the official specification. Please use the translation version of this document as a reference to expedite understanding of the official version.
If these are any uncertainty in translation version of this document, official version takes priority.

○ Electrical characteristics (Ta=25℃, VCC=5V, RT=68kohm, STB1～7=3V)

Parameter	Symbol	Standard value			Units	Conditions	Test circuit
		MIN	TYP	MAX			
【Internal Regulator】							
Output Voltage	VREGA	2.4	2.5	2.6	V	Ireg=1mA	
【Prevention Circuit of Miss Operation by Low Voltage Input】							
Threshold Voltage 1	Vstd1	3.35	3.50	3.65	V	PVCCL Monitor	
Threshold Voltage 2	Vstd2	2.85	3.0	3.15	V	PVCC Monitor	
Threshold Voltage 3	Vstd3	—	2.15	2.30	V	VREGA Monitor	
【 Short Circuit Protection】							
Timer Start Threshold Voltage	Vtc	2.1	2.2	2.3	V	FB Pin Monitor	
SCP Out Source Voltage	Iscp	0.5	1.0	1.5	μA	VSCP=0.1V	
SCP Threshold Voltage	Vtsc	0.45	0.50	0.55	V		
Stand by Voltage	Vssc	—	22	170	mV		
【Oscillator】							
Frequency CH1～4	fosc1	1.0	1.2	1.4	MHz	RT=68kΩ	
Frequency CH5～7	fosc2	0.5	0.6	0.7	MHz	RT=68kΩ	
Max duty 2,3,4 (Step Down)	Dmax1d	–	–	100	%	Vscp=0V ※	
Max duty 5,6,7	Dmax2	86	92	96	%		
Max duty CH1 Lx11	Dmax3	–	–	100	%		
Max duty CH1 Lx12	Dmax4	78	84	90	%		
【Error AMP】							
Input Bias Current	IINV	–	0	50	nA	INV1～7, NON5=7.0V	
INV Threshold Voltage 1	VINV1	0.79	0.80	0.81	V	CH1～4	
INV Threshold Voltage 2	VINV2	0.99	1.00	1.01	V	CH6,7V	
INV Threshold Voltage 3	VINV3	380	400	420	mV	CH7I	
【Base Bias Voltage Vref for Inverted Channel】							
CH5 Output Voltage	VOUT5	-6.09	-6.00	-5.91	V	NON5 12kΩ, 72kΩ	
Line Regulation	DVLi	–	4.0	12.5	mV	VBAT=4.8～8.4V	
Load Regulation	DVLo	–	1.0	7.5	mV	Iref=10μA～100μA	
Output Current when shorted	Ios	0.2	1.0	–	mA	Vref=0V	
【Soft Start】							
CH1,2 Soft Start Time	Tss1,Tss2	3.4	4.4	5.4	msec	RT=68kΩ	
CH3,4 Soft Start Time	Tss3,Tss4	1.2	2.2	3.2	msec	RT=68kΩ	
CH5 Soft Start Time	Tss5	4.4	5.4	6.6	msec	RT=68kΩ	
CH6,7 Soft Start Time	Tss6,Tss7	4.4	5.4	6.6	msec	RT=68kΩ	

Parameter	Symbol	Standard value			Units	Conditions	Test circuit
		MIN	TYP	MAX			
【Output Driver】							
OUT1H Driver Output Voltage H	Vout1H	PVCC-1.0	PVCC-0.5	–	V	IOUT1H=50mA	
OUT1H Driver Output Voltage L	Vout1L	–	0.5	1.0	V	IOUT1L=50mA	
CH1 Lx11 Pin Lowside SW ON Resistance	RON11N	–	300	450	mΩ	PVCC=5V	
CH1 Lx12 Pin Highside SW ON Resistance	RON12p	–	250	400	mΩ	VOUT1=5.0V	
CH1 Lx12 Pin Lowside SW ON Resistance	RON12N	–	150	300	mΩ	PVCC=5V	
CH2,3,4 Highside SW ON Resistance	RON2345p	–	300	450	mΩ	Hx=5V, PVCC=5V PVCCH=10V	
CH2,3,4 Lowside SW ON Resistance	RON2345N	–	300	450	mΩ	Hx=5V, PVCC=5V PVCCH=10V	
CH6 NMOS SW ON Resistance	RON6N	–	500	700	mΩ	PVCCL=5V	
CH7 NMOS SW ON Resistance	RON7N	–	700	900	mΩ	PVCCL=5V	
CH5 Driver Output Voltage H	Vout5H	PVCC-1.0	PVCC-0.5	–	V	IOUT5=50mA, NON5=0.2V PVCC=5V	
CH5 Driver Output Voltage L	Vout5L	–	0.5	1.0	V	IOUT5=-50mA, NON5=-0.2V	
【Regulator】							
Feed back voltage 1	VNF1	0.98	1.0	1.02	V		
Maximum output current 1	Imax1	–	–	150	mA		
Difference of input/output voltage 1	ΔV1	–	150	300	mV	Io=50mA	
Load stability 1	Δvol1	–	10	50	mV	Io=0.1～10mA	
Ripple rejection	RR1	40	50	–	dB	f=120Hz, VRR=-20dBV, Io=1mA	
【Constant current driver】							
Feed back Voltage 2	VNF2	380	400	420	mV		
Maximum output current 2	Imax2	–	–	50	mA		
Difference of input/output voltage 2	ΔV2	–	100	200	mV	Io=10mA	
【Power on switch】							
SWOUT6	Driver Output Voltage	VSAT	VSWIN6 -0.3	VSWIN6 -0.1	–	V	Io=20mA VSWIN6=5V
	OFF Leak Current	ILEAK	–	0	5	μA	STB6=0V
SWOUT7	Driver Output Voltage	VSAT	VSWIN7 -0.3	VSWIN7 -0.1	–	V	Io=10mA VSWIN7=10V
	OFF Leak Current	ILEAK	–	0	5	μA	STB7=0V
【STB】							
STB control Voltage 1	Active	VSTBH1	2.0	–	11	V	STB123,4,5,6,7
	Non Active	VSTBL1	-0.3	–	0.3	V	
STB Pull down Resistance 1		RSTB1	250	400	700	kΩ	STB123,4,5,6,7
STB control Voltage 2	Active	VSTBH2	2.0	–	11	V	STBREG,LED
	Non Active	VSTBL2	-0.3	–	0.3	V	
STB Pull down Resistance 2		RSTB2	250	400	700	kΩ	STBREG,LED
【Circuit Current】							
STAND-by Current 1		ISTB1	–	–	5	μA	STB1～7=0V
Circuit Current 1 (VCC,PVCC current when voltage supplied for the terminal)		Icc1	–	10	15	mA	INV=2.5V, NON=-0.3V
Stand-by Current 2 (PVCCL current when voltage supplied for the terminal)		Icc2	–	95	150	MA	INV=2.5V, NON=-0.3V PVCCL=5.0V
Circuit Current 3 (PVCCH current when voltage supplied for the terminal)		Icc3	–	150	300	μA	INV=2.5V, NON=-0.3V PVCCH=10V

(※1)The protective circuit start working when circuit is operated by 100% duty. So it is possible to use only for transition time shorter than charge time for SCP.

◎This product is not designed for normal operation with in a radioactive environment.

○ Block Diagram

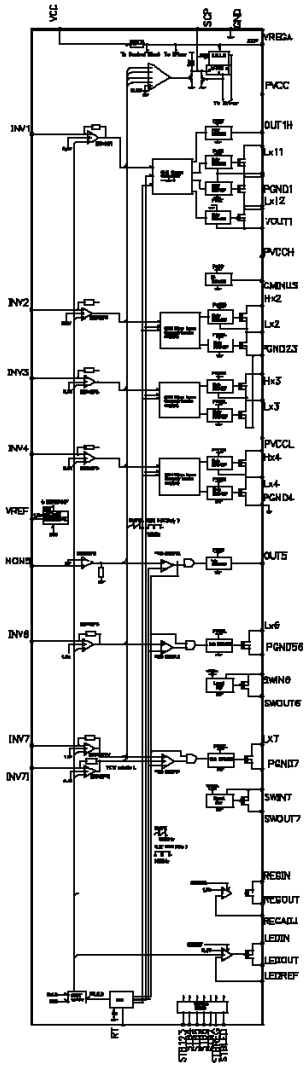

Fig. 1

○ Package

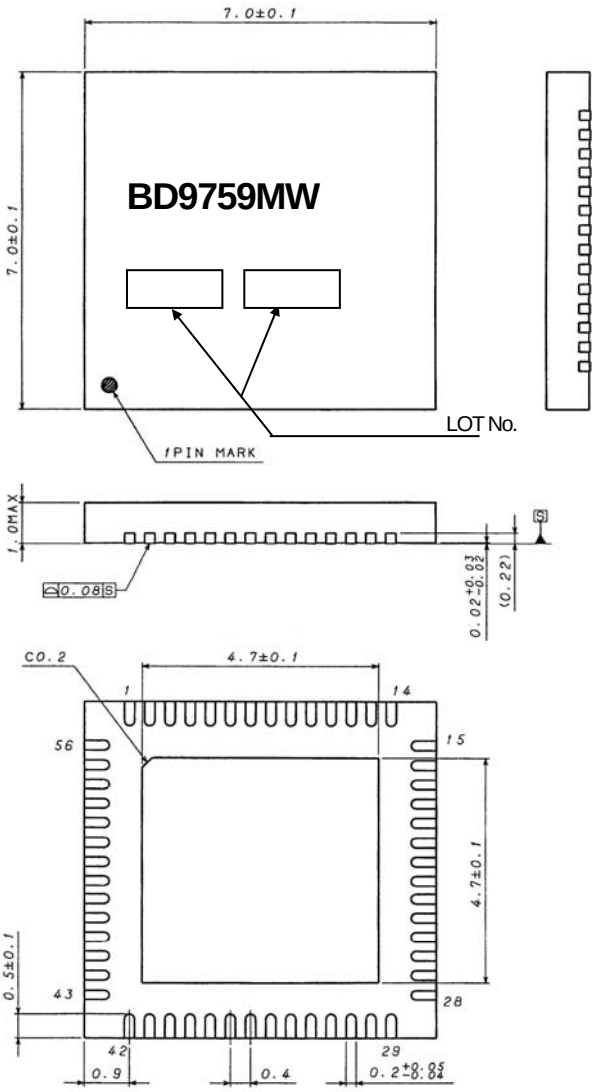

Fig. 2

○ Pin Description

Pin Name	Description	Pin Name	Description
VCC	Power supply	VOUT1	CH1 output voltage
PVCC	Power supply for the output circuit	Lx2, 3, 4, 6, 7	Terminal for connecting inductors
PVCCH	Power supply for the output circuit (High side)	INV 1~4, 6, 7	Error AMP inverted input
PVCCL	Power supply for the output circuit (Low side)	INV7I	Error AMP inverted input
PGND1, 23, 4, 56, 7	Ground terminal for internal FET	NON5	Error AMP non inverted input
GND	Ground terminal	Lx11	Terminal for connecting inductor for CH1 input
VREGA	VREGA output	Lx12	Terminal for connecting inductor for CH1 output
OUT1H,OUT5	Terminal for connecting gate of OUT1H, OUT5 PMOS	RT	For connecting a register to set the OSC freqency
REGIN	Input terminal for REG	SCP	For connecting a capacitor to set up the delay time of the SCP
REGOUT	Output terminal for REG	STBREG	REG ON/OFF switch Active 'H'
REGADJ	Feed back terminal for REG	STBLED	LED ON/OFF switch Active 'H'
LEDIN	Input terminal for LED	STB123, 4, 5, 6, 7	CH1~CH7 ON/OFF switch Active 'H'
LEDOUT	Output terminal for LED	SWIN6, 7	Input terminal for Lord SW
LEDREF	Feed back terminal for LED	SWOUT6, 7	Output Terminal for Load SW
Hx2, 3, 4	Input terminal for synchronous High side switch	CMINUS	Terminal for connecting capacitor for Charge Pump
VREF5	Base bias voltage	–	–

○ Pin Assignment

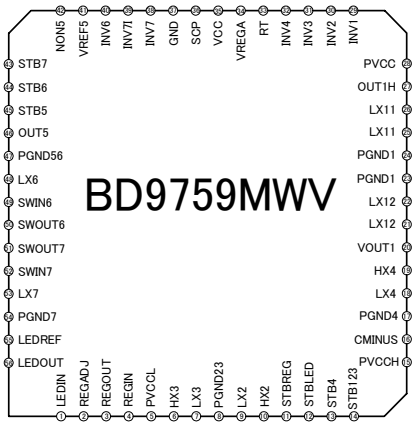

Fig. 3

○ Operation Notes

1.) Absolute maximum ratings
This product is produced with strict quality control. However, the IC may be destroyed if operated beyond its absolute maximum ratings. If the device is destroyed by exceeding the recommended maximum ratings, the failure mode will be difficult to determine. (E.g. short mode, open mode) Therefore, physical protection counter-measures (like fuse) should be implemented when operating conditions beyond the absolute maximum ratings anticipated.

2.) GND potential
Make sure GND is connected at lowest potential. All pins except NON5, must not have voltage below GND. Also, NON5 pin must not have voltage below − 0.3V on start up.

3.) Setting of heat
Make sure that power dissipation does not exceed maximum ratings.

4.) Pin short and mistake fitting
Avoid placing the IC near hot part of the PCB. This may cause damage to IC. Also make sure that the output-to-output and output to GND condition will not happen because this may damage the IC.

5.) Actions in strong magnetic field
Exposing the IC within a strong magnetic field area may cause malfunction.

6.) Mutual impedance
Use short and wide wiring tracks for the main supply and ground to keep the mutual impedance as small as possible. Use inductor and capacitor network to keep the ripple voltage minimum.

7.) Voltage of STB pin
The threshold voltages of STB pin are 0.3V and 1.5V. STB state is set below 0.3V while action state is set beyond 1.5V.
The region between 0.3V and 1.5V is not recommended and may cause improper operation.
The rise and fall time must be under 10msec. In case to put capacitor to STB pin, it is recommended to use under 0.01μF.

8.) Thermal shutdown circuit (TSD circuit)
The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

9.)Rush current at the time of power supply injection.
An IC which has plural power supplies, or CMOS IC could have momentary rush current at the time of power supply injection. Please take care about power supply coupling capacity and width of power Supply and GND pattern wiring.

10.)IC Terminal Input
This IC is a monolithic IC that has a P− board and P+ isolation for the purpose of keeping distance between elements. A P-N junction is formed between the P-layer and the N-layer of each element, and various types of parasitic elements are then formed.
For example, an application where a resistor and a transistor are connected to a terminal (shown in Fig.15):
○When GND > (terminal A) at the resistor and GND > (terminal B) at the transistor (NPN), the P-N junction operates as a parasitic diode.
○When GND > (terminal B) at the transistor (NPN), a parasitic NPN transistor operates as a result of the NHayers of other elements in the proximity of the aforementioned parasitic diode.
Parasitic elements are structurally inevitable in the IC due to electric potential relationships. The operation of parasitic elements Induces the interference of circuit operations, causing malfunctions and possibly the destruction of the IC. Please be careful not to use the IC in a way that would cause parasitic elements to operate. For example, by applying a voltage that is lower than the GND (P-board) to the input terminal.

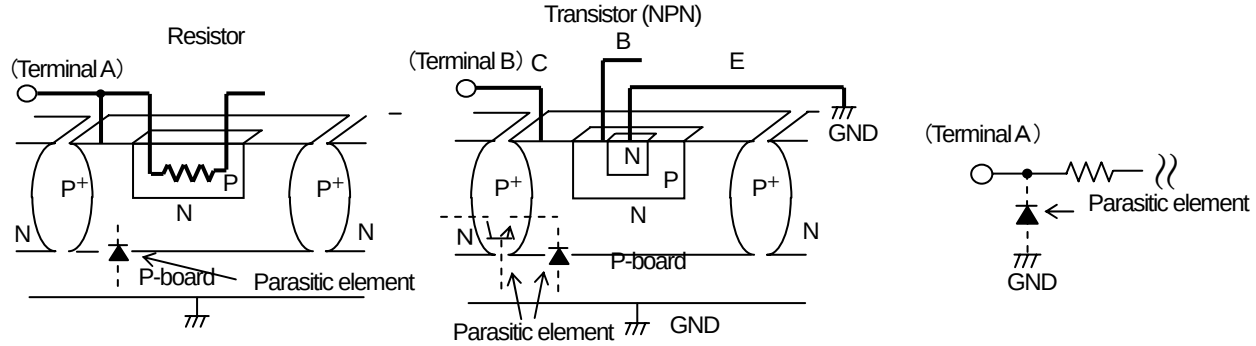

Fig . 3 Simplified structure of a Bipolar IC

Notes

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